4 Channel High Performance Digital Isolator

Features

- Up to 100 Mbps Data Rate
- Up to 5 kV RMS Isolation Rating (WSOP16)
- 10 kV Surge Capability (WSOP16)
- ±150 kV/μs typ CMTI
- Low Power Consumption, typ 3 mA/ch @1 Mbps
- Low Propagation Delay: 12 ns Typical
- Wide Supply Range: 2.25 V to 5.5 V
- Default Output Low (TPT774xF) and High (TPT774x)
- Wide Temperature Range: −40°C to +125°C
- SOP-16 and WSOP-16 package
- ESD Protection Exceeds JESD 22
  - ±6 kV Human-Body Model
  - ±1.5 kV Charged-Device Model
- Safety-Related Certifications:
  - VDE Reinforced Insulation according to DIN VDE V 0884-11: 2017-01
  - 3750 V_{RMS} (SOP-16) Isolation Rating per UL 1577
  - CSA Certification per IEC 60950-1, IEC 62368-1 and IEC 60601-1 End Equipment Standards
  - TUV Certification according to EN 60950-1 and EN 61010-1
  - CQC Certification per GB4943.1-2011

Applications

- Industrial Automation
- Motor Control
- Power Supplies
- Isolated interface and general-purpose isolation

Description

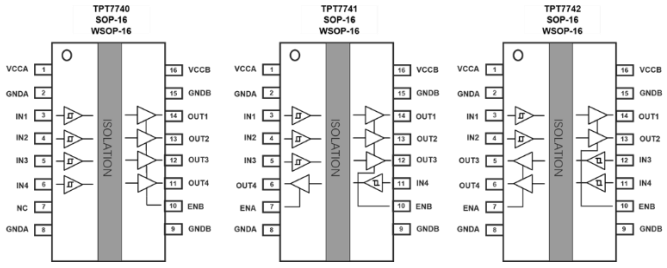
The TPT774x devices are high-performance, 4-channel digital isolators with 5000 V_{RMS} (WSOP-16 packages), 3750 V_{RMS} (SOP-16 package), isolation ratings per UL 1577. These devices are also to be certified by VDE, UL, CSA, and CQC.

The TPT774x devices provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by a double capacitive silicon dioxide (SiO2) insulation barrier. The TPT7740 device has four channels in the same direction while the TPT7741 device has three channels in the forward direction and one channel in opposite direction. The TPT7742 device has 2 channels in the forward direction and 2 channels in opposite direction. In the event of input power or signal loss, the default output is low for devices UVLO suffix F and for high devices without suffix F.

Used in conjunction with isolated power supplies, these devices help prevent noise currents on data buses, such as RS-485, RS-232, and CAN, from damaging sensitive circuitry. Through innovative chip design and layout techniques, the electromagnetic compatibility of the TPT774x devices has been significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance.

TPT774x family is available in SOP-16, and WSOP-16 package, and is characterized from −40°C to +125°C.

Function Block Diagram



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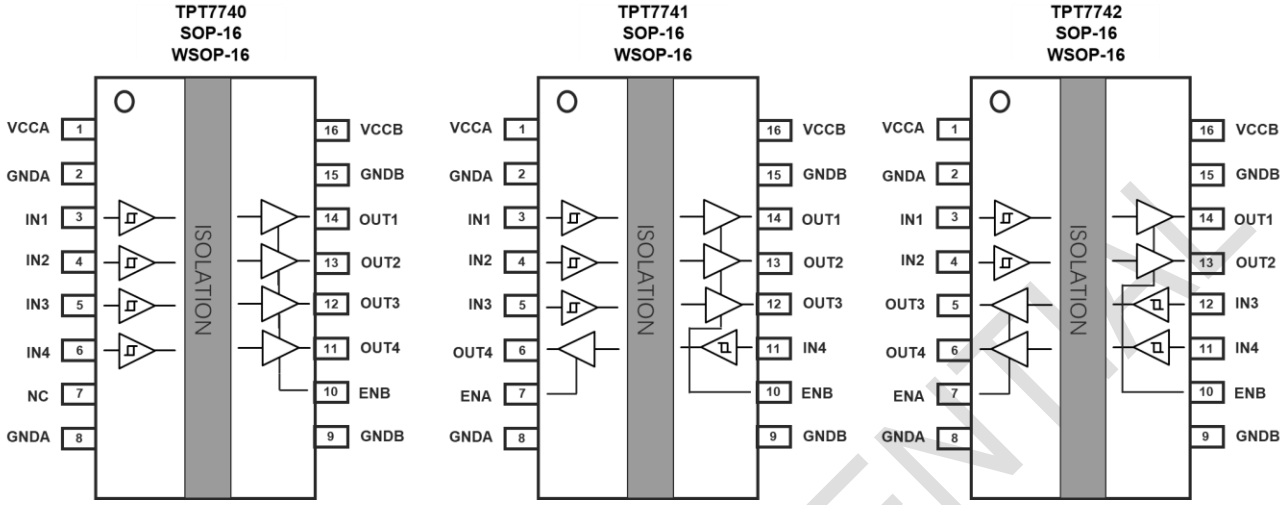
Revision History

Date	Revision	Notes
2021-08-02	Rev.Pre.1	Definition Version Pre.0
2021-10-28	Rev.Pre.2	Added WSOP-16 package information
2022-01-27	Rev.Pre.3	Added Electrical parameter
2022-02-08	Rev.Pre.4	Updated Tape and Reel Information
2022-03-30	Rev.Pre.5	Updated description in page1
2022-04-08	Rev.Pre.6	Updated the order information
2022-05-10	Rev.Pre.7	Fix some typo in description

Pin Configuration and Functions



Pin Functions

Pin				I/O	Description
Name	TPT7740	TPT7741	TPT7742		
VCCA	1	1	1	–	Power supply, VCCA
GNDA	2	2	2	–	Ground connection for VCCA
IN1	3	3	3	I	Input, channel 1
IN2	4	4	4	I	Input, channel 2
IN3	5	5	12	I	Input, channel 3
IN4	6	11	11	I	Input, channel 4
NC	7	-	-		
ENA	-	7	7	I	Side A enable pin
GNDA	8	8	8	–	Ground connection for VCCA
GNDB	9	9	9	–	Ground connection for VCCB
ENB	10	10	10	I	Side B enable pin
OUT4	11	6	6	O	Output, channel 4
OUT3	12	12	5	O	Output, channel 3
OUT2	13	13	13	O	Output, channel 2
OUT1	14	14	14	O	Output, channel 1
GNDB	15	15	15	–	Ground connection for VCCB
VCCB	16	16	16	–	Power supply, VCCB

(1) ENA: Side A OUTx enable when ENA = high or open, and in high-impedance state when ENA is low.
(2) ENB: Side B OUTx enable when ENB = high or open, and in high-impedance state when ENB is low.

Specifications

Absolute Maximum Ratings

Parameter		Min	Max	Unit
V_{CC}	Supply voltage, V_{CCA}, V_{CCB}	−0.5	6	V
V_{IO}	Voltage at IN1, IN2, OUT1, OUT2	−0.5	V_{CC} + 0.5	V
I_O	Output current	−15	15	mA
T_J	Operating virtual junction temperature		150	°C
T_{stg}	Storage temperature	−65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) This data was taken with the JEDEC low effective thermal conductivity test board.
(3) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Parameter	Condition	Value	Unit
HBM, per ANSI/ESDA/JEDEC JS-001/ANSI/ESD STM5.5.1	All Pin	±6	kV
CDM, per ANSI/ESDA/JEDEC JS-002	All Pin	±1.5	kV
IEC, per IEC 61000-4-2; Isolation barrier withstand test	All Side	±7	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device.

Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
V_{CCX}	Supply voltage, V_{CCA}, V_{CCB} (1)	2.25		5.5	V
$V_{CC(UVLO+)}$	UVLO threshold when supply voltage is rising (2)		2	2.25	V
$V_{CC(UVLO+)}$	UVLO threshold when supply voltage is falling (2)	1.7	1.85		V
$V_{HYS(UVLO)}$	Supply voltage UVLO hysteresis	60	150		mV
V_{IH}	High-level input voltage (data input)	2		V_{CC}	V
V_{IL}	Low-level input voltage (data input)	0		0.8	V
f_{data}	Data rate (3)	0		100	Mbps
T_A	Operating ambient temperature	−40	25	125	°C

(1) V_{CCA} is input side V_{CC}; V_{CCB} is output side V_{CC};
(2) $V_{CC(UVLO+)}$, $V_{CC(UVLO+)}$, $V_{HYS(UVLO)}$ are same to V_{CCA} and V_{CCB};
(3) 100 Mbps is the maximum specified data rate, although higher data rates are possible.

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
16-Pin SOP	91	31	°C/W
16-Pin WSOP	102	59	°C/W

Insulation Specifications

Symbol	Parameter	Conditions	Value		Unit
			SOP-16	WSOP-16	
CLR	External clearance	Shortest terminal-to-terminal distance through air	> 3.7	> 7.8	mm
CPG	External creepage	Shortest terminal-to-terminal distance across the package surface	> 3.7	> 7.8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	> 22	> 22	μm
CTI	Comparative tracking index		> 600	> 600	V
	Material group		I	I	
	Installation Classification	For Rated Mains Voltage ≤ 300 V_{RMS}	I-III	I-III	
	Pollution degree		2	2	
C_{IO}	Isolation capacitance	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	~0.5	~0.5	pF
R_{IO}	Isolation resistance	V_{IO} = 500 V	> 10^9	> 10^9	Ω
Isolation voltage (1)					
V_{IORM}	Maximum repetitive isolation voltage	AC voltage	637	1414	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage; TDDB Test	450	1000	V_{RMS}
		DC voltage	637	1414	Vdc
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM}, t = 60 s (qualification); V_{TEST} = 1.2 x V_{IOTM}, t = 1 s (100% production)	5300	7000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage (2)	Test method per IEC 62368-1, 1.2/50 μs waveform, V_{TEST} = 1.6 × V_{IOSM} (qualification)	6000	6000	V_{PK}
q_{pd}	Apparent charge	Method a, After Input/Output safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 × V_{IORM}, t_m = 10 s	≤ 5	≤ 5	pC
		Method a, After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.6 × V_{IORM}, t_m = 10 s	≤ 5	≤ 5	
		Method b1; At routine test (100% production) and preconditioning (type test), V_{ini} = 1.2 x V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.875 × V_{IORM}, t_m = 1 s	≤ 5	≤ 5	

(1) All pins on each side of the barrier tied together creating a two-terminal device.

Electrical Characteristics

V_{CCA} = V_{CCB} = 2.25 V ~ 5.5 V, T_A = −40°C ~ +125°C, Typical value is in V_{CC} = 3.3 V, T_A = +25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input Electrical Specifications						
V_{IH}	Logic Input High Voltage	Input signal, IN1, IN2	2.0			V
V_{IL}	Logic Input Low Voltage	Input signal, IN1, IN2			0.8	V
V_{IT+}	Rising input threshold voltage	Input signal, IN1, IN2		1.6	2	V
V_{IT-}	Falling input threshold voltage	Input signal, IN1, IN2	0.8	1.2		V
V_{HYS}	Input threshold voltage hysteresis			0.4		V
I_{IH}	High-level input current	V_{IH} = V_{CCA} at IN1, IN2 (1)		2.5	10	μA
I_{IL}	Low-level input current	V_{IL} = 0 V at IN1, IN2 (1)	−10	−2.5		μA
I_{OH}	High-level output current	V_{CCB} = 5 V ± 10%			4	mA
		V_{CCB} = 3.3 V ± 10%			2	
		V_{CCB} = 2.5 V ± 10%			1	
I_{OL}	Low-level output current	V_{CCB} = 5 V ± 10%			4	mA
		V_{CCB} = 3.3 V ± 10%			2	
		V_{CCB} = 2.5 V ± 10%			1	
V_{OH}	High-level output voltage	V_{CCB} = 5 V ± 10%, I_{OH} = −4 mA; Test OUT1, OUT2	V_{CCB} – 0.4	V_{CCB} – 0.2		mV
		V_{CCB} = 3.3 V ± 10%, I_{OH} = –2 mA; Test OUT1, OUT2	V_{CCB} – 0.3	V_{CCB} – 0.15		
		V_{CCB} = 2.5 V ± 10%, I_{OH} = –1 mA; Test OUT1, OUT2	V_{CCB} – 0.2	V_{CCB} – 0.1		
V_{OL}	Low-level output voltage	V_{CCB} = 5 V ± 10%, I_{OL} = 4 mA; Test OUT1, OUT2		0.2	0.4	V
		V_{CCB} = 3.3 V ± 10%, I_{OL} = 2 mA; Test OUT1, OUT2		0.15	0.3	
		V_{CCB} = 2.5 V ± 10%, I_{OL} = 1 mA; Test OUT1, OUT2		0.1	0.2	
CMTI	Common-mode transient immunity	Static CMTI		150		kV/μs
		Dynamic CMTI		120		kV/μs
C_i	Input capacitance (1)			2		pF

(1) Provided by bench test and design simulation

Timing Specifications-5 V Supply

V_{CCA} = V_{CCB} = 5 V ± 10%, T_A = −40°C ~ +125°C. Typical value is in V_{CC} = 5 V, T_A = +25°C, C_L = 15 pF to GND.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{data}	Translation data rate				100	Mpbs
t_{PLH}	Propagation delay time			11.5		ns
t_{PHL}	Propagation delay time			12		ns
PWD	Pulse width distortion (1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.5		ns
$t_{sk(CC)}$	Channel-to-channel output skew time (2)	Same direction channels			2.5	ns
$t_{sk(PP)}$	Channel-to-channel output skew time (2)	Same direction channels			4.5	ns
t_r	Output signal rise time (1)			0.7		ns
t_f	Output signal fall time (1)			0.7		ns
Jitter	Eye jitter p-p (1)	f_{data} = 100 Mbps		800		ps
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V.		30		ns
t_{ie}	Time interval error (1)	216 − 1 PRBS data at 100 Mbps (1)		2.4		ns
t_{su}	Setup time			28		us

(1) Provided by bench test and design simulation.

(2) $t_{sk(CC)}$ & $t_{sk(PP)}$ is the shew of delay time between different channel of a single device or different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

Supply Current Characteristics-5 V Supply

V_{CCA} = V_{CCB} = 5 V ± 10%, T_A = −40°C ~ +125°C. Typical value is in V_{CC} = 5 V, T_A = +25°C, C_L = 15 pF to GND.

Parameter	Description		Supply current	Min	Typ	Max	Unit
TPT7740/TPT7741							
Supply current - DC signal	V_I = 0 V, V_I = VCC_I		I_{CCA}		1.8		mA
			I_{CCB}		3.5		
	V_I = VCC_I, V_I = 0 V		I_{CCA}		9.5		
			I_{CCB}		3.9		
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CCA}		6.5		
			I_{CCB}		3.8		
		10 Mbps	I_{CCA}		7.3		
			I_{CCB}		6.2		
		100 Mbps	I_{CCA} (1)		10.6		
			I_{CCB} (1)		29.4		
TPT7742							
Supply current - DC signal	V_I = 0 , V_I = VCC_I		I_{CCA}, I_{CCB}		3.5		mA
	V_I = VCC_I, V_I = 0 V		I_{CCA}, I_{CCB}		9.7		
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CCA}, I_{CCB}		6.2		
		10 Mbps	I_{CCA}, I_{CCB}		7.5		
		100 Mbps	I_{CCA}, I_{CCB} (1)		19.3		

(1) Provided by bench test and design simulation.

(2) VCC_I is the VCC of V_I.

Timing Specifications-3.3 V Supply

V_{CCA} = V_{CCB} = 3.3 V ± 10%, T_A = −40°C ~ +125°C. Typical value is in V_{CC} = 3.3 V, T_A = +25°C, C_L = 15 pF to GND.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{data}	Translation data rate				100	Mpbs
t_{PLH}	Propagation delay time			12.5		ns
t_{PHL}	Propagation delay time			12.2		ns
PWD	Pulse width distortion (1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.3		ns
$t_{sk(CC)}$	Channel-to-channel output skew time (2)	Same direction channels			2.5	ns
$t_{sk(PP)}$	Channel-to-channel output skew time (2)	Same direction channels			4.5	ns
t_r	Output signal rise time (1)			0.7		ns
t_f	Output signal fall time (1)			0.7		ns
Jitter	Eye jitter p-p (1)	f_{data} = 100 Mbps		800		ps
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below 1.7 V.		30		ns
t_{ie}	Time interval error (1)	216 − 1 PRBS data at 100 Mbps		2.4		ns
t_{su}	Setup time			28		μs

(1) Provided by bench test and design simulation.

(2) $t_{sk(CC)}$ & $t_{sk(PP)}$ is the shew of delay time between different channel of a single device or different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

Supply Current Characteristics-3.3 V Supply

V_{CCA} = V_{CCB} = 3.3 V ± 10%, T_A = −40°C ~ +125°C. Typical value is in V_{CC} = 3.3 V, T_A = +25°C, C_L = 15 pF to GND.

Parameter	Description		Supply current	Min	Typ	Max	Unit
TPT7740/TPT7741							
Supply current - DC signal	V_I = 0 V, V_I = VCC_I		I_{CCA}		1.5		mA
			I_{CCB}		3.1		
	V_I = VCC_I, V_I = 0 V		I_{CCA}		8.7		
			I_{CCB}		3.4		
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CCA}		6.1		
			I_{CCB}		3.5		
		10 Mbps	I_{CCA}		6.8		
			I_{CCB}		5.7		
		100 Mbps	I_{CCA} (1)		10.1		
			I_{CCB} (1)		27.4		
TPT7742							
Supply current - DC signal	V_I = 0 V, V_I = VCC_I		I_{CCA}, I_{CCB}		3.2		mA
	V_I = VCC_I, V_I = 0 V		I_{CCA}, I_{CCB}		9.1		
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CCA}, I_{CCB}		5.8		
		10 Mbps	I_{CCA}, I_{CCB}		7.1		
		100 Mbps	I_{CCA}, I_{CCB} (1)		17.6		

(1) Provided by bench test and design simulation

(2) VCC_I is the VCC of V_I

Timing Specifications-2.5 V Supply

V_{CCA} = V_{CCB} = 2.5 V ± 10%, T_A = −40°C ~ +125°C. Typical value is in V_{CC} = 2.5 V, T_A = +25°C, C_L = 15 pF to GND.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{data}	Translation data rate				100	Mpbs
t_{PLH}	Propagation delay time			13.5		ns
t_{PHL}	Propagation delay time			12.2		ns
PWD	Pulse width distortion (1) $\lvert t_{PHL} - t_{PLH} \rvert$			1.3		ns
$t_{sk(CC)}$	Channel-to-channel output skew time (2)	Same direction channels			2.5	ns
$t_{sk(PP)}$	Channel-to-channel output skew time (2)	Same direction channels			4.5	ns
t_r	Output signal rise time (1)			0.7		ns
t_f	Output signal fall time (1)			0.7		ns
Jitter	Eye jitter p-p (1)	f_{data} = 100 Mbps		1000		ps
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below 1.7 V.		30		ns
t_{ie}	Time interval error (1)	216 − 1 PRBS data at 100 Mbps		2.4		ns
t_{su}	Setup time			28		μs

(1) Provided by bench test and design simulation.

(2) $t_{sk(CC)}$ & $t_{sk(PP)}$ is the shew of delay time between different channel of a single device or different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

Supply Current Characteristics-2.5 V Supply

V_{CCA} = V_{CCB} = 2.5 V ± 10%, T_A = −40°C ~ +125°C. Typical value is in V_{CC} = 2.5 V, T_A = +25°C, C_L = 15 pF to GND.

Parameter	Description		Supply current	Min	Typ	Max	Unit
TPT7740/TPT7741							
Supply current - DC signal	V_I = 0 V, V_I = VCC_I		I_{CCA}		1.5		mA
			I_{CCB}		3.1		
	V_I = VCC_I, V_I = 0 V		I_{CCA}		8.7		
			I_{CCB}		3.4		
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CCA}		6.1		
			I_{CCB}		3.5		
		10 Mbps	I_{CCA}		6.8		
			I_{CCB}		5.7		
		100 Mbps	I_{CCA} (1)		8.1		
			I_{CCB} (1)		15.3		
TPT7742							
Supply current - DC signal	V_I = 0 V, V_I = VCC_I		I_{CCA}, I_{CCB}		3.2		mA
	V_I = VCC_I, V_I = 0 V		I_{CCA}, I_{CCB}		8.3		
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CCA}, I_{CCB}		5.5		
		10 Mbps	I_{CCA}, I_{CCB}		6.9		
		100 Mbps	I_{CCA}, I_{CCB} (1)		12.7		

(1) Provided by bench test and design simulation

(2) VCC_I is the VCC of V_I

Test Circuits and Waveforms

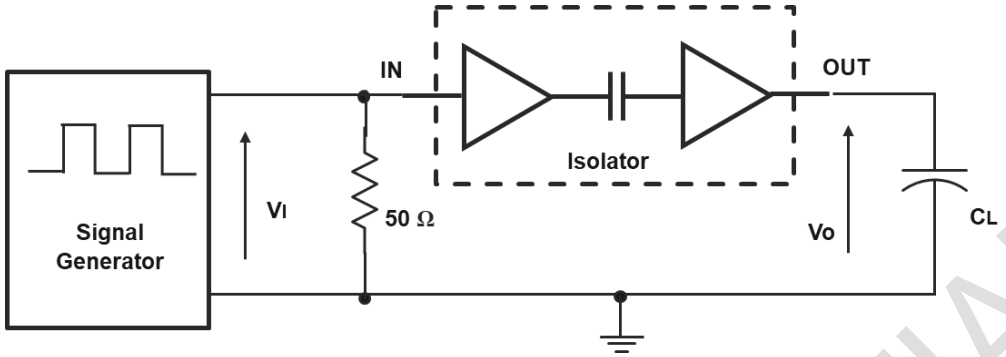


Figure 1 AC Characteristics Test Circuit

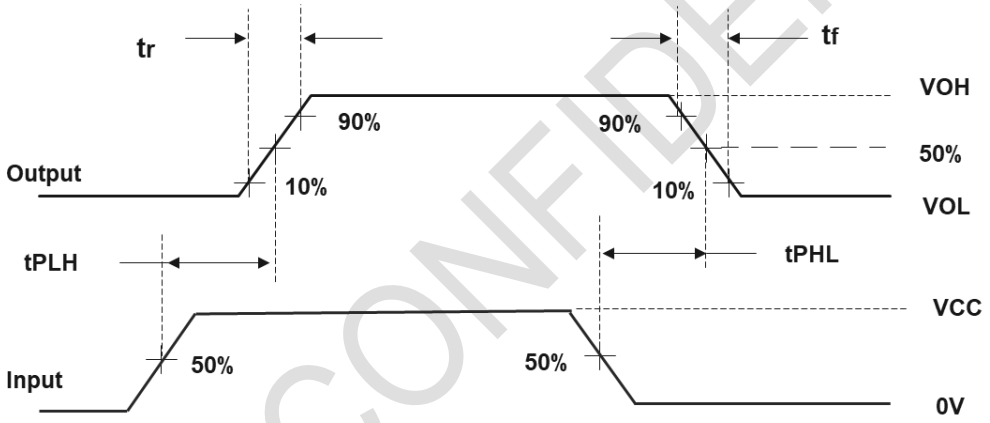


Figure 2 Timing Characteristics Voltage Waveforms

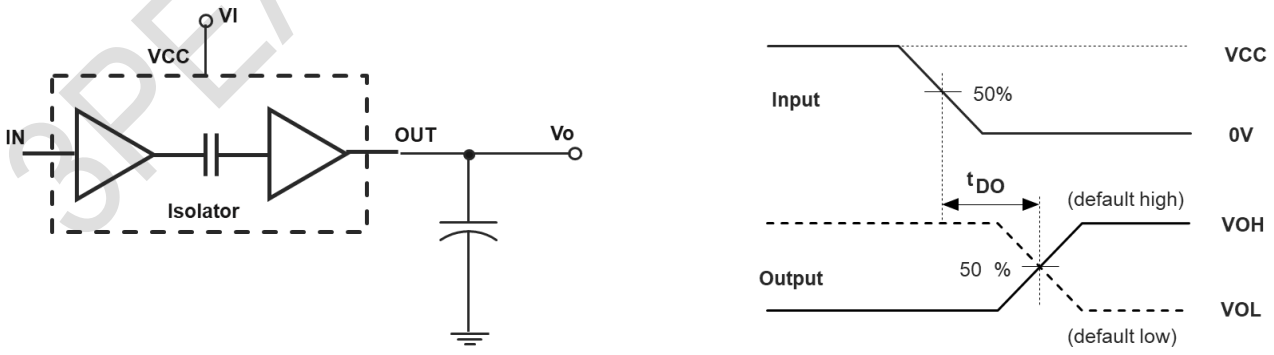


Figure 3 Default Output Delay Time Test Circuit and Voltage Waveforms

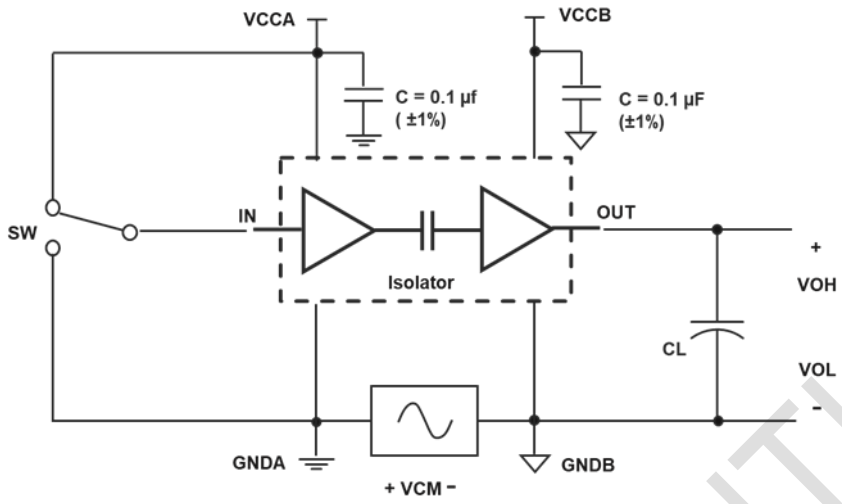


Figure 4 Common-Mode Transient Immunity Test Circuit

Detailed Description

Overview

The TPT774x family design an ON-OFF keying (OOK) modulation circuit to transmit the digital data by the isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage, which builds in an H-CMTI (High-performance Common-mode transient immunity) circuit to protect the normal signal transmission and minimize the radiated emissions due to the high-frequency carrier and IO buffer switching. The block diagram of a digital capacitive isolator shows a functional block diagram of a typical channel in Figure 12.

Function Block Diagram

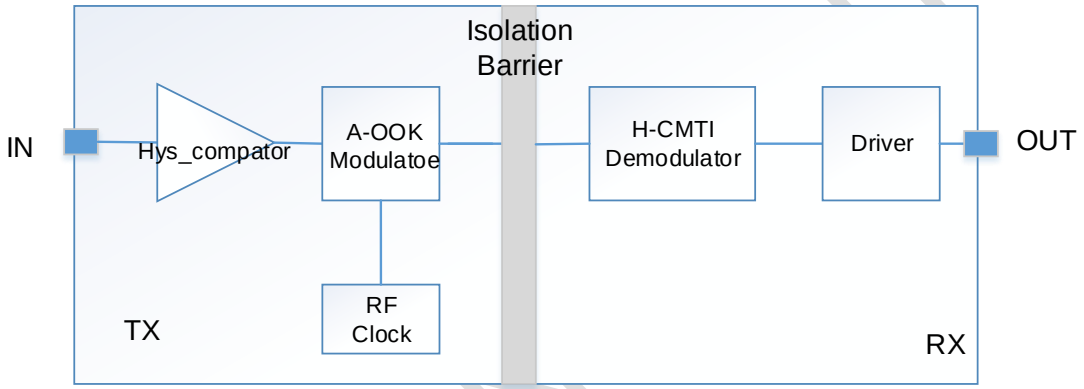


Figure 5 Conceptual Block Diagram of a Digital Capacitive Isolator

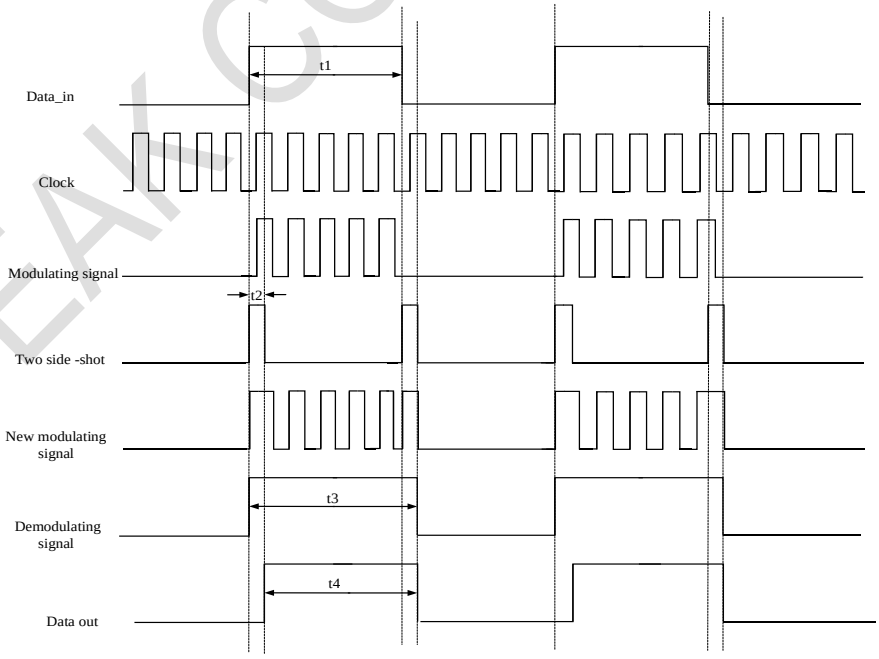


Figure 6 On-Off Keying (OOK) Based Modulation Scheme

Feature Description

The TPT774x family of devices is available in two channel configurations and default output state options to enable a variety of application uses. Table 1 lists the device features of the TPT774x devices.

Part Number	Max Data rate	Channel Direction	Default Output State	Package	Rating Isolation
TPT7740	100 Mbps	4 Forward, 0 Reverse	High	WSOP16	5000 V_{RMS} / 8000 V_{PK}
				SOP16	3750 V_{RMS} / 5250 V_{PK}
TPT7740F	100 Mbps	4 Forward, 0 Reverse	Low	WSOP16	5000 V_{RMS} / 8000 V_{PK}
				SOP16	3750 V_{RMS} / 5250 V_{PK}
TPT7741	100 Mbps	3 Forward, 1 Reverse	High	WSOP16	5000 V_{RMS} / 8000 V_{PK}
				SOP16	3750 V_{RMS} / 5250 V_{PK}
TPT7741F	100 Mbps	3 Forward, 1 Reverse	Low	WSOP16	5000 V_{RMS} / 8000 V_{PK}
				SOP16	3750 V_{RMS} / 5250 V_{PK}
TPT7742	100 Mbps	2 Forward, 2 Reverse	High	WSOP16	5000 V_{RMS} / 8000 V_{PK}
				SOP16	3750 V_{RMS} / 5250 V_{PK}
TPT7742F	100 Mbps	2 Forward, 2 Reverse	Low	WSOP16	5000 V_{RMS} / 8000 V_{PK}
				SOP16	3750 V_{RMS} / 5250 V_{PK}

Device Functional Modes

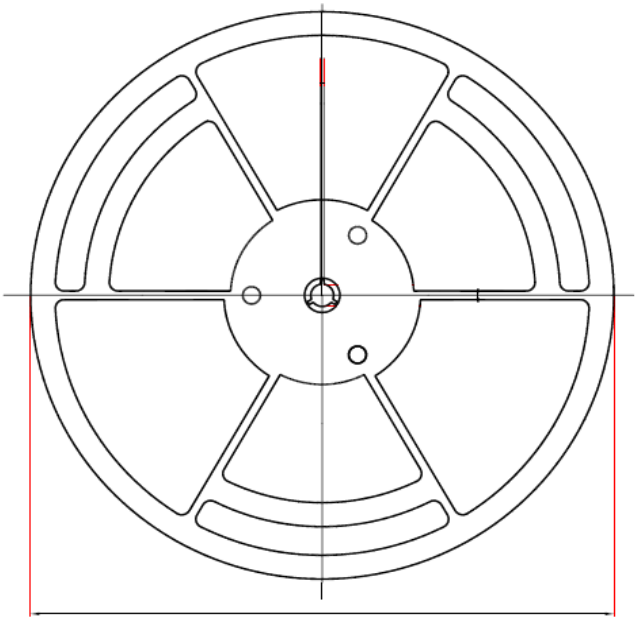
The below table lists the functional modes for the TPT774x devices.

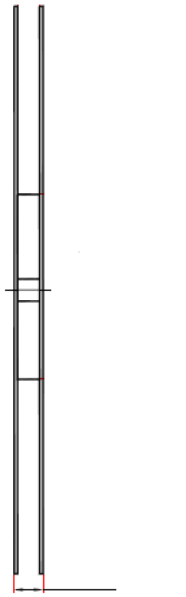
VCC_I	VCC_O	Input (IN1. IN2)	Output (OUT1, OUT2)	Comments
PU	PU	H	H	Normal Operation: A channel output assumes the logic state of the input.
		L	L	
		Open	Default	Default mode: When INx is open, the corresponding channel output goes to the default logic state. The default is High for TPT774x and Low for TPT774xF
PD	PU	X	Default	Default mode: When VCC_I is unpowered, the default is High for TPT774x and Low for TPT774xF When VCC_I transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When VCC_I transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	Undetermined	When VCC_O is unpowered, a channel output is undetermined. When VCC_O transitions from unpowered to powered-up, a channel output assumes the logic state of the input

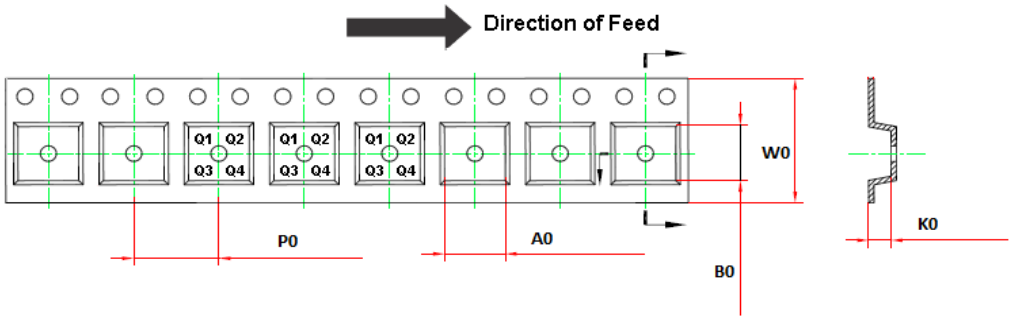
(1) VCC_I = Input-side V_{CCA}; VCC_O = Output-side V_{CCB}; PU = Powered up (V_{CC} ≥ 2.25 V); PD = Powered down (V_{CC} ≤ 1.7 V); X = Irrelevant; H = High level; L = Low level

(2) The outputs are in the undetermined state when 1.7 V < VCC_I, VCC_O < 2.25 V.

Tape and Reel Information



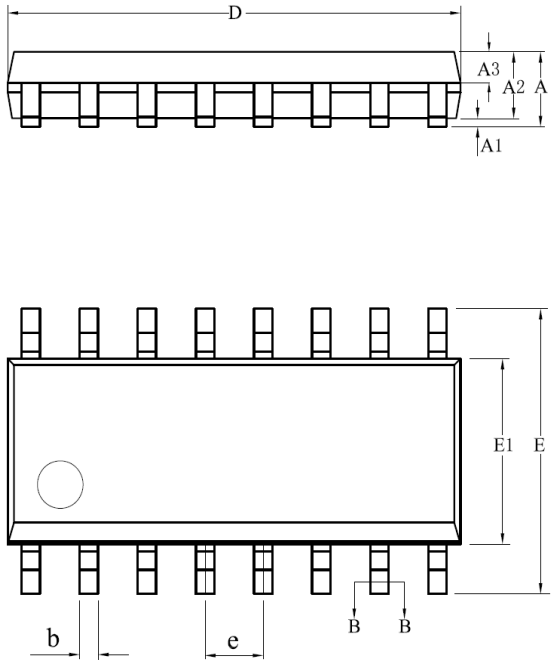




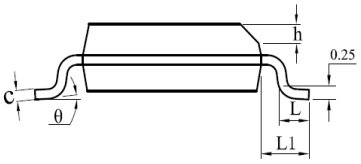
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPT7740-SO3R	16-Pin SOP	330	21.6	6.7	10.4	2.1	8.0	16.0	Q1
TPT7740F-SO3R	16-Pin SOP	330	21.6	6.7	10.4	2.1	8.0	16.0	Q1
TPT7741-SO3R	16-Pin SOP	330	21.6	6.7	10.4	2.1	8.0	16.0	Q1
TPT7741F-SO3R	16-Pin SOP	330	21.6	6.7	10.4	2.1	8.0	16.0	Q1
TPT7742-SO3R	16-Pin SOP	330	21.6	6.7	10.4	2.1	8.0	16.0	Q1
TPT7742F-SO3R	16-Pin SOP	330	21.6	6.7	10.4	2.1	8.0	16.0	Q1
TPT7740-SOBR	16-Pin WSOP	330	22.4	10.9	10.8	3.0	12.0	16.0	Q1
TPT7740F-SOBR	16-Pin WSOP	330	22.4	10.9	10.8	3.0	12.0	16.0	Q1
TPT7741-SOBR	16-Pin WSOP	330	22.4	10.9	10.8	3.0	12.0	16.0	Q1
TPT7741F-SOBR	16-Pin WSOP	330	22.4	10.9	10.8	3.0	12.0	16.0	Q1
TPT7742-SOBR	16-Pin WSOP	330	22.4	10.9	10.8	3.0	12.0	16.0	Q1
TPT7742F-SOBR	16-Pin WSOP	330	22.4	10.9	10.8	3.0	12.0	16.0	Q1

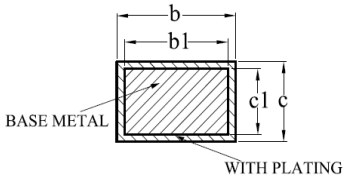
Package Outline Dimensions

SO3R (SOP-16)



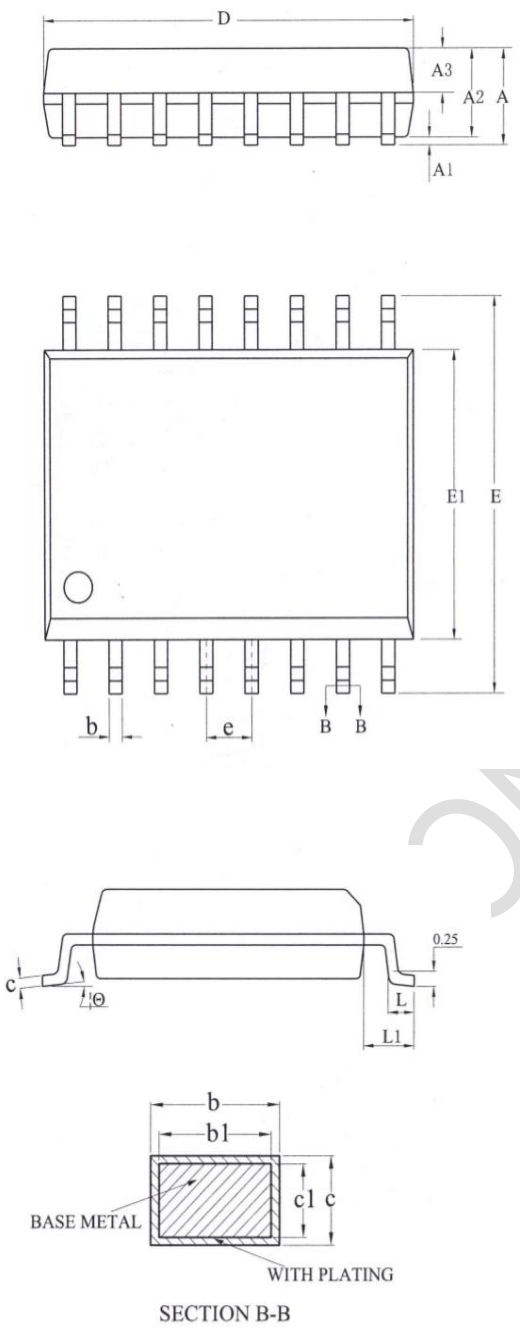
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°





SECTION B-B

SOBR (WSOP16)



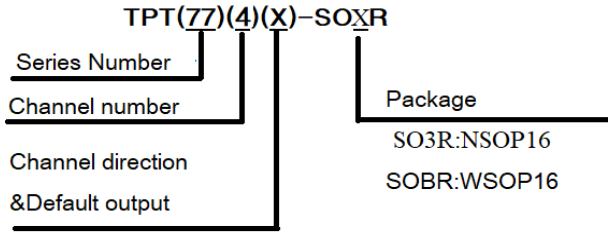
SYMBOL	MILLIMETER			
	MIN	NOM	MAX	
A	—	—	2.65	
A1	0.10	—	0.30	1 3
A2	2.25	2.30	2.35	
A3	0.97	1.02	1.07	
b	0.35	—	0.44	
b1	0.34	0.37	0.39	
c	0.25	—	0.31	
c1	0.24	0.25	0.26	
D	10.10	10.30	10.50	
E	10.26	10.41	10.60	2
E1	7.30	7.50	7.70	
e	1.27BSC			
L	0.55	—	0.85	
L1	1.40BSC			
θ	0	—	8°	

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPT7740-SO3R (1)	−40 to 125°C	16-Pin SOP	T7740	MSL3	Tape and Reel, 2500	Green
TPT7740F-SO3R (1)	−40 to 125°C	16-Pin SOP	7740F	MSL3	Tape and Reel, 2500	Green
TPT7741-SO3R (1)	−40 to 125°C	16-Pin SOP	T7741	MSL3	Tape and Reel, 2500	Green
TPT7741F-SO3R (1)	−40 to 125°C	16-Pin SOP	7741F	MSL3	Tape and Reel, 2500	Green
TPT7742-SO3R (1)	−40 to 125°C	16-Pin SOP	T7742	MSL3	Tape and Reel, 2500	Green
TPT7742F-SO3R (1)	−40 to 125°C	16-Pin SOP	7742F	MSL3	Tape and Reel, 2500	Green
TPT7740-SOBR (1)	−40 to 125°C	16-Pin WSOP	T7740	MSL3	Tape and Reel, 1500	Green
TPT7740F-SOBR (1)	−40 to 125°C	16-Pin WSOP	7740F	MSL3	Tape and Reel, 1500	Green
TPT7741-SOBR	−40 to 125°C	16-Pin WSOP	T7741	MSL3	Tape and Reel, 1500	Green
TPT7741F-SOBR	−40 to 125°C	16-Pin WSOP	7741F	MSL3	Tape and Reel, 1500	Green
TPT7742-SOBR (1)	−40 to 125°C	16-Pin WSOP	T7742	MSL3	Tape and Reel, 1500	Green
TPT7742F-SOBR (1)	−40 to 125°C	16-Pin WSOP	7742F	MSL3	Tape and Reel, 1500	Green

(1). Future product, contact 3PEAK factory for more information and sample

(2). Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.



40:4 Forward/0 Reverse,&OUT=H;
41:3 Forward/1 Reverse,&OUT=H;
42:2 Forward/2 Reverse,&OUT=H;
40F:4 forward/0 Reverse,&OUT=L;
41F:3 forward/1 Reverse,&OUT=L;
42F:2 forward/2 Reverse,&OUT=L;