AX7021B Development Board User Manual

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Alinx Electronic Limited has officially released the 2022 development board (model: AX7021B) based on the AMD ZYNQ7000 development platform. In order to help you quickly understand this development platform, we have compiled this user manual.

This ZYNQ7000 FPGA development platform adopts a SOM and base board mode, which facilitates users' secondary development and utilization of the SOM. The SOM uses AMD's Zynq7000 SOC chip solution, which integrates dual-core ARM Cortex-A9 and FPGA programmable logic on one chip using ARM + FPGA SOC technology. In addition, the SOM contains two 1GB high-speed DDR3 SDRAM chips, one 8GB eMMC storage chip, and one 256Mb QSPI FLASH chip.

We have expanded a rich range of peripheral interfaces for users in base board design, such as 5 Gigabit Ethernet interfaces, 4 USB2.0 HOST interfaces, 1 HDMI output interface, Uart communication interface, SD card holder, 40-pin expansion interface, etc. It meets users' requirements for various Ethernet high-speed data exchange, data storage, video transmission processing, and industrial control, and is a "professional-level" ZYNQ development platform. It provides the possibility for early verification and later application of high-speed Ethernet data transmission and exchange, data processing. We believe that such a product is very suitable for students, engineers, and other groups engaged in ZYNQ development.

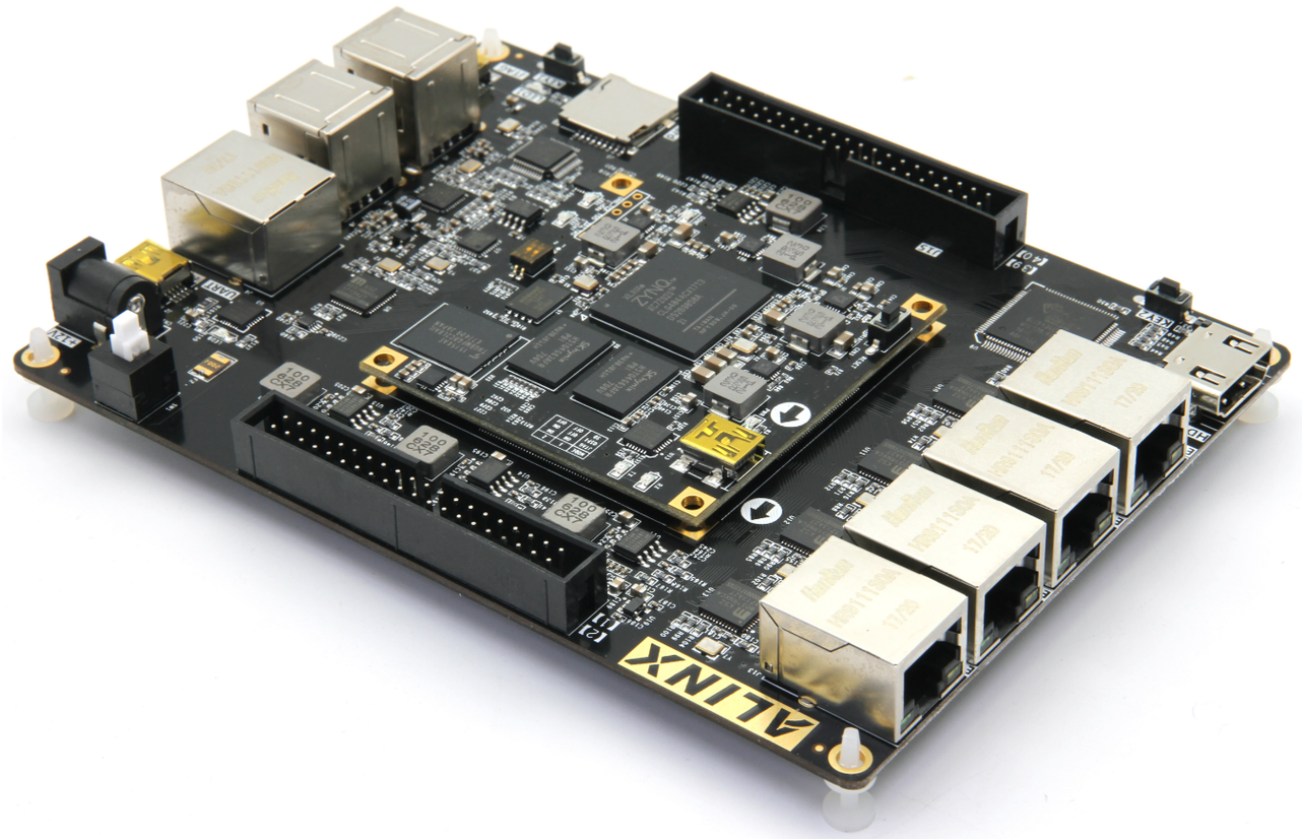


Figure 0-1-1 AX7021B development board

Part 1: Development board introduction

Here is a brief introduction to the functions of the AX7021B ZYNQ development platform.

The entire structure of the development board inherits our consistent SOM + base board pattern. The SOM and base board are connected by high-speed board-to-board connectors.

The SOM is mainly composed of a minimum system of ZYNQ7020 + 2 DDR3 + eMMC + QSPI FLASH, which undertakes the high-speed data processing and storage functions of the ZYNQ system. The data bit width between ZYNQ7020 and the two DDR3 chips is 32 bits, and the capacity of the two DDR3 chips is as high as 1GB. The 8GB eMMC FLASH storage chip and the 256Mb QSPI FLASH are used to statically store the operating system, file system, and user data of ZYNQ. Users can choose different startup methods through the DIP switch on the SOM. ZYNQ7020 uses AMD's Zynq7000 series chip, model XC7Z020-2CLG484I. The ZYNQ7020 chip can

be divided into a processor system part, Processor System (PS), and a programmable logic part, Programmable Logic (PL).

The base board has expanded the SOM with rich peripheral interfaces, including 5 Gigabit Ethernet interfaces, 4 USB2.0 HOST interfaces, 1 HDMI output interface, 1 SD Card interface, 1 UART USB interface, 1 SD card interface, 2 40-pin expansion ports, and some button LEDs.

The following is a schematic diagram of the structure of the entire development system.

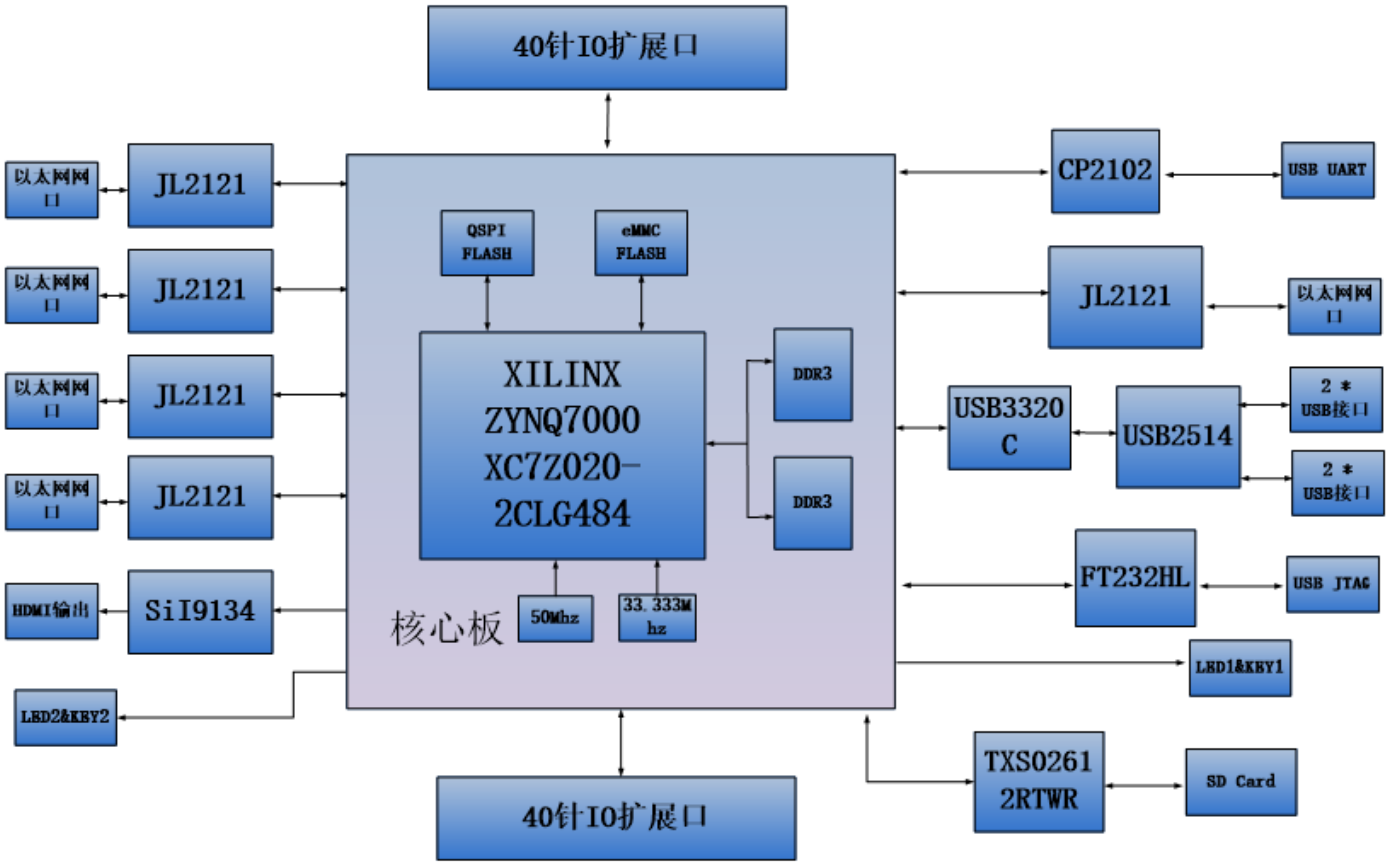


Figure 1-1-1 schematic diagram of AX7021B development board structure

Through this diagram, we can see the interfaces and functions that our development platform can contain.

- ZYNQ7000 SOM

It consists of XC7Z020 + 1GB DDR3 + 8GB eMMC FLASH + 256Mb QSPI FLASH. In addition, there are two crystal oscillators providing clocks, one is 33.3333MHz for the PS system, and the other is 50MHz for the PL logic.

- Gigabit Ethernet interface

5 10/100M/1000M Ethernet RJ45 interfaces are used for exchanging Ethernet data with computers or other network devices. The network interface chip uses Jinglue's JL2121 industrial-grade GPHY chip, with 1 Ethernet connection to the PS end of the ZYNQ chip and 4 Ethernet connections to the PL end of the ZYNQ chip.

- HDMI display output

1 channel HDMI output interface, we use SIL9134 HDMI coding chip of Silion Image company, the highest support 1080P@60Hz output, support 3D output.

- USB Uart interface

2-Way Uart to USB interface for communication with computer, convenient for user debugging. 1-Way is on the SOM, which works independently, and 1-Way is on the base board, which is used for whole board debugging. The serial port chip uses Silicon Labs CP2102GM USB-UAR chip, and the USB interface uses MINI USB interface.

- Micro SD card holder

1-Way Micro SD card holder for storing operating system mirroring and file systems.

- 40-Pin expansion port

Two 40-pin 2.54mm spacing expansion ports can be used to connect various Alinx modules (binocular cameras, TFT LCD screens, high-speed AD modules, etc.). The expansion ports include 1 5V power supply, 2 3.3V power supplies, 3 ground ports, and 34 IO ports.

- USB JTAG port

1 JTAG debugging interface, using MINI USB interface, users can debug and download the ZYNQ system through USB cable and onboard JTAG circuit.

- LED lights

9 Light Emitting Diode LEDs, 6 on the SOM and 3 on the base board. 1 power indicator light on the SOM, 1 DONE configuration indicator light, 2 user indicator lights, and 2 serial port transceiver indicator lights. There is 1 power indicator light and 2 user indicator lights on the base board.

- Button

3 buttons, 1 reset button on the SOM, 2 user buttons on the base board.

Part 2: **AC7021B SOM**

1. Introduction

AC7021B (**SOM model, the same below**) SOM, ZYNQ chip is based on AMD's ZYNQ7000 series XC7Z020-2CLG484I. The PS system of ZYNQ chip integrates two ARM Cortex ™ - A9 processors,

AMBA ® interconnect, internal memory, external memory interface and peripherals. The FPGA of ZYNQ chip contains rich programmable logic units, DSP and internal RAM.

This SOM uses two SK Hynix H5TQ4G63AFR-PBI DDR3 chips, each with a DDR capacity of 4Gbit. The two DDR chipsets combine a 32-bit data bus width, and the read and write data clock frequency between ZYNQ and DDR3 is as high as 533Mhz. This configuration can meet the high-bandwidth data processing needs of the system.

In order to connect with the base board, the four board-to-board connectors of this SOM have expanded the USB interface, Gigabit Ethernet interface, SD card interface, and other remaining MIO ports on the PS side. In addition, almost all IO ports (198) of BANK13, BANK33, BAN34, and BANK35 on the PL side can be modified by replacing the LDO chip on the SOM to meet the requirements of users who do not need level interfaces. For users who need a large amount of IO, this SOM will be a good choice. Moreover, the IO connection part, the wiring between the ZYNQ chip and the interface has been processed equally and differentially, and the SOM size is only 60 * 60 (mm), which is very suitable for secondary development.

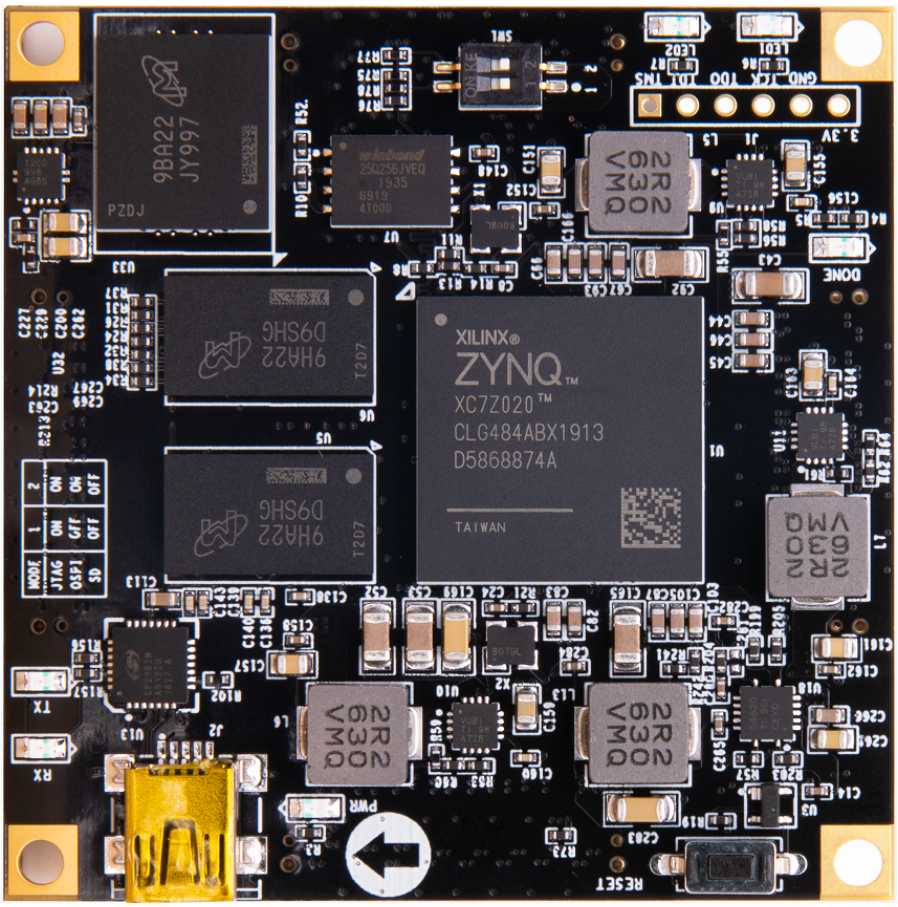


Figure 2-1-1 AC7021B SOM Front View

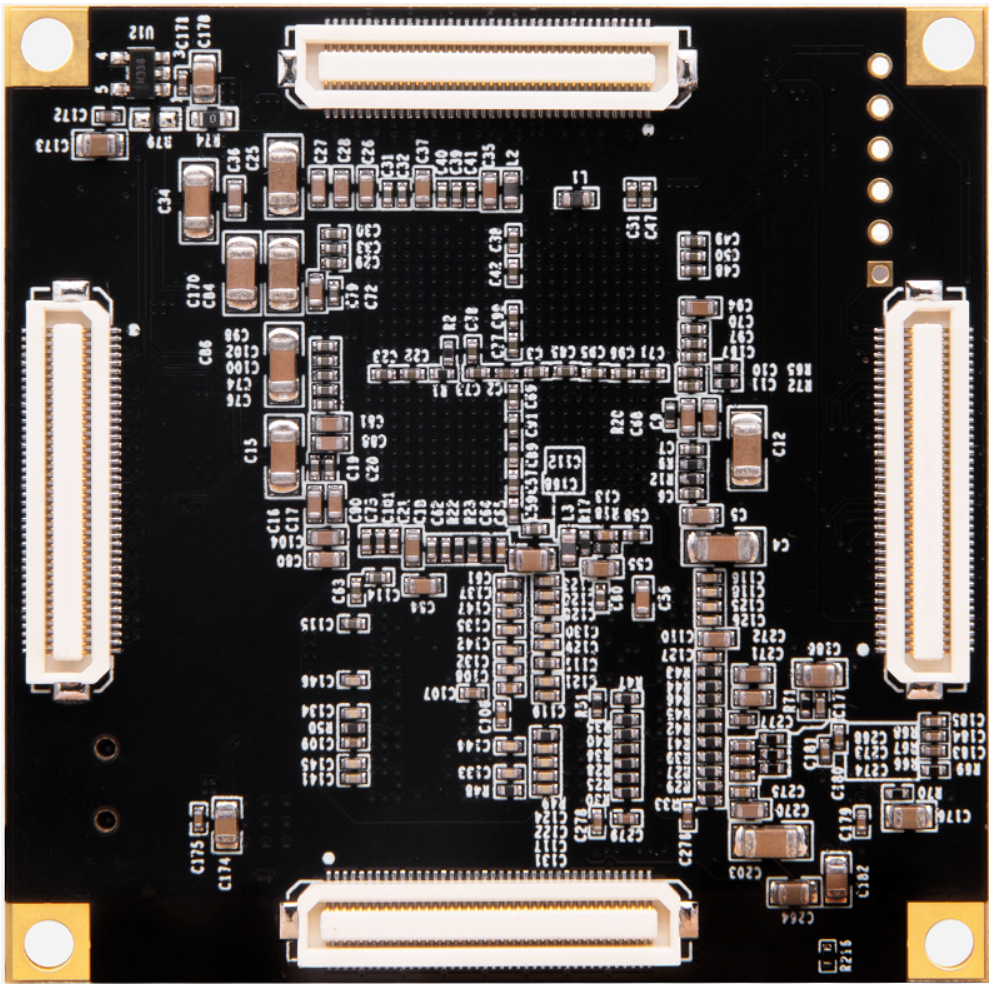


Figure 2-1-2 AC7021B SOM Back View

2. ZYNQ chip

The development board uses AMD's Zynq7000 series chip, model XC7Z020-2CLG484I. The PS system of the chip integrates two ARM Cortex ™ - A9 processors, AMBA ® interconnect, internal memory, external memory interface and peripherals. These peripherals mainly include USB bus interface, Ethernet interface, SD/SDIO interface, I2C bus interface, CAN bus interface, UART interface, GPIO, etc. PS can run independently and start under power-on or reset. The overall block diagram of the ZYNQ7000 chip is shown in Figure 2-2-1

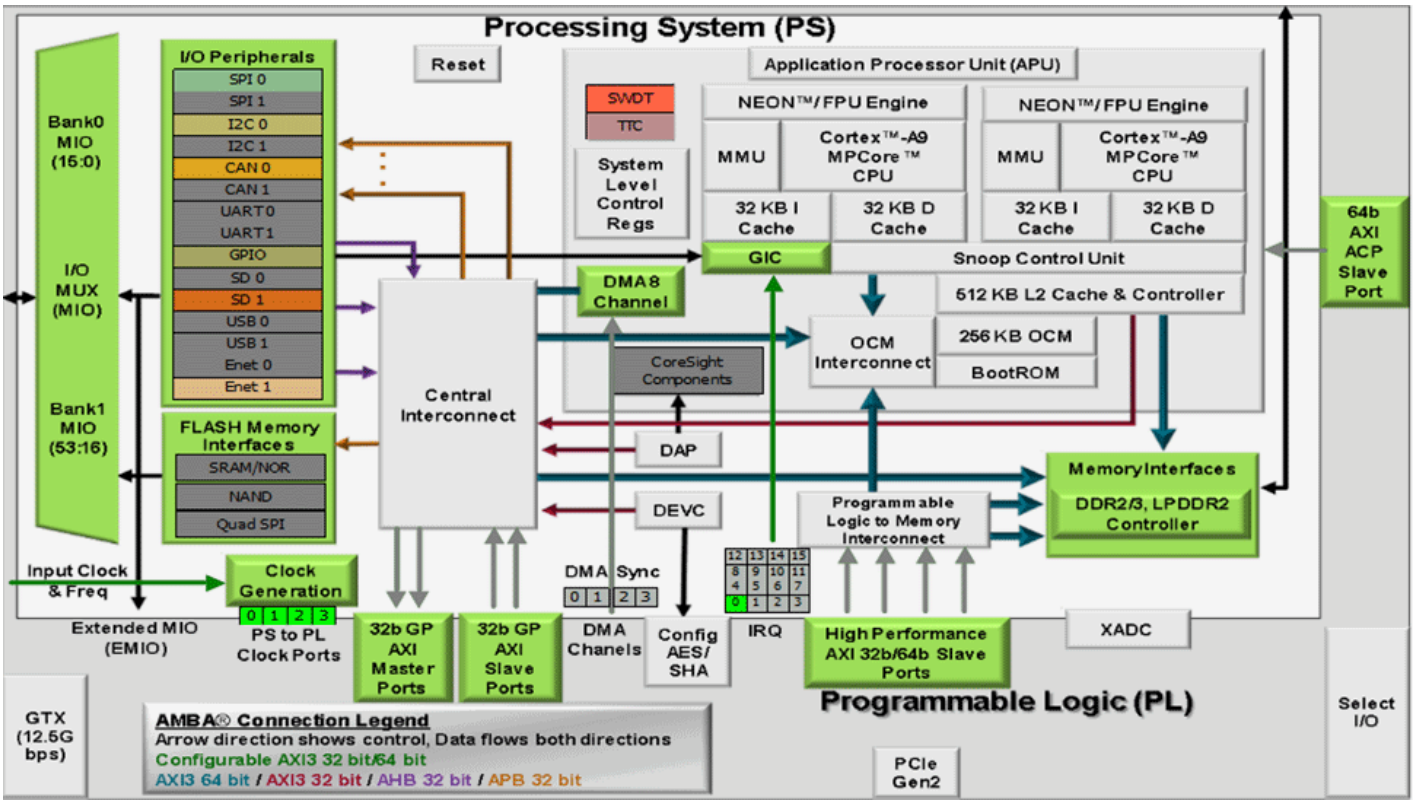


Figure 2-2-1 General block diagram of ZYNQ7000 chip

The main parameters of the PS system are as follows:

- Application processor based on ARM dual-core CortexA9, ARM-v7 architecture, up to 1GHz
- 32KB level 1 instruction and data cache per CPU, 512KB level 2 cache shared by 2 CPUs
- On-chip boot ROM and 256KB on-chip RAM
- External storage interface, supporting 16/32 bit DDR2 and DDR3 interfaces
- Two gigabit network interface cards support: divergent-aggregate DMA, GMII, RGMII, SGMII interfaces
- Two USB2.0 OTG interfaces, each supporting up to 12 nodes
- Two CAN2.0B bus interfaces
- Two SD cards, SDIO, MMC compatible controllers
- 2 SPI, 2 UARTs, 2 I2C interfaces
- 4 groups of 32-bit GPIO, 54 (32 + 22) as PS system IO, 64 connected to PL
- High bandwidth connections within PS and from PS to PL

The main parameters of the PL logic part are as follows:

- Logic Cells: 85K;
- Look up table LUTs: 53,200

- Triggers (flip-flops): 106,400
- Multiplier 18x25MACCs: 220;
- Block RAM：4.9Mb；
- Two AD converters can measure on-chip voltage, temperature sensing, and up to 17 external differential input channels, 1MBPS.

The speed level of XC7Z020-2CLG484I chip is -2, industrial grade, packaged as BGA484, pin spacing is 0.8mm. The specific chip model definition of ZYNQ7000 series is shown in the following figure 2-2-2.

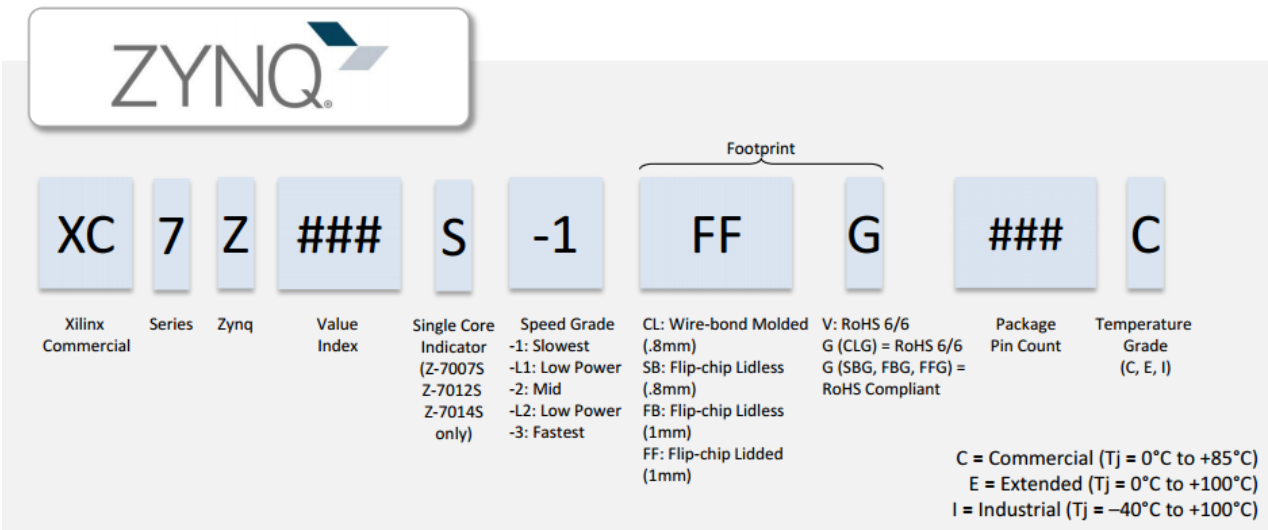


Figure 2-2-2 ZYNQ model naming rule definition

3. DDR3 DRAM

The AC7021B SOM is equipped with two Micron DDR3 SDRAM chips (a total of 1GB), model MT41K256M16TW-107 (compatible with H5TQ4G63AFR-PBI). The bus width of DDR3 SDRAM is 32 bits. The maximum operating speed of DDR3 SDRAM can reach 533MHz (data rate 1066Mbps). The DDR3 storage system is directly connected to the memory interface of BANK 502 in the ZYNQ processing system (PS). The specific configuration of DDR3 SDRAM is shown in the following table 2-3-1.

Locus number	Chip model	Capacity	Manufacturer
U5,U6	MT41K256M16TW-107	256M x 16bit	Micron

Table 2-3-1 DDR3 SDRAM Configuration

The hardware design of DDR3 requires strict consideration of signal integrity. We have fully considered matching resistors/end point resistors, wiring impedance control, and wiring length control in circuit design and PCB design to ensure the high-speed and stable operation of DDR3.

The hardware connection of DDR3 DRAM is shown in Figure 2-3-1:

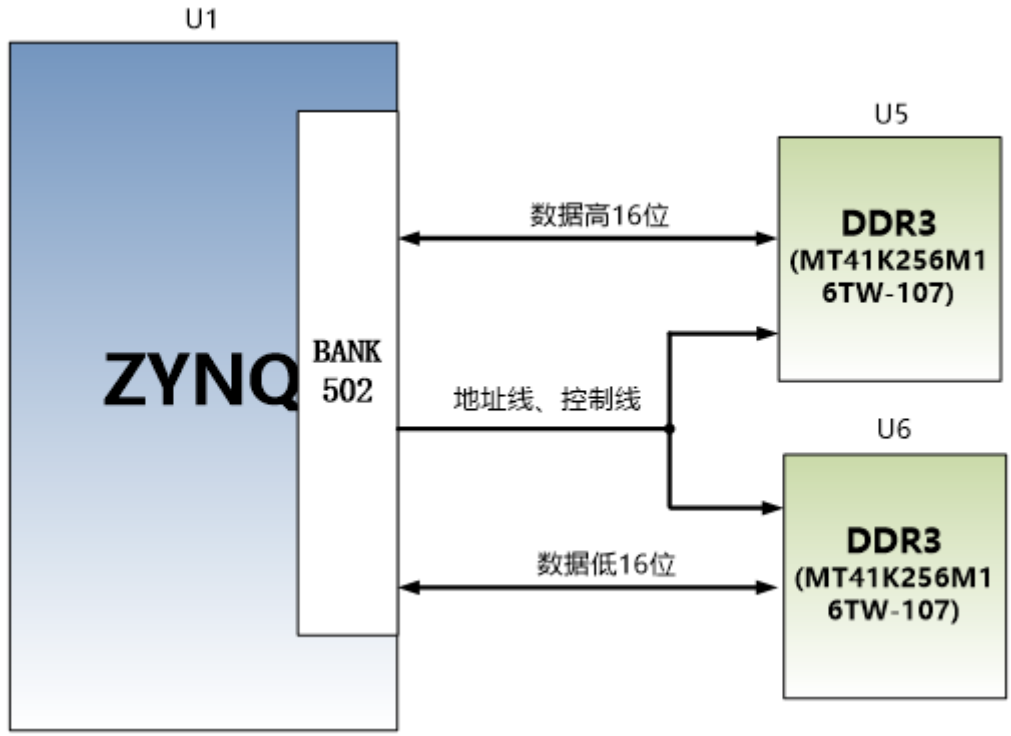


Figure 2-3-1 DDR3 DRAM schematic part

DDR3 DRAM pin allocation:

Signal name	ZYNQ pin name	ZYNQ pin number
DDR3_DQS0_P	PS_DDR_DQS_P0_502	C2
DDR3 _ DQS0 _ N	PS_DDR_DQS_N0_502	D2
DDR3_DQS1_P	PS_DDR_DQS_P1_502	H2
DDR3 _ DQS1 _ N	PS_DDR_DQS_N1_502	J2
DDR3_DQS2_P	PS_DDR_DQS_P2_502	N2
DDR3 _ DQS2 _ N	PS_DDR_DQS_N2_502	P2
DDR3_DQS3_P	PS_DDR_DQS_P3_502	V2
DDR3 _ DQS4 _ N	PS_DDR_DQS_N3_502	W2
DDR3_D0	PS_DDR_DQ0_502	D1

DDR3_D1	PS_DDR_DQ1_502	C3
DDR3_D2	PS_DDR_DQ2_502	B2
DDR3_D3	PS_DDR_DQ3_502	D3
DDR3_D4	PS_DDR_DQ4_502	E3
DDR3_D5	PS_DDR_DQ5_502	E1
DDR3_D6	PS_DDR_DQ6_502	F2
DDR3_D7	PS_DDR_DQ7_502	F1
DDR3_D8	PS_DDR_DQ8_502	G2
DDR3_D9	PS_DDR_DQ9_502	G1
DDR3_D10	PS_DDR_DQ10_502	L1
DDR3_D11	PS_DDR_DQ11_502	L2
DDR3_D12	PS_DDR_DQ12_502	L3
DDR3_D13	PS_DDR_DQ13_502	K1
DDR3_D14	PS_DDR_DQ14_502	J1
DDR3_D15	PS_DDR_DQ15_502	K3
DDR3_D16	PS_DDR_DQ16_502	M1
DDR3_D17	PS_DDR_DQ17_502	T3
DDR3_D18	PS_DDR_DQ18_502	N3
DDR3_D19	PS_DDR_DQ19_502	T1
DDR3_D20	PS_DDR_DQ20_502	R3
DDR3_D21	PS_DDR_DQ21_502	T2
DDR3_D22	PS_DDR_DQ22_502	M2
DDR3_D23	PS_DDR_DQ23_502	R1
DDR3_D24	PS_DDR_DQ24_502	AA3
DDR3_D25	PS_DDR_DQ25_502	U1
DDR3_D26	PS_DDR_DQ26_502	AA1

DDR3_D27	PS_DDR_DQ27_502	U2
DDR3_D28	PS_DDR_DQ28_502	W1
DDR3_D29	PS_DDR_DQ29_502	Y3
DDR3_D30	PS_DDR_DQ30_502	W3
DDR3_D31	PS_DDR_DQ31_502	Y1
DDR3_DM0	PS_DDR_DM0_502	B1
DDR3_DM1	PS_DDR_DM1_502	H3
DDR3_DM2	PS_DDR_DM2_502	P1
DDR3_DM3	PS_DDR_DM3_502	AA2
DDR3_A0	PS_DDR_A0_502	M4
DDR3_A1	PS_DDR_A1_502	M5
DDR3_A2	PS_DDR_A2_502	K4
DDR3_A3	PS_DDR_A3_502	L4
DDR3_A4	PS_DDR_A4_502	K6
DDR3_A5	PS_DDR_A5_502	K5
DDR3_A6	PS_DDR_A6_502	J7
DDR3_A7	PS_DDR_A7_502	J6
DDR3_A8	PS_DDR_A8_502	J5
DDR3_A9	PS_DDR_A9_502	H5
DDR3_A10	PS_DDR_A10_502	J3
DDR3_A11	PS_DDR_A11_502	G5
DDR3_A12	PS_DDR_A12_502	H4
DDR3_A13	PS_DDR_A13_502	F4
DDR3_A14	PS_DDR_A14_502	G4
DDR3_BA0	PS_DDR_BA0_502	L7
DDR3_BA1	PS_DDR_BA1_502	L6

DDR3_BA2	PS_DDR_BA2_502	M6
DDR3_S0	PS_DDR_CS_B_502	P6
DDR3_RAS	PS_DDR_RAS_B_502	R5
DDR3_CAS	PS_DDR_CAS_B_502	P3
DDR3_WE	PS_DDR_WE_B_502	R4
DDR3_ODT	PS_DDR_ODT_502	P5
DDR3_RESET	PS_DDR_DRST_B_502	F3
DDR3_CLK0_P	PS_DDR_CKP_502	N4
DDR3_CLK0_N	PS_DDR_CKN_502	N5
DDR3_CKE	PS_DDR_CKE_502	V3

Table 2-3-2 DDR4 SDRAM Configuration

4. QSPI Flash

The SOM is equipped with a 256MBit Quad-SPI FLASH chip, model W25Q256FVEI, which uses the 3.3V CMOS voltage standard. Due to the non-volatile characteristics of QSPI FLASH, it can be used as a system startup device to store system startup mirroring. These mirroring mainly include FPGA bit files, ARM application code, and other user data files. The specific model and related parameters of QSPI FLASH are shown in Table 2-4-1.

Locus number	Chip type	Capacity	Manufacturer
U7	W25Q256FVEI	32M Byte	Winbond

Table 2-4-1 QSPI Flash models and parameters

QSPI FLASH is connected to the GPIO port of the PS part of the ZYNQ chip BANK500. In the system design, it is necessary to configure the GPIO port function of these PS ends as the QSPI FLASH interface. As shown in Figure 2-4-1 is the part of QSPI Flash in the schematic diagram.

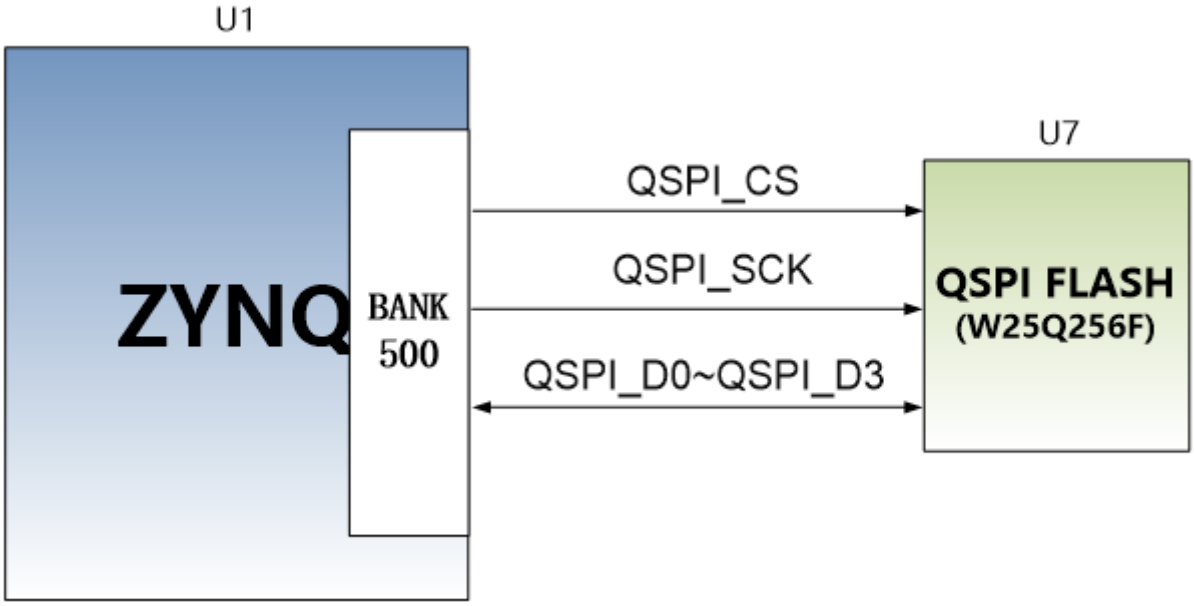


Figure 2-4-1 QSPI Flash connection diagram

Configure chip pin allocation:

Signal name	ZYNQ pin name	ZYNQ pin number
QSPI_SCK	PS_MIO6_500	A4
QSPI_CS	PS_MIO1_500	A1
QSPI_D0	PS_MIO2_500	A2
QSPI_D1	PS_MIO3_500	F6
QSPI_D2	PS_MIO4_500	E4
QSPI_D3	PS_MIO5_500	A3

Table 2-4-2 QSPI Flash pin assignments

5. eMMC Flash

The SOM is equipped with a large-capacity 8GB eMMC FLASH chip, model MTFC8GAKAJCN-4MIT\FEMDRW008G-88A39（both are compatible with board, subject to shipment for specific types）, which supports the HS-MMC interface of JEDEC e-MMC V5.0 standard, and the level supports 1.8V or 3.3V. The data width of eMMC FLASH and ZYNQ connection is 4 bits. Due to the large capacity and non-volatile characteristics of eMMC FLASH, it can be used as a large-capacity storage device in ZYNQ system, such as storing ARM applications, system files, and other user data files. The specific model and related parameters of eMMC FLASH are shown in Table 2-5-1.

Locus number	Chip type	capacity	manufacturer
U33	FEMDRW008G-88A39 MTFC8GAKAICN-4MIT	8G Byte	Micron Longsys

Table 2-5-1 eMMC Flash models and parameters

The eMMC FLASH is connected to the GPIO port of the PS part of the ZYNQ chip BANK501, and the GPIO port function of these PS ends needs to be configured as the SD interface in the system design. As shown in the figure 2-5-1 is the part of the eMMC Flash in the schematic diagram.

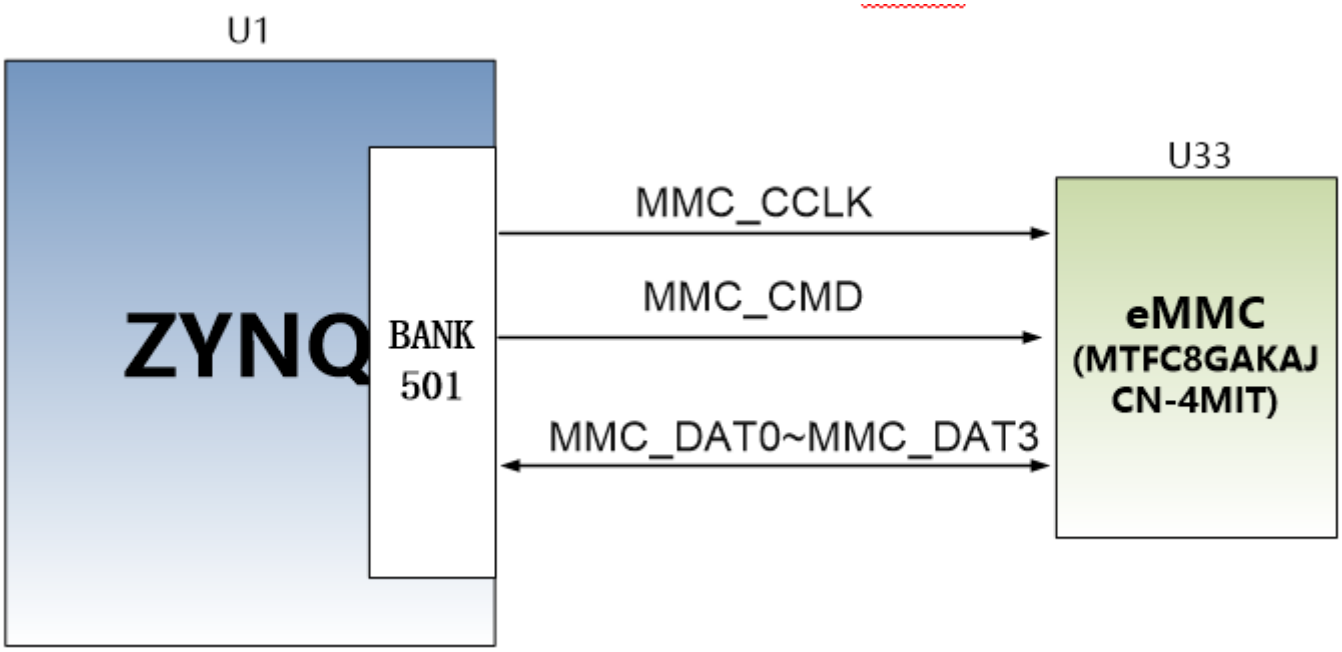


Figure 2-5-1 eMMC Flash connection diagram

Configure chip pin allocation:

Signal name	ZYNQ pin name	ZYNQ pin number
MMC_CCLK	PS_MIO48_501	D11
MMC_CMD	PS_MIO47_501	B10
MMC_D0	PS_MIO46_501	D12
MMC_D1	PS_MIO49_501	C14

MMC_D2	PS_MIO50_501	D13
MMC_D3	PS_MIO51_501	C10

Table 2-5-2 eMMC Flash Pin Allocation

6. Clock configuration

The AC7021B SOM provides active clocks for the PS system and PL logic, allowing the PS system and PL logic to work independently.

PS system clock source

The ZYNQ chip provides a 33.333MHz clock input for the PS part through the X1 crystal oscillator on the development board. The clock input is connected to the PS_CLK_500 pin of the BANK500 of the ZYNQ chip. Its schematic is shown in Figure 2-6-1:

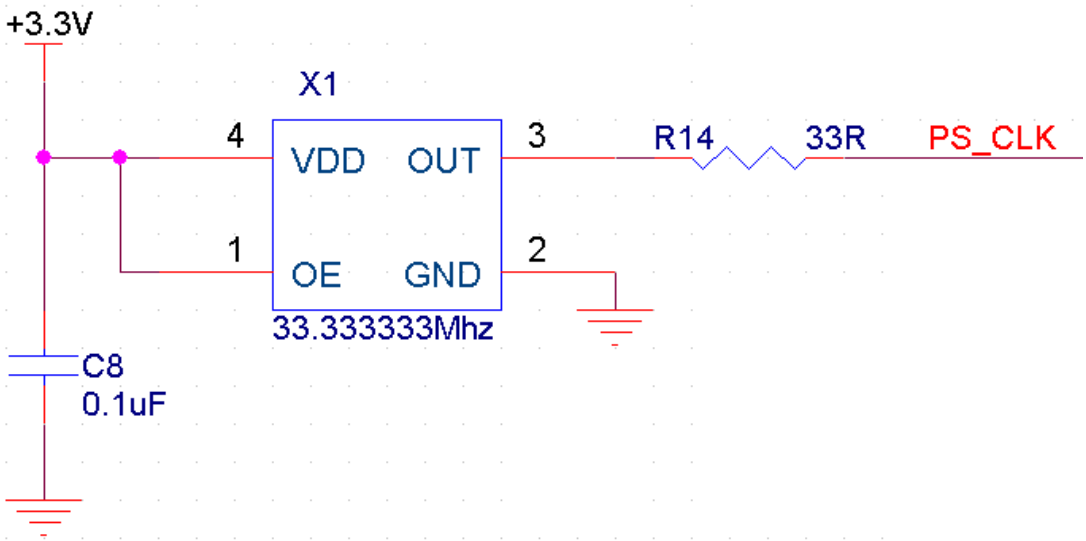


Figure 2-6-1 Active crystal oscillator in the PS section

Clock pin allocation:

Signal name	ZYNQ pin
PS_CLK_500	**F7**

Table 2-6-1 PS Clock Pin Allocation

4.2 PL system clock source

The AC7021B SOM provides a single-ended 50MHz PL system clock source with a 3.3V power supply. The crystal oscillator output is connected to the timestamp oracle (MRCC) of the FPGA BANK13, which can be used to drive user logic circuits in the FPGA. The schematic of the clock source is shown in Figure 2-6-3

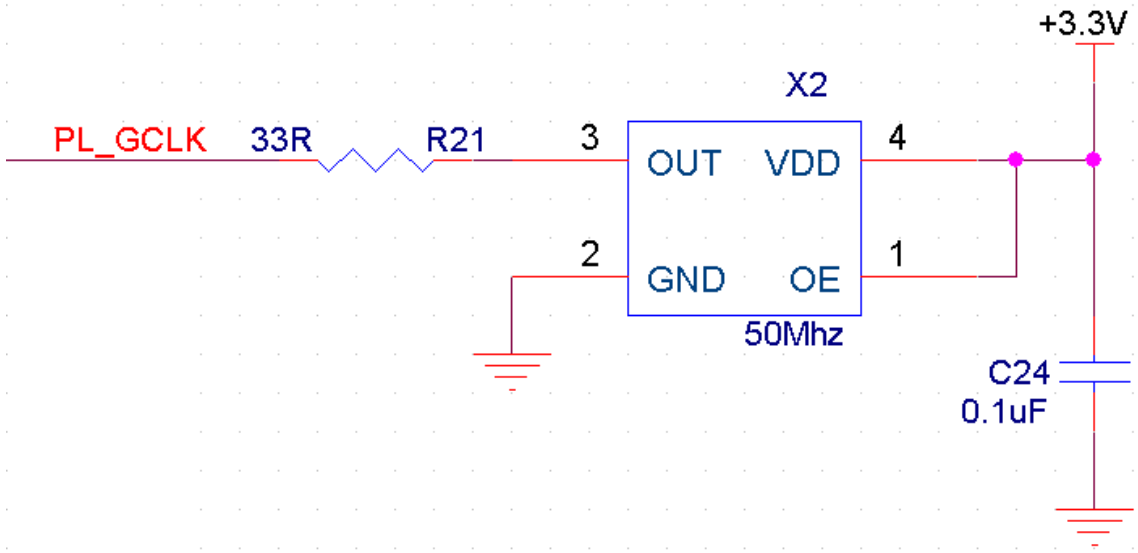


Figure 2-6-3 PL system clock source

PL clock pin allocation:

Signal name	ZYNQ pin
PL_GCLK	Y9

Table 2-6-2 PL Clock Pin Allocation

7. USB to serial port

In order for the AC7021B SOM to work and debug independently, we have equipped the SOM with a Uart to USB interface for separate power supply and debugging. The conversion chip uses the USB-UAR chip of Silicon Labs CP2102GM, and the USB interface uses the MINI USB interface. It can be connected to the USB port of the upper PC with a USB cable for separate power supply and serial data communication of the SOM.

The schematic diagram of USB Uart circuit design is shown in the following figure.

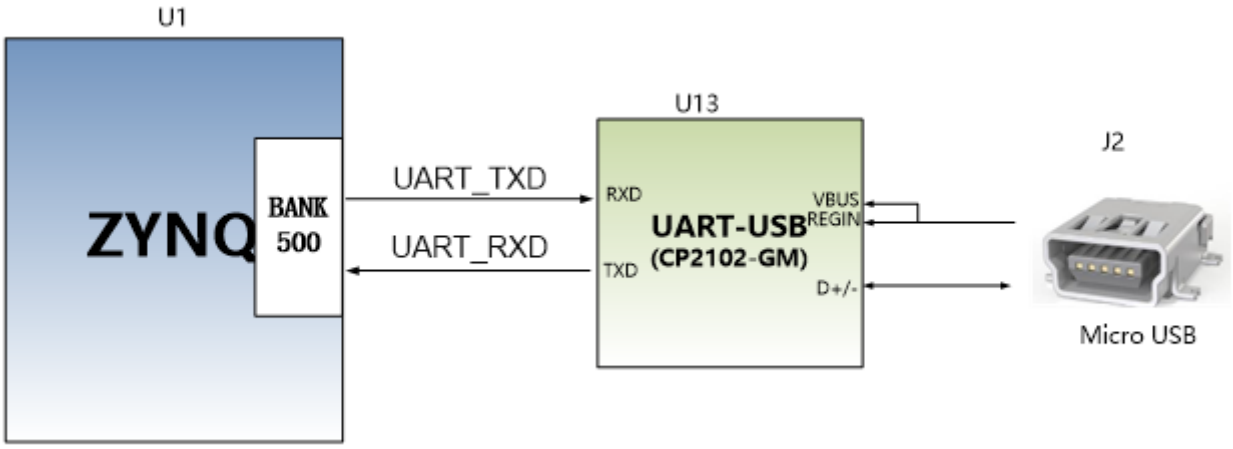
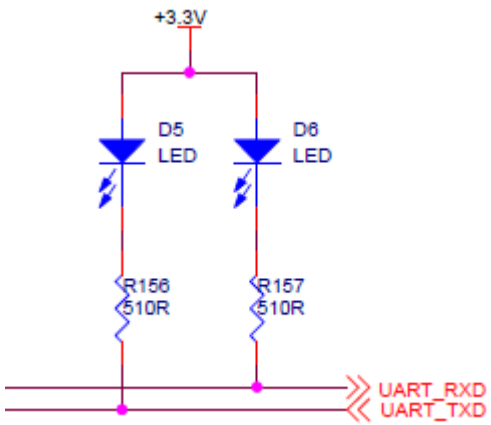


Figure 2-7-1 schematic diagram of USB to serial port

At the same time, two LED indicator lights (D5 and D6) with screen prints of RX and TX on the PCB are set for the serial port signal. The RX and TX LED lights will indicate whether the serial port has received or sent data, as shown in the figure below.



2-7-3 USB to serial signal indicator

ZYNQ pin allocation for UART to serial port:

Signal name	ZYNQ pin name	ZYNQ pin number	Remarks
UART_RXD	PS_MIO14_500	B6	Uart data entry
UART_TXD	PS_MIO15_500	E6	Uart data output

Table 2-7-1 USB to Serial Pin Allocation

8. LED lights

There are 6 red LED lights on the AC7021B SOM, including 1 power indicator light (PWR), 1 configuration LED light (DONE), 2 user LED lights (LED1~ LED2), and the other two UART transmit and receive indicator lights (TX, RX). When the SOM is powered, the power indicator light will light up; when the FPGA configuration program is completed, the configuration LED light will light up. One user LED light is connected to the MIO of PS, and the other is connected to the IO of PL. Users can control the on and off through the program. When the IO voltage of the user LED light is high, the user LED light will turn off, and when the IO voltage is low, the user LED will light up. The schematic diagram of the hardware connection of the LED lamp is shown in Figure 2-8-1:

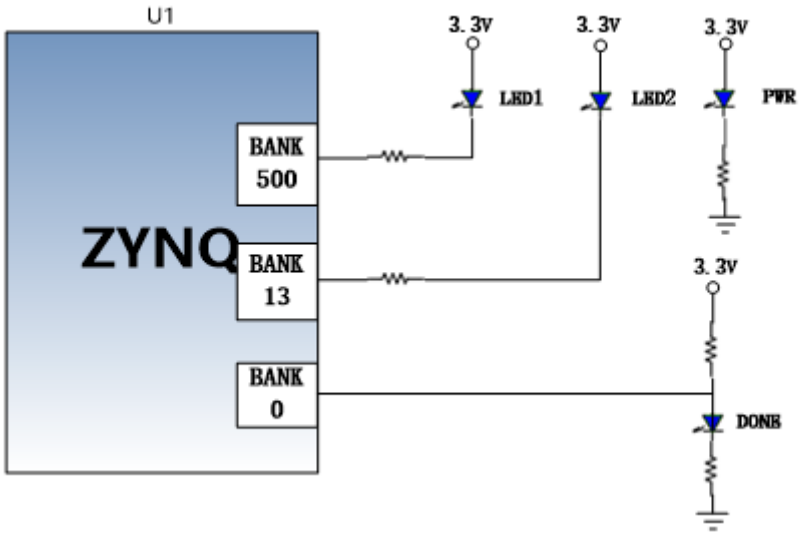


Figure 2-8-1 SOM LED lamp hardware connection schematic

Figure 2-8-2 is the actual picture of the LED light on the SOM

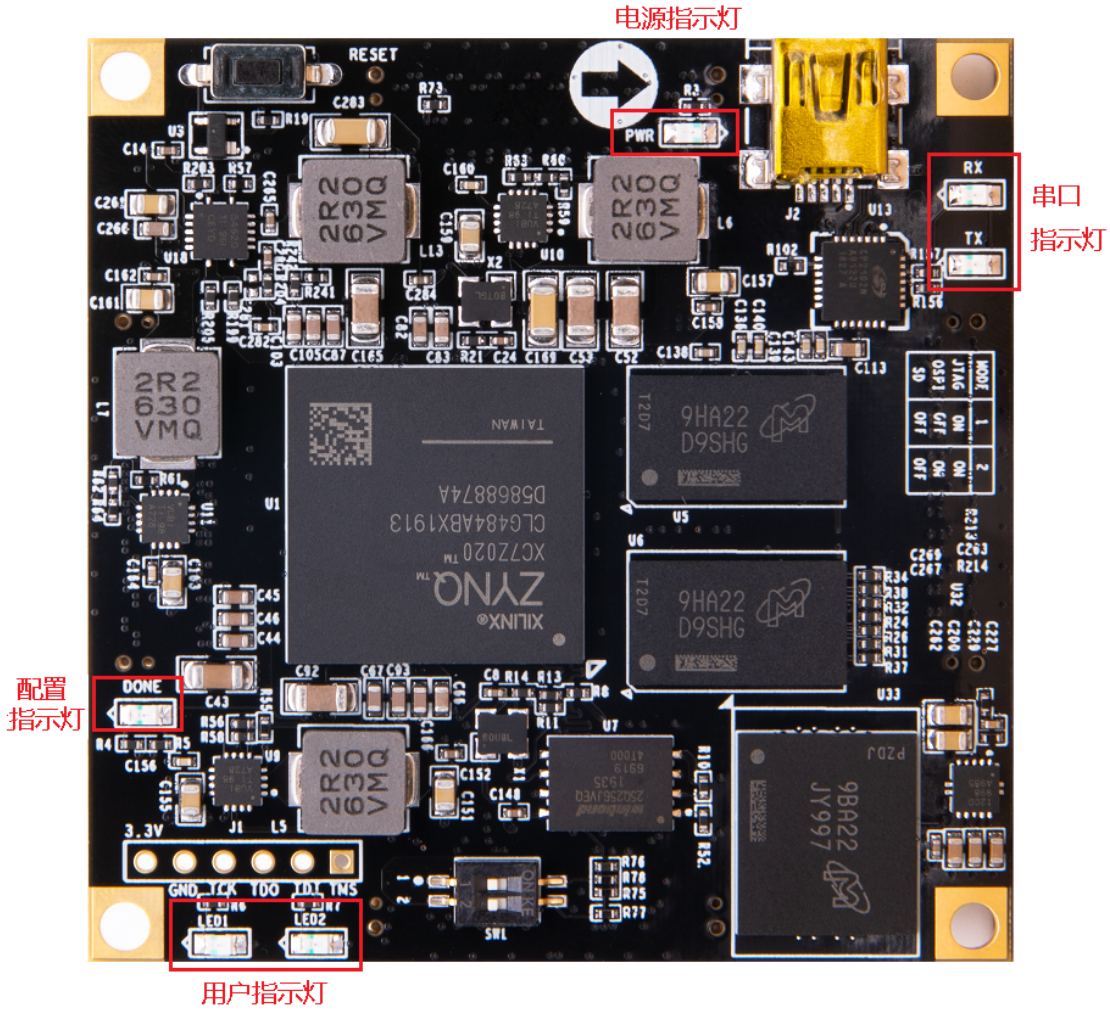


Figure 2-8-2 LED light physical diagram of the SOM

Pin allocation for user LED lights

Signal name	ZYNQ pin name	ZYNQ pin number	Remarks
MIO0_LED	PS_MIO0_500	G6	User LED1 lamp
PL_LED	IO_0_13	R7	User LED2 lamp

Table 2-8-1 LED Lamp Pin Distribution

9. Reset button

The AC7021B SOM has a reset button RESET and circuit. The reset signal is connected to the ZYNQ chip PS reset pin. Users can use this reset button to reset the ZYNQ system. When the reset button is pressed, the reset chip will generate a low-level reset signal to the ZYNQ chip. The schematic diagram of the connection between the reset button and the reset chip is shown in Figure 2-9-1.

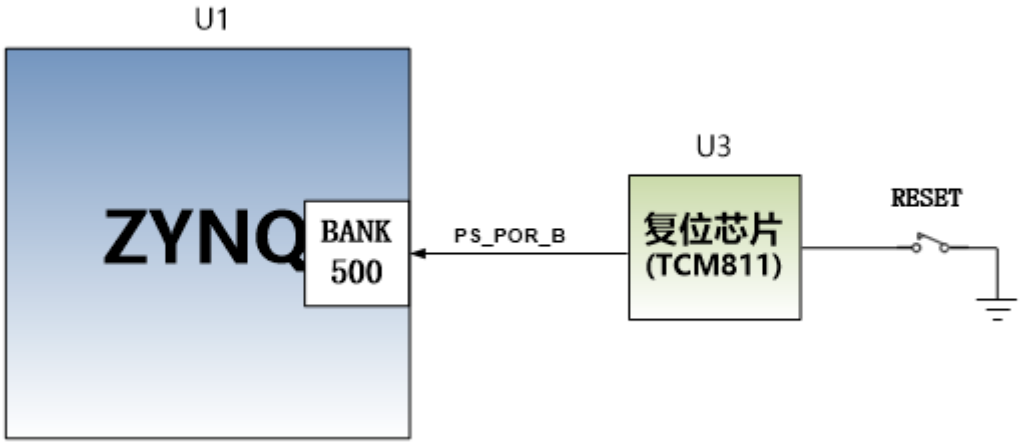


Figure 2-9-1 schematic diagram of the reset button connection

ZYNQ pin assignment for reset button

Signal name	ZYNQ pin name	ZYNQ pin number	Remarks
PS_FOR_B	PS_FOR_B_500	B5	ZYNQ system reset signal

Table 2-9-1 Reset key pin assignment

10. JTAG interface

On the AC7021B SOM, we also reserved the JTAG test seat J1 for the SOM to download and debug JTAG separately. Figure 2-10-1 is the schematic diagram of the JTAG port, which involves six signals: TMS, TDI, TDO, TCK, GND, + 3.3V.

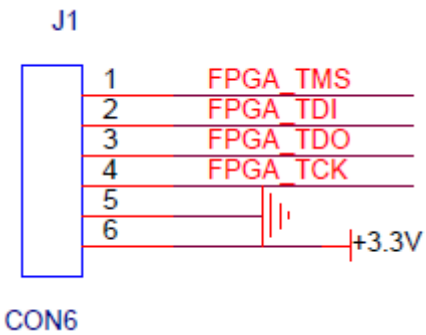


Figure 2-10-1 JTAG interface part of the SOM schematic

The JTAG interface J1 on the SOM uses a single row of test holes with a spacing of 2.54mm and 6 pins. If users need to connect and debug with JTAG on the SOM, they need to solder a single row of 6 pins.

11. DIP switch

The AC7021B SOM has a 2-bit DIP switch SW1 to configure the startup mode of the ZYNQ system. The AC7021B system development platform supports three startup modes. These three startup modes are JTAG debugging mode, QSPI FLASH and SD card startup mode. After the XC7Z020 chip is powered on, it will detect the level of the responding MIO ports (MIO5 and MIO4) to determine which startup mode. Users can choose different startup modes through the DIP switch SW1 on the SOM. The SW1 startup mode configuration is shown in the table 2-11-1 below.

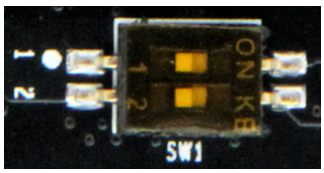
SW1	Dial position (1, 2)	MIO5, MIO4 level	Startup mode
	ON、ON	0、0	JTAG
	OFF、OFF	1、1	SD card
	OFF、ON	1、0	QSPI FLASH

Table 2-11-1 SW1 Startup Mode Configuration

12. Power supply

The power supply voltage of AC7021B SOM is DC5V. When used alone, it is powered by Mini USB interface. When connected to base board, it is powered by base board. Please note that Mini USB and base board should not be powered at the same time to avoid damage. The power supply design diagram on the board is shown in the following figure 2-12-1:

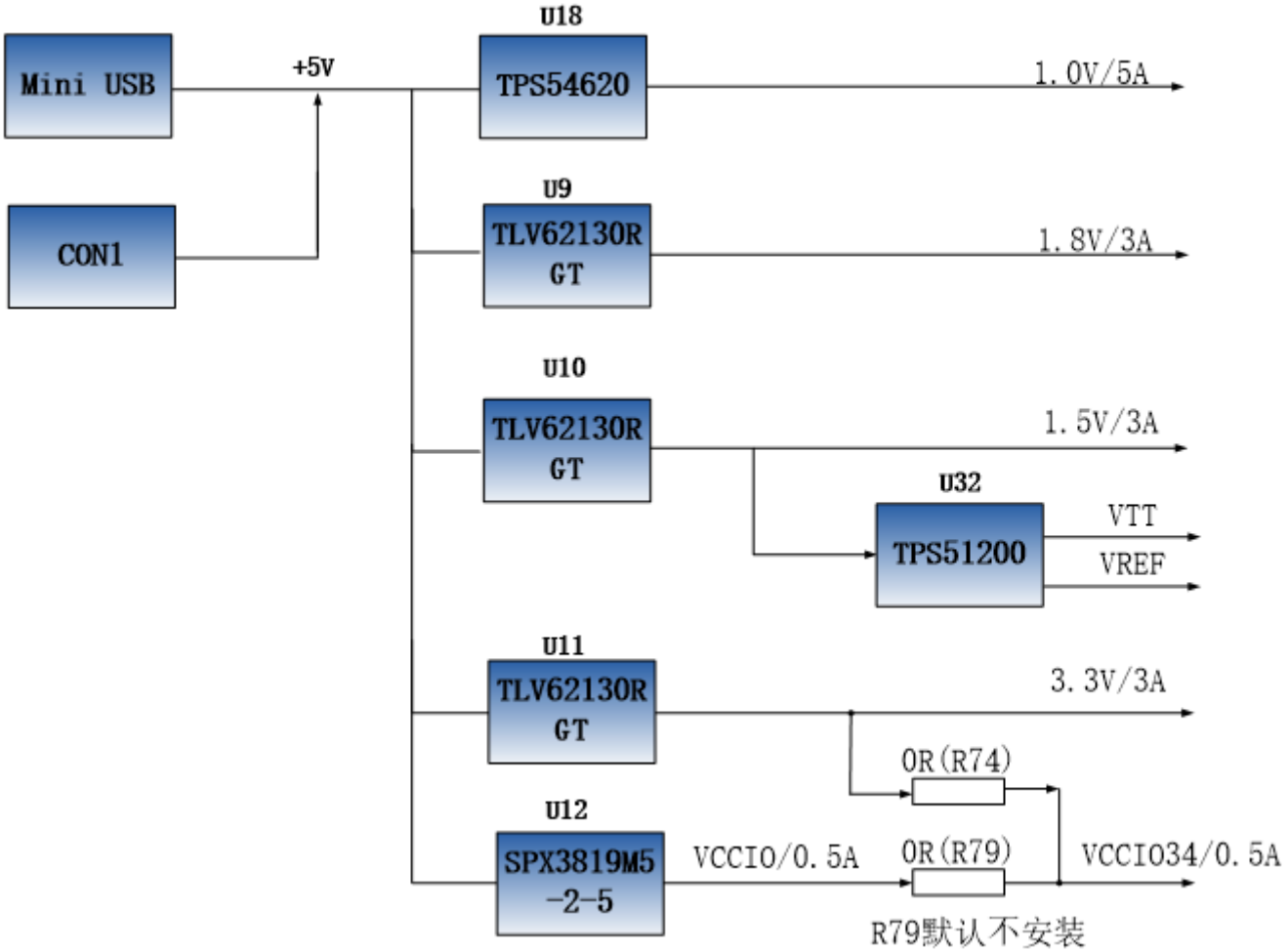


Figure 2-12-1 Power interface part in schematic

The development board is powered by + 5V, which is converted into + 1.0V, + 1.8V, + 1.5V, + 3.3V four-way power supply through four DC/DC power chips TPS54620 and TLV62130RGT. The output current of + 1.0V can reach up to 5A, and the other three power supplies are 3A. A VCCIO 2.5V power supply is generated through one LDO SPX3819M5-2-5. As long as the VCCIO 2.5V power supply is reserved for the FPGA's BANK33 and BANK34 BANK power supplies, users can choose the power supplies of BANK33 and BANK34 through two 0-ohm resistors (R74, R79). By default, R74 is installed on the development board, and the resistor of R79 is not installed, so the power supplies of BANK33 and BANK34 are + 3.3V. Users can change the resistor to make the IO output of BANK33 and 34 2.5V voltage standard. 1.5V generates the VTT and V The functions of each power distribution are shown in the following table:

Power supply	Function
+1.0V	Core voltage for PS and PL sections of ZYNQ
+1.8V	ZYNQ PS and PL part auxiliary voltage, BANK501 IO voltage, eMMC
+3.3V	ZYNQ Bank0, Bank500, Bank13, Bank35 VCCIO, QSIP FLASH, Clock crystal oscillator

+1.5V	DDR3, ZYNQ Bank501
VREF, VTT （+0.75V）	DDR3
VCCIO(+2.5V)	Reserved for ZYNQ Bank33, Bank34

Table 2-12-1 Power Interface Functions

Because the power supply of ZYNQ FPGA has the requirement of power-on sequence, in the circuit design, we have designed the circuit according to the power supply requirements of the chip, and the power-on sequence is + 1.0V- > + 1.8V- > (+ 1.5V, + 3.3V, VCCIO) to ensure the normal operation of the chip.

13. Structure diagram

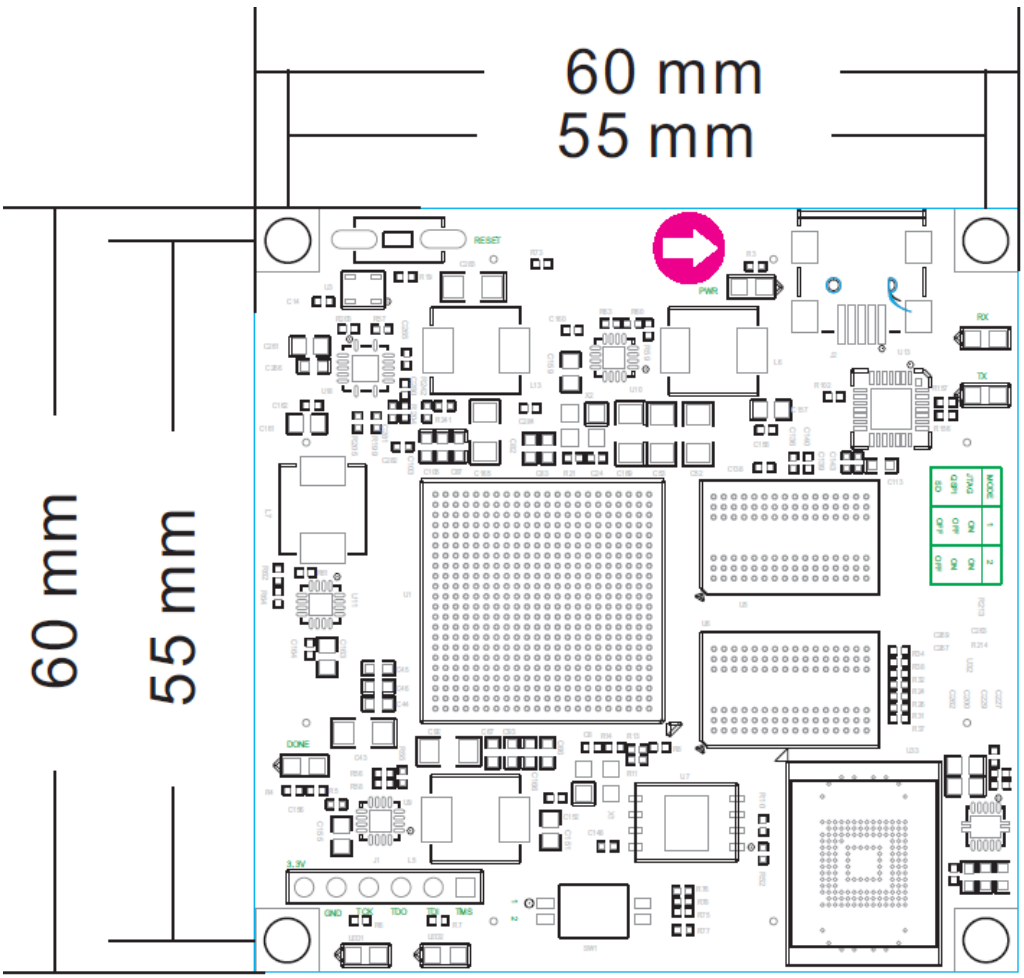


Figure 2-13-1 Top View

14. Connector pin definition

The SOM has a total of 4 high-speed expansion ports, which are connected to the base board using 4 80Pin inter-board connectors (CON1~ CON4). The PIN pin spacing of the connectors is 0.5mm (connector model AXK580137YG, base board corresponding connector model AXK680337YG). Among them, CON1 is connected to the power input, PS's MIO signal and JTAG signal, CON2~ CON4 is connected to PL's BANK13, BANK33, BANK34, and BANK35's IO signal. The IO level of BANK33 and BANK34 can be changed by replacing the LDO chip (U12) on the board, and the default is 3.3V.

Pin assignment for CON1 connectors

CON1 pin	Signal name	ZYNQ pin number	CON1 pin	Signal name	ZYNQ pin number
1	+5V	-	2	+5V	-
3	+5V	-	4	+5V	-
5	+5V	-	6	+5V	-
7	+5V	-	8	+5V	-
9	GND	-	10	GND	-
11	PS_MIO13	A6	12	ETH_TXD0	E9
13	PS_MIO12	C5	14	ETH_TXD1	A7
15	-	-	16	ETH_TXD2	E10
17	-	-	18	ETH_TXD3	A8
19	GND	-	20	GND	-
21	-	-	22	ETH_TXCK	D6
23	-	-	24	ETH_TXCTL	F11
25	-	-	26	ETH_RXD3	A13
27	-	-	28	ETH_RXD2	F12
29	GND	-	30	GND	-
31	PS_MIO7	D5	32	ETH_RXD1	B7
33	PS_MIO8	E5	34	ETH_RXD0	E11
35	PS_MIO9	C4	36	ETH_RXCTL	D7

37	PS_MIO11	B4	38	ETH_RXCK	A14
39	GND	-	40	GND	-
41	-	-	42	ETH_MDC	D10
43	-	-	44	ETH_MDIO	C12
45	-	-	46	OTG_STP	A11
47	-	-	48	OTG_DIR	E8
49	GND	-	50	GND	-
51	XADC_VP	L11	52	OTG_CLK	A9
53	XADC_VN	M12	54	OTG_NXT	F9
55	-	-	56	OTG_DATA0	C7
57	PS_MIO10	G7	58	OTG_DATA1	G13
59	GND	-	60	GND	-
61	SD_CLK	E14	62	OTG_DATA2	B12
63	SD_D1	B11	64	OTG_DATA3	F14
65	SD_D0	D8	66	OTG_DATA4	A12
67	SD_CMD	C8	68	OTG_DATA5	B14
69	GND	-	70	GND	-
71	SD_D3	B9	72	OTG_DATA6	F13
73	SD_D2	E13	74	OTG_DATA7	C13
75	-	-	76	-	-
77	FPGA_TMS	G12	78	FPGA_TCK	G11
79	FPGA_TDO	G14	80	FPGA_TDI	H13

Table 2-14-1 Pin Allocation for con1 Connectors

Pin assignment for CON2 connectors

CON2 pin	Signal name	ZYNQ pin number	CON2 pin	Signal name	ZYNQ pin number

1	B13_L1_N	V9	2	B33_L4_N	W21
3	B13_L1_P	V10	4	B33_L4_P	W20
5	B33_L10_P	AB19	6	B33_L3_N	W22
7	B33_L10_N	AB20	8	B33_L3_P	V22
9	GND	-	10	GND	-
11	B13_L4_N	W12	12	B33_L2_N	U22
13	B13_L4_P	V12	14	B33_L2_P	T22
15	B34_L6_N	M16	16	B13_L5_N	U11
17	B34_L6_P	M15	18	B13_L5_P	U12
19	GND	-	20	GND	-
21	B13_L12_N	Y8	22	B33_IO25	U14
23	B13_IO25	U7	24	B34_IO25	R15
25	B13_L23_N	W7	26	B13_L6_P	U10
27	B13_L23_P	V7	28	B13_L6_N	U9
29	GND	-	30	GND	-
31	B13_L13_N	Y5	32	B13_L19_P	R6
33	B13_L13_P	Y6	34	B13_L19_N	T6
35	B13_L24_N	W5	36	B13_L22_P	U6
37	B13_L24_P	W6	38	B13_L22_N	U5
39	GND	-	40	GND	-
41	B33_L11_P	Y19	42	B13_L20_P	T4
43	B33_L11_N	AA19	44	B13_L20_N	U4
45	B33_L5_P	U20	46	B13_L3_P	W11
47	B33_L5_N	V20	48	B13_L3_N	W10
49	GND	-	50	GND	-
51	B33_L1_P	T21	52	B13_L10_P	Y11

53	B33_L1_N	U21	54	B13_L10_N	Y10
55	B13_L7_P	AA12	56	B13_L2_P	V8
57	B13_L7_N	AB12	58	B13_L2_N	W8
59	GND	-	60	GND	-
61	B13_L8_N	AB11	62	B13_L14_P	AA7
63	B13_L8_P	AA11	64	B13_L14_N	AA6
65	B13_L9_N	AB9	66	B13_L16_P	AB5
67	B13_L9_P	AB10	68	B13_L16_N	AB4
69	GND	-	70	GND	-
71	B13_L11_N	AA8	72	B13_L18_N	AA4
73	B13_L11_P	AA9	74	B13_L18_P	Y4
75	B13_L17_N	AB6	76	B13_L15_P	AB2
77	B13_L17_P	AB7	78	B13_L15_N	AB1
79	B13_L21_N	V4	80	B13_L21_P	V5

Table 2-14-2 Pin assignment for con2 connectors

Pin assignment for CON3 connectors

CON3 pin	Signal name	ZYNQ pin number	CON3 pin	Signal name	ZYNQ pin number
1	B34_L2_P	J16	2	B34_L12_N	L19
3	B34_L2_N	J17	4	B34_L12_P	L18
5	B34_L11_P	K19	6	B34_L10_N	L22
7	B34_L11_N	K20	8	B34_L10_P	L21
9	GND	-	10	GND	-
11	B34_L7_P	J18	12	B34_L3_N	L16
13	B34_L7_N	K18	14	B34_L3_P	K16
15	B34_L1_P	J15	16	B34_L15_N	M22

17	B34_L1_N	K15	18	B34_L15_P	M21
19	GND	-	20	GND	-
21	B34_L17_P	R20	22	B34_L16_P	N22
23	B34_L17_N	R21	24	B34_L16_N	P22
25	B34_L14_N	N20	26	B34_L20_N	P18
27	B34_L14_P	N19	28	B34_L20_P	P17
29	GND	-	30	GND	-
31	B34_L5_N	N18	32	B34_L13_P	M19
33	B34_L5_P	N17	34	B34_L13_N	M20
35	B33_L9_P	Y20	36	B34_L21_N	T17
37	B33_L9_N	Y21	38	B34_L21_P	T16
39	GND	-	40	GND	-
41	B33_L8_P	AA21	42	B33_L6_N	V19
43	B33_L8_N	AB21	44	B33_L6_P	V18
45	B33_L12_N	AA18	46	B33_L16_P	U17
47	B33_L12_P	Y18	48	B33_L16_N	V17
49	GND	-	50	GND	-
51	B33_L13_P	W17	52	B33_L17_N	AB17
53	B33_L13_N	W18	54	B33_L17_P	AA17
55	B33_L18_N	AB16	56	B33_L7_P	AA22
57	B33_L18_P	AA16	58	B33_L7_N	AB22
59	GND	-	60	GND	-
61	B33_L21_N	Y15	62	B33_L19_N	V15
63	B33_L21_P	W15	64	B33_L19_P	V14
65	B33_L24_P	AB14	66	B33_L15_N	U16
67	B33_L24_N	AB15	68	B33_L15_P	U15

69	GND	-	70	GND	-
71	B33_L23_N	AA13	72	B33_L14_P	W16
73	B33_L23_P	Y13	74	B33_L14_N	Y16
75	B33_L20_N	W13	76	B33_L22_P	Y14
77	B33_L20_P	V13	78	B33_L22_N	AA14
79	B34_IO0	H15	80	B33_IO0	U19

Table 2-14-3 Pin assignment for con3 connectors

Pin assignment for CON4 connectors

CON4 pin	Signal name	ZYNQ pin number	CON4 pin	Signal name	ZYNQ pin number
1	B35_L7_N	B15	2	B35_L9_P	A16
3	B35_L7_P	C15	4	B35_L9_N	A17
5	B35_L8_P	B16	6	B35_L10_P	A18
7	B35_L8_N	B17	8	B35_L10_N	A19
9	GND	-	10	GND	-
11	B35_L11_N	C18	12	B35_L15_P	A21
13	B35_L11_P	C17	14	B35_L15_N	A22
15	B35_L13_N	B20	16	B35_L18_N	B22
17	B35_L13_P	B19	18	B35_L18_P	B21
19	GND	-	20	GND	-
21	B35_L14_N	C20	22	B35_L16_N	C22
23	B35_L14_P	D20	24	B35_L16_P	D22
25	B35_L12_P	D18	26	B35_L17_N	D21
27	B35_L12_N	C19	28	B35_L17_P	E21
29	GND	-	30	GND	-

31	B35_L2_N	D17	32	B35_L23_N	F22
33	B35_L2_P	D16	34	B35_L23_P	F21
35	B35_L1_N	E16	36	B35_L22_N	G21
37	B35_L1_P	F16	38	B35_L22_P	G20
39	GND	-	40	GND	-
41	B35_L21_P	E19	42	B34_L8_N	J22
43	B35_L21_N	E20	44	B34_L8_P	J21
45	B35_L24_P	H22	46	B35_L20_N	F19
47	B35_L24_N	G22	48	B35_L20_P	G19
49	GND	-	50	GND	-
51	B35_L6_P	G17	52	B35_L19_N	H20
53	B35_L6_N	F17	54	B35_L19_P	H19
55	B35_L4_P	G15	56	B34_L9_P	J20
57	B35_L4_N	G16	58	B34_L9_N	K21
59	GND	-	60	GND	-
61	B35_L3_N	D15	62	B35_IO25	H18
63	B35_L3_P	E15	64	B35_IO0	H17
65	B34_L24_N	R16	66	B34_L4_P	L17
67	B34_L24_P	P16	68	B34_L4_N	M17
69	GND	-	70	GND	-
71	B34_L23_P	R18	72	B34_L18_N	P21
73	B34_L23_N	T18	74	B34_L18_P	P20
75	B35_L5_P	F18	76	B34_L22_P	R19
77	B35_L5_N	E18	78	B34_L22_N	T19
79	B34_L19_P	N15	80	B34_L19_N	P15

Table 2-14-4 Pin assignment for con4 connectors

Part 3: Base board

1. Introduction

Through the previous function introduction, we can understand the functions of the base board

- 5 10/100M/1000M Ethernet RJ-45 interfaces
- 1 channel HDMI output display interface
- 4 USB HOST ports
- 1 USB Uart communication interface
- 1 channel SD card interface
- 2-Way 40-pin expansion port
- JTAG debug interface
- 2 independent buttons
- 2 user LED lights

2. Gigabit Ethernet interface

The AX7021B base board has 5 Gigabit Ethernet interfaces, of which 1 Ethernet interface is connected to the PS system end, and the other 4 Ethernet interfaces are connected to the logical IO port of PL. The 4 Gigabit Ethernet interfaces connected to the PL end need to be mounted on the AXI bus system of ZYNQ through program call IP.

The Ethernet chip uses Jinglue Semiconductor's industrial-grade Ethernet GPHY chip (JL2121-N040I) to provide network communication services for users. The Ethernet PHY chip on the PS side is connected to the GPIO interface of the PS side BANK501 of ZYNQ. The Ethernet PHY chip on the PL side is connected to the IO of BANK33 and BANK34. The JL2121 chip supports network transmission rates of 10/100/1000 Mbps and communicates data with the MAC layer of the Zynq7000 system through the RGMII interface. The JL2121D supports MDI/MDX Self-Adaptation, various speed Self-Adaptation, Master/Slave Self-Adaptation, and MDIO bus for PHY register management.

When the JL2121 is powered on, it will detect the level status of some specific IO to determine its operating mode. Table 3-2-1 describes the default setting information after the GPHY chip is powered on.

Configure pin	Explanation	Configuration value
RXD3_ADR0		PHY Address 001

RXC_ADR1 RXCTL_ADR2	PHY address for MDIO/MDC mode	
RXD1_TXDLY	TX clock 2ns delay	Delay time
RXD0_RXDLY	RX clock 2ns delay	Delay time

Table 3-2-1 PHY chip default configuration values

When the network is connected to Gigabit Ethernet, the data transmission between ZYNQ and PHY chip JL2121 communicates through the RGMII bus, with a transmission clock of 125Mhz, and the data is sampled at the rising edge and falling sample of the clock.

When the network is connected to 100Mbps Ethernet, the data transmission between ZYNQ and PHY chip JL2121 communicates through the RMII bus, with a transmission clock of 25Mhz. The data is sampled at the rising edge and falling sample of the clock.

Figure 3-2-1 is a schematic diagram of ZYNQ PS end 1 Ethernet PHY chip connection:

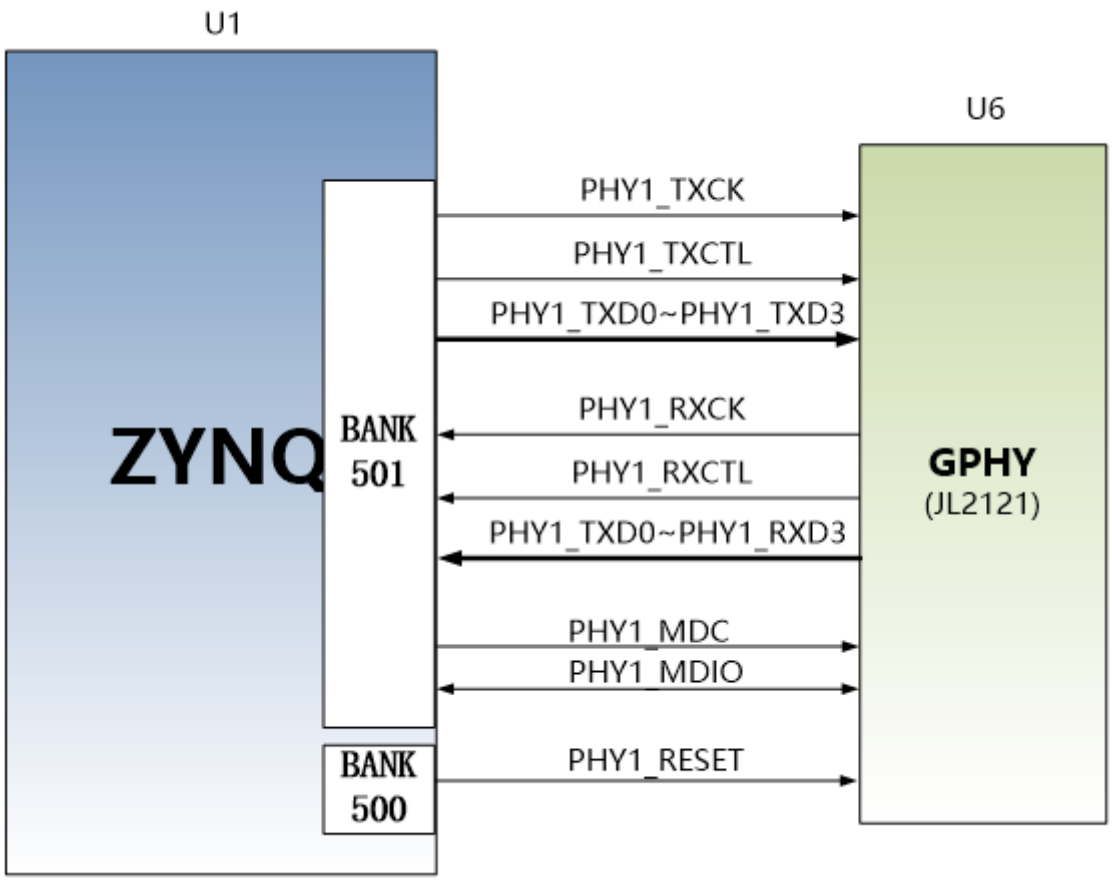


Figure 3-2-1 ZYNQ PS system and GPHY connection schematic

Figure 3-2-2 is a schematic diagram of ZYNQ PL end 4-way Ethernet PHY chip connection:

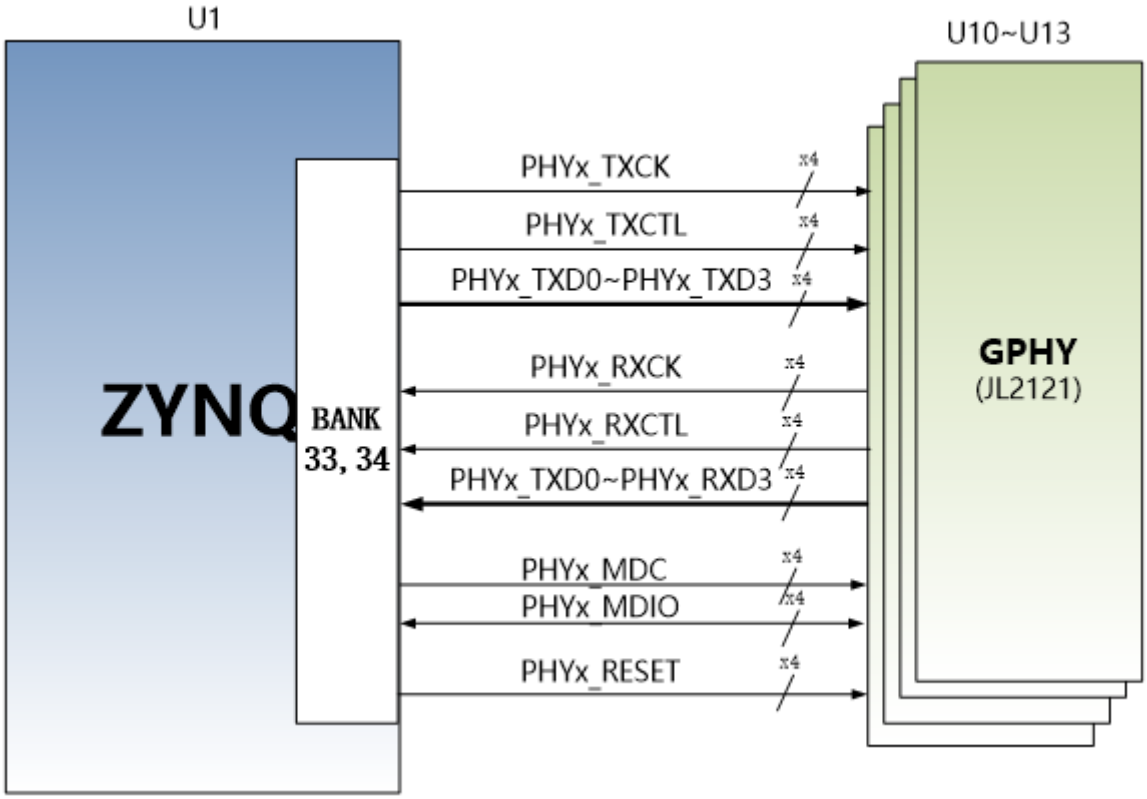


Figure 3-2-2 ZYNQ PL end and 4 GPHY connection schematic diagram

The allocation of the first Gigabit Ethernet pin on the PS end is as follows:

Signal name	ZYNQ pin name	ZYNQ pin number	Remarks
PHY1_TXCK	PS_MIO16_501	D6	RGMII transmission clock
PHY1_TXD0	PS_MIO17_501	E9	Send data bit0
PHY1_TXD1	PS_MIO18_501	A7	Send data bit1
PHY1_TXD2	PS_MIO19_501	E10	Send data bit2
PHY1_TXD3	PS_MIO20_501	A8	Send data bit3
PHY1_TXCTL	PS_MIO21_501	F11	Send enable signal
PHY1_RXCK	PS_MIO22_501	A14	RGMII receive clock
PHY1_RXD0	PS_MIO23_501	E11	Received data Bit0
PHY1_RXD1	PS_MIO24_501	B7	Receive data Bit1
PHY1_RXD2	PS_MIO25_501	F12	Receive data Bit2
PHY1_RXD3	PS_MIO26_501	A13	Receive data Bit3

PHY1_RXCTL	PS_MIO27_501	D7	Receive data valid signal
PHY1_MDC	PS_MIO52_501	D10	MDIO management clock
PHY1_MDIO	PS_MIO53_501	C12	MDIO manages data
PHY1_RESET	PS_MIO7_500	D5	Reset signal

Table 3-2-2 PS Ethernet Pin Allocation

The second Gigabit Ethernet pin allocation at the PL end is as follows:

Signal name	ZYNQ pin name	ZYNQ pin number	Remarks
PHY2_TXCK	B34_L17_N	R21	RGMII transmission clock
PHY2_TXD0	B34_L5_P	N17	Send data bit0
PHY2_TXD1	B34_L5_N	N18	Send data bit1
PHY2_TXD2	B34_L14_P	N19	Send data bit2
PHY2_TXD3	B34_L14_N	N20	Send data bit3
PHY2_TXCTL	B34_L17_P	R20	Send enable signal
PHY2_RXCK	B34_L11_P	K19	RGMII receive clock
PHY2_RXD0	B34_L7_P	J18	Received data Bit0
PHY2_RXD1	B34_L7_N	K18	Receive data Bit1
PHY2_RXD2	B34_L1_P	J15	Receive data Bit2
PHY2_RXD3	B34_L1_N	K15	Receive data Bit3
PHY2_RXCTL	B34_L11_N	K20	Receive data valid signal
PHY2_MDC	B34_L2_N	J17	MDIO management clock
PHY2_MDIO	B34_L2_P	J16	MDIO manages data
PHY2_RESET	B34_L12_N	L19	Reset signal

Table 3-2-3 PL Ethernet Second Pin Allocation

The allocation of the third Gigabit Ethernet pin at the PL end is as follows:

Signal name	ZYNQ pin name	ZYNQ pin number	Remarks
PHY3_TXCK	B34_L3_P	K16	RGMII transmission clock
PHY3_TXD0	B34_L12_P	L18	Send data bit0
PHY3_TXD1	B34_L10_N	L22	Send data bit1
PHY3_TXD2	B34_L10_P	L21	Send data bit2
PHY3_TXD3	B34_L3_N	L16	Send data bit3
PHY3_TXCTL	B34_L15_N	M22	Send enable signal
PHY3_RXCK	B34_L13_P	M19	RGMII receive clock
PHY3_RXD0	B34_L20_N	P18	Received data Bit0
PHY3_RXD1	B34_L16_N	P22	Receive data Bit1
PHY3_RXD2	B34_L16_P	N22	Receive data Bit2
PHY3_RXD3	B34_L15_P	M21	Receive data Bit3
PHY3_RXCTL	B34_L20_P	P17	Receive data valid signal
PHY3_MDC	B34_L13_N	M20	MDIO management clock
PHY3_MDIO	B34_L21_N	T17	MDIO manages data
PHY3_RESET	B34_L21_P	T16	Reset signal

Table 3-2-4 PL Ethernet Third Pin Allocation

The allocation of the fourth Gigabit Ethernet pin at the PL end is as follows:

Signal name	ZYNQ pin name	ZYNQ pin number	Remarks
PHY4_TXCK	B33_L17_P	AA17	RGMII transmission clock
PHY4_TXD0	B33_L6_P	V18	Send data bit0
PHY4_TXD1	B33_L16_P	U17	Send data bit1

PHY4_TXD2	B33_L16_N	V17	Send data bit2
PHY4_TXD3	B33_L17_N	AB17	Send data bit3
PHY4_TXCTL	B33_L7_P	AA22	Send enable signal
PHY4_RXCK	B33_L14_P	W16	RGMII receive clock
PHY4_RXD0	B33_L15_N	U16	Received data Bit0
PHY4_RXD1	B33_L19_P	V14	Receive data Bit1
PHY4_RXD2	B33_L19_N	V15	Receive data Bit2
PHY4_RXD3	B33_L7_N	AB22	Receive data Bit3
PHY4_RXCTL	B33_L15_P	U15	Receive data valid signal
PHY4_MDC	B33_L14_N	Y16	MDIO management clock
PHY4_MDIO	B33_L22_P	Y14	MDIO manages data
PHY4_RESET	B33_L22_N	AA14	Reset signal

Table 3-2-5 PL Ethernet Fourth Pin Allocation

The fifth Gigabit Ethernet pin allocation at the PL end is as follows:

Signal name	ZYNQ pin name	ZYNQ pin number	Remarks
PHY5_TXCK	B33_L24_N	AB15	RGMII transmission clock
PHY5_TXD0	B33_L20_P	V13	Send data bit0
PHY5_TXD1	B33_L20_N	W13	Send data bit1
PHY5_TXD2	B33_L23_P	Y13	Send data bit2
PHY5_TXD3	B33_L23_N	AA13	Send data bit3
PHY5_TXCTL	B33_L24_P	AB14	Send enable signal
PHY5_RXCK	B33_L13_P	W17	RGMII receive clock
PHY5_RXD0	B33_L18_N	AB16	Received data Bit0
PHY5_RXD1	B33_L18_P	AA16	Receive data Bit1

PHY5_RXD2	B33_L21_N	Y15	Receive data Bit2
PHY5_RXD3	B33_L21_P	W15	Receive data Bit3
PHY5_RXCTL	B33_L13_N	W18	Receive data valid signal
PHY5_MDC	B33_L12_P	Y18	MDIO management clock
PHY5_MDIO	B33_L12_N	AA18	MDIO manages data
PHY5_RESET	B33_L6_N	V19	Reset signal

Table 3-2-6 PL Ethernet Fifth Pin Allocation

3. USB 2.0 Host Interface

The AX7021B base board has four USB2.0 HOST interfaces. The USB2.0 transceiver uses a 1.8V, high-speed USB3320C-EZK chip that supports the ULPI standard interface, and extends four USB HOST interfaces through a USB HUB chip USB2514. The ZYNQ USB bus interface is connected to the USB3320C-EZK transceiver to achieve high-speed data communication in USB2.0 Host mode. The USB data and control signals of the USB3320C are connected to the IO port of the BANK501 on the PS side of the ZYNQ chip, and the USB interface differential signal (DP/DM) is connected to the USB2514 chip to expand four USB interfaces. Two 24MHz crystal oscillators provide system clocks for the USB3320C and USB2514 chips, respectively.

The USB interface is a flat USB interface (USB Type A), which facilitates users to connect different USB slave peripherals (such as USB mouse and USB keyboard) at the same time. In addition, the base board also provides + 5V power supply for each USB interface.

The schematic diagram of the connection between ZYNQ processor and USB3320C-EZK chip and USB2514 chip is shown in 3-3-1:

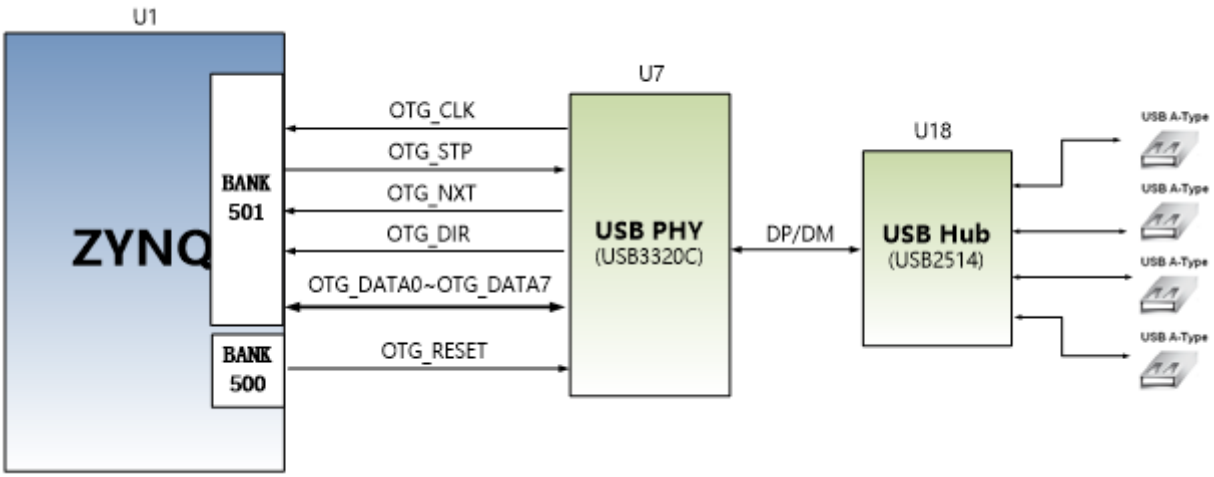


Figure 3-3-1 Schematic connection between Zynq7000 and USB chip

USB2.0 pin distribution:

Signal name	ZYNQ pin name	ZYNQ pin number	Remarks
OTG_DATA4	PS_MIO28_501	A12	USB data Bit4
OTG_DIR	PS_MIO29_501	E8	USB data direction signal
OTG_STP	PS_MIO30_501	A11	USB stop signal
OTG_NXT	PS_MIO31_501	F9	USB next data signal
OTG_DATA0	PS_MIO32_501	C7	USB data Bit0
OTG_DATA1	PS_MIO33_501	G13	USB data Bit1
OTG_DATA2	PS_MIO34_501	B12	USB data Bit2
OTG_DATA3	PS_MIO35_501	F14	USB data Bit3
OTG_CLK	PS_MIO36_501	A9	USB clock signal
OTG_DATA5	PS_MIO37_501	B14	USB data Bit5
OTG_DATA6	PS_MIO38_501	F13	USB data Bit6
OTG_DATA7	PS_MIO39_501	C13	USB data Bit7
OTG_RESETN	PS_MIO8_500	E5	USB reset signal

Table 3-3-1 USB2.0 pin distribution

4. HDMI output interface

The implementation of the HDMI output interface is to use the SIL9134 HDMI (DVI) encoding chip of Silion Image Company, which supports up to 1080P@60Hz output and 3D output.

Among them, the video digital interface, audio digital interface and I2C configuration interface of SIL9134 are connected to the BANK35 IO of the ZYNQ7000 PL part. The ZYNQ7000 system initializes and controls the SIL9134 through the I2C pin. The hardware connection schematic diagram of SIL9134 chip and ZYNQ7000 is shown in the following figure 3-4-1:

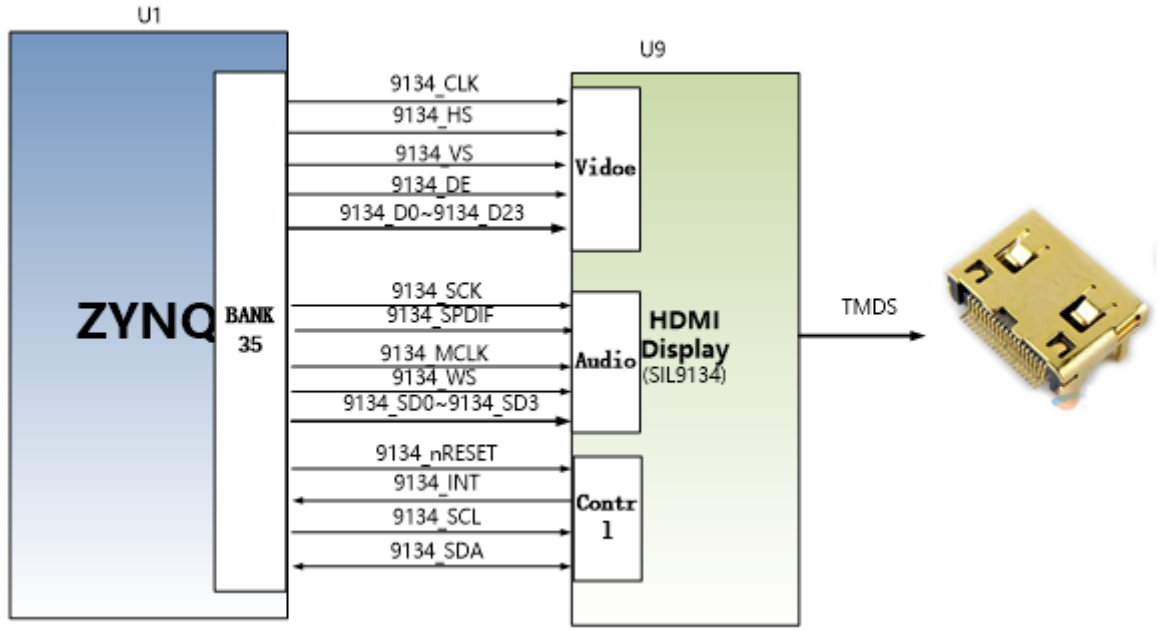


Figure 3-4-1 HDMI interface design schematic

Pin allocation of ZYNQ:

Signal name	ZYNQ pin name	ZYNQ pin number	Remarks
9134_CLK	B35_L4_N	G16	9134 Video Signal Clock
9134_HS	B35_L21_P	E19	9134 Video signal line synchronization
9134_VS	B35_L1_P	F16	9134 Video signal column synchronization
9134_DE	B35_L21_N	E20	9134 video signal is valid
9134_D[0]	B35_L24_P	H22	9134 Video signal data 0
9134_D[1]	B35_L24_N	G22	9134 Video signal data 1
9134_D[2]	B35_L6_P	G17	9134 Video signal data 2
9134_D[3]	B35_L6_N	F17	9134 Video signal data 3
9134_D[4]	B35_L4_P	G15	9134 Video signal data 4
9134_D[5]	B35_L3_N	D15	9134 Video signal data 5
9134_D[6]	B35_L3_P	E15	9134 Video signal data 6
9134_D[7]	B35_L5_P	F18	9134 Video signal data 7

9134_D[8]	B35_L5_N	E18	9134 Video signal data 8
9134_D[9]	B35_IO0	H17	9134 Video signal data 9
9134_D[10]	B35_IO25	H18	9134 Video signal data 10
9134_D[11]	B35_L19_P	H19	9134 Video signal data 11
9134_D[12]	B35_L19_N	H20	9134 Video signal data 12
9134_D[13]	B35_L20_P	G19	9134 Video signal data 13
9134_D[14]	B35_L20_N	F19	9134 Video signal data 14
9134_D[15]	B35_L22_P	G20	9134 Video signal data 15
9134_D[16]	B35_L22_N	G21	9134 Video signal data 16
9134_D[17]	B35_L23_P	F21	9134 Video signal data 17
9134_D[18]	B35_L23_N	F22	9134 Video signal data 18
9134_D[19]	B35_L17_P	E21	9134 Video signal data 19
9134_D[20]	B35_L17_N	D21	9134 Video signal data 20
9134_D[21]	B35_L16_P	D22	9134 Video signal data 21
9134_D[22]	B35_L16_N	C22	9134 Video signal data 22
9134_D[23]	B35_L18_P	B21	9134 Video signal data 23
9134_SCK	B35_L13_P	B19	9134 Audio interface I2S clock

9134_SPDIF	B35_L1_N	E16	9134 Audio S/PDIF input
9134_MCLK	B35_L2_P	D16	9134 Audio Input Master Clock
9134_WS	B35_L14_N	C20	9134 Audio interface I2S word selection
9134_SD0	B35_L14_P	D20	9134 Audio interface I2S data
9134_SD1	B35_L12_P	D18	9134 Audio interface I2S data
9134_SD2	B35_L12_N	C19	9134 Audio interface I2S data
9134_SD3	B35_L2_N	D17	9134 Audio interface I2S data
9134_nRESET	B35_L11_P	C17	9134 reset signal
9134_INT	B35_L13_N	B20	9134 interrupt signal
9134_SCL	B35_L18_N	B22	9134 IIC control clock
9134_SDA	B35_L15_N	A22	9134 IIC control data

Table 3-4-1 HDMI Output Interface Pin Allocation

5. USB to serial port

The AX7021B base board is also equipped with a serial port interface for overall debugging of the ZYNQ7000 system. The conversion chip uses the USB-UAR chip of Silicon Labs CP2102GM, and the USB interface uses the MINI USB interface. It can be connected to the USB port of the PC with a single USB cable for separate power supply and serial data communication of the SOM.

The schematic diagram of the USB Uart circuit design is shown in the following figure 3-5-1:

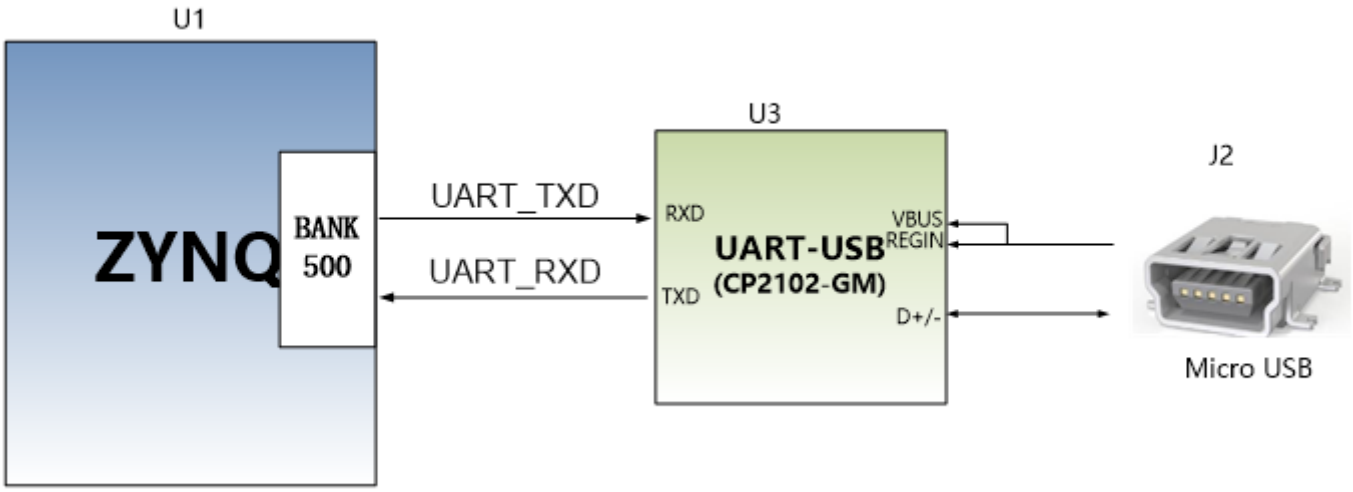


Figure 3-5-1 schematic diagram of USB to serial port

ZYNQ pin allocation for UART to serial port:

Signal name	ZYNQ pin name	ZYNQ pin number	Remarks
UART_RXD	PS_MIO13_500	A6	Uart data entry
UART_TXD	PS_MIO12_500	C5	Uart data output

Table 3-5-1 USB to Serial Pin Allocation

6. SD card slot

The AX7021B base board includes a Micro SD card interface to provide users with access to SD card memory for storing BOOT programs for ZYNQ chips, Linux operating system kernels, file systems, and other user data files.

The SDIO signal is connected to the IO signal of the PS BANK501 of ZYNQ, because the VCCMIO of the BANK is set to 1.8V, but the data level of the SD card is 3.3V. Here we connect it through the TXS02612 level converter. The schematic diagram of the PS and SD card connectors of Zynq7000 is shown in Figure 3-6-1.

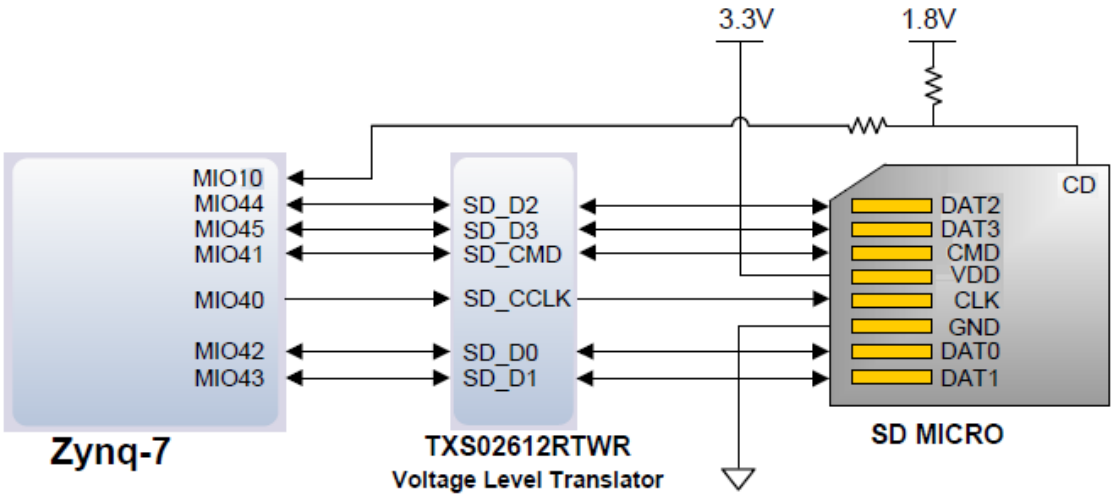


Figure 3-6-1 SD card connection diagram

SD card slot pin distribution

Signal name	ZYNQ pin name	ZYNQ pin number	Remarks
SD_CLK	PS_MIO40	E14	SD clock signal
SD_CMD	PS_MIO41	C8	SD command signal
SD_D0	PS_MIO42	D8	SD Data0
SD_D1	PS_MIO43	B11	SD Data1
SD_D2	PS_MIO44	E13	SD Data2
SD_D3	PS_MIO45	B9	SD Data3
SD_CD	PS_MIO10	G7	SD card insertion signal

Table 3-6-1 SD Card Pin Allocation

7. JTAG interface

The JTAG download and debugging circuit is already integrated on the AX7021B base board, so users do not need to purchase additional AMD downloaders. With just one USB cable, ZYNQ development and debugging can be carried out. On the development board, the USB and ZYNQ JTAG debugging signals TCK, TDO, TMS, TDI of the PC are implemented through a FTDI USB bridge chip FT232HL for data communication. Figure 3-7-1 is the schematic diagram of the JTAG port on the development board.

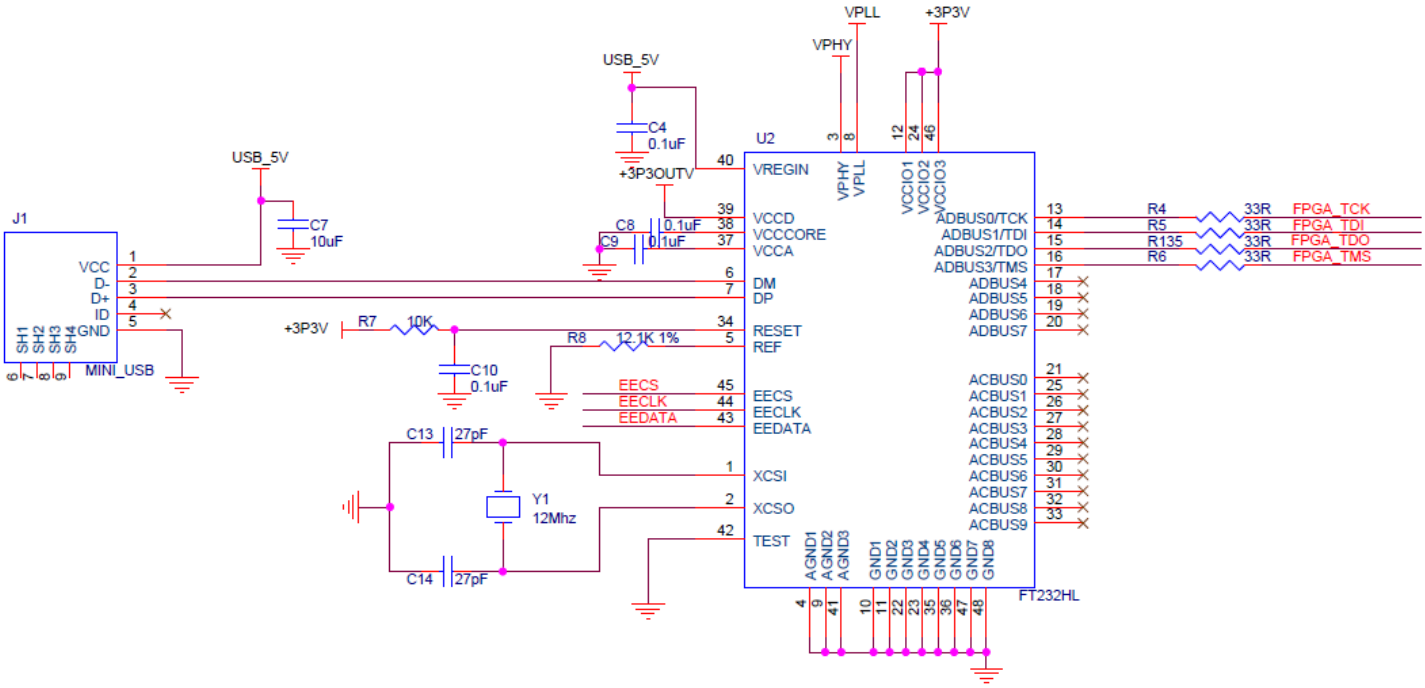


Figure 3-7-1 JTAG interface part in schematic

On the AX7021B development board, the JTAG interface is in the form of a USB interface. Users can use the USB cable we provide to connect a PC to the JTAG interface for ZYNQ system debugging.

8. LED lights

The AX7021B base board has three red LED lights, one of which is the power indicator light (PWR), and two are the user LED lights (LED1~ LED2). When the base board is powered, the power indicator light will light up; one of the two user LED lights is connected to the MIO of PS, and the other is connected to the IO of PL. The user can control the on and off through the program. When the IO voltage connected to the user LED light is high, the user LED light will turn off. When the IO voltage connected to the user LED light is low, the user LED will light up. The schematic diagram of the hardware connection of the LED light is shown in Figure 3-8-1:

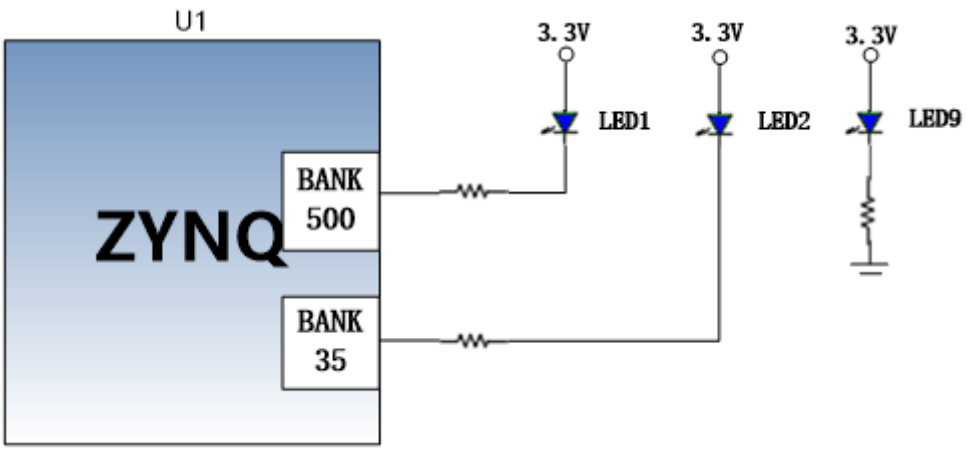


Figure 3-8-1 base board LED lamp hardware connection diagram

Pin assignment for base board user LED lights

Signal name	ZYNQ pin name	ZYNQ pin number	Remarks
PS_LED	PS_MIO9_500	C4	User LED1 lamp
PL_LED	B35_L9_P	A16	User LED2 lamp

Table 3-8-1 User LED Lamp Pin Allocation

9. User button

The AX7021B base board has two user buttons KEY1 and KEY2. KEY1 is connected to the MIO pin of the ZYNQ chip PS, and KEY2 is connected to the IO pin of the ZYNQ chip PL. When the button is pressed, the signal is low, and the ZYNQ chip detects the low level to determine whether the button is pressed. The schematic diagram of the user button connection is shown in Figure 3-9-1.

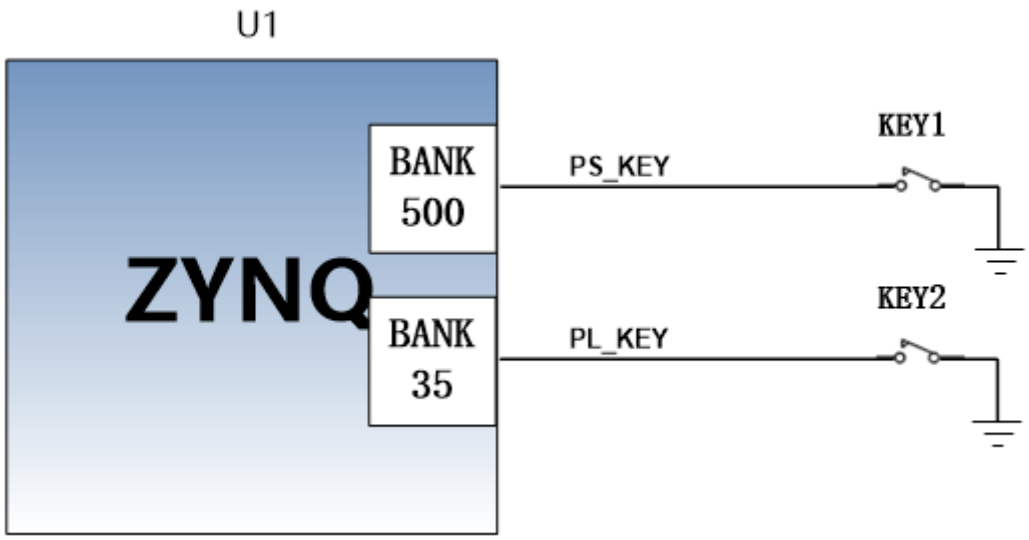


Figure 3-9-1 user key connection diagram

ZYNQ pin assignment for user keys

Signal name	ZYNQ pin name	ZYNQ pin number	Remarks
PS_KEY	PS_MIO11_500	B4	User buttons on PS side
PL_KEY	B35_L9_N	A17	User buttons on PL side

Figure 3-9-1 schematic diagram of the reset button connection

10. Expansion port

The AX7021B base board reserves two 40-pin expansion ports J15 and J16 with a standard spacing of 2.54mm, which are used to connect various modules of Alinx or external circuits designed by users. The expansion port has 40 signals, including 1 5V power supply, 2 3.3V power supplies, 3 ground ports, and 34 IO ports. **Do not directly connect the IO to the 5V device to avoid burning out the ZYNQ7000 chip. If you want to connect the 5V device, you need to connect the level conversion chip.**

33 ohms of discharge is connected in series between the expansion port and the ZYNQ7000 connection to protect the ZYNQ7000 chip from damage caused by external voltage or current. The circuit of the expansion port (J15) is shown in the following figure 3-10-1

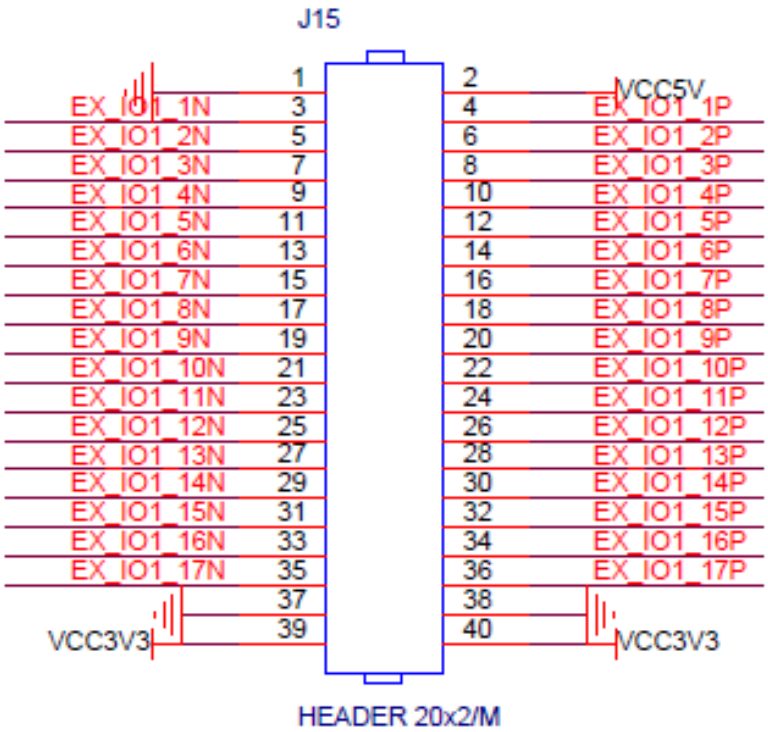


Figure 3-10-1 Schematic diagram of J15 expansion port

Pin allocation for J15 expansion port ZYNQ

Pin numbering	ZYNQ pin	Pin numbering	ZYNQ pin
1	GND	**2**	+5V
3	T21	**4**	U21
5	U20	**6**	V20
7	Y19	**8**	AA19
9	J21	**10**	J22

11	K21	**12**	J20
13	P16	**14**	R16
15	M17	**16**	L17
17	T18	**18**	R18
19	P20	**20**	P21
21	T19	**22**	R19
23	P15	**24**	N15
25	M16	**26**	M15
27	AB19	**28**	AB20
29	W22	**30**	V22
31	W21	**32**	W20
33	AA21	**34**	AB21
35	Y21	**36**	Y20
37	GND	**38**	GND
39	+3.3V	**40**	+3.3V

Table 3-10-1 Expansion Port J15 Pin Allocation

The circuit of the expansion port (J16) is shown in Figure 3-10-2 below

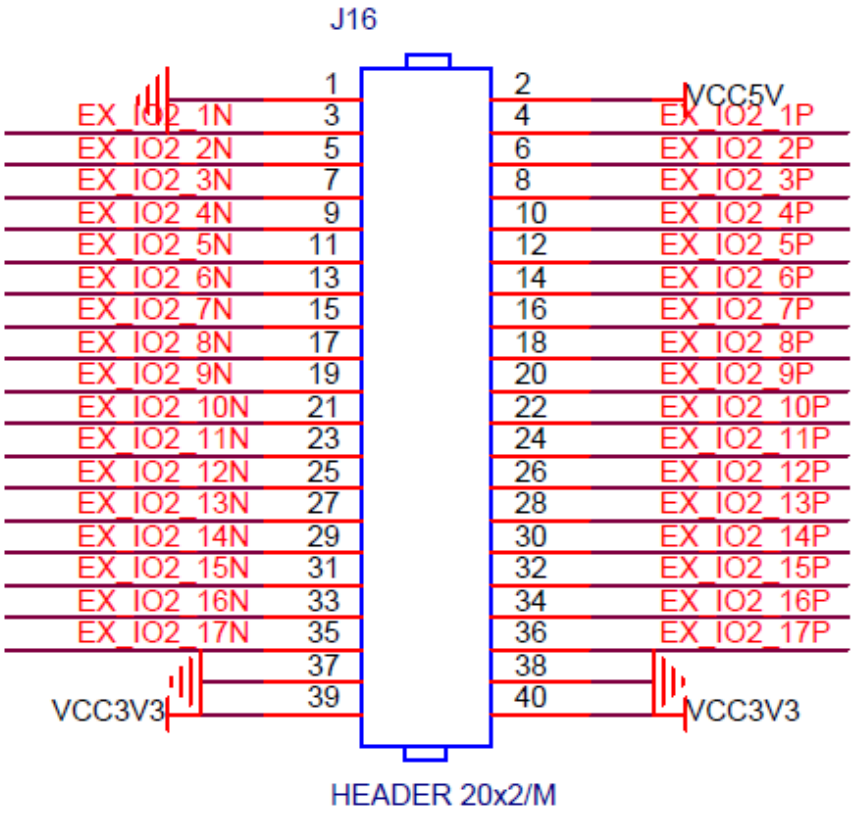


Figure 3-10-2 Schematic diagram of J16 expansion port

Pin allocation for J16 expansion port ZYNQ

Pin numbering	ZYNQ pin	Pin numbering	ZYNQ pin
1	GND	**2**	+5V
3	V12	**4**	W12
5	U12	**6**	U11
7	U9	**8**	U10
9	T6	**10**	R6
11	U5	**12**	U6
13	U4	**14**	T4
15	W10	**16**	W11
17	Y10	**18**	Y11
19	W8	**20**	V8
21	AA6	**22**	AA7

23	AA11	**24**	AB11
25	AB4	**26**	AB5
27	AB1	**28**	AB2
29	Y4	**30**	AA4
31	AB10	**32**	AB9
33	AA9	**34**	AA8
35	AB7	**36**	AB6
37	GND	**38**	GND
39	+3.3V	**40**	+3.3V

Table 3-10-2 Expansion Port J16 Pin Allocation

11. Power supply

The input voltage of the power supply of the development board is DC12V. Please use the power supply that comes with the development board and do not use other specifications to avoid damaging the development board. The base board is converted to + 5V, + 3.3V, and 1.8V power supplies through 3 DC/DC power supply chips ETA1471. The current output of the DCDC power supply is 3A. In addition, there is also an LDO chip on the board with a default output of 3.3V. If the BANK power supply of the SOM's BANK33 and BANK34 is replaced with other voltage levels, the output of the LDO chip on the base board also needs to be modified accordingly.

The power supply design on the extension is shown 3-11-1 figure below:

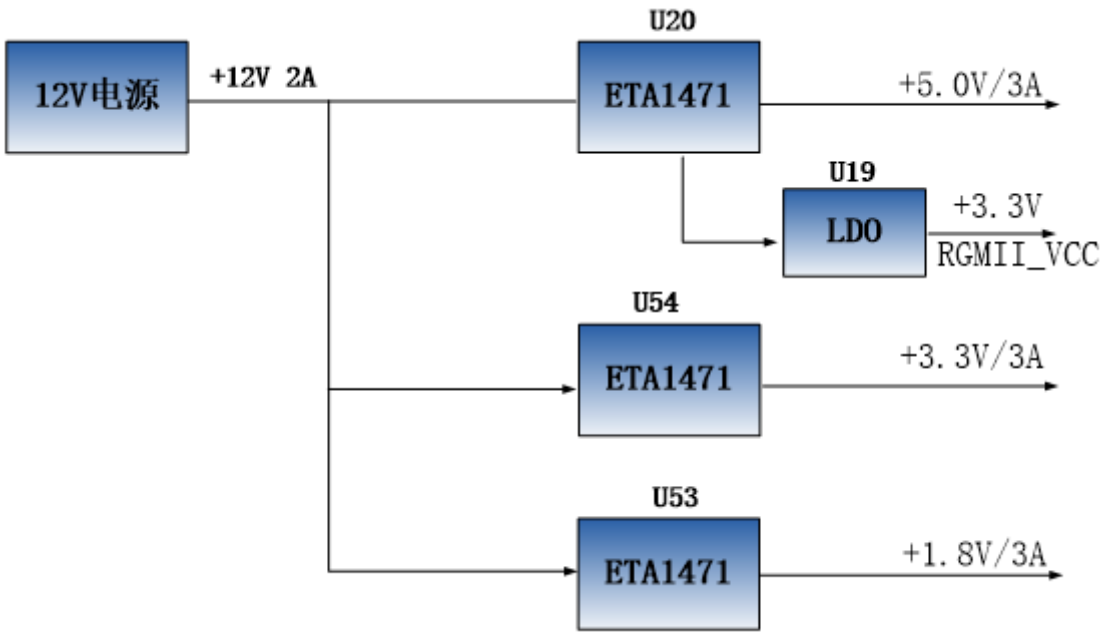


Figure 3-11-1 base board power supply schematic

12. base board structure diagram

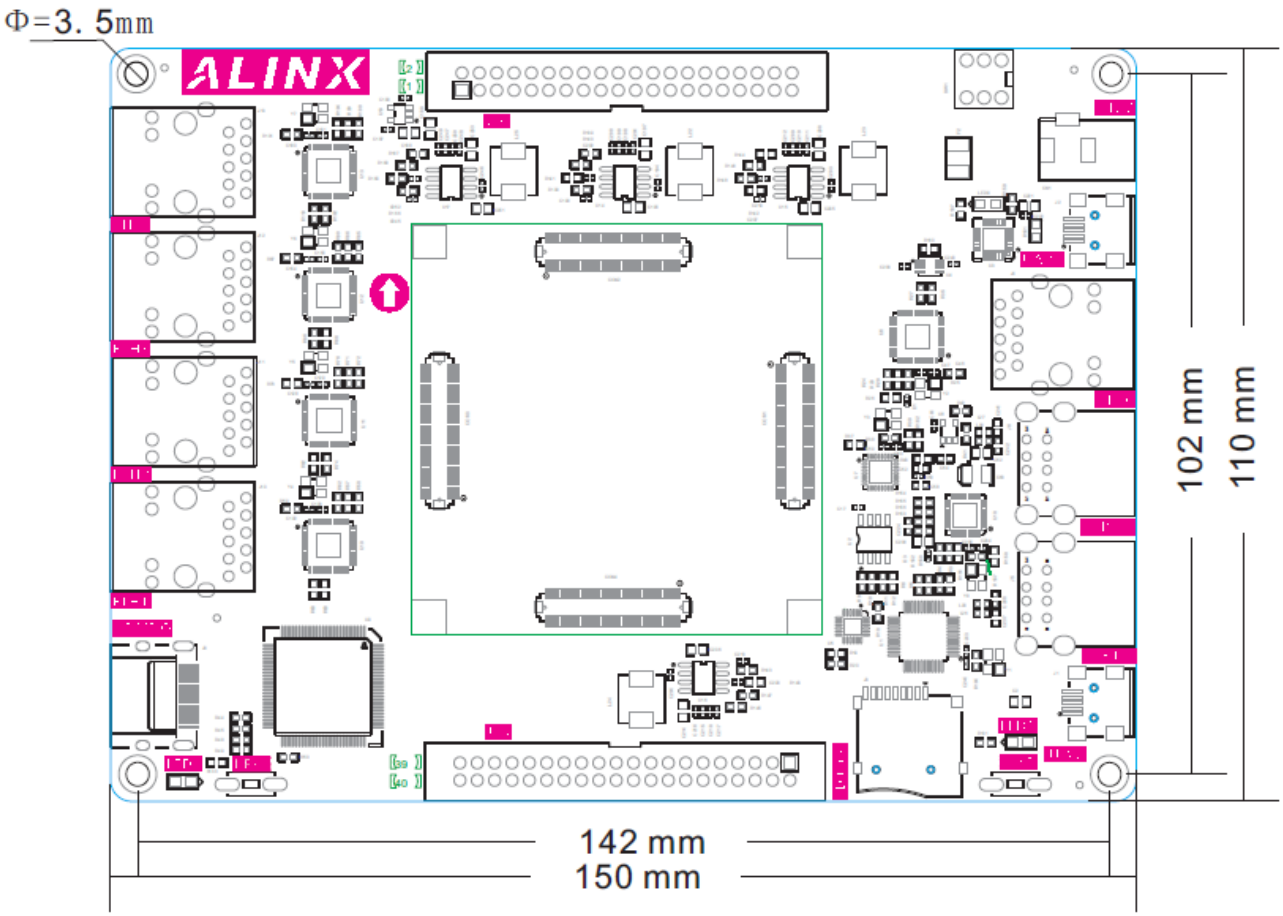


Figure 3-12-1 Top View