ARTIX-7 FPGA Development Board AX7101 User Manual

ALINX

Version Record

Version	Date	Release By	Description
Rev 1.2	2020-10-30	Rachel Zhou	First Release

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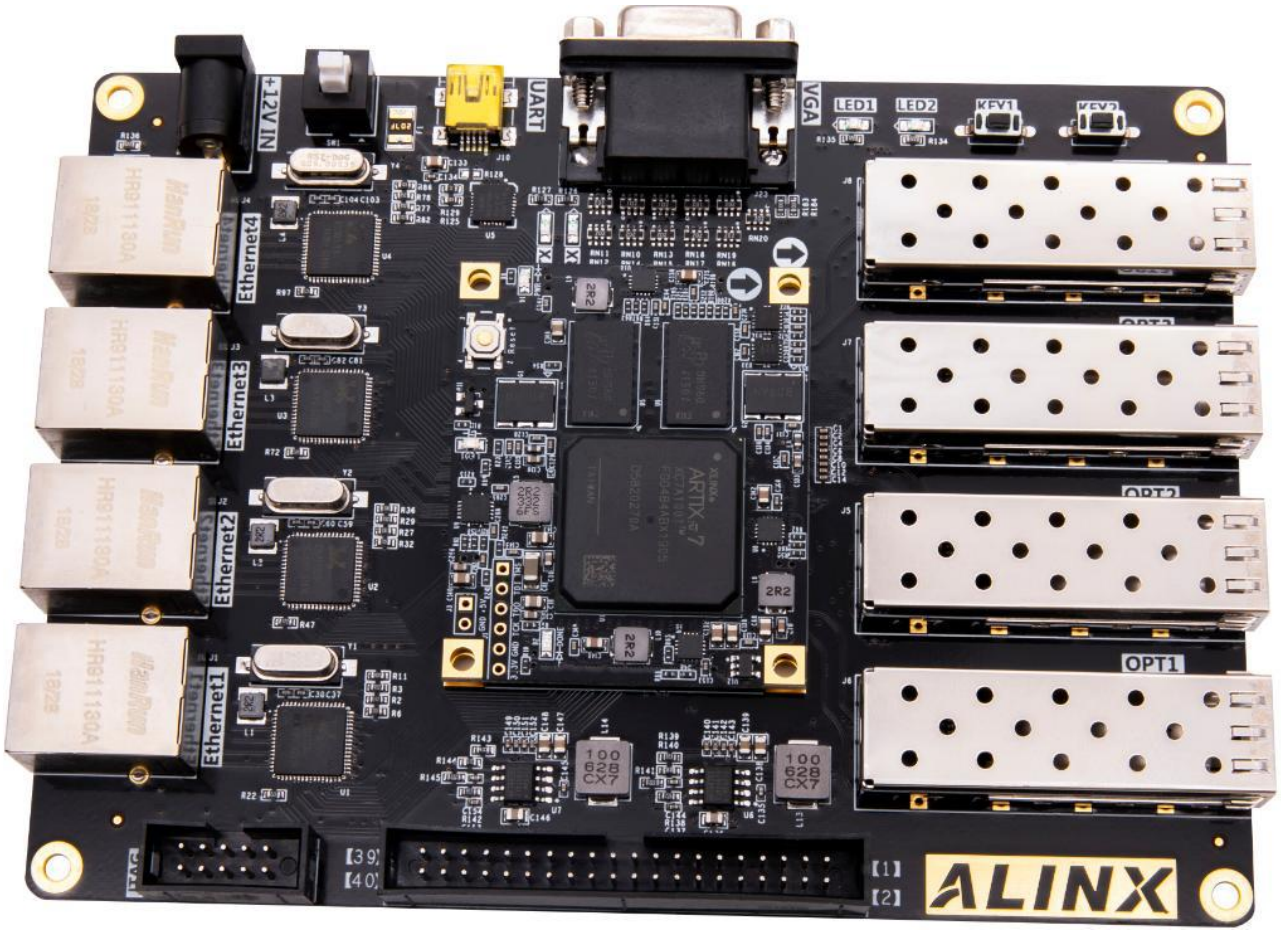
This ARTIX-7 FPGA development platform (**Module: AX7101**) adopts the core board + carrier board mode, which is convenient for users to use the core board for secondary development.

In the design of carrier Board, we have extended 4 fiber interfaces and 4 Gigabit Ethernet interfaces. It meets user's requirements for high-speed data transmission and exchange. It is a "Versatile" and “Professional” ARTIX-7 FPGA development platform. It provides the applications for multi-channel video transmission, multi-channel networks, fiber-optic communication, and data processing. This product is very suitable for students, engineers and other groups engaged data communication and video image processing.



Part 1: FPGA Development Board Introduction

The entire structure of the AX7101 FPGA development board is inherited from our consistent “core board + carrier board” model. A high-speed inter-board connector is used between the core board and the carrier board.

The core board is mainly composed of FPGA + 2 DDR3 + QSPI FLASH, which undertakes the functions of high-speed data processing and storage of FPGA, high-speed data reading and writing between FPGA and two DDR3s, data bit width is 32 bits, and the bandwidth of the whole system is up to 25Gb. /s(800M*32bit); The two DDR3 capacities are up to 8Gbit, which meets the need for high buffers during data processing. The selected FPGA is the XC7A100T chip of XILINX's ARTIX-7 series, in BGA 484 package. The communication frequency between the XC7A100T and DDR3 reaches 400Mhz and the data rate is 800Mhz, which fully meets the needs of high-speed multi-channel data processing. In addition, the XC7A100T FPGA features four GTP high-speed transceivers with speeds up to 6.6Gb/s per channel, making it ideal for fiber-optic communications and PCIe data communications.

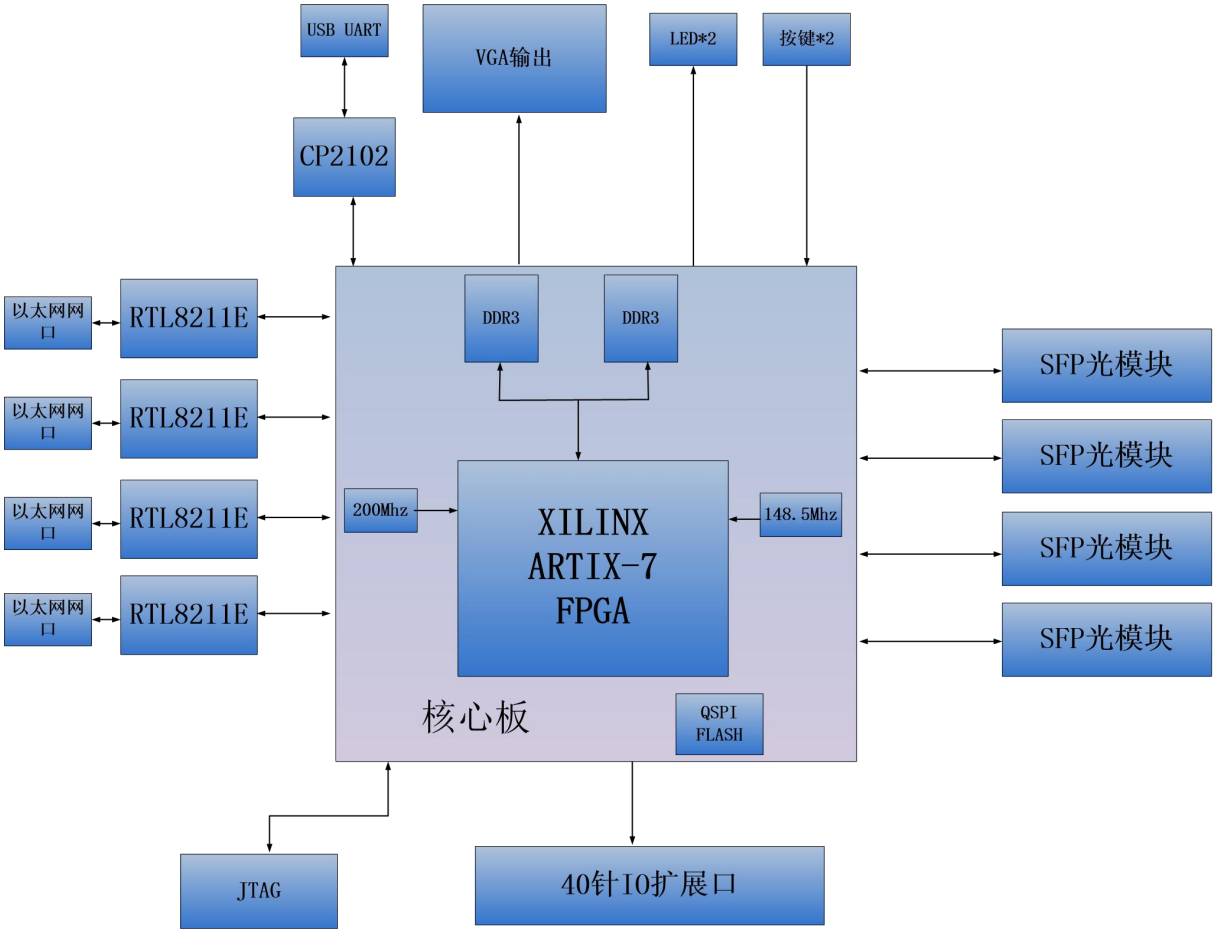


Figure 1-1-1: The Schematic Diagram of the AX7101

Through this diagram, you can see the interfaces and functions that the AX7101 FPGA Development Board contains:

- Artix-7 FPGA core board

  The core board consists of XC7A100T + 8Gb DDR3 + 128Mb QSPI FLASH. There are two high-precision Sitime LVDS differential crystals, one at 200MHz and the other at 125MHz, providing stable clock input for FPGA systems and GTP modules.

- 4-channel Gigabit Ethernet Interface RJ-45 interface

  The Gigabit Ethernet interface chip uses Realtek's RTL8211EG Ethernet PHY chip to provide network communication services to users. RTL8211EG chip supports 10/100/1000 Mbps network transmission rate. Full duplex and adaptive

- 4-channel high-speed SFP Interface

  The four high-speed transceivers of the GTP transceiver of ARTIX-7 FPGA are connected to the transmission and reception of four optical modules to realize four high-speed optical fiber communication interfaces. Each fiber optic data communication receives and transmits at speeds up to 6.6 Gb/s.

- 1-channel VGA Output interface

  16-bit color VGA analog output, RGB565 format, can generate 32 gradient grade red and blue signals and 64 gradient grade green signals

- 1-channel Uart to USB interface

  1 Uart to USB interface for communication with the computer for user debugging. The serial port chip is the USB-UAR chip of Silicon Labs CP2102GM, and the USB interface is the MINI USB interface.

- 40-pin expansion port

  40-pin 0.1inch spacing expansion port can be connected to various ALINX modules (binocular camera, TFT LCD screen, high-speed AD module, etc.). The expansion port contains 1 channel 5V power supply, 2 channel 3.3V power supply, 3 way ground, 34 IOs port.

- JTAG Interface

  A 10-pin 0.1 spacing standard JTAG ports for FPGA program download and debugging.

- Key

  2 Keys; 1 reset Key (on the core board)

- LED Light

  3 user LEDs (1 on the core board and 2 on the Carrier Board)

Part 2: AC7100B core board

Part 2.1: AC7100B Core Board Introduction

AC7100B (core board model, the same below) FPGA core board, it is based on XILINX's ARTIX-7 series 100T XC7A100T-2FGG484I. It is a high-performance core board with high speed, high bandwidth and high capacity. It is suitable for high-speed data communication, video image processing, high-speed data acquisition, etc.

This AC7100 core board uses two pieces of MICRON's MT41J256M16HA-125 DDR3 chip, each DDR has a capacity of 4Gbit; two DDR chips are combined into a 32-bit data bus width, and the read/write data bandwidth between FPGA and DDR3 is up to 25Gb; such a configuration can meet the needs of high bandwidth data processing.

The AC7100B core board expands 180 standard IO ports of 3.3V level, 15 standard IO ports of 1.5V level, and 4 pairs of GTP high speed RX/TX differential signals. For users who need a lot of IO, this core board will be a good choice. Moreover, the routing between the FPGA chip and the interface is equal length and differential processing, and the core board size is only 45*55 (mm), which is very suitable for secondary development.

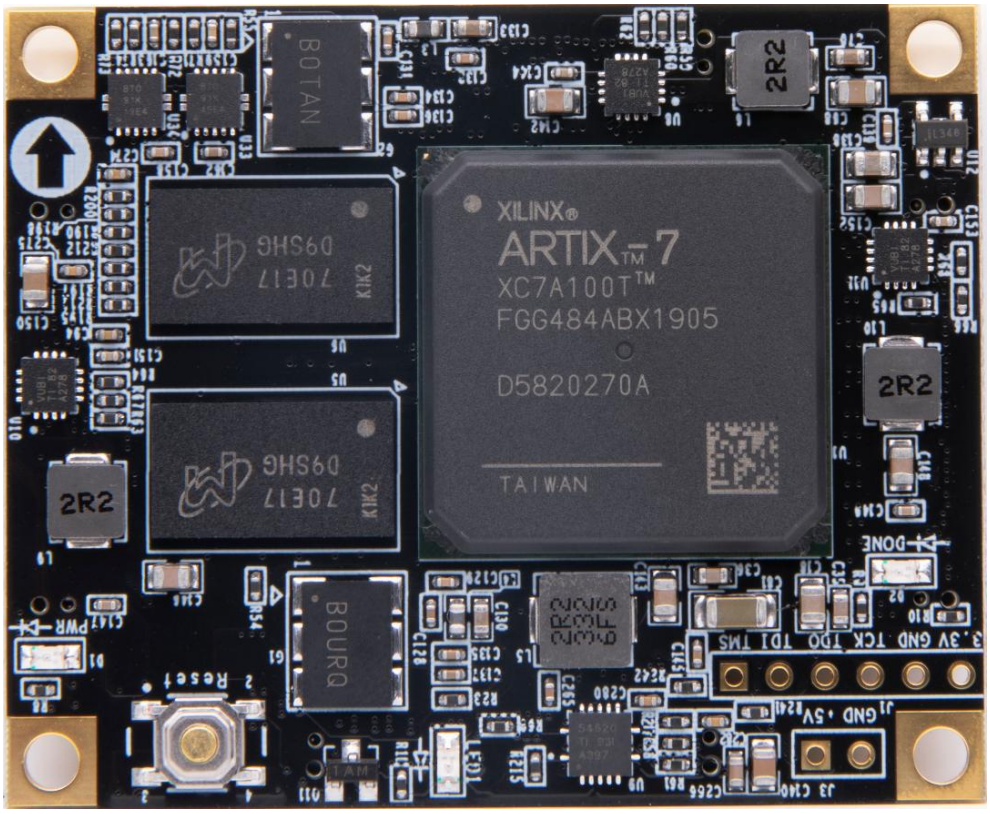


Figure 2-1-1: AC7100B Core Board (Front View)

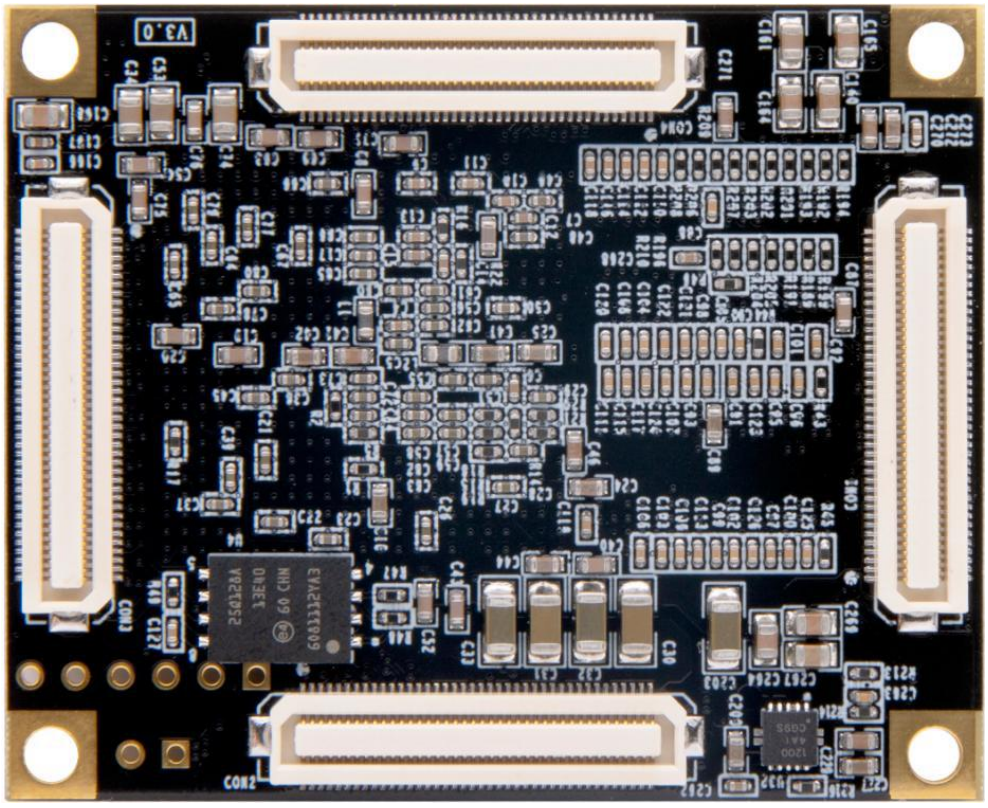


Figure 2-1-2: AC7100B Core Board (Rear View)

Part 2.2: FPGA Chip

As mentioned above, the FPGA model we use is XC7A100T-2FGG484I, which belongs to Xilinx's Artix-7 series. The speed grade is 2, and the temperature grade is industry grade. This model is a FGG484 package with 484 pins. Xilinx ARTIX-7 FPGA chip naming rules as below

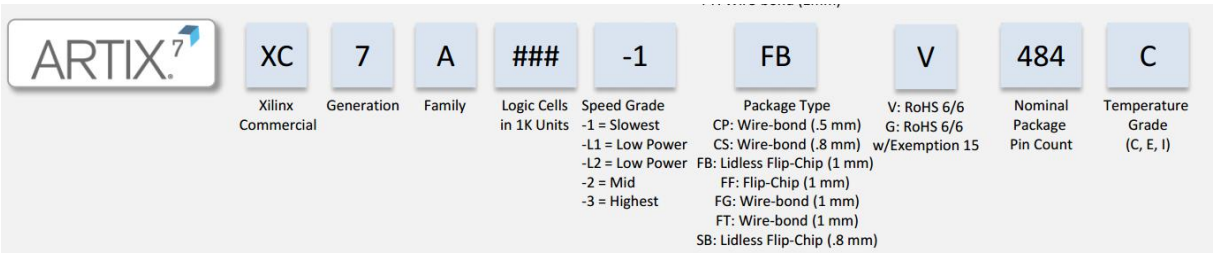


Figure 2-2-1: The Specific Chip Model Definition of ARTIX-7 Series

Figure 2-2-2: FPGA chip on board

The main parameters of the FPGA chip XC7A100T are as follows

Name	Specific parameters
Logic Cells	101440
Slices	15850
CLB flip-flops	126800
Block RAM（kb）	4860
DSP Slices	240
PCIe Gen2	1
XADC	1 XADC, 12bit, 1Mbps AD
GTP Transceiver	4 GTP, 6.6Gb/s max
Speed Grade	-2
Temperature Grade	Industrial

FPGA power supply system

Artix-7 FPGA power supplies are V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, V_{CCO}, $V_{MGTAVCC}$ and $V_{MGTAVTT}$. V_{CCINT} is the FPGA core power supply pin, which needs to be connected to 1.0V; V_{CCBRAM} is the power supply pin of FPGA block RAM, connect to 1.0V; V_{CCAUX} is FPGA auxiliary power supply pin, connect 1.8V; V_{CCO} is the voltage of each BANK of FPGA, including BANK0, BANK13~16, BANK34~35. On AC7100 FPGA core board, BANK34 and BANK35 need to be connected to DDR3, the voltage connection of BANK is 1.5V, and the voltage of other BANK is 3.3V. The VCCO of BANK15 and BANK16 is powered by the LDO, and can be changed by replacing the LDO chip. VMGTAVCC is the supply voltage of the FPGA internal GTP transceiver, connected to 1.0V; VMGTAVTT is the termination voltage of the GTP transceiver, connected to 1.2V.

The Artix-7 FPGA system requires that the power-up sequence be powered by VCCINT, then VCCBRAM, then VCCAUX, and finally VCCO. If VCCINT and VCCBRAM have the same voltage, they can be powered up at the same time. The order of power outages is reversed. The power-up sequence of the GTP transceiver is VCCINT, then VMGTAVCC, then VMGTAVTT. If VCCINT and VMGTAVCC have the same voltage, they can be powered up at the same time. The power-off sequence is just the opposite of the power-on sequence.

Part 2.3: Active Differential Crystal

The AC7100B core board is equipped with two Sitime active differential crystals, one is 200MHz, the model is SiT9102-200.00MHz, the system main clock for FPGA and used to generate DDR3 control clock; the other is 125MHz, model is SiT9102 -125MHz, reference clock input for GTP transceivers.

Part 2.3.1: 200Mhz Active Differential clock

G1 in Figure 2-3-1 is the 200M active differential crystal that provides the development board system clock source. The crystal output is connected to the

BANK34 global clock pin MRCC (R4 and T4) of the FPGA. This 200Mhz differential clock can be used to drive the user logic in the FPGA. Users can configure the PLLs and DCMs inside the FPGA to generate clocks of different frequencies.

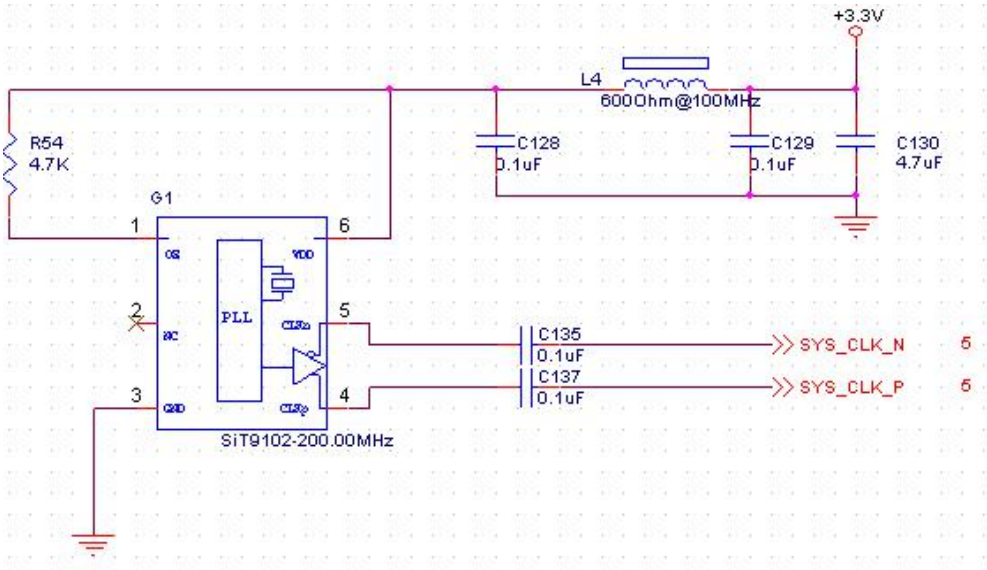


Figure 2-3-1: 200Mhz Active Differential Crystal Schematic

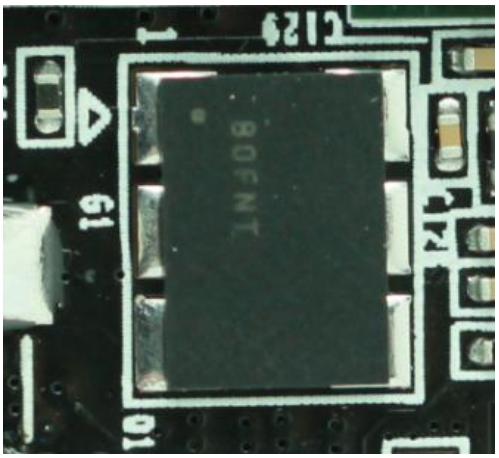


Figure 2-3-2: 200Mhz Active Differential Crystal on the Core Board

200Mhz Differential Clock Pin Assignment

Signal Name	FPGA PIN
SYS_CLK_P	R4
SYS_CLK_N	T4

Part 2.3.2: 125Mhz Active Differential Crystal

G2 in Figure 2-3-3 is the 125Mhz active differential crystal, which is the reference input clock provided to the GTP module inside the FPGA. The crystal

output is connected to the GTP BANK216 clock pins MGTREFCLK0P (F6) and MGTREFCLK0N (E6) of the FPGA.

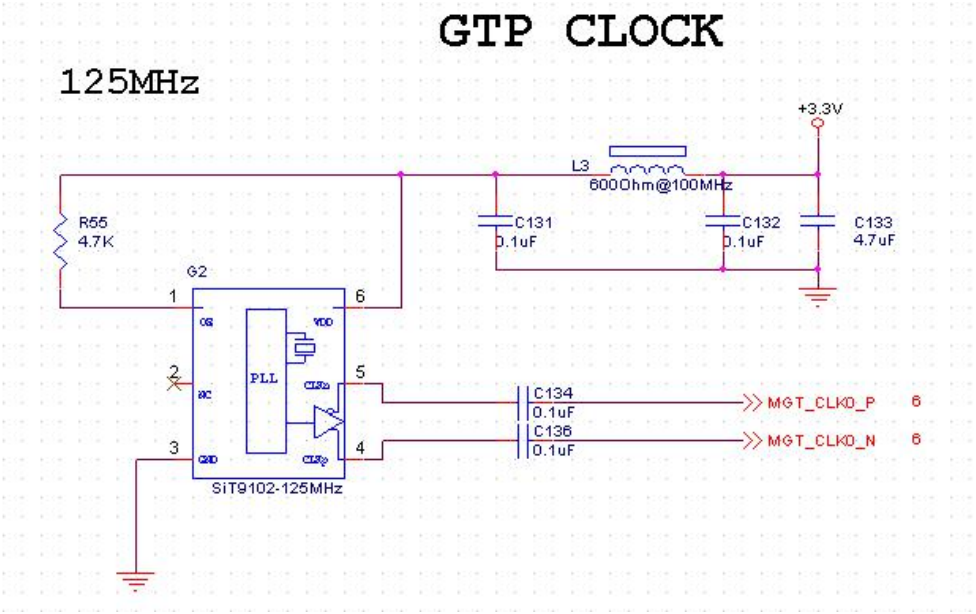


Figure 2-3-3: 125Mhz Active Differential Crystal Schematic

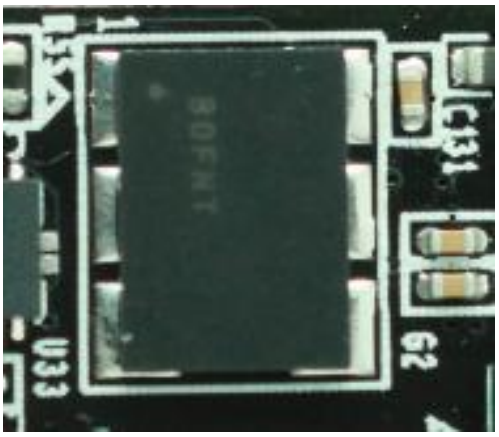


Figure 2-3-4: 125Mhz Active Differential Crystal on the Core Board

125Mhz Differential Clock Pin Assignment

Net Name	FPGA PIN
MGT_CLK0_P	F6
MGT_CLK0_N	E6

Part 2.4: DDR3 DRAM

The FPGA core board AC7100B is equipped with two Micron 4Gbit (512MB) DDR3 chips, model MT41J256M16HA-125 (compatible with MT41K256M16HA-125). The DDR3 SDRAM has a maximum operating speed of 800MHz (data rate 1600Mbps). The DDR3 memory system is directly connected to the memory interface of the BANK 34 and BANK35 of the FPGA. The specific configuration of DDR3 SDRAM is shown in Table 2-4-1.

Bit Number	Chip Model	Capacity	Factory
U5,U6	MT41J256M16HA-125	256M x 16bit	Micron

Table 2-4-1: DDR3 SDRAM Configuration

The hardware design of DDR3 requires strict consideration of signal integrity. We have fully considered the matching resistor/terminal resistance, trace impedance control, and trace length control in circuit design and PCB design to ensure high-speed and stable operation of DDR3. The hardware connection diagram of DDR3 DRAM is shown in Figure 2-4-1:

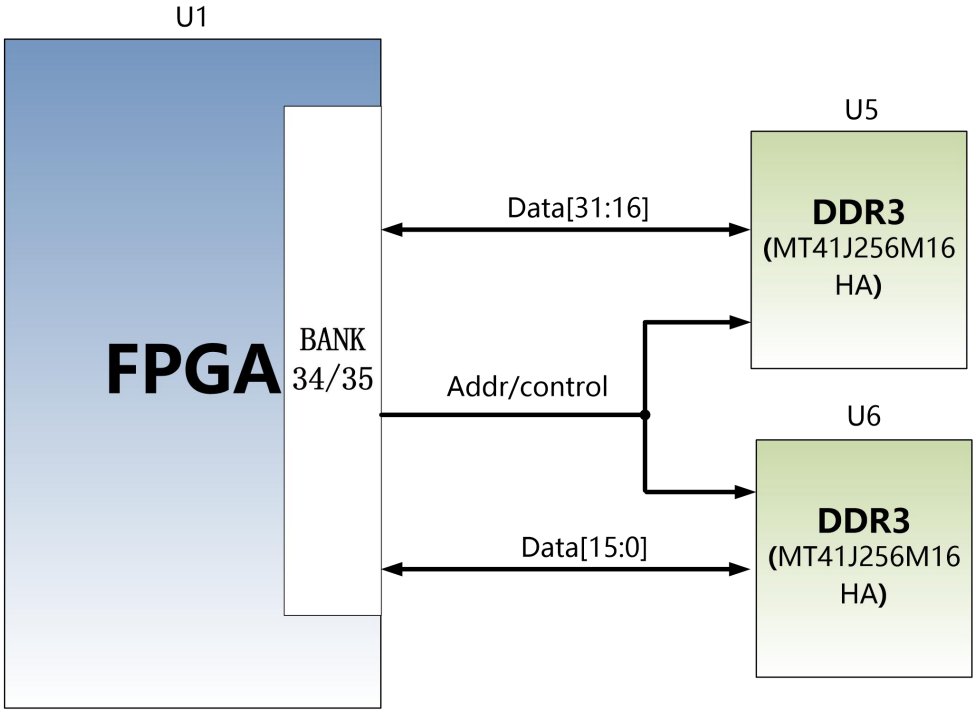


Figure 2-4-1: The DDR3 DRAM Schematic

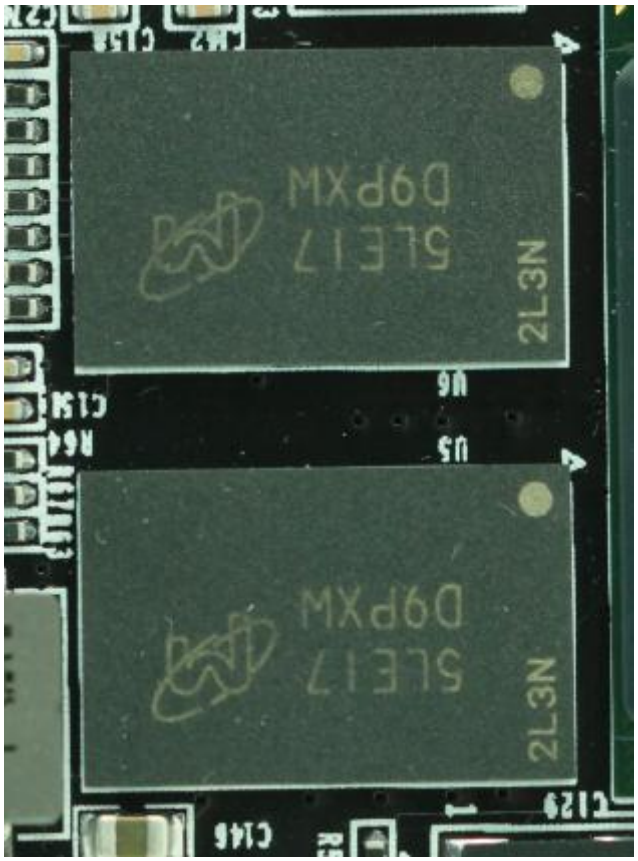


Figure 2-4-2: The DDR3 on the Core Board

DDR3 DRAM pin assignment:

Net Name	FPGA PIN Name	FPGA P/N
DDR3_DQS0_P	IO_L3P_T0_DQS_AD5P_35	E1
DDR3_DQS0_N	IO_L3N_T0_DQS_AD5N_35	D1
DDR3_DQS1_P	IO_L9P_T1_DQS_AD7P_35	K2
DDR3_DQS1_N	IO_L9N_T1_DQS_AD7N_35	J2
DDR3_DQS2_P	IO_L15P_T2_DQS_35	M1
DDR3_DQS2_N	IO_L15N_T2_DQS_35	L1
DDR3_DQS3_P	IO_L21P_T3_DQS_35	P5
DDR3_DQS3_N	IO_L21N_T3_DQS_35	P4
DDR3_DQ[0]	IO_L2P_T0_AD12P_35	C2
DDR3_DQ [1]	IO_L5P_T0_AD13P_35	G1
DDR3_DQ [2]	IO_L1N_T0_AD4N_35	A1
DDR3_DQ [3]	IO_L6P_T0_35	F3

DDR3_DQ [4]	IO_L2N_T0_AD12N_35	B2
DDR3_DQ [5]	IO_L5N_T0_AD13N_35	F1
DDR3_DQ [6]	IO_L1P_T0_AD4P_35	B1
DDR3_DQ [7]	IO_L4P_T0_35	E2
DDR3_DQ [8]	IO_L11P_T1_SRCC_35	H3
DDR3_DQ [9]	IO_L11N_T1_SRCC_35	G3
DDR3_DQ [10]	IO_L8P_T1_AD14P_35	H2
DDR3_DQ [11]	IO_L10N_T1_AD15N_35	H5
DDR3_DQ [12]	IO_L7N_T1_AD6N_35	J1
DDR3_DQ [13]	IO_L10P_T1_AD15P_35	J5
DDR3_DQ [14]	IO_L7P_T1_AD6P_35	K1
DDR3_DQ [15]	IO_L12P_T1_MRCC_35	H4
DDR3_DQ [16]	IO_L18N_T2_35	L4
DDR3_DQ [17]	IO_L16P_T2_35	M3
DDR3_DQ [18]	IO_L14P_T2_SRCC_35	L3
DDR3_DQ [19]	IO_L17N_T2_35	J6
DDR3_DQ [20]	IO_L14N_T2_SRCC_35	K3
DDR3_DQ [21]	IO_L17P_T2_35	K6

Part 2.5: QSPI Flash

The FPGA core board AC7100B is equipped with one 128MBit QSPI FLASH, and the model is N25Q128, which uses the 3.3V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, it can be used as a boot device for the system to store the boot image of the system. These images mainly include FPGA bit files, ARM application code, core application code and other user data files. The specific models and related parameters of QSPI FLASH are shown in Table 2-5-1.

Position	Model	Capacity	Factory
U8	N25Q128	128M Bit	Numonyx

Table 2-5-1: QSPI FLASH Specification

QSPI FLASH is connected to the dedicated pins of BANK0 and BANK14 of

the FPGA chip. The clock pin is connected to CCLK0 of BANK0, and other data and chip select signals are connected to D00~D03 and FCS pins of BANK14 respectively. Figure 2-5-1 shows the hardware connection of QSPI Flash.

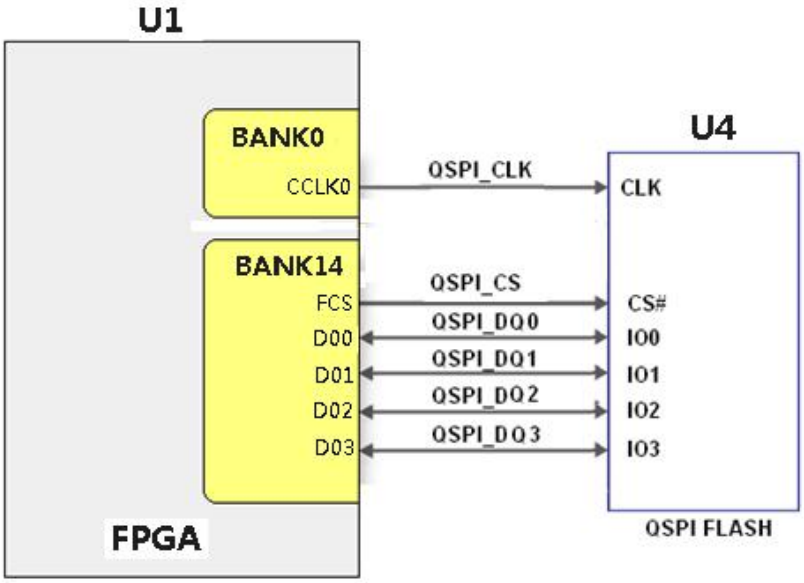


Figure 2-5-1: QSPI Flash Schematic

QSPI Flash pin assignments:

Net Name	FPGA PIN Name	FPGA P/N
QSPI_CLK	CCLK_0	L12
QSPI_CS	IO_L6P_T0_FCS_B_14	T19
QSPI_DQ0	IO_L1P_T0_D00_MOSI_14	P22
QSPI_DQ1	IO_L1N_T0_D01_DIN_14	R22
QSPI_DQ2	IO_L2P_T0_D02_14	P21
QSPI_DQ3	IO_L2N_T0_D03_14	R21

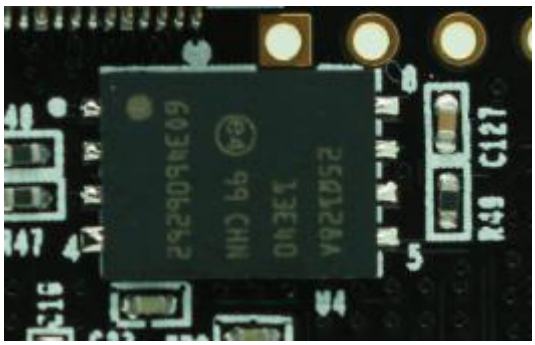


Figure 2-5-2: QSPI on the Core Board

Part 2.6: LED Light on Core Board

There are 3 red LED lights on the AC7100B FPGA core board, one of which is the power indicator light (PWR), one is the configuration LED light (DONE), and one is the user LED light. When the core board is powered, the power indicator will illuminate; when the FPGA is configured, the configuration LED will illuminate. The user LED light is connected to the IO of the BANK34, the user can control the light on and off by the program. When the IO voltage connected to the user LED is high, the user LED is off. When the connection IO voltage is low, the user LED will be lit. The schematic diagram of the LED light hardware connection is shown in Figure 2-6-1:

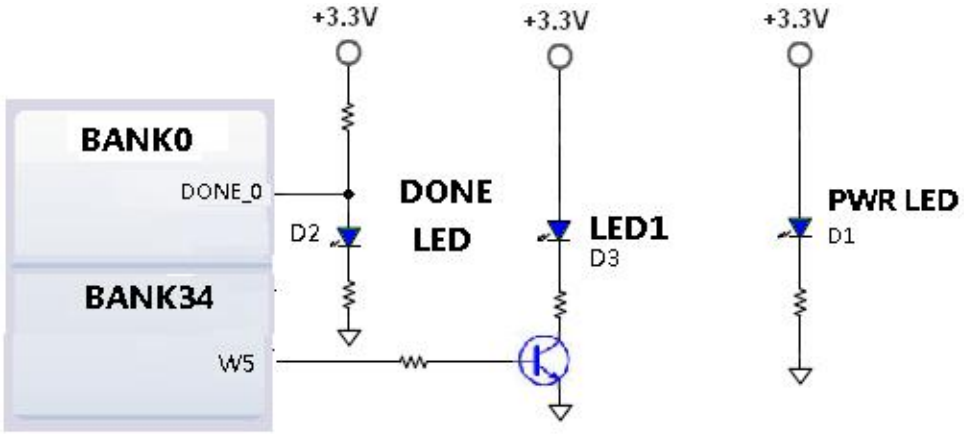


Figure 2-6-1: LED lights on core board Schematic

User LEDs Pin Assignment

Signal Name	FPGA Pin Name	FPGA Pin Number	Description
LED1	IO_L15N_T2_DQS_34	W5	User LED

Part 2.7: Reset key

There is a reset key on the AC7100B FPGA core board. The reset key is connected to the normal IO of the BANK34 of the FPGA chip. The user can use this reset key to initialize the FPGA program. When the key is pressed in the design, the signal voltage input to IO is low, and the reset signal is valid; when the key is not pressed, the signal input to IO is high. The schematic diagram of

the reset key connection is shown in Figure 2-7-1:

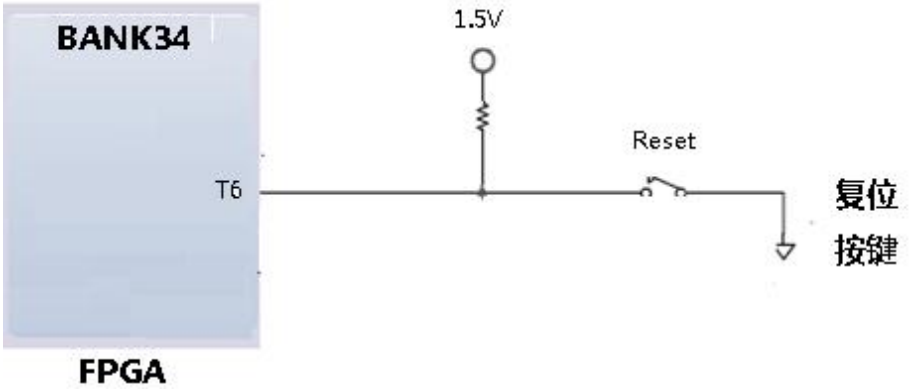


Figure 2-7-1: Reset key Schematic

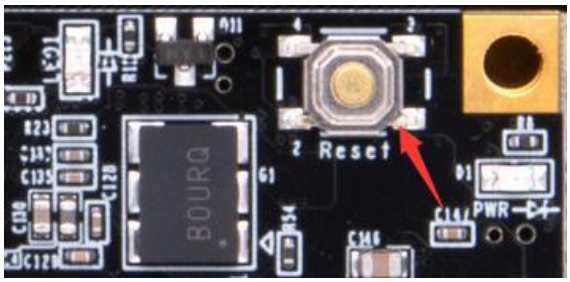


Figure 2-7-2: Reset key on the Core Board

Reset key pin assignment

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
RESET_N	IO_L17N_T2_34	T6	Reset Key

Part 2.8: JTAG Interface

The JTAG test socket J1 is reserved on the AC7100B core board for JTAG download and debugging when the core board is used alone. Figure 2-8-1 is the schematic part of the JTAG port, which involves TMS, TDI, TDO, TCK. , GND, +3.3V these six signals.

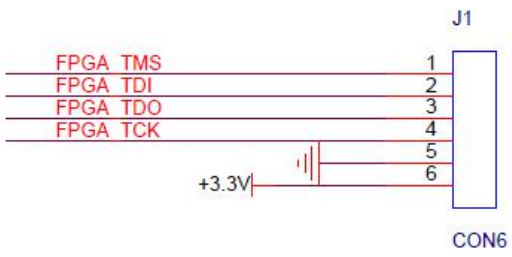


Figure 2-8-1: JTAG Interface Schematic

The JTAG interface J1 on AC7100B FPGA core board uses a 6-pin 2.54mm pitch single-row test hole. If you need to use the JTAG connection to debug on the core board, you need to solder a 6-pin single-row pin header. Figure 2-8-2 shows the JTAG interface J1 on the AC7100B FPGA core board.

Figure 2-8-2: JTAG Interface on Core Board

Part 2.9: Power Interface on the Core Board

In order to make the AC7100B FPGA core board work alone, the core board reserve a 2 PIN interface (J3), and power the core board separately by connecting a 5V power supply. Among them, PIN1 pin is connected to +5V, PIN2 pin is grounded, and the positive and negative pins should not be connected wrongly.

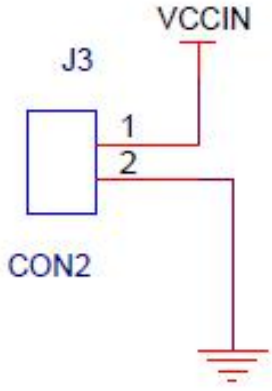


Figure 2-9-1: J3 interface schematic

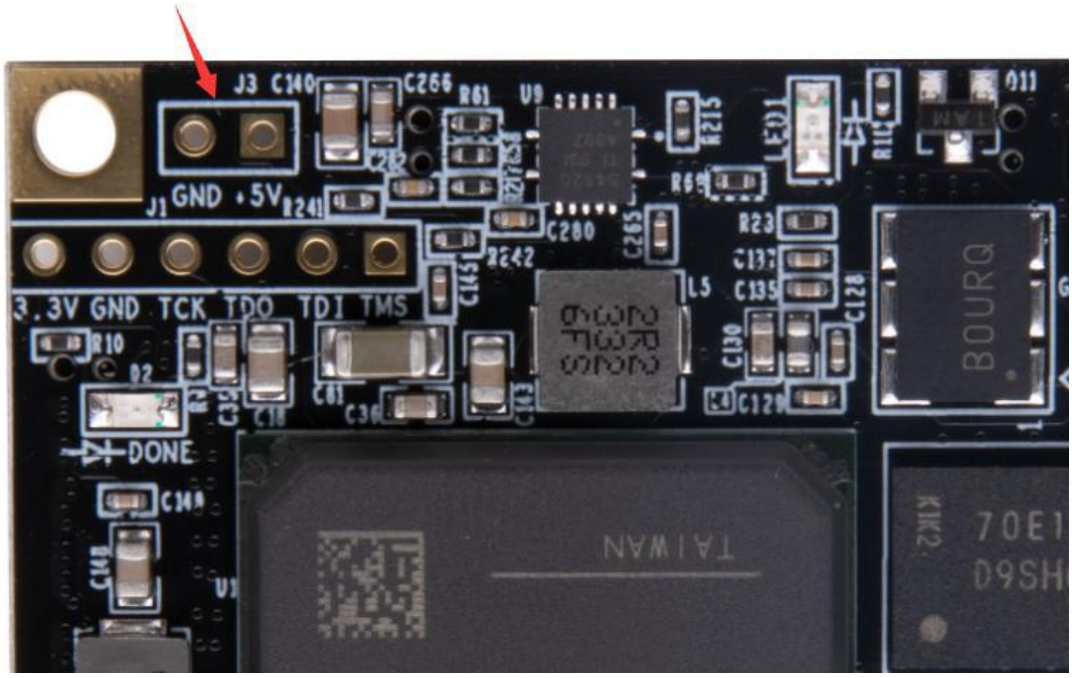


Figure 2-9-2：J3 interface on the Core Board

Part 2.10: Board to Board Connectors pin assignment

The core board has a total of four high-speed board to board connectors. The core board uses four 80-pin inter-board connectors to connect to the carrier board. The IO port of the FPGA is connected to the four connectors by differential routing. The pin spacing of the connectors is 0.5mm, insert to the board to board connectors on the carrier board for high-speed data communication.

Board to Board Connectors CON1

The 80-pin board to board connectors CON1, which are used to connect with the VCCIN power supply (+5V) and ground on the carrier board, extend the normal IOs of the FPGA. It should be noted here that 15 pins of CON1 are connected to the IO port of BANK34, because the BANK34 connection is connected to DDR3. Therefore, the voltage standard of all IOs of this BANK34 is 1.5V.

Pin Assignment of Board to Board Connectors CON1

CON1 Pin	Signal Name	FPGA Pin	Voltage Level	CON1 Pin	Signal Name	FPGA Pin	Voltage Level
PIN1	VCCIN	-	+5V	PIN2	VCCIN	-	+5V
PIN3	VCCIN	-	+5V	PIN4	VCCIN	-	+5V
PIN5	VCCIN	-	+5V	PIN6	VCCIN	-	+5V
PIN7	VCCIN	-	+5V	PIN8	VCCIN	-	+5V
PIN9	GND	-	Ground	PIN10	GND	-	Ground
PIN11	NC	-	-	PIN12	NC	-	-
PIN13	NC	-	-	PIN14	NC	-	-
PIN15	NC	-	-	PIN16	B13_L4_P	AA15	3.3V
PIN17	NC	-	-	PIN18	B13_L4_N	AB15	3.3V
PIN19	GND	-	Ground	PIN20	GND	-	Ground
PIN21	B13_L5_P	Y13	3.3V	PIN22	B13_L1_P	Y16	3.3V
PIN23	B13_L5_N	AA14	3.3V	PIN24	B13_L1_N	AA16	3.3V
PIN25	B13_L7_P	AB11	3.3V	PIN26	B13_L2_P	AB16	3.3V
PIN27	B13_L7_P	AB12	3.3V	PIN28	B13_L2_N	AB17	3.3V
PIN29	GND	-	Ground	PIN30	GND	-	Ground
PIN31	B13_L3_P	AA13	3.3V	PIN32	B13_L6_P	W14	3.3V
PIN33	B13_L3_N	AB13	3.3V	PIN34	B13_L6_N	Y14	3.3V
PIN35	B34_L23_P	Y8	1.5V	PIN36	B34_L20_P	AB7	1.5V
PIN37	B34_L23_N	Y7	1.5V	PIN38	B34_L20_N	AB6	1.5V
PIN39	GND	-	Ground	PIN40	GND	-	Ground
PIN41	B34_L18_N	AA6	1.5V	PIN42	B34_L21_N	V8	1.5V
PIN43	B34_L18_P	Y6	1.5V	PIN44	B34_L21_P	V9	1.5V
PIN45	B34_L19_P	V7	1.5V	PIN46	B34_L22_P	AA8	1.5V
PIN47	B34_L19_N	W7	1.5V	PIN48	B34_L22_N	AB8	1.5V
PIN49	GND	-	Ground	PIN50	GND	-	Ground
PIN51	XADC_VN	M9	ADC	PIN52	NC		
PIN53	XADC_VP	L10	ADC	PIN54	B34_L25	U7	1.5V
PIN55	NC	-	-	PIN56	B34_L24_P	W9	1.5V
PIN57	NC	-	-	PIN58	B34_L24_N	Y9	1.5V

PIN59	GND	-	Ground	PIN60	GND	-	Ground
PIN61	B16_L1_N	F14	3.3V	PIN62	NC	-	-
PIN63	B16_L1_P	F13	3.3V	PIN64	NC	-	-
PIN65	B16_L4_N	E14	3.3V	PIN66	NC	-	-
PIN67	B16_L4_P	E13	3.3V	PIN68	NC	-	-
PIN69	GND	-	Ground	PIN70	GND	-	Ground
PIN71	B16_L6_N	D15	3.3V	PIN72	NC	-	-

Board to Board Connectors CON2

The 80-pin female connection header CON2 is used to extend the normal IO of the BANK13 and BANK14 of the FPGA. The voltage standards of both BANKs are 3.3V.

Pin Assignment of Board to Board Connectors CON2

CON1 Pin	Signal Name	FPGA Pin	Voltage Level	CON1 Pin	Signal Name	FPGA Pin	Voltage Level
PIN1	B13_L16_P	W15	3.3V	PIN2	B14_L16_P	V17	3.3V
PIN3	B13_L16_N	W16	3.3V	PIN4	B14_L16_N	W17	3.3V
PIN5	B13_L15_P	T14	3.3V	PIN6	B13_L14_P	U15	3.3V
PIN7	B13_L15_N	T15	3.3V	PIN8	B13_L14_N	V15	3.3V
PIN9	GND	-	Ground	PIN10	GND	-	Ground
PIN11	B13_L13_P	V13	3.3V	PIN12	B14_L10_P	AB21	3.3V
PIN13	B13_L13_N	V14	3.3V	PIN14	B14_L10_N	AB22	3.3V
PIN15	B13_L12_P	W11	3.3V	PIN16	B14_L8_N	AA21	3.3V
PIN17	B13_L12_N	W12	3.3V	PIN18	B14_L8_P	AA20	3.3V
PIN19	GND	-	Ground	PIN20	GND	-	Ground
PIN21	B13_L11_P	Y11	3.3V	PIN22	B14_L15_N	AB20	3.3V
PIN23	B13_L11_N	Y12	3.3V	PIN24	B14_L15_P	AA19	3.3V
PIN25	B13_L10_P	V10	3.3V	PIN26	B14_L17_P	AA18	3.3V
PIN27	B13_L10_N	W10	3.3V	PIN28	B14_L17_N	AB18	3.3V
PIN29	GND	-	Ground	PIN30	GND	-	Ground
PIN31	B13_L9_N	AA11	3.3V	PIN32	B14_L6_N	T20	3.3V

PIN33	B13_L9_P	AA10	3.3V	PIN34	B13_IO0	Y17	3.3V
PIN35	B13_L8_N	AB10	3.3V	PIN36	B14_L7_N	W22	3.3V
PIN37	B13_L8_P	AA9	3.3V	PIN38	B14_L7_P	W21	3.3V
PIN39	GND	-	Ground	PIN40	GND	-	Ground
PIN41	B14_L11_N	V20	3.3V	PIN42	B14_L4_P	T21	3.3V
PIN43	B14_L11_P	U20	3.3V	PIN44	B14_L4_N	U21	3.3V
PIN45	B14_L14_N	V19	3.3V	PIN46	B14_L9_P	Y21	3.3V
PIN47	B14_L14_P	V18	3.3V	PIN48	B14_L9_N	Y22	3.3V
PIN49	GND	-	Ground	PIN50	GND	-	Ground
PIN51	B14_L5_N	R19	3.3V	PIN52	B14_L12_N	W20	3.3V
PIN53	B14_L5_P	P19	3.3V	PIN54	B14_L12_P	W19	3.3V
PIN55	B14_L18_N	U18	3.3V	PIN56	B14_L13_N	Y19	3.3V
PIN57	B14_L18_P	U17	3.3V	PIN58	B14_L13_P	Y18	3.3V
PIN59	GND	-	Ground	PIN60	GND	-	Ground
PIN61	B13_L17_P	T16	3.3V	PIN62	B14_L3_N	V22	3.3V
PIN63	B13_L17_N	U16	3.3V	PIN64	B14_L3_P	U22	3.3V
PIN65	B14_L21_N	P17	3.3V	PIN66	B14_L20_N	T18	3.3V
PIN67	B14_L21_P	N17	3.3V	PIN68	B14_L20_P	R18	3.3V
PIN69	GND	-	Ground	PIN70	GND	-	Ground
PIN71	B14_L22_P	P15	3.3V	PIN72	B14_L19_N	R14	3.3V
PIN73	B14_L22_N	R16	3.3V	PIN74	B14_L19_P	P14	3.3V
PIN75	B14_L24_N	R17	3.3V	PIN76	B14_L23_P	N13	3.3V
PIN77	B14_L24_P	P16	3.3V	PIN78	B14_L23_N	N14	3.3V
PIN79	B14_IO0	P20	3.3V	PIN80	B14_IO25	N15	3.3V

Board to Board Connectors CON3

The 80-pin connector CON3 is used to extend the normal IO of the BANK15 and BANK16 of the FPGA. In addition, four JTAG signals are also connected to the carrier board via the CON3 connector. The voltage standards of BANK15 and BANK16 can be adjusted by an LDO chip. The default installed LDO is 3.3V. If you want to output other standard levels, you can replace it with

a suitable LDO.

Pin Assignment of Board to Board Connectors CON3

CON1 Pin	Signal Name	FPGA Pin	Voltage Level	CON1 Pin	Signal Name	FPGA Pin	Voltage Level
PIN1	B15_IO0	J16	3.3V	PIN2	B15_IO25	M17	3.3V
PIN3	B16_IO0	F15	3.3V	PIN4	B16_IO25	F21	3.3V
PIN5	B15_L4_P	G17	3.3V	PIN6	B16_L21_N	A21	3.3V
PIN7	B15_L4_N	G18	3.3V	PIN8	B16_L21_P	B21	3.3V
PIN9	GND	-	Ground	PIN10	GND	-	Ground
PIN11	B15_L2_P	G15	3.3V	PIN12	B16_L23_P	E21	3.3V
PIN13	B15_L2_N	G16	3.3V	PIN14	B16_L23_N	D21	3.3V
PIN15	B15_L12_P	J19	3.3V	PIN16	B16_L22_P	E22	3.3V
PIN17	B15_L12_N	H19	3.3V	PIN18	B16_L22_N	D22	3.3V
PIN19	GND	-	Ground	PIN20	GND	-	Ground
PIN21	B15_L11_P	J20	3.3V	PIN22	B16_L24_P	G21	3.3V
PIN23	B15_L11_N	J21	3.3V	PIN24	B16_L24_N	G22	3.3V
PIN25	B15_L1_N	G13	3.3V	PIN26	B15_L8_N	G20	3.3V
PIN27	B15_L1_P	H13	3.3V	PIN28	B15_L8_P	H20	3.3V
PIN29	GND	-	Ground	PIN30	GND	-	Ground
PIN31	B15_L5_P	J15	3.3V	PIN32	B15_L7_N	H22	3.3V
PIN33	B15_L5_N	H15	3.3V	PIN34	B15_L7_P	J22	3.3V
PIN35	B15_L3_N	H14	3.3V	PIN36	B15_L9_P	K21	3.3V
PIN37	B15_L3_P	J14	3.3V	PIN38	B15_L9_N	K22	3.3V
PIN39	GND	-	Ground	PIN40	GND	-	Ground
PIN41	B15_L19_P	K13	3.3V	PIN42	B15_L15_N	M22	3.3V
PIN43	B15_L19_N	K14	3.3V	PIN44	B15_L15_P	N22	3.3V
PIN45	B15_L20_P	M13	3.3V	PIN46	B15_L6_N	H18	3.3V
PIN47	B15_L20_N	L13	3.3V	PIN48	B15_L6_P	H17	3.3V
PIN49	GND	-	Ground	PIN50	GND	-	Ground
PIN51	B15_L14_P	L19	3.3V	PIN52	B15_L13_N	K19	3.3V
PIN53	B15_L14_N	L20	3.3V	PIN54	B15_L13_P	K18	3.3V
PIN55	B15_L21_P	K17	3.3V	PIN56	B15_L10_P	M21	3.3V

PIN57	B15_L21_N	J17	3.3V	PIN58	B15_L10_N	L21	3.3V
PIN59	GND	-	Ground	PIN60	GND	-	Ground
PIN61	B15_L23_P	L16	3.3V	PIN62	B15_L18_P	N20	3.3V
PIN63	B15_L23_N	K16	3.3V	PIN64	B15_L18_N	M20	3.3V
PIN65	B15_L22_P	L14	3.3V	PIN66	B15_L17_N	N19	3.3V
PIN67	B15_L22_N	L15	3.3V	PIN68	B15_L17_P	N18	3.3V
PIN69	GND	-	Ground	PIN70	GND	-	Ground
PIN71	B15_L24_P	M15	3.3V	PIN72	B15_L16_P	M18	3.3V
PIN73	B15_L24_N	M16	3.3V	PIN74	B15_L16_N	L18	3.3V
PIN75	NC	-		PIN76	NC	-	
PIN77	FPGA_TCK	V12	3.3V	PIN78	FPGA_TDI	R13	3.3V
PIN79	FPGA_TDO	U13	3.3V	PIN80	FPGA_TMS	T13	3.3V

Board to Board Connectors CON4

The 80-Pin connector CON4 is used to extend the normal IO and GTP high-speed data and clock signals of the FPGA BANK16. The voltage standard of the IO port of BANK16 can be adjusted by an LDO chip. The default installed LDO is 3.3V. If the user wants to output other standard levels, it can be replaced by a suitable LDO. The high-speed data and clock signals of the GTP are strictly differential routed on the core board. The data lines are equal in length and kept at a certain interval to prevent signal interference.

Pin Assignment of Board to Board Connectors CON4

CON1 Pin	Signal Name	FPGA Pin	Voltage Level	CON1 Pin	Signal Name	FPGA Pin	Voltage Level
PIN1	NC		-	NC		-	NC
PIN3	NC		-	NC		-	NC
PIN5	NC		-	NC		-	NC
PIN7	NC		-	NC		-	NC
PIN9	GND	-	Ground	PIN10	GND	-	Ground
PIN11	NC		-	PIN12	MGT_TX2_P	B6	Differential
PIN13	NC		-	PIN14	MGT_TX2_N	A6	Differential

PIN15	GND	-	Ground	PIN16	GND	-	Ground
PIN17	MGT_TX3_P	D7	Differential	PIN18	MGT_RX2_P	B10	Differential
PIN19	MGT_TX3_N	C7	Differential	PIN20	MGT_RX2_N	A10	Differential
PIN21	GND	-	Ground	PIN22	GND	-	Ground
PIN23	MGT_RX3_P	D9	Differential	PIN24	MGT_TX0_P	B4	Differential
PIN25	MGT_RX3_N	C9	Differential	PIN26	MGT_TX0_N	A4	Differential
PIN27	GND	-	Ground	PIN28	GND	-	Ground
PIN29	MGT_TX1_P	D5	Differential	PIN30	MGT_RX0_P	B8	Differential
PIN31	MGT_TX1_N	C5	Differential	PIN32	MGT_RX0_N	A8	Differential
PIN33	GND	-	Ground	PIN34	GND	-	Ground
PIN35	MGT_RX1_P	D11	Differential	PIN36	MGT_CLK1_P	F10	Differential
PIN37	MGT_RX1_N	C11	Differential	PIN38	MGT_CLK1_N	E10	Differential
PIN39	GND	-	Ground	PIN40	GND	-	Ground
PIN41	B16_L5_P	E16	3.3V	PIN42	B16_L2_P	F16	3.3V
PIN43	B16_L5_N	D16	3.3V	PIN44	B16_L2_N	E17	3.3V
PIN45	B16_L7_P	B15	3.3V	PIN46	B16_L3_P	C14	3.3V
PIN47	B16_L7_N	B16	3.3V	PIN48	B16_L3_N	C15	3.3V
PIN49	GND	-	Ground	PIN50	GND	-	Ground
PIN51	B16_L9_P	A15	3.3V	PIN52	B16_L10_P	A13	3.3V
PIN53	B16_L9_N	A16	3.3V	PIN54	B16_L10_N	A14	3.3V
PIN55	B16_L11_P	B17	3.3V	PIN56	B16_L12_P	D17	3.3V
PIN57	B16_L11_N	B18	3.3V	PIN58	B16_L12_N	C17	3.3V
PIN59	GND	-	Ground	PIN60	GND	-	Ground
PIN61	B16_L13_P	C18	3.3V	PIN62	B16_L14_P	E19	3.3V
PIN63	B16_L13_N	C19	3.3V	PIN64	B16_L14_N	D19	3.3V
PIN65	B16_L15_P	F18	3.3V	PIN66	B16_L16_P	B20	3.3V
PIN67	B16_L15_N	E18	3.3V	PIN68	B16_L16_N	A20	3.3V
PIN69	GND	-	Ground	PIN70	GND	-	Ground
PIN71	B16_L17_P	A18	3.3V	PIN72	B16_L18_P	F19	3.3V
PIN73	B16_L17_N	A19	3.3V	PIN74	B16_L18_N	F20	3.3V
PIN75	B16_L19_P	D20	3.3V	PIN76	B16_L20_P	C22	3.3V
PIN77	B16_L19_N	C20	3.3V	PIN78	B16_L20_N	B22	3.3V

PIN79	NC	-		PIN80	NC	-	

Part 2.11: Power Supply

The AC7100B FPGA core board is powered by DC5V via carrier board, and it is powered by the J3 interface when it is used alone. Please be careful not to supply power to J3 interface and the carrier board at the same time to avoid damage. The power supply design diagram on the board is shown in Figure 2-11-1.

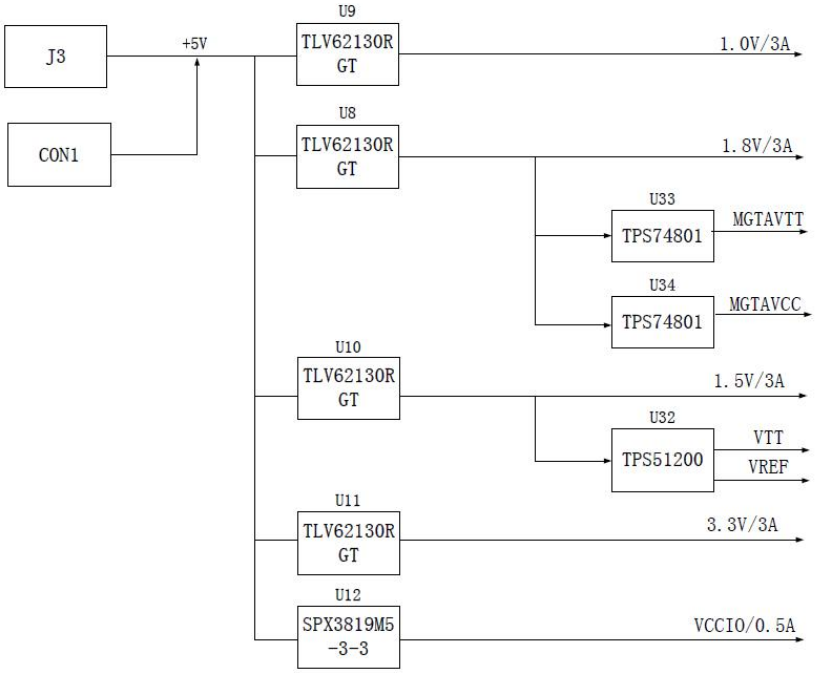


Figure 2-11-1：Power Supply on core board schematic

The development board is powered by +5V and converted to +3.3V, +1.5V, +1.8V, +1.0V four-way power supply through four DC/DC power supply chip TLV62130RGT. The output current can be up to 3A per channel. VCCIO is generated by one LDOSPX3819M5-3-3. VCCIO mainly supplies power to BANK15 and BANK16 of FPGA. Users can change the IO of BANK15,16 to different voltage standards by replacing their LDO chip. 1.5V Generates the VTT and VREF voltages required by DDR3 via TI's TPS51200. The 1.8V power supply MGTAVTT MGTAVCC for the GTP transceiver is generated by TI's TPS74801 chip. The functions of each power distribution are shown in the

following table:

Power Supply	Function
+1.0V	FPGA Core Voltage
+1.8V	FPGA auxiliary voltage, TPS74801 power supply
+3.3V	VCCIO of Bank0,Bank13 and Bank14 of FPGA,QSIP FLASH, Clock Crystal
+1.5V	DDR3, Bank34 and Bank35 of FPGA
VREF,VTT(+0.75V)	DDR3
MVCCIP(+3.3V)	FPGA Bank15, Bank16
MGTAVTT(+1.2V)	GTP Transceiver Bank216 of FPGA
MGTVCCAUX(+1.8V)	GTP Transceiver Bank216 of FPGA

Because the power supply of Artix-7 FPGA has the power-on sequence requirement, in the circuit design, we have designed according to the power requirements of the chip, and the power-on is 1.0V->1.8V->(1.5 V, 3.3V, VCCIO) and 1.0V-> MGTAVCC -> MGTAVTT, the circuit design to ensure the normal operation of the chip.

The power circuit on the AC7100B FPGA core board is shown in Figure 2-11-2:

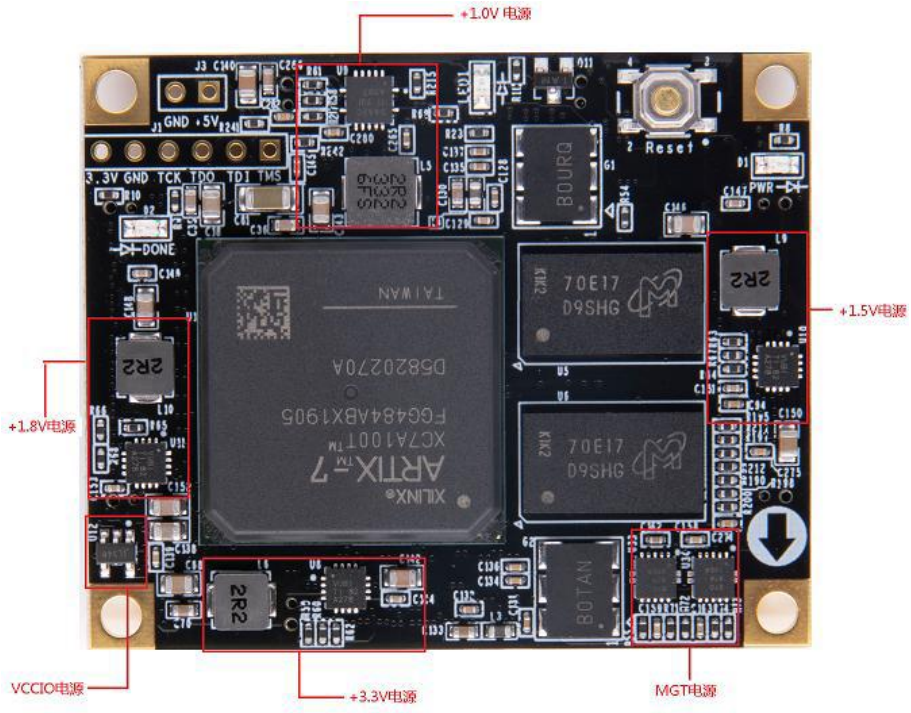


Figure 2-11-2: Power Supply on the AC7100B FPGA Core Board

Part 2.12: Structure Diagram

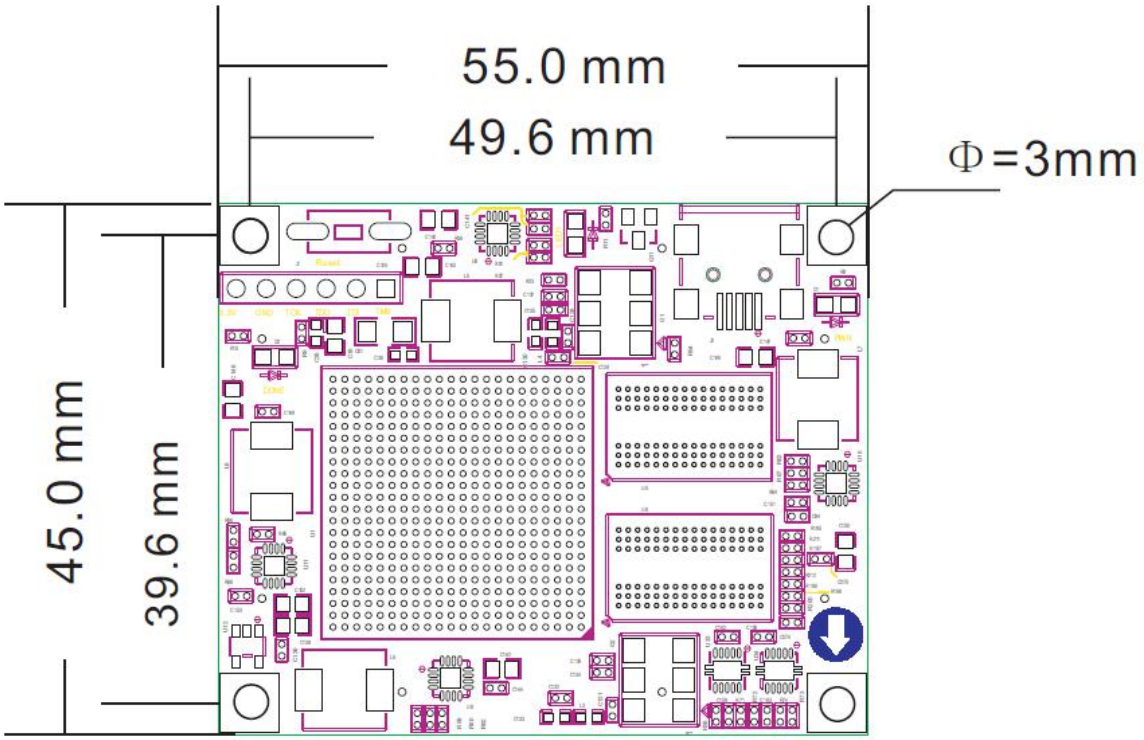


Figure 2-12-1: AC7100B FPGA Core board (Top view)

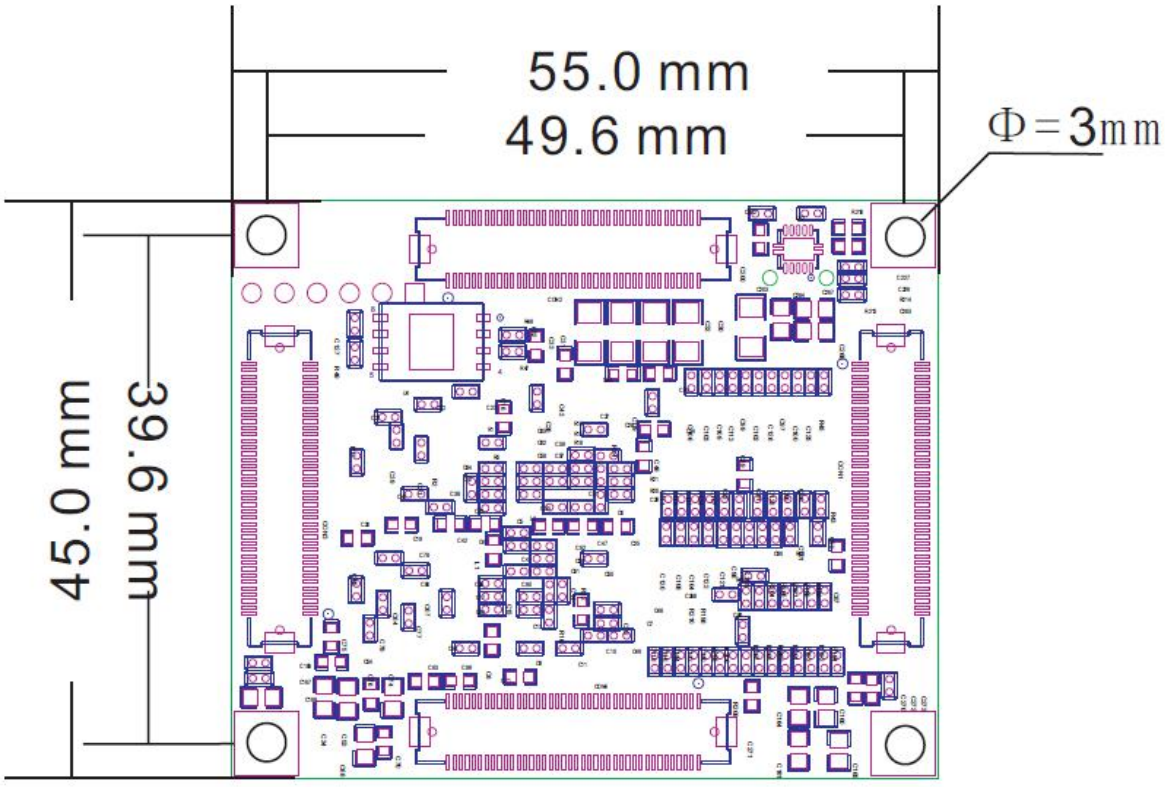
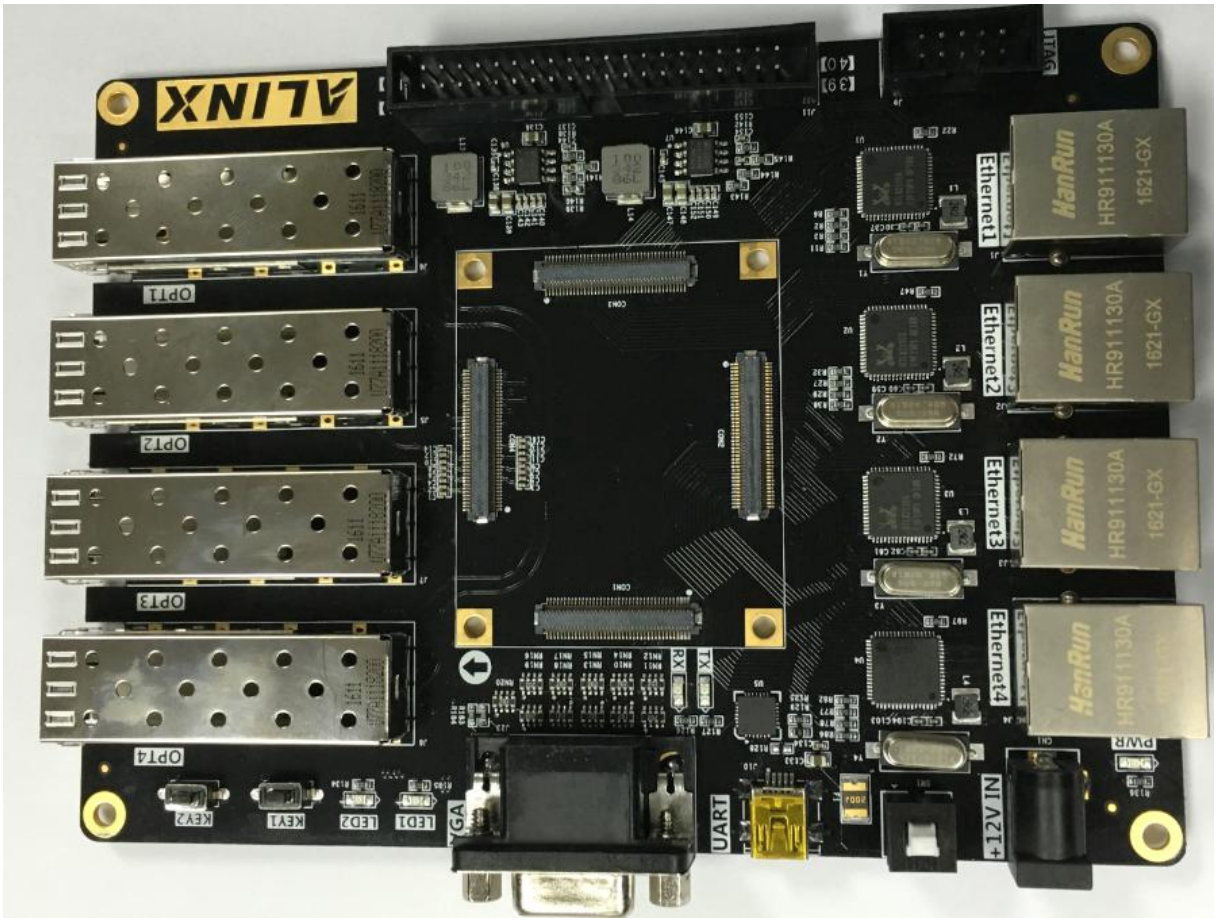


Figure 2-12-2: AC7100B FPGA Core board (Bottom view)

Part 3: Carrier Board



Part 3.1: Carrier Board Introduction

Through the previous function introduction, you can understand the function of the carrier board part

- 4-channel 10/100M/1000M Ethernet RJ-45 interface
- 4-channel SFP interface
- 1-channel 16-bit VGA output interface
- 1-channel USB Uart debug interface
- 40-pin expansion ports
- JTAG debugging interface
- 2 independent Keys
- 2 user LED lights

Part 3.2: Gigabit Ethernet Interface

The AX7101 FPGA carrier board provides users with 4-channel Gigabit network communication service through the Realtek RTL8211EG Ethernet PHY chip. The RTL8211EG chip supports 10/100/1000 Mbps network transmission rate and communicates with the FPGA through the GMII interface. RTL8211EG supports MDI/MDX adaptive, various speed adaptations, Master/Slave adaptation, and support for MDIO bus for PHY register management.

The RTL8211EG will detect the level status of some specific IOs to determine their working mode after powered on. Table 3-1-1 describes the default setup information after the GPHY chip is powered on.

Configuration Pin	Instructions	Configuration value
PHYAD[2:0]	MDIO/MDC Mode PHY Address	PHY Address 011
SELRGV	3.3V, 2.5V, 1.5/1.8V voltage selection	3.3V
AN[1:0]	Auto-negotiation configuration	(10/100/1000M) adaptive
RX Delay	RX clock 2ns delay	Delay
TX Delay	TX clock 2ns delay	Delay
Mode	RGMII or GMII selection	GMII

Table 3-2-1: PHY chip default configuration value

When the network is connected to Gigabit Ethernet, the data transmission of FPGA and PHY chip RTL8211EG is communicated through the GMII bus, the transmission clock is 125Mhz. The receive clock E_RXC is provided by the PHY chip, the transmit clock E_GTXC is provided by the FPGA, and the data is sampled on the rising edge of the clock.

When the network is connected to 100M Ethernet, the data transmission of FPGA and PHY chip RTL8211EG is communicated through the GMII bus, the transmission clock is 25Mhz. The receive clock E_RXC is provided by the PHY chip, the transmit clock E_GTXC is provided by the FPGA, and the data is

sampled on the rising edge of the clock.

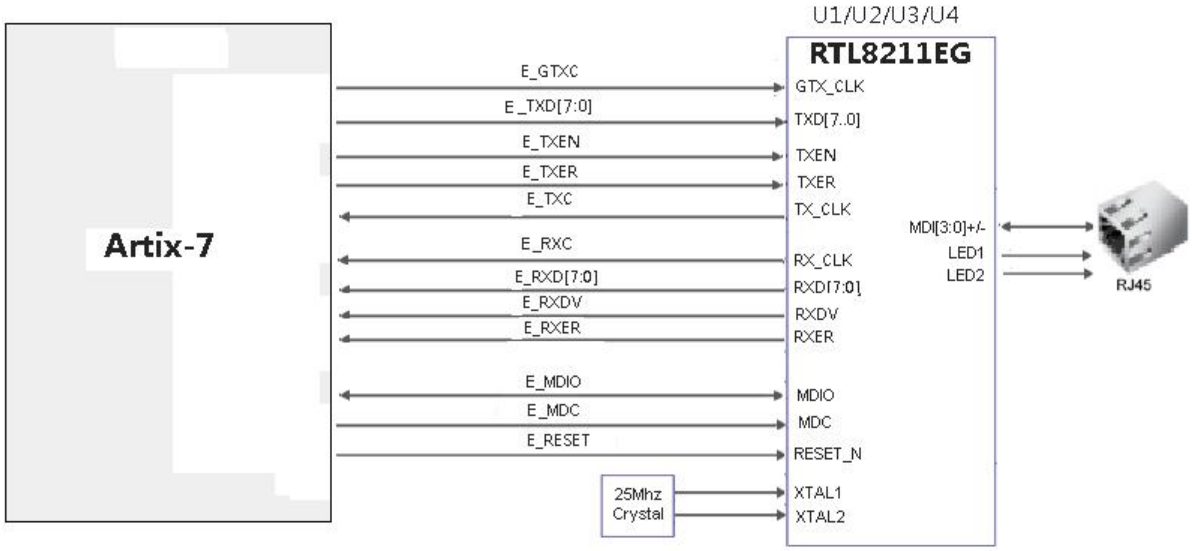


Figure 3-2-1: Gigabit Ethernet Interface Schematic

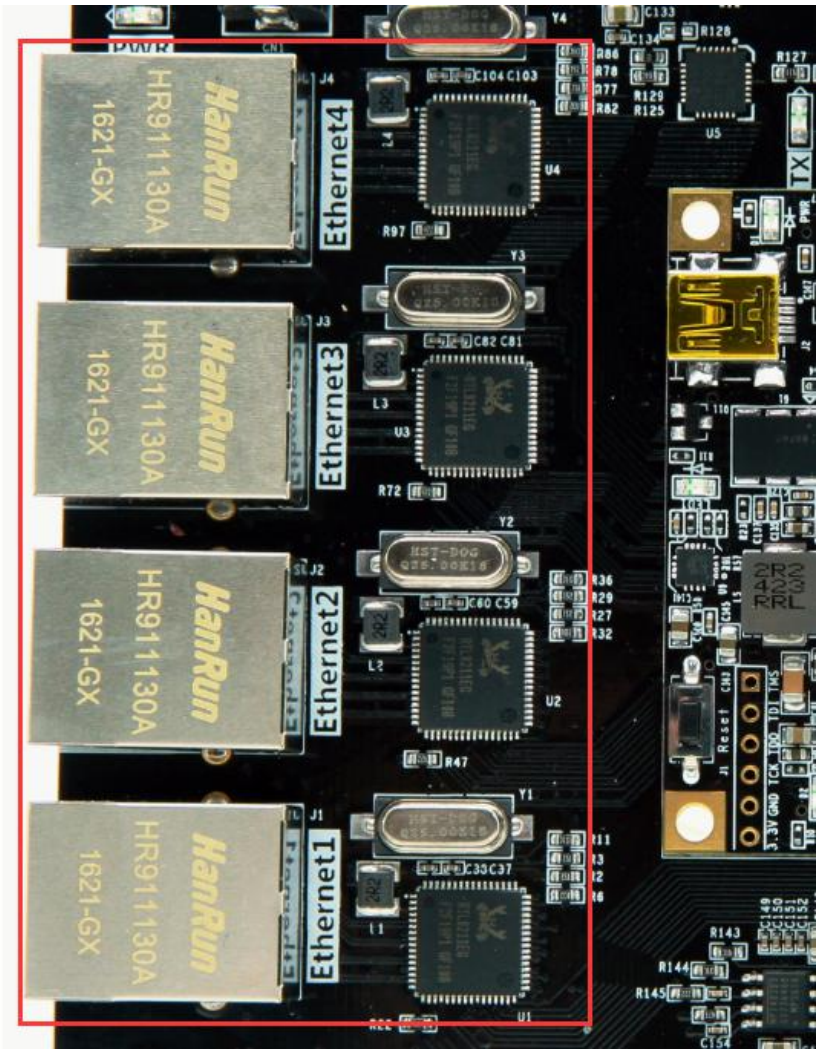


Figure 3-3-2: Gigabit Ethernet interface on the Carrier Board

The 1st channel Gigabit Ethernet pin assignments are as follows:

Signal Name	FPGA Pin	Description
E1_GTXC	G21	Ethernet GMII transmit clock
E1_TXD0	D22	Ethernet Transmit Data bit0
E1_TXD1	H20	Ethernet Transmit Data bit1
E1_TXD2	H22	Ethernet Transmit Data bit2
E1_TXD3	J22	Ethernet Transmit Data bit3
E1_TXD4	K22	Ethernet Transmit Data bit4
E1_TXD5	L19	Ethernet Transmit Data bit5
E1_TXD6	K19	Ethernet Transmit Data bit6
E1_TXD7	L20	Ethernet Transmit Data bit7
E1_TXEN	G22	Ethernet transmit enable signal
E1_TXER	K17	Ethernet transmit error signal
E1_TXC	K21	Ethernet GMII transmit clock
E1_RXC	K18	Ethernet GMII receive clock
E1_RXDV	M22	Ethernet receive data valid signal
E1_RXER	N18	Ethernet receiving data error
E1_RXD0	N22	Ethernet Receive Data Bit0
E1_RXD1	H18	Ethernet Receive Data Bit1
E1_RXD2	H17	Ethernet Receive Data Bit2
E1_RXD3	M21	Ethernet Receive Data Bit3
E1_RXD4	L21	Ethernet Receive Data Bit4
E1_RXD5	N20	Ethernet Receive Data Bit5
E1_RXD6	M20	Ethernet Receive Data Bit6
E1_RXD7	N19	Ethernet Receive Data Bit7
E1_COL	M18	Ethernet Collision signal
E1_CRS	L18	Ethernet Carrier Sense Signal
E1_RESET	G20	Ethernet Reset Signal
E1_MDC	J17	Ethernet Management Clock
E1_MDIO	L16	Ethernet Management Data

The 2nd channel Gigabit Ethernet pin assignments are as follows：

Signal Name	FPGA Pin	Description
E2_GTXC	M16	Ethernet GMII transmit clock
E2_TXD0	L15	Ethernet Transmit Data bit0
E2_TXD1	K16	Ethernet Transmit Data bit1
E2_TXD2	W15	Ethernet Transmit Data bit2
E2_TXD3	W16	Ethernet Transmit Data bit3
E2_TXD4	V17	Ethernet Transmit Data bit4
E2_TXD5	W17	Ethernet Transmit Data bit5
E2_TXD6	U15	Ethernet Transmit Data bit6
E2_TXD7	V15	Ethernet Transmit Data bit7
E2_TXEN	M15	Ethernet transmit enable signal
E2_TXER	T15	Ethernet sends an error signal
E2_TXC	T14	Ethernet GMII transmit clock
E2_RXC	J20	Ethernet GMII receive clock
E2_RXDV	L13	Ethernet receive data valid signal
E2_RXER	G13	Ethernet receiving data error
E2_RXD0	M13	Ethernet Receive Data Bit0
E2_RXD1	K14	Ethernet Receive Data Bit1
E2_RXD2	K13	Ethernet Receive Data Bit2
E2_RXD3	J14	Ethernet Receive Data Bit3
E2_RXD4	H14	Ethernet Receive Data Bit4
E2_RXD5	H15	Ethernet Receive Data Bit5
E2_RXD6	J15	Ethernet Receive Data Bit6
E2_RXD7	H13	Ethernet Receive Data Bit7
E2_COL	J11	Ethernet Collision signal
E2_CRS	E22	Ethernet Carrier Sense Signal
E2_RESET	L14	Ethernet Reset Signal
E2_MDC	AB21	Ethernet Management Clock
E2_MDIO	AB22	Ethernet Management Data

The 3rd channel Gigabit Ethernet pin assignments are as follows：

Signal Name	FPGA Pin	Description
E3_GTXC	AA21	Ethernet GMII transmit clock
E3_TXD0	W11	Ethernet Transmit Data bit0
E3_TXD1	W12	Ethernet Transmit Data bit1
E3_TXD2	Y11	Ethernet Transmit Data bit2
E3_TXD3	Y12	Ethernet Transmit Data bit3
E3_TXD4	W10	Ethernet Transmit Data bit4
E3_TXD5	AA11	Ethernet Transmit Data bit5
E3_TXD6	AA10	Ethernet Transmit Data bit6
E3_TXD7	AB10	Ethernet Transmit Data bit7
E3_TXEN	V14	Ethernet transmit enable signal
E3_TXER	AA9	Ethernet sends an error signal
E3_TXC	V10	Ethernet GMII transmit clock
E3_RXC	V13	Ethernet GMII receive clock
E3_RXDV	AA20	Ethernet receive data valid signal
E3_RXER	U21	Ethernet receiving data error
E3_RXD0	AB20	Ethernet Receive Data Bit0
E3_RXD1	AA19	Ethernet Receive Data Bit1
E3_RXD2	AA18	Ethernet Receive Data Bit2
E3_RXD3	AB18	Ethernet Receive Data Bit3
E3_RXD4	Y17	Ethernet Receive Data Bit4
E3_RXD5	W22	Ethernet Receive Data Bit5
E3_RXD6	W21	Ethernet Receive Data Bit6
E3_RXD7	T21	Ethernet Receive Data Bit7
E3_COL	Y21	Ethernet Collision signal
E3_CRS	Y22	Ethernet Carrier Sense Signal
E3_RESET	T20	Ethernet Reset Signal
E3_MDC	V20	Ethernet Management Clock
E3_MDIO	V19	Ethernet Management Data

The 4th channel Gigabit Ethernet pin assignments are as follows:

Signal Name	FPGA Pin	Description
E4_GTXC	P20	Ethernet GMII transmit clock
E4_TXD0	R17	Ethernet Transmit Data bit0
E4_TXD1	P15	Ethernet Transmit Data bit1
E4_TXD2	N17	Ethernet Transmit Data bit2
E4_TXD3	P17	Ethernet Transmit Data bit3
E4_TXD4	T16	Ethernet Transmit Data bit4
E4_TXD5	U17	Ethernet Transmit Data bit5
E4_TXD6	U18	Ethernet Transmit Data bit6
E4_TXD7	P19	Ethernet Transmit Data bit7
E4_TXEN	P16	Ethernet transmit enable signal
E4_TXER	R19	Ethernet sends an error signal
E4_TXC	U16	Ethernet GMII transmit clock
E4_RXC	Y18	Ethernet GMII receive clock
E4_RXDV	W20	Ethernet receive data valid signal
E4_RXER	N13	Ethernet receiving data error
E4_RXD0	W19	Ethernet Receive Data Bit0
E4_RXD1	Y19	Ethernet Receive Data Bit1
E4_RXD2	V22	Ethernet Receive Data Bit2
E4_RXD3	U22	Ethernet Receive Data Bit3
E4_RXD4	T18	Ethernet Receive Data Bit4
E4_RXD5	R18	Ethernet Receive Data Bit5
E4_RXD6	R14	Ethernet Receive Data Bit6
E4_RXD7	P14	Ethernet Receive Data Bit7
E4_COL	N14	Ethernet Collision signal
E4_CRS	N15	Ethernet Carrier Sense Signal
E4_RESET	R16	Ethernet Reset Signal
E4_MDC	V18	Ethernet Management Clock
E4_MDIO	U20	Ethernet Management Data

Part 3.3: SFP Interface

The AX7101 FPGA carrier board has four optical interfaces. Users can purchase SFP optical modules (1.25G, 2.5G optical modules on the market) and insert them into these four optical interfaces for optical data communication. The four fiber interfaces are connected to the two RX/TX of the GNK transceiver of the FPGA. The TX signal and the RX signal are connected to the FPGA and the optical module through the DC blocking capacitor in differential signal mode. The TX and RX data rates are up to each 6.6Gb/s per channel. The reference clock for the GTX transceiver is provided by the 125Mhz differential clock of AC7100B FPGA core board.

Figure 3-3-1 detailed the schematic diagram of FPGA and fiber design

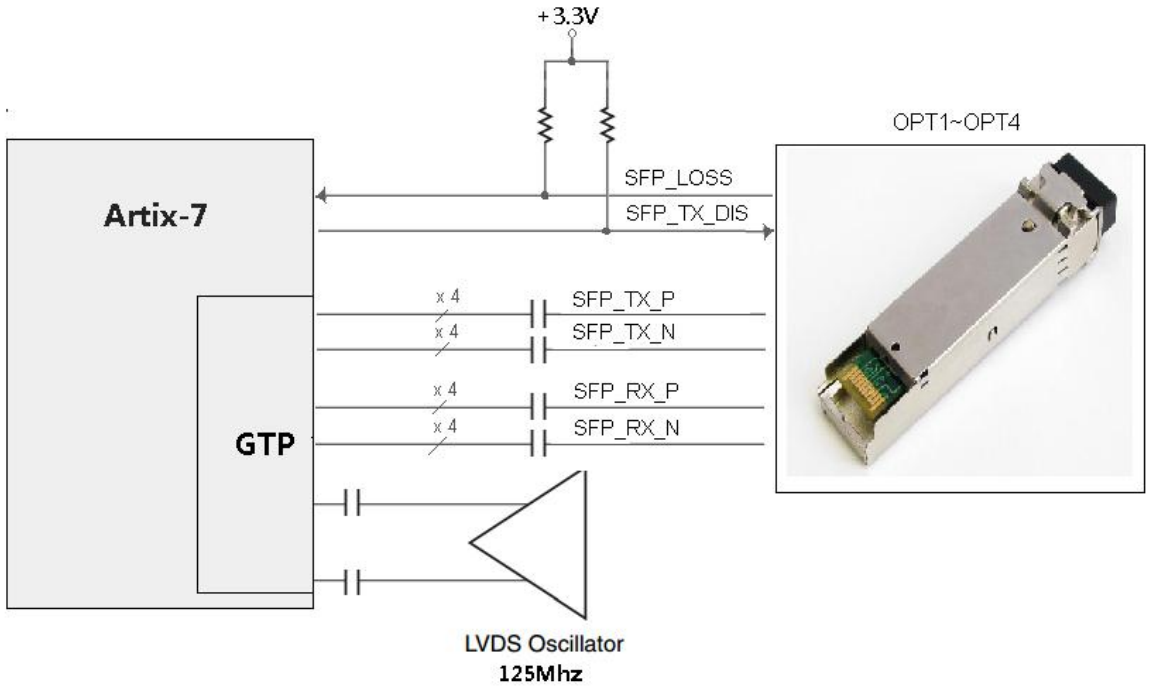


Figure 3-3-1: SFP Interface Schematic

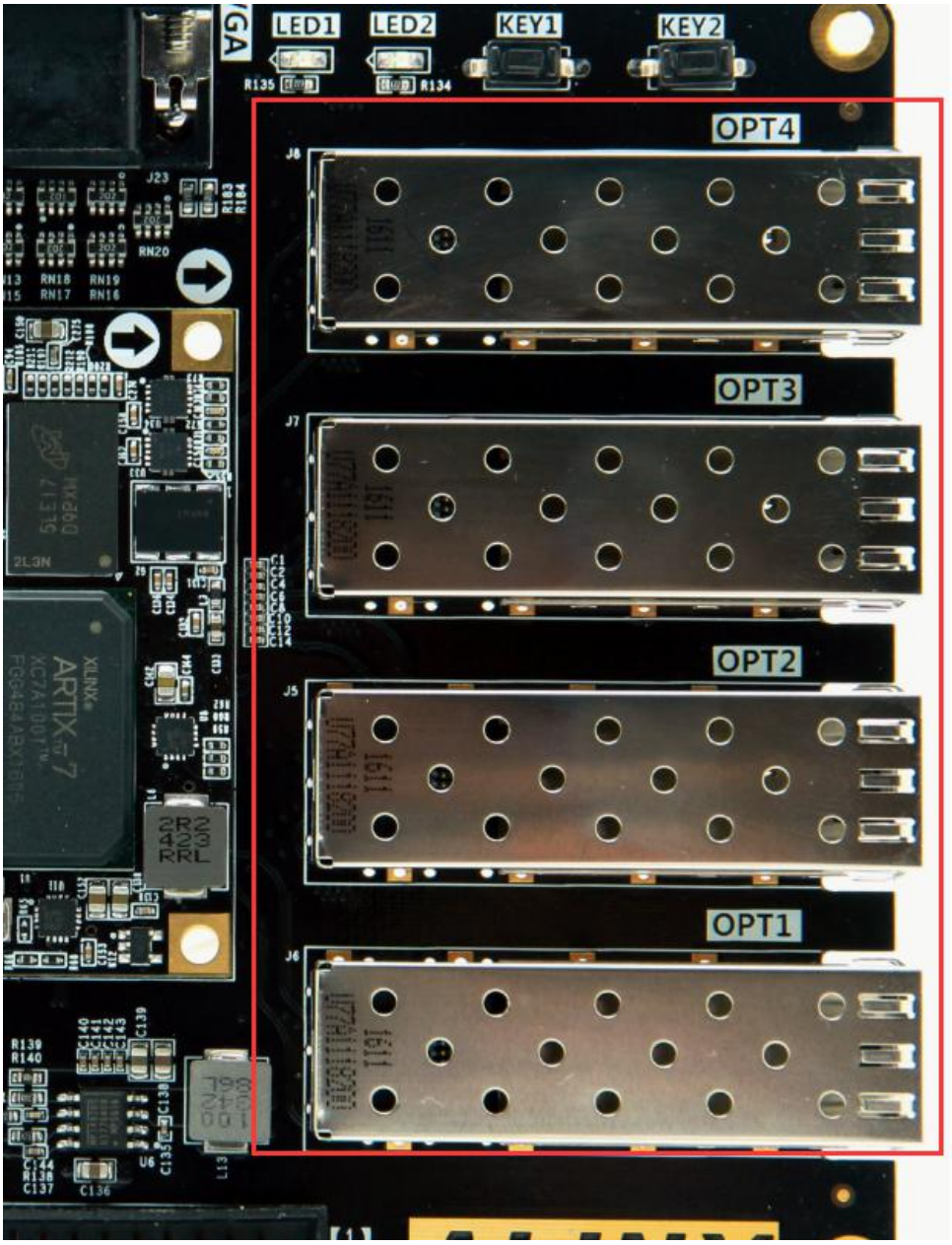


Figure 3-3-2: SFP interfaces on the Carrier Board

The 1st fiber interface FPGA pin assignment is as follows:

Signal Name	FPGA PIN	Description
SFP1_TX_P	B4	SFP1 Data Transfer (Positive)
SFP1_TX_N	A4	SFP1 Data Transfer (Negative)
SFP1_RX_P	B8	SFP1 Data Receiver (Positive)
SFP1_RX_P	A8	SFP1 Data Receiver (Negative)
SFP1_TX_DIS	A15	SFP1 Optical Transfer Disable, active high
SFP1_LOSS	B15	SFP1 Optical LOSS, High level means no light signal is received

The 2nd fiber interface FPGA pin assignment is as follows:

Signal Name	FPGA PIN	Description
SFP2_TX_P	D5	SFP2 Data Transfer (Positive)
SFP2_TX_N	C5	SFP2 Data Transfer (Negative)
SFP2_RX_P	D11	SFP2 Data Receiver (Positive)
SFP2_RX_P	C11	SFP2 Data Receiver (Negative)
SFP2_TX_DIS	A16	SFP2 Optical Transfer Disable, active high
SFP2_LOSS	B16	SFP2 Optical LOSS, High level means no light signal is received

The 3rd fiber interface FPGA pin assignment is as follows:

Signal Name	FPGA PIN	Description
SFP3_TX_P	B6	SFP3 Data Transfer (Positive)
SFP3_TX_N	A6	SFP3 Data Transfer (Negative)
SFP3_RX_P	B10	SFP3 Data Receiver (Positive)
SFP3_RX_P	A10	SFP3 Data Receiver (Negative)
SFP3_TX_DIS	A13	SFP3 Optical Transfer Disable, active high
SFP3_LOSS	C14	SFP3 Optical LOSS, High level means no light signal is received

The 4th fiber interface FPGA pin assignment is as follows:

Signal Name	FPGA PIN	Description
SFP4_TX_P	D7	SFP4 Data Transfer (Positive)
SFP4_TX_N	C7	SFP4 Data Transfer (Negative)
SFP4_RX_P	D9	SFP4 Data Receiver (Positive)
SFP4_RX_P	C9	SFP4 Data Receiver (Negative)
SFP4_TX_DIS	A14	SFP4 Optical Transfer Disable, active high
SFP4_LOSS	C15	SFP4 Optical LOSS, High level means no light signal is received

Part 3.4: VGA display interface

The VGA interface is the most important interface on a computer monitor, also known as the D-Sub interface. The VGA interface is a D-type interface with a total of 15 pinholes, divided into three rows, five in each row. More important are three RGB color component signals and two scan sync signals HSYNC and

VSYNC pins. Pins 1, 2, and 3 are red, green, and blue primary color analog voltages, which are 0 to 0.714V peak-peak, 0V is colorless, and 0.714V is full color. Some non-standard displays use a full color level of 1Vpp. The three primary color source terminals and terminal matching resistors are both 75 ohms. Detail as Figure 3-4-1:

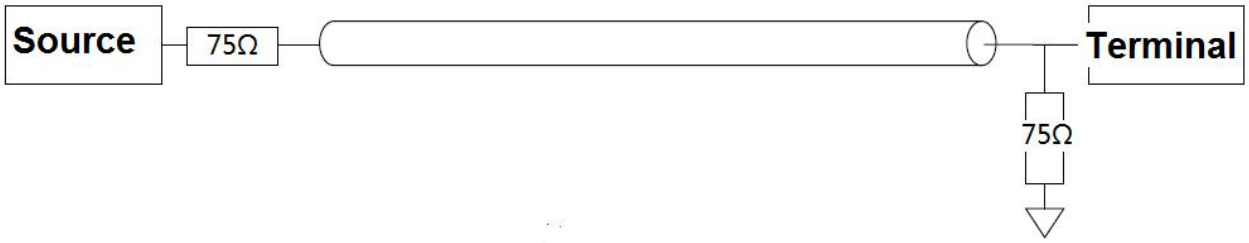


Figure 3-4-1: VGA Video Signal Transmission Diagram

HSYNC and VSYNC are line data synchronization and frame data synchronization, respectively, which are TTL levels. The FPGA can only output digital signals, while the R, G, and B required by the VGA are analog signals. The digital to analog signal of the VGA is realized by a simple resistor circuit. This resistor circuit can generate 32 gradient grade red and blue signals and 64 gradient grade green signals (RGB 5-6-5). The VGA interface part of the circuit is shown in Figure 3-4-2.

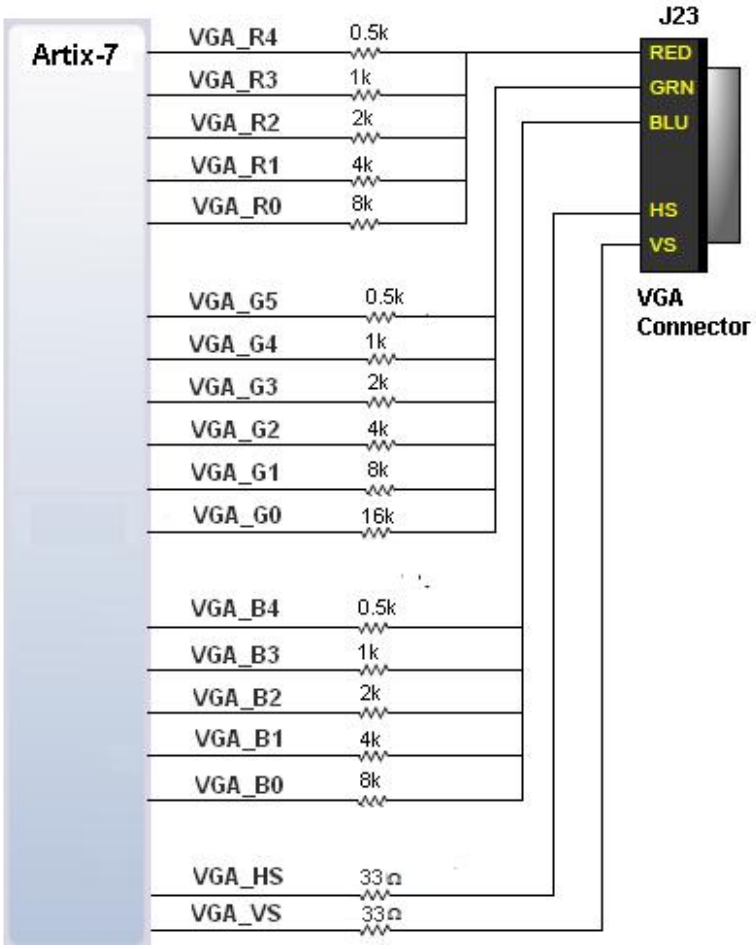


Figure 3-4-2: VGA Display Interface Schematic

Figure 3-4-3: VGA Display Interface on the Carrier Board

VGA Pin Assignment:

Signal Name	FPGA Pin	Description
VGA_B[0]	D14	BLUE[0]
VGA_B[1]	E14	BLUE[1]
VGA_B[2]	E13	BLUE[2]
VGA_B[3]	F13	BLUE[3]

VGA_B[4]	F14	BLUE[4]
VGA_G[0]	D15	GREEN[0]
VGA_G[1]	AB13	GREEN[1]
VGA_G[2]	W14	GREEN[2]
VGA_G[3]	AA14	GREEN[3]
VGA_G[4]	AA13	GREEN[4]
VGA_G[5]	AB12	GREEN[5]
VGA_R[0]	AB16	RED[0]
VGA_R[1]	Y16	RED[1]
VGA_R[2]	AA16	RED[2]
VGA_R[3]	Y13	RED[3]
VGA_R[4]	AB17	RED[4]
VGA_HS	C13	Horizontal sync signal
VGA_VS	B13	Vertical sync signal

Part 3.5: USB to Serial Port

The AX7101 FPGA carrier board includes the USB-UAR chip of Silicon Labs CP2102GM. The USB interface uses the MINI USB interface. It can be connected to the USB port of the upper PC for serial data communication with a USB cable. The schematic diagram of the USB Uart circuit design is shown in Figure 3-5-1:

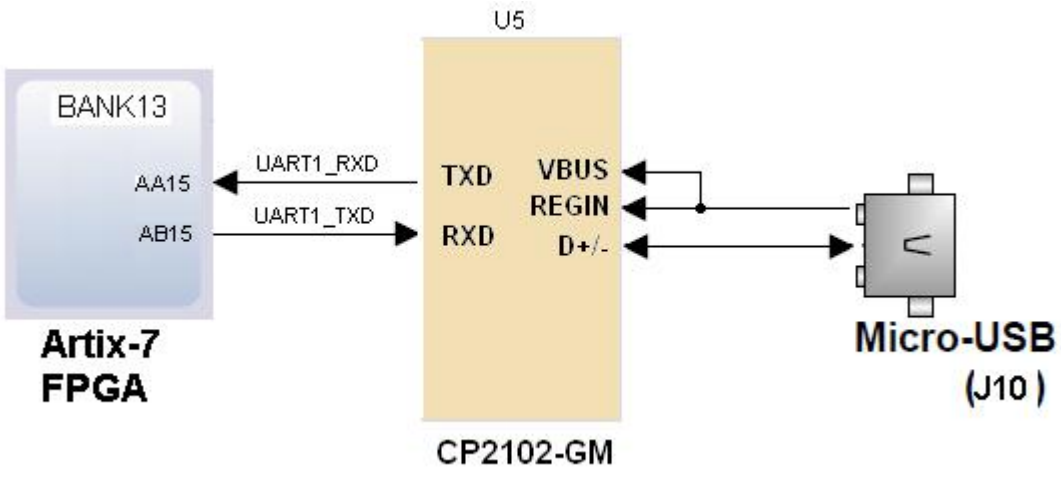


Figure 3-5-1: USB to serial port schematic

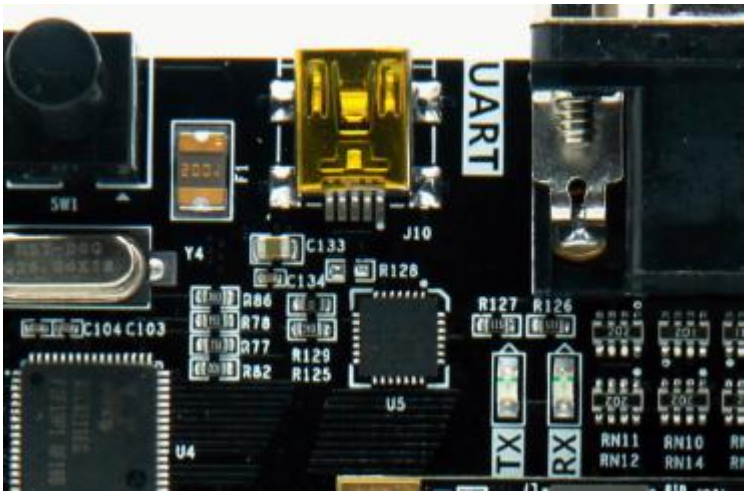


Figure 3-5-2: USB to serial port on the Carrier Board

Two LED indicators (LED4 and LED3) are set for the serial port signal, and the silkscreen on the PCB is TX and RX, indicating that the serial port has data transmission or reception, as shown in the following Figure 3-5-3

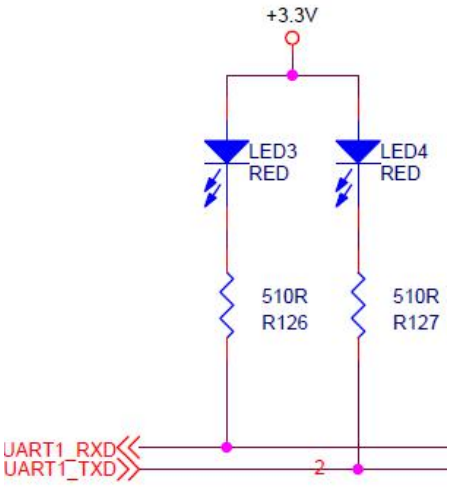


Figure 3-5-3: Serial Port communication LED Indicators Schematic

USB to serial port pin assignment:

Signal Name	FPGA PIN
UART_RXD	AA15
UART_TXD	AB15

Part 3.6: Expansion Header

The AX7101 FPGA carrier board is reserved with one 0.1inch spacing standard 40-pin expansion header J11 which is used to connect the ALINX modules or the external circuit designed by the user. The expansion port has 40 signals, of which 1-channel 5V power supply, 2-channel 3.3 V power supply, 3-channle ground and 34 IOs. **Do not directly connect the IO directly to the 5V device to avoid burning the FPGA. If you want to connect 5V equipment, you need to connect level conversion chip.**

A 33 ohm resistor is connected in series between the expansion port and the FPGA connection to protect the FPGA from external voltage or current. The circuit of the expansion port (J11) is shown in Figure 3-6-1.

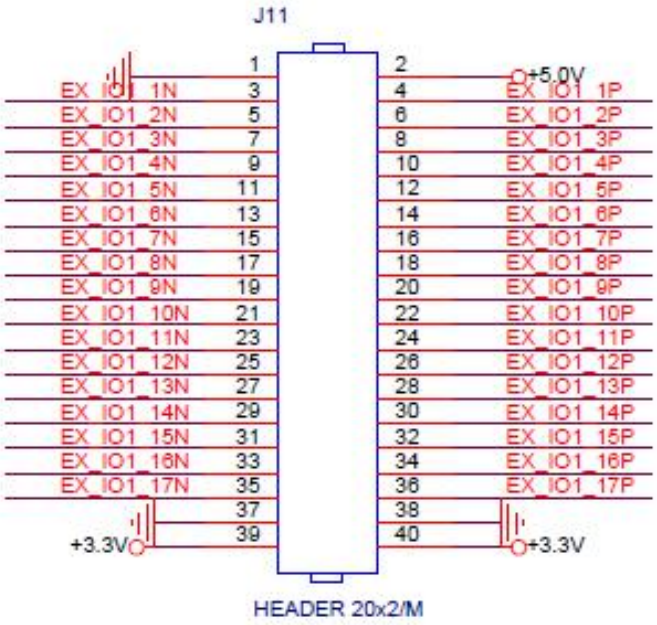


Figure 3-6-1: Expansion header J11 schematic

Figure 3-6-2: Expansion header J11 on the Carrier Board

J11 Expansion Header Pin Assignment

J11 Pin Number	FPGA Pin	J11 Pin Number	FPGA Pin
1	GND	**2**	+5V
3	B22	**4**	C22
5	A20	**6**	B20
7	F20	**8**	F19
9	J16	**10**	F15
11	F21	**12**	M17
13	A21	**14**	B21
15	D21	**16**	E21
17	G18	**18**	G17
19	H19	**20**	J19
21	G16	**22**	G15
23	D19	**24**	E19
25	C20	**26**	D20
27	A19	**28**	A18
29	E18	**30**	F18
31	C19	**32**	C18
33	B18	**34**	B17
35	C17	**36**	D17
37	GND	**38**	GND
39	+3.3V	**40**	+3.3V

Part 3.7: JTAG Interface

A JTAG interface is reserved on the AX7101 FPGA carrier board for downloading FPGA programs or firmware to FLASH. In order to prevent damage to the FPGA chip caused by hot plugging, a protection diode is added to the JTAG signal to ensure that the voltage of the signal is within the range accepted by the FPGA to avoid damage of the FPGA chip.

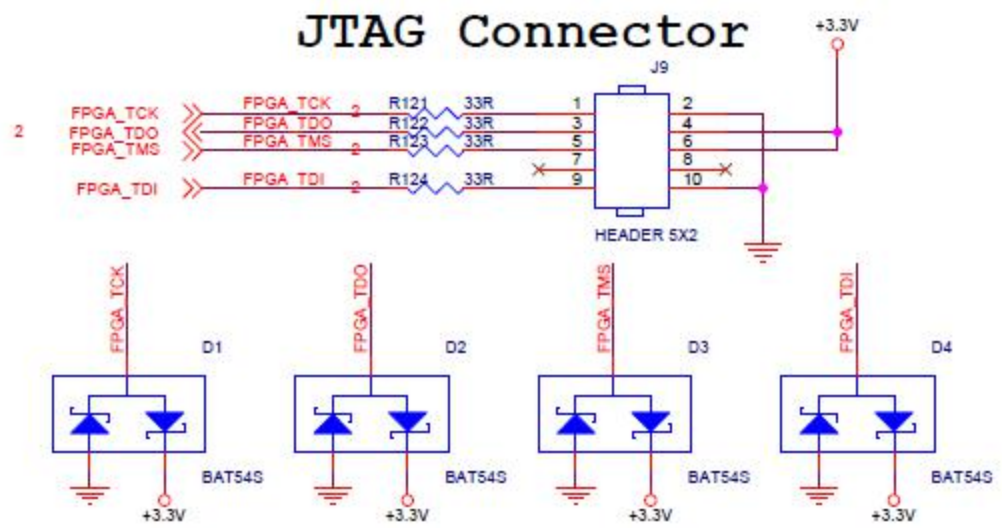


Figure 3-7-1: JTAG Interface Schematic

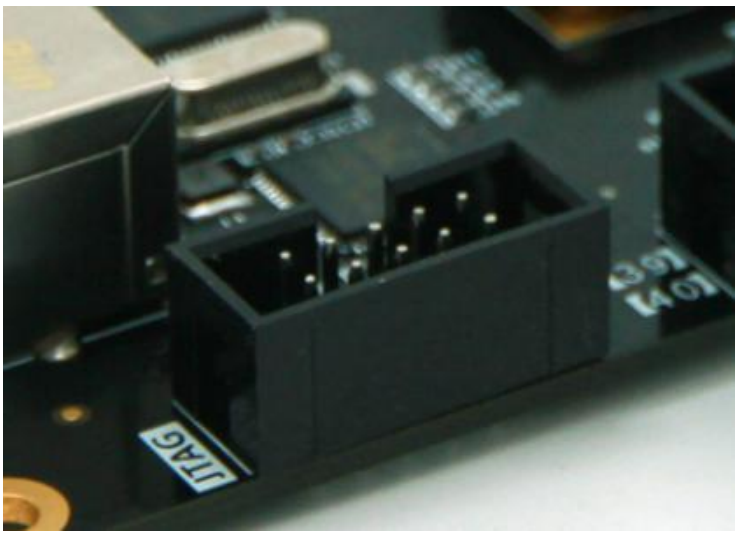


Figure 3-7-2: JTAG Interface on the Carrier Board

Be careful not to hot swap when JTAG cable is plugged and unplugged.

Part 3.8: Keys

The AX7101 FPGA carrier board contains two user Keys KEY1~KEY2. All Keys are connected to the normal IO of the FPGA. The Key is active low. When the Key is pressed, the IO input voltage of the FPGA is low. When no Key is pressed, The IO input voltage of the FPGA is high. The circuit of the Key part is shown in Figure 3-8-1.

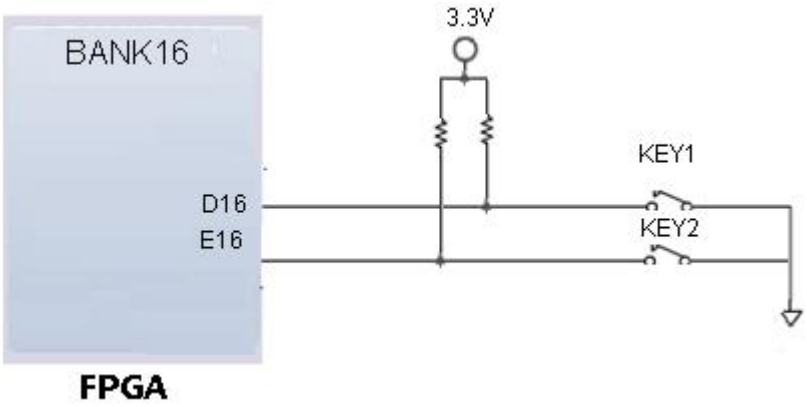


Figure 3-8-1: Key Schematic

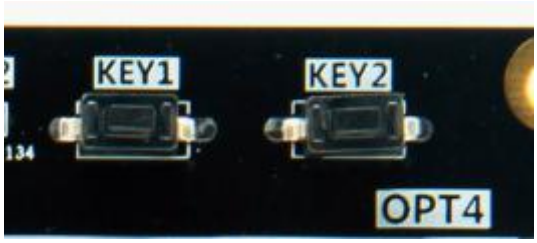


Figure 3-8-2: Four Keys on the carrier board

Keys Pin Assignment

Net Name	FPGA PIN
KEY1	D16
KEY2	E16

Part 3.9: LED Light

There are three red LEDs on the AX7101 FPGA Carrier Board, one of which is the power indicator (PWR), two are users LED lights (LED1~LED2). When the board is powered on, the power indicator will light up; User LED1~LED2 are connected to the normal IO of the FPGA. When the IO voltage connected to the user LED is configured low level, the user LED lights up. When the connected IO voltage is configured as high level, the user LED will be extinguished. The schematic diagram of the user LEDs hardware connection is shown in Figure 3-9-1.

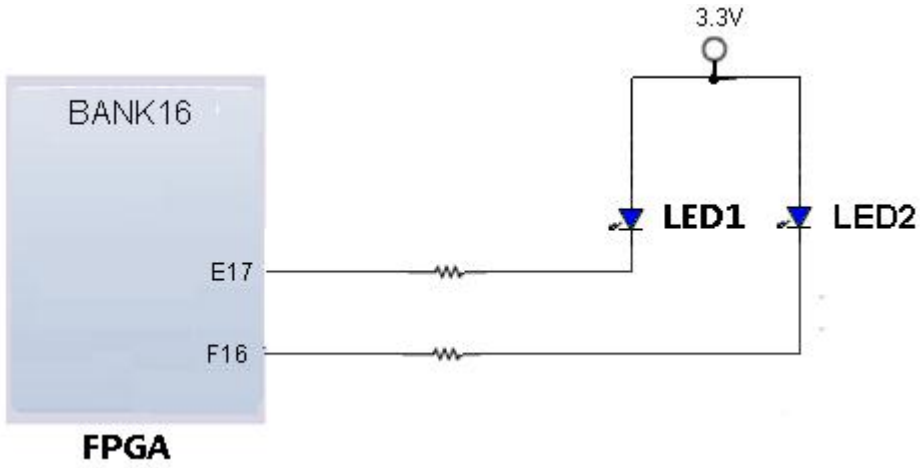


Figure 3-9-1: The User LEDs Schematic

Figure 3-9-2: The User LEDs on the Carrier Board

Pin assignment of user LED lights

Signal Name	FPGA PIN
KEY1	E17
KEY2	F16

Part 3.10: Power Supply

The power input voltage of the The AX7101 FPGA carrier board is DC12V. The Carrier Board is converted into +5V and +3.3V two-way power supply through two DC/DC power chip MP1482. In addition, the +5V power supply on the Carrier Board supplies power to the core board through the inter-board connector. The power supply design on the expansion is shown in Figure 3-10-1.

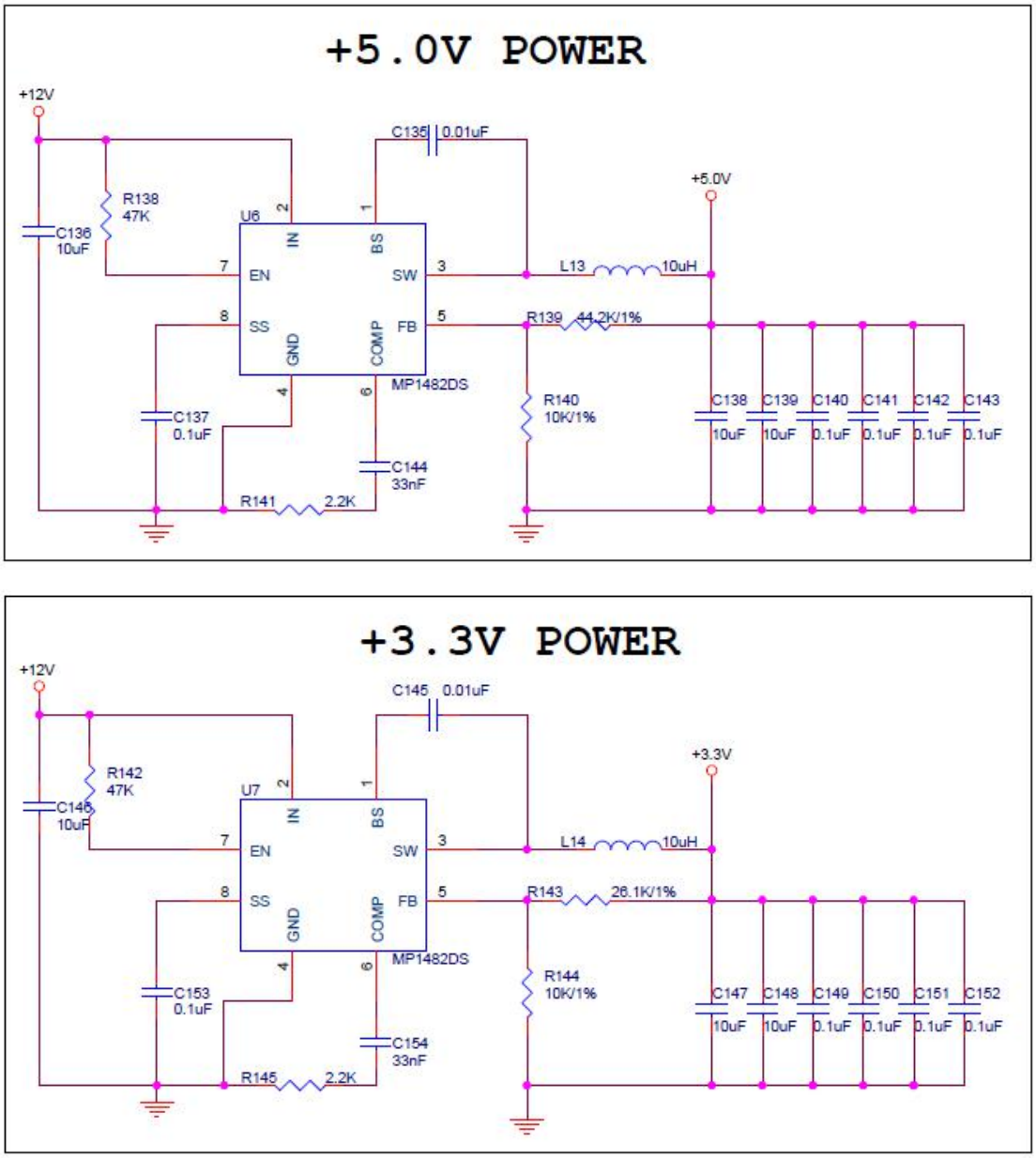


Figure 3-10-1 Power Design Schematic on the Carrier Board

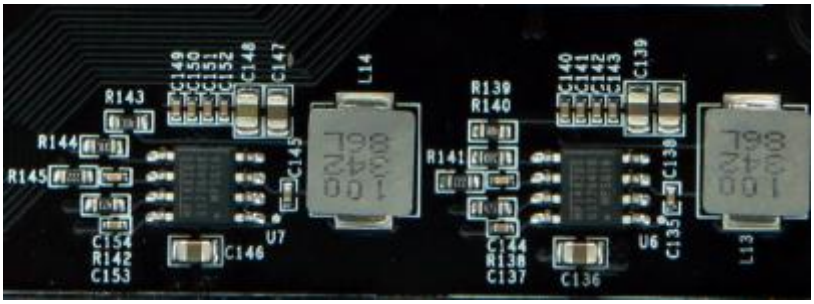


Figure 3-10-2: Power circuit on the Carrier Board