Xilinx ZYNQ7000 Development Platform User Manual

AX7450B

Development Board

ALINX ELECTRONIC LIMITED

WWW.EN.ALINX.COM

Version Record

Version	Date	Release By	Description
Rev 1.0	2024/4/3	Kathy Xia	First Release

Table of Contents

The development board (model: AX7450B) 2020 based on the XILINX ZYNQ7000 development platform of Alinx Electronic Technology has been officially released. In order to let you quickly understand this development platform, we have compiled this user manual.

This ZYNQ7000 FPGA development platform uses XILINX's Zynq7000 SOC chip XC7Z100 solution, which uses ARM + FPGA SOC technology to integrate dual-core ARM Cortex-A9 and FPGA programmable logic on a single chip. ZYNQ has two 512MB high-speed DDR3 SDRAM chips mounted on the PS side and four 512MB high-speed DDR3 SDRAM chips mounted on the PL side. In addition, there are one 8GB eMMC memory chip and two 256Mb QSPI FLASH chips on the PS side.

In terms of peripheral circuits, we have expanded a wealth of interfaces for users, such as a PCIex8 interface, a Gigabit Ethernet interface, a USB2.0 OTG interface, an HDMI output interface, a UART serial interface, an SD card interface, one FMC HPC expansion interface and two SMA interfaces. It is a "professional" ZYNQ development platform to meet the requirements of users for various high-speed data exchange, data storage, video transmission processing and industrial control. It is possible for high-speed data transmission and exchange, early verification, and later application of data processing. It is believed that such a product is very suitable for students, engineers and other groups engaged in ZYNQ development.

Figure 1: AX7450B development board

Part 1: Development Board Introduction

Here is a brief introduction to the functions of this AX7450B ZYNQ development platform.

The development board is mainly composed of ZYNQ7100 main chip, 6 DDR3, 1 eMMC, 2 QSPI FLASH and some peripheral interfaces. ZYNQ7100 adopts the Zynq7000 series chip of Xilinx Company, and the model is XC7Z100-2FFG900. ZYNQ710 chip can be divided into Processor System (PS) and Programmable Logic (PL). Two DDR3s are hung on the PS end of the ZYNQ7100 chip, and four DDR3s are hung on the PL end. The capacity of each DDR3 is up to 512M bytes, so that the ARM system and the FPGA system can independently process and store data. The 8GB eMMC FLASH memory chip and two 256Mb QSPI FLASHs on the PS side are used to statically store ZYNQ's operating system, file system and user data.

The AX7450B development board expands a wealth of peripheral interfaces, including a PCIex8 interface, a Gigabit Ethernet interface, a USB2.0 OTG interface, a UART serial interface, an SD card interface, an FMC HPC expansion interface, two SMA interfaces, some keys, and LEDs.

The following figure shows the structure of the entire development system:

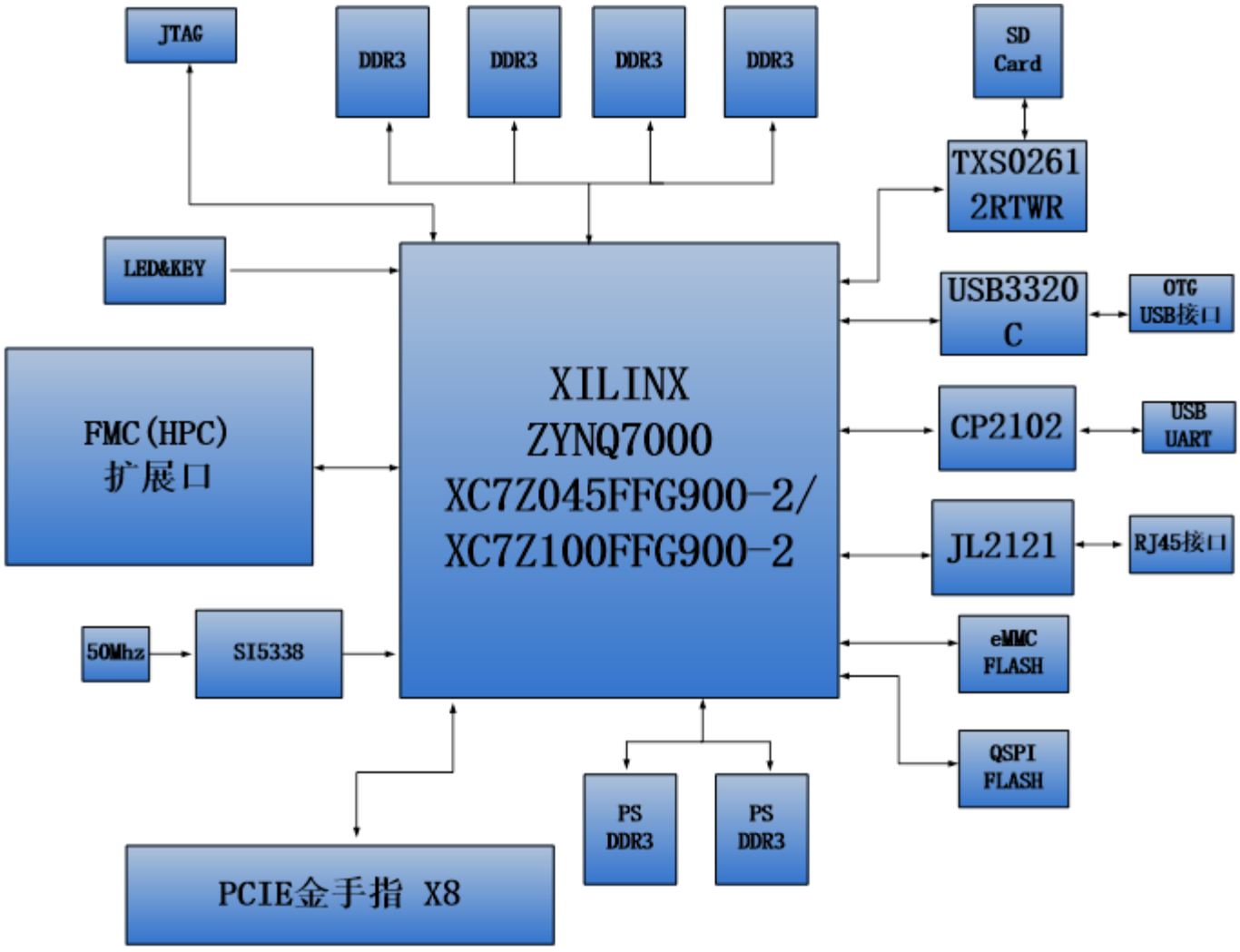


Figure 2: Structure of AX7450B

Through this diagram, we can see the interfaces and functions that our development platform can contain.

- **Xilinx ARM + FPGA chip Zynq-7000 XC7Z100-2FFG900.**

- **DDR3**

With 6 large 512MB (3GB) high speed DDR3 SDRAM. Two of them are mounted on the PS side to form a 32-bit data width, which can be used as the cache of ZYNQ chip data and the memory of the operating system. The other four chips are hung on the PL side to form a 64-bit data width, which can be used as data storage, image analysis cache and data processing of FPGA.

- **eMMC**

An 8GB eMMC FLASH memory chip is mounted on the PS side, and the user stores operating system files or other user data.

- **QSPI FLASH**

Two 256Mbit QSPI FLASH memory chips can be used to store Uboot files, system files and user data of ZYNQ chip.

- **PCIe interface**

It supports PCI Express 2.0 standard, provides standard PCIe x8 high-speed data transmission interface, and the communication rate of single channel can be up to 5GBaud.

- **Gigabit Ethernet interface**

One 10/100M/1,000M Ethernet RJ45 interface is used for Ethernet data exchange with computers or other network devices. The JL2121 industrial GPHY chip of Jinglue Semiconductor is used as the network interface chip, and the Ethernet is connected to the PS end of the ZYNQ chip.

- **USB2.0 interface**

It is used for OTG communication with PC or USB device, and the connector adopts MINI USB interface.

- **USB Uart interface**

The 1-channel Uart to USB interface is used to communicate with the computer, which is convenient for users to debug. The USB interface adopts MINI USB interface.

- **Micro SD deck**

1-channel Micro SD deck for storing OS images and file systems.

- **FMC HPC expansion port**

A standard FMC HPC expansion port, which can be externally connected to XILINX or various FMC modules of Alinx (HDMI input and output module, binocular camera module, high-speed AD module, etc.). The FMC expansion port contains 84 pairs of differential IO signals and 8 high-speed GTX transceiver signals.

- **JTAG interface**

One USB JTAG interface, debug and download the ZYNQ system through the downloader.

- **SMA port**

2-channel SMA interface, user can connect external trigger signal or clock signal.

- **Clock**

A 33.333 MHz active crystal oscillator is mounted on the board to provide a stable clock source for the PS system, and a 50 MHz active crystal oscillator provides an additional clock for the PL logic; in addition, a programmable clock chip is mounted on the board to provide a clock source for the GTX and provide a reference clock for PCIE, optical fiber and DDR operation.

- **Led light**

1 power indicator, 1 DONE indicator, 4 user debug LEDs, 1 front panel bi-color LED.

- **Key**

2 buttons, 1 reset button, 1 PL user button.

Part 2: ZYNQ chip

The development board uses Xilinx's Zynq7000 series chip, model XC7Z100-2FFG900. The PS system of the chip integrates two ARM Cortex™-A9 processors, AMBA® interconnect, internal memory, external memory interface and peripherals. These peripherals mainly include USB interface, Ethernet interface, SD/SDIO interface, I2C interface, CAN interface, UART interface and GPIO. The PS can operate independently and start on power-up or reset. The overall block diagram of ZYNQ7000 chip is shown in Figure 3.

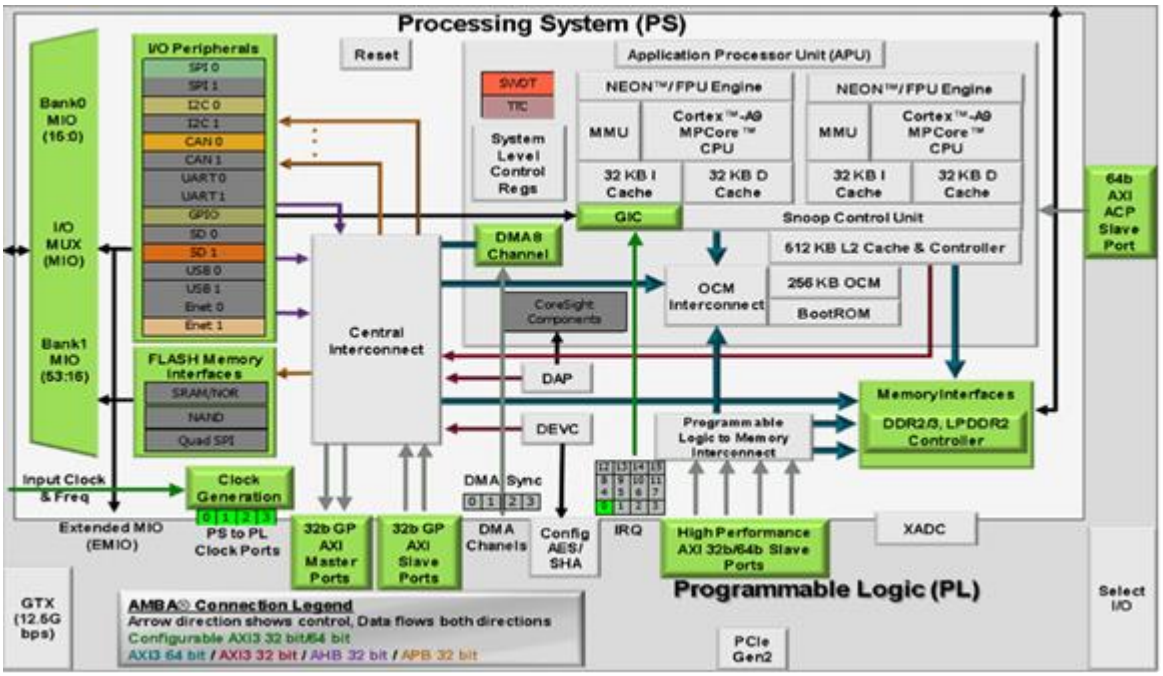


Figure 3: Overall block diagram of ZYNQ7000 chip

The main parameters of PS system are as follows:

- ARM dual-core Cortex A9-based application processor with ARM-v7 architecture up to 800MHz.
- 32KB level 1 instruction and data cache per CPU, 512KB level 2 cache shared by 2 CPUs.
- On-chip boot ROM and 256KB on-chip RAM.
- External storage interface, supporting 16/32-bit DDR2 and DDR3 interfaces.
- Two Gigabit NICs support: Divergent-Aggregate DMA, GMII, RGMII, SGMII interfaces.
- Two USB 2.0 OTG interfaces, each supporting up to 12 nodes.
- Two CAN2.0B bus interfaces.
- Two SD card, SDIO, MMC compatible controllers.
- 2 SPI, 2 UARTs, 2 I2C interface.
- 54 IO with multi-function configuration, which can be configured as common IO or peripheral control interface by software.
- High-bandwidth connections within PS and PS to PL

The main parameters of PL logic part are as follows:

- Logic Cells: 444K.
- Lookup table LUTs: 277 400.
- Flip-flops: 554,800.
- Multiplier 18 x25 MACCs: 2020.
- Block RAM：26.5Mb.
- 16-channel high-speed GTX transceiver supporting PCIE Gen2x8.
- 2 AD converters for on-chip voltage measurement, temperature sensing, and up to 17 external differential input channels, 1MBPS.

The speed grade of XC7Z100-2FFG900I chip is -2, industrial grade, the package is FGG900, and the pin pitch is 1.0mm. The specific chip model definition of ZYNQ7000 series is shown in Figure 4 below.

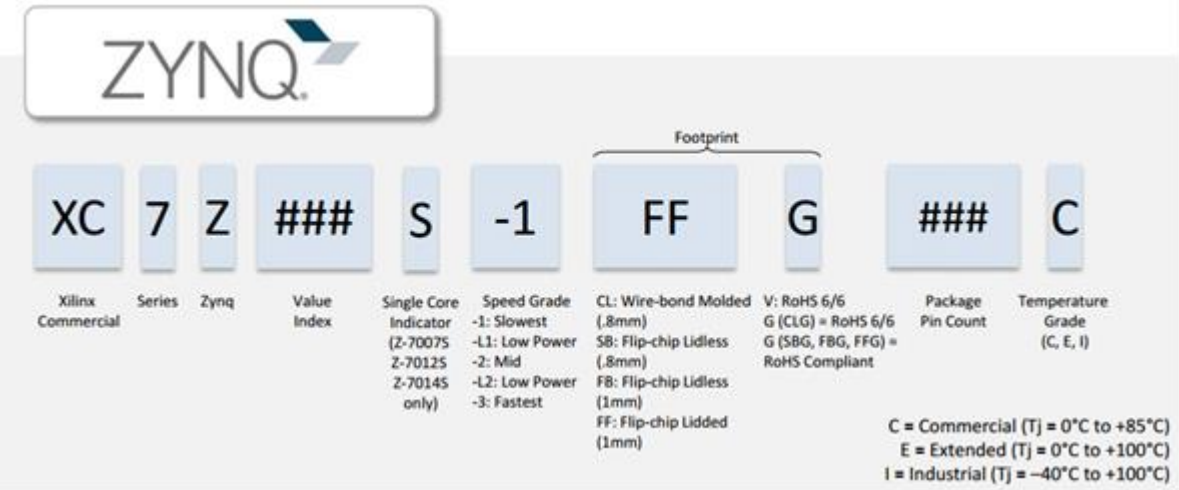


Figure 4: Definition of ZYNQ Model Naming Rules

Figure 5 is the physical picture of the XC7Z100 chip used in the development board.

Figure 5: XC7Z100 Chip

Part 3: DDR3 DRAM

The AX7450B board is equipped with six Micron 512MB DDR3 chips, model MT41J256M16HA-125 (compatible with MT41K256M16 HA-125). The PS side is mounted with 2 pieces to form a 32-bit data width, and the PL side is mounted with 4 pieces to form a 64-bit data width. The maximum running speed of DDR3 SDRAM on PS side can reach 533MHz (data rate 1066Mbps), and two DDR3 memory systems are directly connected to the memory interface of BANK 502 of ZYNQ processing system (PS). The maximum running speed of DDR3 SDRAM on the PL side can reach 800MHz (data rate 1600Mbps), and four DDR3 storage systems are connected to the BANK33 and BANK34 interfaces of the FPGA. The specific configuration of DDR3 SDRAM is shown in Table 1 below.

Tag number	Chip model	Capacity	Manufacturer
U5,U6,U8,U9,U11,U12	MT41J256M16HA-125	256M x 16bit	Micron

Table 1: DDR3 SDRAM Configuration

The hardware design of DDR3 needs to strictly consider the signal integrity. We have fully considered the matching resistor/termination resistor, trace impedance control, and trace equal length control in the circuit design and PCB design to ensure the high-speed and stable operation of DDR3.

The hardware connection mode of DDR3 DRAM on the PS side is shown in Figure 6:

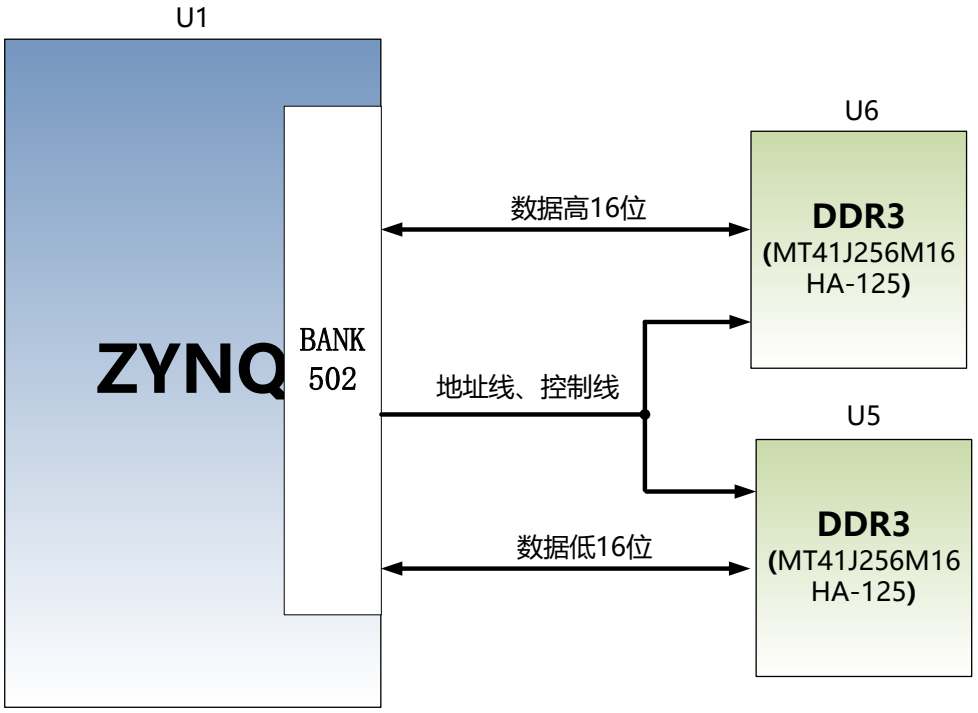


Figure 6: DDR3 DRAM Schematic Section on PS side

The hardware connection mode of DDR3 DRAM on the PL side is shown in Figure 7:

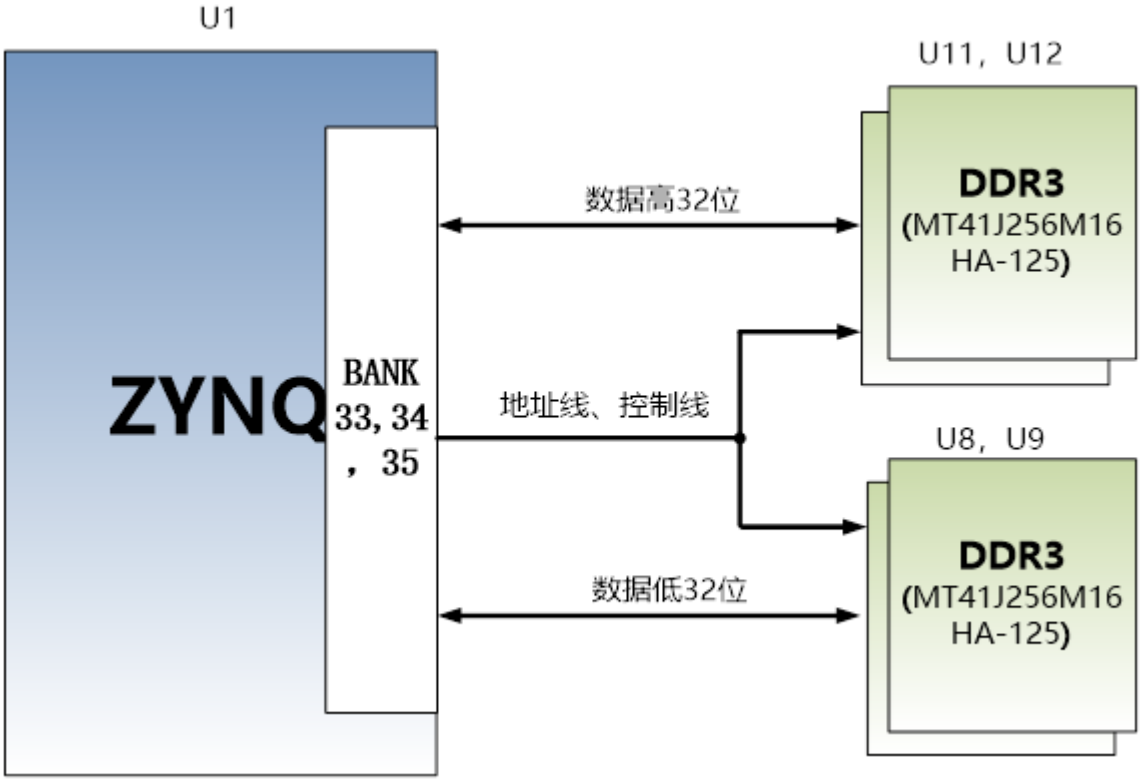


Figure 7: DDR3 DRAM Schematic Section on PL side

PS-side DDR3 DRAM pin assignment:

Signal name	ZYNQ pin name	ZYNQ pin number
PS_DDR3_DQS0_P	PS_DDR_DQS_P0_502	C26
PS_DDR3_DQS0_N	PS_DDR_DQS_N0_502	B26
PS_DDR3_DQS1_P	PS_DDR_DQS_P1_502	C29
PS_DDR3_DQS1_N	PS_DDR_DQS_N1_502	B29
PS_DDR3_DQS2_P	PS_DDR_DQS_P2_502	G29
PS_DDR3_DQS2_N	PS_DDR_DQS_N2_502	F29
PS_DDR3_DQS3_P	PS_DDR_DQS_P3_502	L28
PS_DDR3_DQS4_N	PS_DDR_DQS_N3_502	L29
PS_DDR3_D0	PS_DDR_DQ0_502	A25
PS_DDR3_D1	PS_DDR_DQ1_502	E25
PS_DDR3_D2	PS_DDR_DQ2_502	B27
PS_DDR3_D3	PS_DDR_DQ3_502	D25
PS_DDR3_D4	PS_DDR_DQ4_502	B25
PS_DDR3_D5	PS_DDR_DQ5_502	E26
PS_DDR3_D6	PS_DDR_DQ6_502	D26
PS_DDR3_D7	PS_DDR_DQ7_502	E27
PS_DDR3_D8	PS_DDR_DQ8_502	A29
PS_DDR3_D9	PS_DDR_DQ9_502	A27
PS_DDR3_D10	PS_DDR_DQ10_502	A30
PS_DDR3_D11	PS_DDR_DQ11_502	A28
PS_DDR3_D12	PS_DDR_DQ12_502	C28
PS_DDR3_D13	PS_DDR_DQ13_502	D30
PS_DDR3_D14	PS_DDR_DQ14_502	D28
PS_DDR3_D15	PS_DDR_DQ15_502	D29
PS_DDR3_D16	PS_DDR_DQ16_502	H27
PS_DDR3_D17	PS_DDR_DQ17_502	G27
PS_DDR3_D18	PS_DDR_DQ18_502	H28
PS_DDR3_D19	PS_DDR_DQ19_502	E28
PS_DDR3_D20	PS_DDR_DQ20_502	E30
PS_DDR3_D21	PS_DDR_DQ21_502	F28
PS_DDR3_D22	PS_DDR_DQ22_502	G30
PS_DDR3_D23	PS_DDR_DQ23_502	F30
PS_DDR3_D24	PS_DDR_DQ24_502	J29
PS_DDR3_D25	PS_DDR_DQ25_502	K27
PS_DDR3_D26	PS_DDR_DQ26_502	J30
PS_DDR3_D27	PS_DDR_DQ27_502	J28
PS_DDR3_D28	PS_DDR_DQ28_502	K30
PS_DDR3_D29	PS_DDR_DQ29_502	M29
PS_DDR3_D30	PS_DDR_DQ30_502	L30
PS_DDR3_D31	PS_DDR_DQ31_502	M30
PS_DDR3_DM0	PS_DDR_DM0_502	C27
PS_DDR3_DM1	PS_DDR_DM1_502	B30
PS_DDR3_DM2	PS_DDR_DM2_502	H29
PS_DDR3_DM3	PS_DDR_DM3_502	K28
PS_DDR3_A0	PS_DDR_A0_502	L25

PS_DDR3_A1	PS_DDR_A1_502	K26
PS_DDR3_A2	PS_DDR_A2_502	L27
PS_DDR3_A3	PS_DDR_A3_502	G25
PS_DDR3_A4	PS_DDR_A4_502	J26
PS_DDR3_A5	PS_DDR_A5_502	G24
PS_DDR3_A6	PS_DDR_A6_502	H26
PS_DDR3_A7	PS_DDR_A7_502	K22
PS_DDR3_A8	PS_DDR_A8_502	F27
PS_DDR3_A9	PS_DDR_A9_502	J23
PS_DDR3_A10	PS_DDR_A10_502	G26
PS_DDR3_A11	PS_DDR_A11_502	H24
PS_DDR3_A12	PS_DDR_A12_502	K23
PS_DDR3_A13	PS_DDR_A13_502	H23
PS_DDR3_A14	PS_DDR_A14_502	J24
PS_DDR3_BA0	PS_DDR_BA0_502	M27
PS_DDR3_BA1	PS_DDR_BA1_502	M26
PS_DDR3_BA2	PS_DDR_BA2_502	M25
PS_DDR3_S0	PS_DDR_CS_B_502	N22
PS_DDR3_RAS	PS_DDR_RAS_B_502	N24
PS_DDR3_CAS	PS_DDR_CAS_B_502	M24
PS_DDR3_WE	PS_DDR_WE_B_502	N23
PS_DDR3_ODT	PS_DDR_ODT_502	L23
PS_DDR3_RESET	PS_DDR_DRST_B_502	F25
PS_DDR3_CLK0_P	PS_DDR_CKP_502	K25
PS_DDR3_CLK0_N	PS_DDR_CKN_502	J25
PS_DDR3_CKE	PS_DDR_CKE_502	M22

Table 3: PS-side DDR3 DRAM pin assignment

PL-side DDR3 DRAM pin assignment:

Signal name	ZYNQ pin name	ZYNQ pin number
PL_DDR3_DM0	IO_L4P_T0_35	J14
PL_DDR3_DQS0_N	IO_L3N_T0_DQS_AD1N_35	K13
PL_DDR3_DQS0_P	IO_L3P_T0_DQS_AD1P_35	L13
PL_DDR3_D0	IO_L5N_T0_AD9N_35	J15
PL_DDR3_D1	IO_L2N_T0_AD8N_35	H13
PL_DDR3_D2	IO_L1P_T0_AD0P_35	L15
PL_DDR3_D3	IO_L2P_T0_AD8P_35	J13
PL_DDR3_D4	IO_L5P_T0_AD9P_35	K15
PL_DDR3_D5	IO_L1N_T0_AD0N_35	L14
PL_DDR3_D6	IO_L6P_T0_35	J16
PL_DDR3_D7	IO_L4N_T0_35	H14
PL_DDR3_DM1	IO_L12N_T1_MRCC_35	F14
PL_DDR3_DQS1_N	IO_L9N_T1_DQS_AD3N_35	F12
PL_DDR3_DQS1_P	IO_L9P_T1_DQS_AD3P_35	G12
PL_DDR3_D8	IO_L8N_T1_AD10N_35	G14
PL_DDR3_D9	IO_L10N_T1_AD11N_35	E12
PL_DDR3_D10	IO_L7N_T1_AD2N_35	G16

PL_DDR3_D11	IO_L11N_T1_SRCC_35	D13
PL_DDR3_D12	IO_L10P_T1_AD11P_35	F13
PL_DDR3_D13	IO_L11P_T1_SRCC_35	E13
PL_DDR3_D14	IO_L8P_T1_AD10P_35	G15
PL_DDR3_D15	IO_L12P_T1_MRCC_35	F15
PL_DDR3_DM2	IO_L16N_T2_35	C16
PL_DDR3_DQS2_N	IO_L15N_T2_DQS_AD12N_35	E17
PL_DDR3_DQS2_P	IO_L15P_T2_DQS_AD12P_35	F17
PL_DDR3_D16	IO_L18N_T2_AD13N_35	A17
PL_DDR3_D17	IO_L16P_T2_35	D16
PL_DDR3_D18	IO_L17P_T2_AD5P_35	C17
PL_DDR3_D19	IO_L14P_T2_AD4P_SRCC_35	D15
PL_DDR3_D20	IO_L17N_T2_AD5N_35	B16
PL_DDR3_D21	IO_L13N_T2_MRCC_35	E15
PL_DDR3_D22	IO_L18P_T2_AD13P_35	B17
PL_DDR3_D23	IO_L14N_T2_AD4N_SRCC_35	D14
PL_DDR3_DM3	IO_L20P_T3_AD6P_35	C12
PL_DDR3_DQS3_N	IO_L21N_T3_DQS_AD14N_35	A15
PL_DDR3_DQS3_P	IO_L21P_T3_DQS_AD14P_35	B15
PL_DDR3_D24	IO_L22P_T3_AD7P_35	C11
PL_DDR3_D25	IO_L23P_T3_35	B14
PL_DDR3_D26	IO_L22N_T3_AD7N_35	B11
PL_DDR3_D27	IO_L24N_T3_AD15N_35	A12
PL_DDR3_D28	IO_L24P_T3_AD15P_35	A13
PL_DDR3_D29	IO_L19P_T3_35	C14
PL_DDR3_D30	IO_L20N_T3_AD6N_35	B12
PL_DDR3_D31	IO_L23N_T3_35	A14
PL_DDR3_DM4	IO_L2P_T0_33	L1
PL_DDR3_DQS4_N	IO_L3N_T0_DQS_33	K2
PL_DDR3_DQS4_P	IO_L3P_T0_DQS_33	K3
PL_DDR3_D32	IO_L1N_T0_33	J3
PL_DDR3_D33	IO_L4N_T0_33	L2
PL_DDR3_D34	IO_L1P_T0_33	J4
PL_DDR3_D35	IO_L4P_T0_33	L3
PL_DDR3_D36	IO_L2N_T0_33	K1
PL_DDR3_D37	IO_L6P_T0_33	K6
PL_DDR3_D38	IO_L5N_T0_33	J5
PL_DDR3_D39	IO_L5P_T0_33	K5
PL_DDR3_DM5	IO_L12P_T1_MRCC_33	G5
PL_DDR3_DQS5_N	IO_L9N_T1_DQS_33	H1
PL_DDR3_DQS5_P	IO_L9P_T1_DQS_33	J1
PL_DDR3_D40	IO_L11P_T1_SRCC_33	H4
PL_DDR3_D41	IO_L10N_T1_33	G1
PL_DDR3_D42	IO_L8P_T1_33	H6
PL_DDR3_D43	IO_L7N_T1_33	F2
PL_DDR3_D44	IO_L10P_T1_33	H2
PL_DDR3_D45	IO_L12N_T1_MRCC_33	G4
PL_DDR3_D46	IO_L8N_T1_33	G6

PL_DDR3_D47	IO_L11N_T1_SRCC_33	H3
PL_DDR3_DM6	IO_L14N_T2_SRCC_33	F3
PL_DDR3_DQS6_N	IO_L15N_T2_DQS_33	D5
PL_DDR3_DQS6_P	IO_L15P_T2_DQS_33	E6
PL_DDR3_D48	IO_L18P_T2_33	E1
PL_DDR3_D49	IO_L17P_T2_33	E3
PL_DDR3_D50	IO_L16N_T2_33	D3
PL_DDR3_D51	IO_L14P_T2_SRCC_33	F4
PL_DDR3_D52	IO_L18N_T2_33	D1
PL_DDR3_D53	IO_L13N_T2_MRCC_33	E5
PL_DDR3_D54	IO_L16P_T2_33	D4
PL_DDR3_D55	IO_L17N_T2_33	E2
PL_DDR3_DM7	IO_L23N_T3_33	B1
PL_DDR3_DQS7_N	IO_L21N_T3_DQS_33	A4
PL_DDR3_DQS7_P	IO_L21P_T3_DQS_33	A5
PL_DDR3_D56	IO_L22P_T3_33	C2
PL_DDR3_D57	IO_L24N_T3_33	A2
PL_DDR3_D58	IO_L20N_T3_33	B4
PL_DDR3_D59	IO_L20P_T3_33	B5
PL_DDR3_D60	IO_L22N_T3_33	C1
PL_DDR3_D61	IO_L24P_T3_33	A3
PL_DDR3_D62	IO_L19P_T3_33	C4
PL_DDR3_D63	IO_L23P_T3_33	B2
PL_DDR3_A14	IO_L22N_T3_34	K10
PL_DDR3_A13	IO_L7P_T1_34	J11
PL_DDR3_A12	IO_L13P_T2_MRCC_34	H9
PL_DDR3_A11	IO_L20N_T3_34	J9
PL_DDR3_A10	IO_L18N_T2_34	G7
PL_DDR3_A9	IO_L9P_T1_DQS_34	H12
PL_DDR3_A8	IO_L23P_T3_34	L10
PL_DDR3_A7	IO_L10P_T1_34	E10
PL_DDR3_A6	IO_L19P_T3_34	L7
PL_DDR3_A5	IO_L8N_T1_34	D11
PL_DDR3_A4	IO_L15N_T2_DQS_34	H8
PL_DDR3_A3	IO_L10N_T1_34	D10
PL_DDR3_A2	IO_L7N_T1_34	H11
PL_DDR3_A1	IO_L21P_T3_DQS_34	L8
PL_DDR3_A0	IO_L18P_T2_34	H7
PL_DDR3_BA2	IO_L9N_T1_DQS_34	G11
PL_DDR3_BA1	IO_L21N_T3_DQS_34	K8
PL_DDR3_BA0	IO_L22P_T3_34	K11
PL_DDR3_CLK0_P	IO_L12P_T1_MRCC_34	D9
PL_DDR3_CLK0_N	IO_L12N_T1_MRCC_34	D8
PL_DDR3_RAS	IO_L13N_T2_MRCC_34	G9
PL_DDR3_S0	IO_L16P_T2_34	F8
PL_DDR3_WE	IO_L16N_T2_34	F7
PL_DDR3_CAS	IO_L17P_T2_34	E7
PL_DDR3_CKE	IO_L17N_T2_34	D6

PL_DDR3_ODT	IO_L20P_T3_34	J10
PL_DDR3_RESET	IO_L8P_T1_34	E11

Table 4: PL-side DDR3 DRAM pin assignment

Part 4: QSPI Flash

The development board is equipped with two 256MBit Quad-SPI FLASH chips, model W25Q256FVEI, which uses a 3.3V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, it can be used as the boot device of the system to store the boot image of the system. These images mainly include FPGA bit files, ARM application code and other user data files. See Table 5 for the specific model and relevant parameters of QSPI FLASH.

Tag number	Type of chip	Capacity	Manufacturer
U13, U14	W25Q256FVEI	32M Byte	Winbond

Table 5: QSPI Flash Models and Parameters

QSPI FLASH is connected to the GPIO port of BANK500 of the PS part of the ZYNQ chip. In the system design, it is necessary to configure the GPIO port function of these PS ends as QSPI FLASH interface. Figure 8 shows the portion of the QSPI Flash in the schematic.

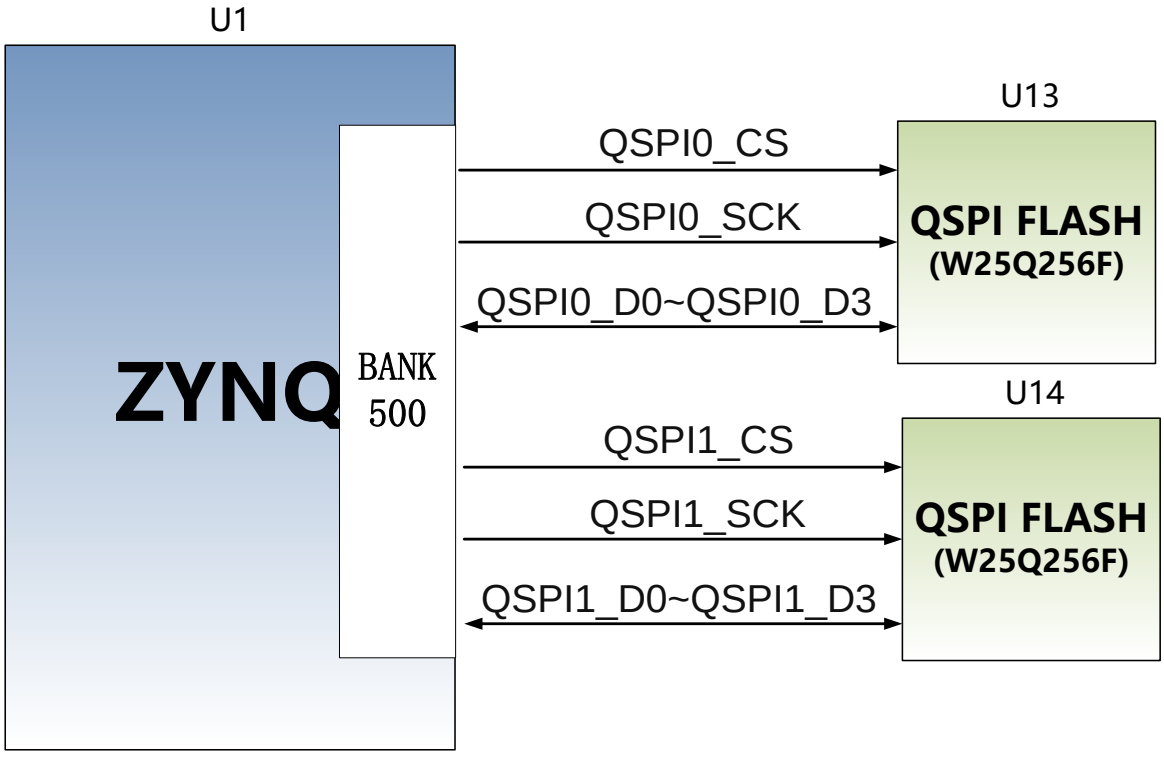


Figure 8: QSPI Flash Connection Diagram

Configure chip pin assignment:

Signal name	ZYNQ pin name	ZYNQ pin number
QSPI0_SCK	PS_MIO6_500	D24
QSPI0_CS	PS_MIO1_500	D23
QSPI0_D0	PS_MIO2_500	F23

QSPI0_D1	PS_MIO3_500	C23
QSPI0_D2	PS_MIO4_500	E23
QSPI0_D3	PS_MIO5_500	C24
QSPI1_SCK	PS_MIO9_500	A24
QSPI1_CS	PS_MIO0_500	F24
QSPI1_D0	PS_MIO10_500	E22
QSPI1_D1	PS_MIO11_500	A23
QSPI1_D2	PS_MIO12_500	E21
QSPI1_D3	PS_MIO13_500	F22

Table 6: QSPI Flash Configure chip pin assignment

Part 5: eMMC Flash

The development board is equipped with a large-capacity 8GB eMMC FLASH chip, model THGBMFG6C1LBAIL, which supports the HS-MMC interface of JEDEC e-MMC V5.0 standard, and the level supports 1.8 V or 3.3 V. The data width of eMMC FLASH and ZYNQ connections is 4 bits. Due to its large capacity and non-volatile characteristics, eMMC FLASH can be used as a large-capacity storage device in the ZYNQ system, such as storing ARM applications, system files, and other user data files. See Table 5-1 for the specific model and relevant parameters of eMMC FLASH.

Tag number	Type of chip	Capacity	Manufacturer
U11	THGBMFG6C1LBAIL	8G Byte	TOSHIBA

Table 7: eMMC Flash Models and Parameters

EMMC FLASH is connected to the GPIO port of BANK501 of the PS part of the ZYNQ chip. In the system design, it is necessary to configure the GPIO port function of these PS ends as an SD interface. Figure 9 shows the part of eMMC Flash in the schematic.

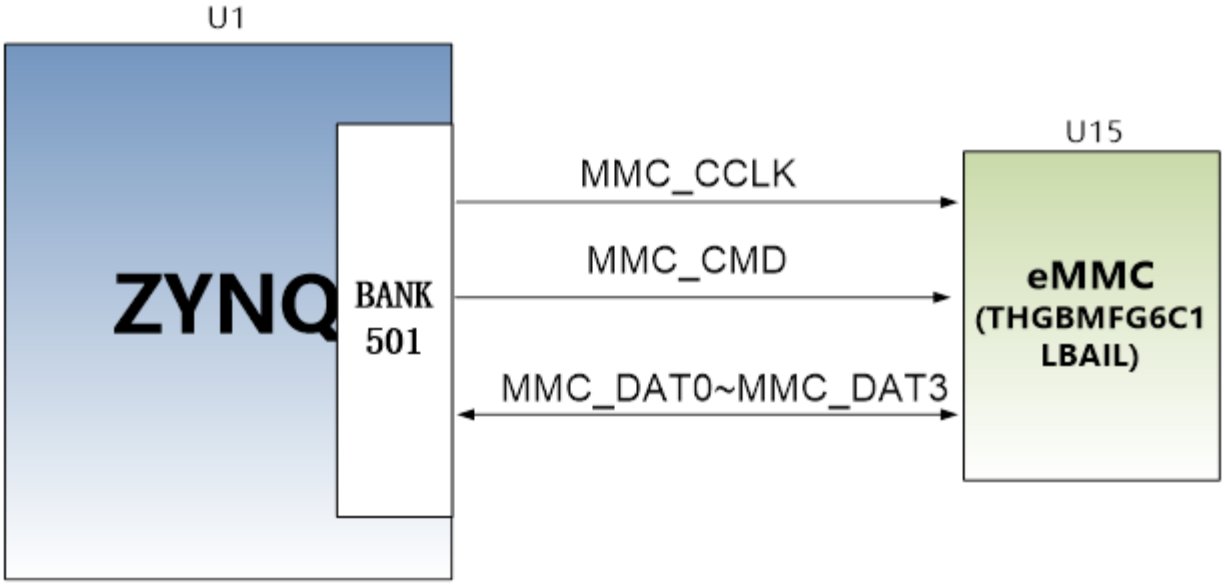


Figure 9: eMMC Flash Connection Diagram

Configure chip pin assignment:

Signal name	ZYNQ pin name	ZYNQ pin number
MMC_CCLK	PS_MIO48_501	C19
MMC_CMD	PS_MIO47_501	A18
MMC_D0	PS_MIO46_501	F20
MMC_D1	PS_MIO49_501	D18
MMC_D2	PS_MIO50_501	A19
MMC_D3	PS_MIO51_501	F19

Table 8: eMMC Flash chip pin assignment

Part 6: Clock configuration

Single-ended and differential active clocks are provided on the AX7450B development board for the PS system and PL logic sections, respectively, allowing the PS system and PL logic to operate independently. The other board provides the differential clock source for the high-speed transceiver GTX.

PS system clock source:

The ZYNQ chip provides a 33.333 MHz clock input to the PS section via the X4 crystal on the development board. The clock input is connected to the PS_CLK_500 pin of the BANK500 of the ZYNQ chip. The schematic diagram is shown in Figure 10:

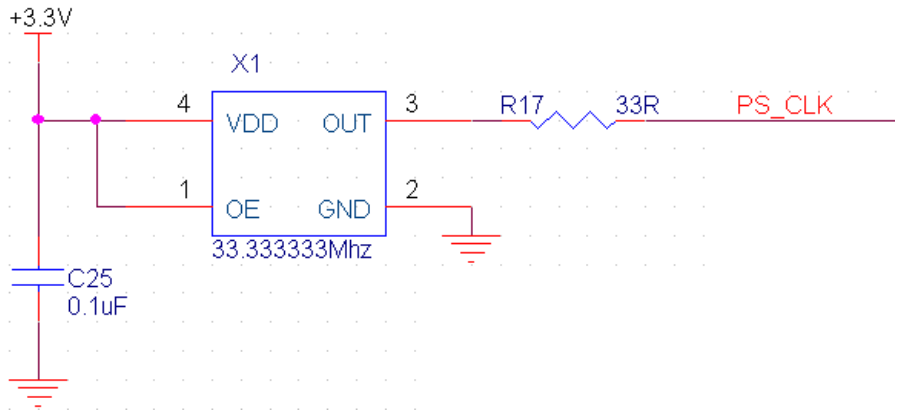


Figure 10: Active Crystal Oscillator of PS Section

Clock pin assignment:

Signal name	ZYNQ pin
PS_CLK	A22

Table 9: Clock pin assignment

PL system clock source:

A single-ended, 50 MHz, 1.8V PL system clock source is provided on the board. The output of the crystal oscillator is connected to the local clock (SRCC) of the FPGA BANK9. This clock can be used to drive the user logic circuit in the FPGA. The schematic diagram of the clock source is shown in Figure 11.

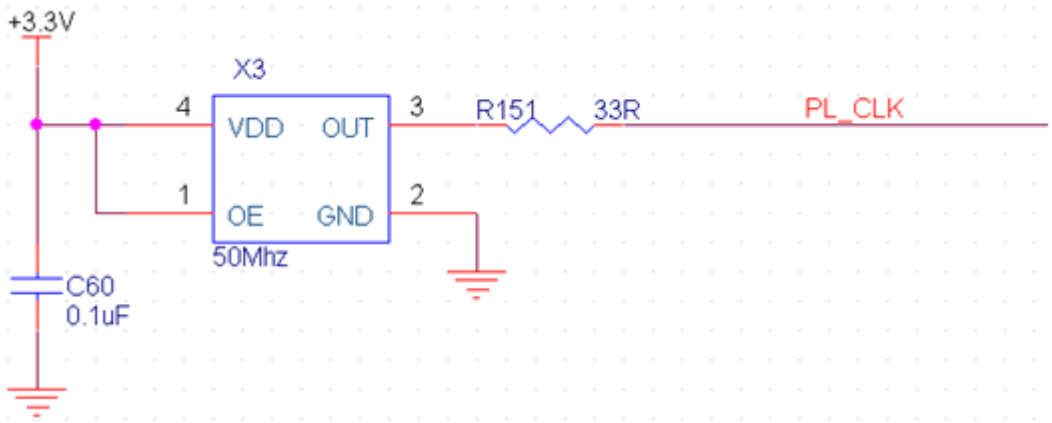


Figure 11: Active Crystal Oscillator of PL Section

PL clock pin assignment:

Signal name	ZYNQ pin
PL_CLK	AB19

Table 10: Clock pin assignment

DDR reference clock:

A 200Mhz differential crystal oscillator is provided to BANK34 as the reference clock of the DDR controller of PL.

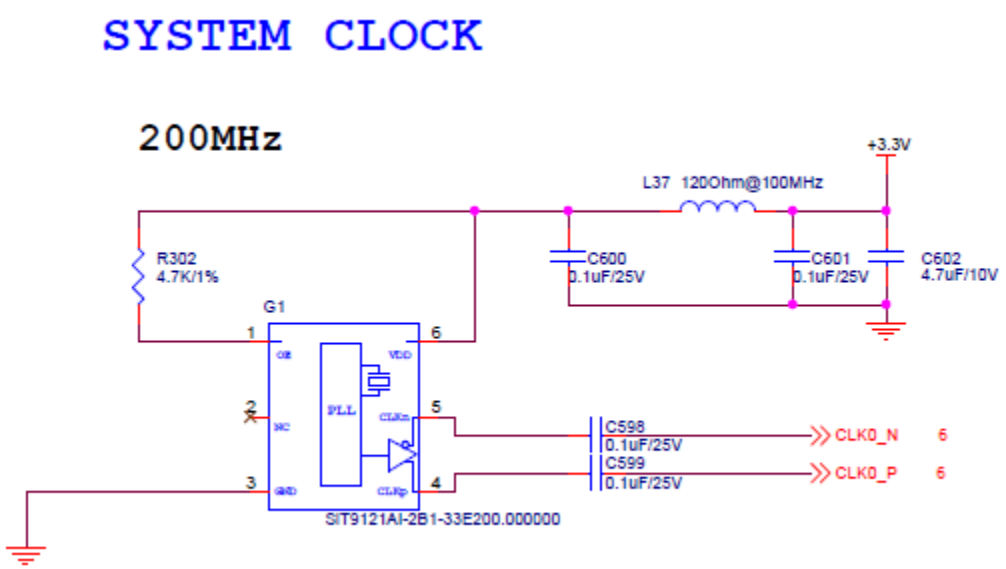


Figure 12: 200Mhz Clock Reference Source

PL clock pin assignment:

Signal name	ZYNQ pin
CLK0_P	F9
CLK0_N	E9

Table 11: PL clock pin assignment

Transceiver reference clock:

A 156.25 MHz differential crystal is provided to BANK110 as the reference clock for the SPF of the GTX transceiver.

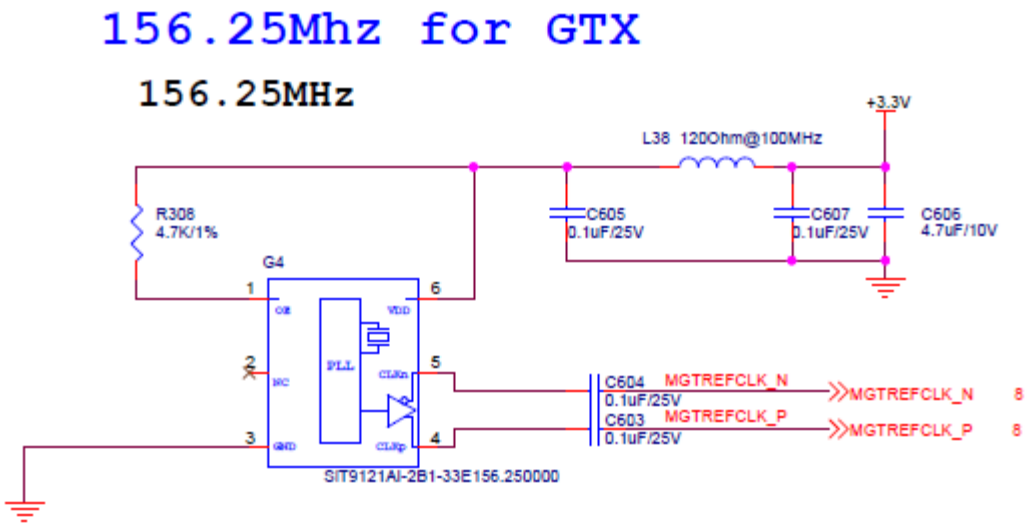


Figure 13: 156.25Mhz Clock Reference Source

Transceiver reference clock pin assignment:

Signal name	ZYNQ pin
MGTREFCLK_P	AC8
MGTREFCLK_N	AC7

Table 12: Transceiver reference clock pin assignment

Part 7: USB to serial port

The development board is equipped with a Uart to USB interface for separate power supply and debugging of the module. The conversion chip adopts the USB-UAR chip of Silicon Labs CP2102GM, and the USB interface adopts the MINI USB interface, which can be connected to the USB port of the upper PC with a USB cable for separate power supply of the module and serial port data communication.

The schematic diagram of the USB Uart circuit design is shown in the following figure:

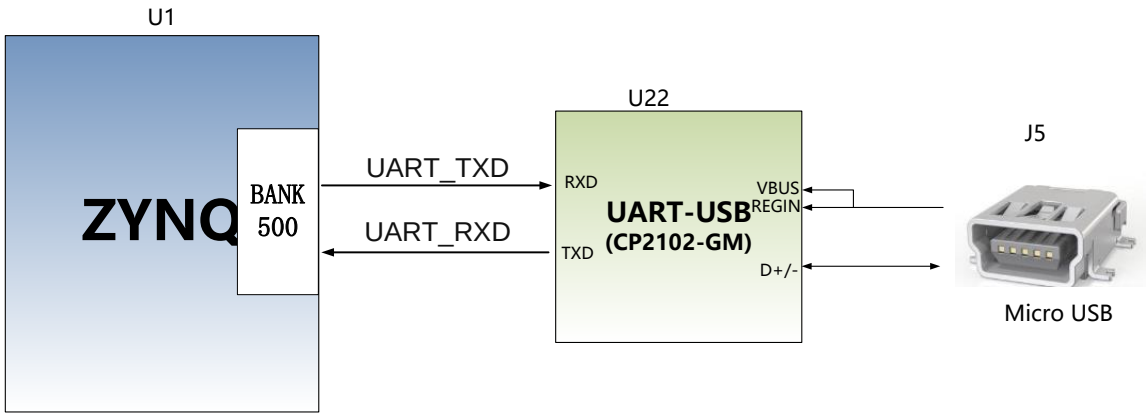


Figure 14: Schematic diagram of USB to serial port

ZYNQ pin assignment from USB to serial port:

Signal name	ZYNQ pin name	ZYNQ pin number	Remark
UART_RXD	PS_MIO14_500	B22	Uart Data Input
UART_TXD	PS_MIO15_500	C22	Uart Data Output

Table 13: ZYNQ pin assignment from USB to serial port

Part 8: Gigabit Ethernet interface

The AX7450B development board has one gigabit Ethernet interface, which is connected to the MIO interface of BANK501 at the PS system end. The Ethernet chip adopts the industrial Ethernet GPHY chip (JL2121-N040I) of Jinglue Semiconductor to provide network communication services for users. The JL2121 chip supports 10/100/1,000 Mbps network transmission rates and communicates with the MAC layer of the Zynq7000 system through the RGMII interface. JL2121 supports MDI/MDX self-adaptation, various speed self-adaptation and Master/Slave self-adaptation, and supports register management of PHY by MDIO bus.

When the JL2121 is powered on, it will detect the level state of some specific IOs to determine its own operating mode. Table 14 describes the default settings for the GPHY chip after power-up.

Configure the Pin	Explain	Configuration value
RXD3_ADR0 RXC_ADR1 RXCTL_ADR2	PHY Address for MDIO/MDC Mode	PHY Address is 001
RXD1_TXDLY	TX clock 2 ns delay	Delay
RXD0_RXDLY	RX clock 2 ns delay	Delay

Table 14: Default configuration values of PHY chip

When the network is connected to Gigabit Ethernet, the data of ZYNQ and PHY chip JL2121 are transmitted through RGMII bus. The transmission clock is 125Mhz, and the data is sampled at the rising edge and falling edge of the clock.

When the network is connected to 100M Ethernet, the data transmission of ZYNQ and PHY chip JL2121 is communicated through MII bus, and the transmission clock is 25 Mhz. Data is sampled on the rising and falling edges of the clock.

Figure 15 shows the connection diagram of the Ethernet PHY chip at the ZYNQ PS end:

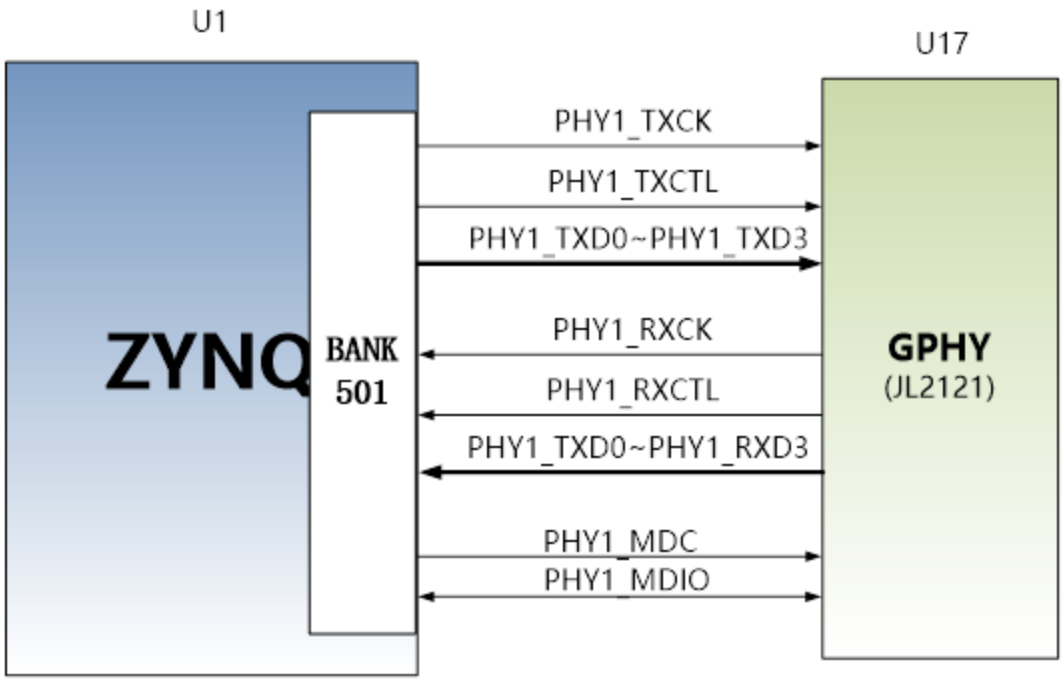


Figure 14: Schematic diagram of connection between ZYNQ PS system and GPHY

The PS-side Gigabit Ethernet pins are assigned as follows:

Signal name	ZYNQ pin name	ZYNQ pin number	Remark
PHY1_TXCK	PS_MIO16_501	L19	RGMII transmit clock
PHY1_TXD0	PS_MIO17_501	K21	Transmit data bit 0
PHY1_TXD1	PS_MIO18_501	K20	Send data bit1
PHY1_TXD2	PS_MIO19_501	J20	Send data bit2
PHY1_TXD3	PS_MIO20_501	M20	Transmit data bit 3
PHY1_TXCTL	PS_MIO21_501	J19	Send enable signal
PHY1_RXCK	PS_MIO22_501	L20	RGMII receive clock
PHY1_RXD0	PS_MIO23_501	J21	Receive data Bit0
PHY1_RXD1	PS_MIO24_501	M19	Receive data Bit1
PHY1_RXD2	PS_MIO25_501	G19	Receive data Bit2
PHY1_RXD3	PS_MIO26_501	M17	Receive data Bit3
PHY1_RXCTL	PS_MIO27_501	G20	Receive data valid signal
PHY1_MDC	PS_MIO52_501	D19	MDIO manages the clock
PHY1_MDIO	PS_MIO53_501	C18	MDIO manages data

Table 15: PS-side Gigabit Ethernet pin assignment

Part 9: USB2.0 OTG interface

There is a USB 2.0 OTG interface on the AX7450B development board. The USB2.0 transceiver uses a 1.8V, high-speed USB3320C-EZK chip supporting ULPI standard interface to achieve high-speed USB2.0 Host mode data communication.

The USB data and control signals of the USB3320C are connected to the IO port of BANK501 at the PS end of the ZYNQ chip, and the USB interface differential signal (DP/DM) is connected to the USB2514 chip to expand four

USB interfaces. A 24 MHz crystal oscillator provides the clock for the USB3320C chip respectively, and the USB interface is a MINI USB port.

The schematic diagram of connection between ZYNQ processor and USB port of USB3320C-EZK chip is shown in Figure 15:

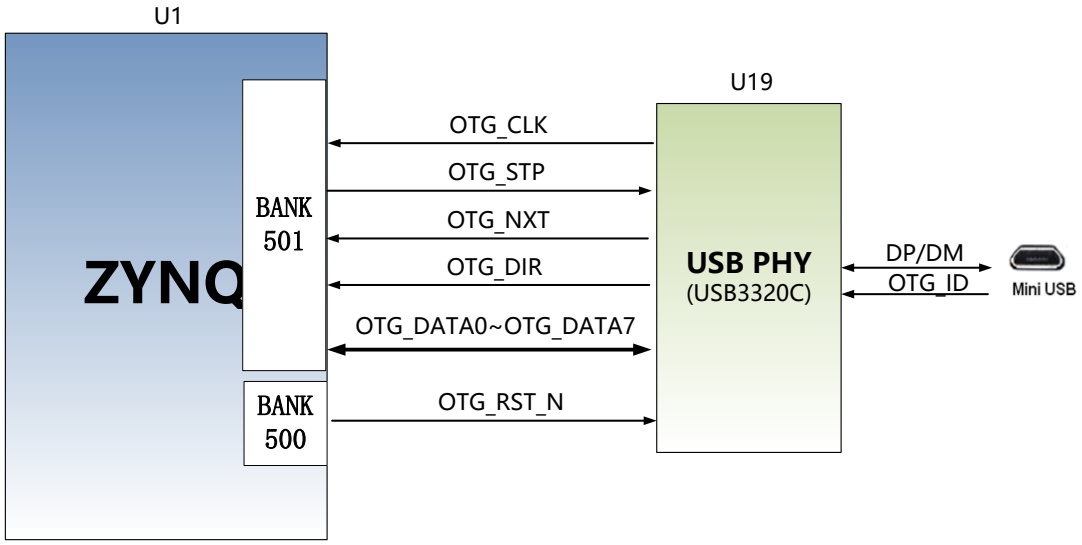


Figure 15: Schematic diagram of connection between Zynq7000 and USB chip

USB2.0 pin assignment:

Signal name	ZYNQ pin name	ZYNQ pin number	Remark
OTG_DATA4	PS_MIO28_501	L17	USB Data Bit 4
OTG_DIR	PS_MIO29_501	H22	USB data direction signal
OTG_STP	PS_MIO30_501	L18	USB stop signal
OTG_NXT	PS_MIO31_501	H21	USB next data signal
OTG_DATA0	PS_MIO32_501	K17	USB Data Bit 0
OTG_DATA1	PS_MIO33_501	G22	USB Data Bit 1
OTG_DATA2	PS_MIO34_501	K18	USB data Bit2
OTG_DATA3	PS_MIO35_501	G21	USB Data Bit 3
OTG_CLK	PS_MIO36_501	H17	USB clock signal
OTG_DATA5	PS_MIO37_501	B21	USB data Bit5
OTG_DATA6	PS_MIO38_501	A20	USB Data Bit 6
OTG_DATA7	PS_MIO39_501	F18	USB Data Bit 7
OTG_RST_N	PS_MIO7_500	B24	USB reset signal

Table 16: USB2.0 pin assignment

Part 10: PCIe Slot

There is a PCIe x8 interface on the AX7450B development board, and 8 pairs of transceivers are connected to the golden fingers of PCIe x8, which can realize the data communication of PCIe x8, PCIe x4, PCIe x2 and PCIe x1.

The transceiver signals of the PCIe interface are directly connected to the GTX transceivers of ZYNQ BANK111 and BANK112. The 8-channel TX signals and RX signals are all connected to the ZYNQ transceivers in a differential

signal manner, and the single-channel communication rate can reach 5G bit bandwidth.

The design diagram of the PCIe interface of the development board is shown in Figure 16 below, in which the TX transmit signal is connected in AC coupling mode.

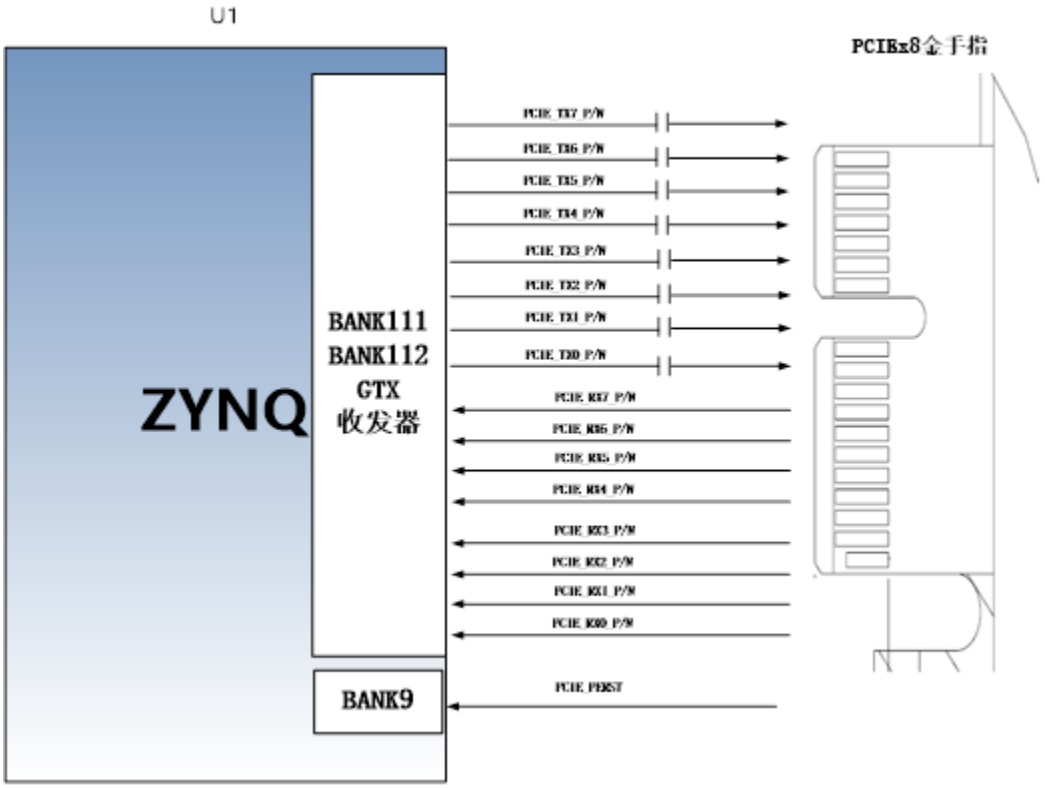


Figure 16: Schematic Diagram of PCIe Design

The PCIe x8 interface FPGA pin assignments are as follows:

Signal name	ZYNQ pin name	ZYNQ pin number	Remark
PCIE_RX0_P	BANK112_RX3_P	P6	PCIE channel 0 data receiving positive
PCIE_RX0_N	BANK112_RX3_N	P5	PCIE Channel 0 Data Receive Negative
PCIE_RX1_P	BANK112_RX2_P	T6	PCIE channel 1 data receiving positive
PCIE_RX1_N	BANK112_RX2_N	T5	PCIE Channel 1 Data Receive Negative
PCIE_RX2_P	BANK112_RX1_P	U4	PCIE channel 2 data receiving positive
PCIE_RX2_N	BANK112_RX1_N	U3	PCIE Channel 2 Data Receive Negative
PCIE_RX3_P	BANK112_RX0_P	V6	PCIE channel 3 data receiving positive
PCIE_RX3_N	BANK112_RX0_N	V5	PCIE Channel 3 Data Receive Negative
PCIE_RX4_P	BANK111_RX3_P	AA4	PCIE Channel 4 Data Reception Positive
PCIE_RX4_N	BANK111_RX3_N	AA3	PCIE Channel 4 Data Receive Negative
PCIE_RX5_P	BANK111_RX2_P	Y6	PCIE channel 5 data receiving positive
PCIE_RX5_N	BANK111_RX2_N	Y5	PCIE Channel 5 Data Receive Negative
PCIE_RX6_P	BANK111_RX1_P	AB6	PCIE channel 6 data receiving positive
PCIE_RX6_N	BANK111_RX1_N	AB5	PCIE Channel 6 Data Receive Negative
PCIE_RX7_P	BANK111_RX0_P	AC4	PCIE channel 7 data receiving positive
PCIE_RX7_N	BANK111_RX0_N	AC3	PCIE Channel 7 Data Receive Negative
PCIE_TX0_P	BANK112_TX3_P	N4	PCIE channel 0 data sending positive
PCIE_TX0_N	BANK112_TX3_N	N3	PCIE channel 0 data transmission negative

PCIE_TX1_P	BANK112_TX2_P	P2	PCIE Channel 1 Data Sending Positive
PCIE_TX1_N	BANK112_TX2_N	P1	PCIE channel 1 data transmission negative
PCIE_TX2_P	BANK112_TX1_P	R4	PCIE Channel 2 Data Sending Positive
PCIE_TX2_N	BANK112_TX1_N	R3	PCIE channel 2 data transmission negative
PCIE_TX3_P	BANK112_TX0_P	T2	PCIE Channel 3 Data Sending Positive
PCIE_TX3_N	BANK112_TX0_N	T1	PCIE channel 3 data transmission negative
PCIE_TX4_P	BANK111_TX3_P	V2	PCIE Channel 4 Data Sending Positive
PCIE_TX4_N	BANK111_TX3_N	V1	PCIE channel 4 data transmission negative
PCIE_TX5_P	BANK111_TX2_P	W4	PCIE Channel 5 Data Sending Positive
PCIE_TX5_N	BANK111_TX2_N	W3	PCIE channel 5 data transmission negative
PCIE_TX6_P	BANK111_TX1_P	Y2	PCIE Channel 6 Data Sending Positive
PCIE_TX6_N	BANK111_TX1_N	Y1	PCIE channel 6 data transmission negative
PCIE_TX7_P	BANK111_TX0_P	AB2	PCIE Channel 7 Data Sending Positive
PCIE_TX7_N	BANK111_TX0_N	AB1	PCIE channel 7 data transmission negative
PCIE_PERST	IO_L12N_T1_MRCC_9	AD19	Reset signal of PCIE board

Table 17: PCIe x8 interface FPGA pin assignment

Part 11: TF Card slot

The AX7450B development board includes a Micro-type of TF card interface to provide user access to the TF card memory, which is used to store the BOOT program of the ZYNQ chip, the Linux operating system kernel, the file system, and other user data files.

The SDIO signal is connected to the IO signal of ZYNQ's PS BANK501. Because the VCCIO of this BANK is set to 1.8V, but the data level of the SD card is 3.3V. Here we connect it through the TXS02612 level shifter. The schematic of the Zynq7000 PS and SD card connectors is shown in Figure 17.

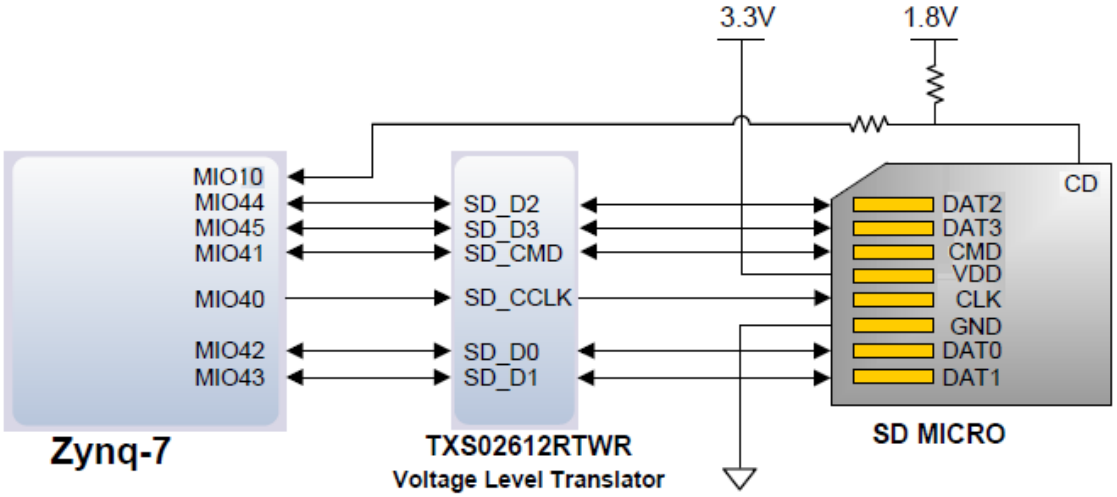


Figure 17: Schematic diagram of SD card connection

SD card slot pin assignment:

Signal name	ZYNQ pin name	ZYNQ pin number	Remark
SD_CLK	PS_MIO40	B20	SD clock signal
SD_CMD	PS_MIO41	J18	SD command signal

SD_D0	PS_MIO42	D20	SD Data 0
SD_D1	PS_MIO43	E18	SD Data 1
SD_D2	PS_MIO44	E20	SD Data 2
SD_D3	PS_MIO45	H18	SD Data 3

Table 18: SD card slot pin assignment

Part 12: FMC connector

The AX7450B development board is equipped with a standard FMC HPC expansion port, which can be externally connected to XILINX or various FMC modules of Alinx (HDMI input and output modules, binocular camera modules, high-speed AD modules, etc.). The FMC expansion port contains 84 pairs of differential IO signals and 8 high-speed GTX transceiver signals.

The 84 pairs of differential signals of the FMC expansion port are connected to the IO of BANK10 ~ 13 of the ZYNQ chip. The IO level standard is determined by the voltage VADJ and VIO_B of BANK. The output voltage of these two power supplies can be changed by configuring the PMIC chip LP873220 through the program. For example, configure the voltage of VADJ and VIO_B to 2.5V, so that 84 pairs of differential signals support LVDS data communication. The other 8 channels of GTX transceiver signals and reference clock signals are respectively connected to the GTX transceivers and clock inputs of ZYNQ BANK109 and BANK110. A schematic of the Zynq7000 and FMC connectors is shown in Figure 18.

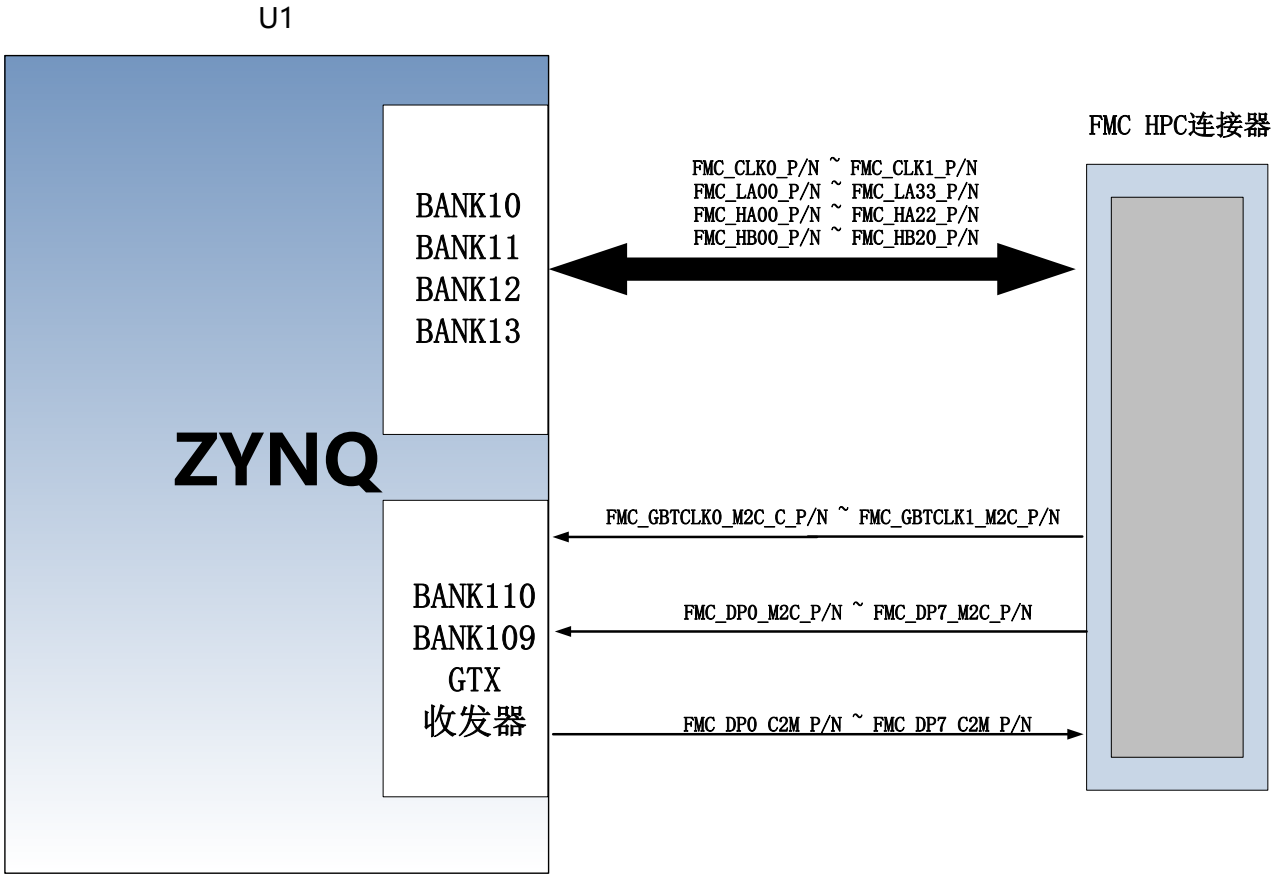


Figure 18: Schematic diagram of FMC connector connection

FMC connector pin assignment:

FMC pin number	Signal name	ZYNQ pin number	Remark
J2	FMC_CLK1_C2M_P	R25	FMC 1st output reference clock P
J3	FMC_CLK1_C2M_N	R26	FMC 1st output reference clock N
H4	FMC_CLK0_M2C_P	AE13	FMC channel 0 input reference clock P
H5	FMC_CLK0_M2C_N	AF13	FMC channel 0 input reference clock N
G2	FMC_CLK0_C2M_P	AF20	FMC channel 0 input reference clock P
G3	FMC_CLK0_C2M_N	AG20	FMC channel 0 input reference clock N
G6	FMC_LA00_CC_P	AF15	FMC LA Channel 0 Data (Clock) P
G7	FMC_LA00_CC_N	AG15	FMC LA Channel 0 Data (Clock) N
D8	FMC_LA01_CC_P	AG17	FMC LA 1st data (clock) P
D9	FMC_LA01_CC_N	AG16	FMC LA 1st data (clock) N
H7	FMC_LA02_P	AA15	FMC LA Channel 2 Data P
H8	FMC_LA02_N	AA14	FMC LA Channel 2 Data N
G9	FMC_LA03_P	AC14	FMC LA Channel 3 Data P
G10	FMC_LA03_N	AC13	FMC LA Channel 3 Data N
H10	FMC_LA04_P	AD14	FMC LA Channel 4 Data P
H11	FMC_LA04_N	AD13	FMC LA Channel 4 Data N
D11	FMC_LA05_P	AG12	FMC LA Channel 5 Data P
D12	FMC_LA05_N	AH12	FMC LA Channel 5 Data N
C10	FMC_LA06_P	AD16	FMC LA Channel 6 Data P
C11	FMC_LA06_N	AD15	FMC LA Channel 6 Data N
H13	FMC_LA07_P	AH14	FMC LA Channel 7 Data P
H14	FMC_LA07_N	AH13	FMC LA Channel 7 Data N
G12	FMC_LA08_P	AE12	FMC LA Channel 8 Data P
G13	FMC_LA08_N	AF12	FMC LA 8th Channel Data N
D14	FMC_LA09_P	AJ14	FMC LA Channel 9 Data P
D15	FMC_LA09_N	AJ13	FMC LA Channel 9 Data N
C14	FMC_LA10_P	AJ15	FMC LA 10th Channel Data P
C15	FMC_LA10_N	AK15	FMC LA 10th Channel Data N
H16	FMC_LA11_P	AJ16	FMC LA Channel 11 Data P
H17	FMC_LA11_N	AK16	FMC LA 11th data N
G15	FMC_LA12_P	AE16	FMC LA Channel 12 Data P
G16	FMC_LA12_N	AE15	FMC LA 12th data N
D17	FMC_LA13_P	AH17	FMC LA Channel 13 Data P
D18	FMC_LA13_N	AH16	FMC LA Channel 13 Data N
C18	FMC_LA14_P	AF18	FMC LA 14th Channel Data P
C19	FMC_LA14_N	AF17	FMC LA 14th Channel Data N
H19	FMC_LA15_P	AE18	FMC LA Channel 15 Data P
H20	FMC_LA15_N	AE17	FMC LA Channel 15 Data N
G18	FMC_LA16_P	AH18	FMC LA Channel 16 Data P
G19	FMC_LA16_N	AJ18	FMC LA Channel 16 Data N
D20	FMC_LA17_CC_P	AG21	FMC LA 17th data (clock) P
D21	FMC_LA17_CC_N	AH21	FMC LA Channel 17 Data (Clock) N
C22	FMC_LA18_CC_P	AD23	FMC LA 18th Data (Clock) P
C23	FMC_LA18_CC_N	AE23	FMC LA 18th Data (Clock) N
H22	FMC_LA19_P	AB21	FMC LA Channel 19 Data P
H23	FMC_LA19_N	AB22	FMC LA Channel 19 Data N
G21	FMC_LA20_P	W21	FMC LA Channel 20 Data P

G22	FMC_LA20_N	Y21	FMC LA Channel 20 Data N
H25	FMC_LA21_P	AK17	FMC LA 21st data P
H26	FMC_LA21_N	AK18	FMC LA Channel 21 Data N
G24	FMC_LA22_P	AD21	FMC LA Channel 22 Data P
G25	FMC_LA22_N	AE21	FMC LA Channel 22 Data N
D23	FMC_LA23_P	AF19	FMC LA 23rd data P
D24	FMC_LA23_N	AG19	FMC LA Channel 23 Data N
H28	FMC_LA24_P	AG22	FMC LA Channel 24 Data P
H29	FMC_LA24_N	AH22	FMC LA Channel 24 Data N
G27	FMC_LA25_P	AJ21	FMC LA Channel 25 Data P
G28	FMC_LA25_N	AK21	FMC LA 25th Channel Data N
D26	FMC_LA26_P	AH19	FMC LA Channel 26 Data P
D27	FMC_LA26_N	AJ19	FMC LA Channel 26 Data N
C26	FMC_LA27_P	AJ20	FMC LA Channel 27 Data P
C27	FMC_LA27_N	AK20	FMC LA Channel 27 Data N
H31	FMC_LA28_P	AJ23	FMC LA 28th Channel Data P
H32	FMC_LA28_N	AJ24	FMC LA 28th Channel Data N
G30	FMC_LA29_P	AK22	FMC LA 29th channel data P
G31	FMC_LA29_N	AK23	FMC LA 29th channel data N
H34	FMC_LA30_P	AG24	FMC LA 30th data P
H35	FMC_LA30_N	AG25	FMC LA 30th data N
G33	FMC_LA31_P	AH23	FMC LA 31st channel data P
G34	FMC_LA31_N	AH24	FMC LA 31st Channel Data N
H37	FMC_LA32_P	AC24	FMC LA 32nd data P
H38	FMC_LA32_N	AD24	FMC LA 32nd data N
G36	FMC_LA33_P	AF23	FMC LA 33rd channel data P
G37	FMC_LA33_N	AF24	FMC LA 33rd Channel Data N
F4	FMC_HA00_CC_P	AC28	FMC HA Channel 0 Data (Clock) P
F5	FMC_HA00_CC_N	AD28	FMC HA Channel 0 Data (Clock) N
E2	FMC_HA01_CC_P	AB27	FMC HA 1st Data (Clock) P
E3	FMC_HA01_CC_N	AC27	FMC HA 1st Data (Clock) N
K7	FMC_HA02_P	AJ26	FMC HA Channel 2 Data P
K8	FMC_HA02_N	AK26	FMC HA Channel 2 Data N
J6	FMC_HA03_P	AE25	FMC HA Channel 3 Data P
J7	FMC_HA03_N	AF25	FMC HA Channel 3 Data N
F7	FMC_HA04_P	AB25	FMC HA Channel 4 Data P
F8	FMC_HA04_N	AB26	FMC HA Channel 4 Data N
E6	FMC_HA05_P	Y26	FMC HA Channel 5 Data P
E7	FMC_HA05_N	Y27	FMC HA Channel 5 Data N
K10	FMC_HA06_P	Y28	FMC HA Channel 6 Data P
K11	FMC_HA06_N	AA29	FMC HA Channel 6 Data N
J9	FMC_HA07_P	AJ28	FMC HA Channel 7 Data P
J10	FMC_HA07_N	AJ29	FMC HA Channel 7 Data N
F10	FMC_HA08_P	AD25	FMC HA Channel 8 Data P
F11	FMC_HA08_N	AE26	FMC HA 8th channel data N
E9	FMC_HA09_P	AC26	FMC HA Channel 9 Data P
E10	FMC_HA09_N	AD26	FMC HA Channel 9 Data N
K13	FMC_HA10_P	AA27	FMC HA Channel 10 Data P

K14	FMC_HA10_N	AA28	FMC HA 10th Channel Data N
J12	FMC_HA11_P	Y30	FMC HA Channel 11 Data P
J13	FMC_HA11_N	AA30	FMC HA Channel 11 Data N
F13	FMC_HA12_P	AG26	FMC HA Channel 12 Data P
F14	FMC_HA12_N	AG27	FMC HA Channel 12 Data N
E12	FMC_HA13_P	AE27	FMC HA Channel 13 Data P
E13	FMC_HA13_N	AF27	FMC HA Channel 13 Data N
J15	FMC_HA14_P	AF29	FMC HA 14th Channel Data P
J16	FMC_HA14_N	AG29	FMC HA 14th Channel Data N
F16	FMC_HA15_P	AK27	FMC HA Channel 15 Data P
F17	FMC_HA15_N	AK28	FMC HA Channel 15 Data N
E15	FMC_HA16_P	AH26	FMC HA Channel 16 Data P
E16	FMC_HA16_N	AH27	FMC HA Channel 16 Data N
K16	FMC_HA17_CC_P	AE28	FMC HA 17th Data (Clock) P
K17	FMC_HA17_CC_N	AF28	FMC HA 17th data (clock) N
J18	FMC_HA18_P	AF30	FMC HA Channel 18 Data P
J19	FMC_HA18_N	AG30	FMC HA Channel 18 Data N
F19	FMC_HA19_P	AJ30	FMC HA Channel 19 Data P
F20	FMC_HA19_N	AK30	FMC HA Channel 19 Data N
E18	FMC_HA20_P	AH28	FMC HA Channel 20 Data P
E19	FMC_HA20_N	AH29	FMC HA Channel 20 Data N
K19	FMC_HA21_P	AB29	FMC HA Channel 21 Data P
K20	FMC_HA21_N	AB30	FMC HA Channel 21 Data N
J21	FMC_HA22_P	AD30	FMC HA Channel 22 Data P
J22	FMC_HA22_N	AE30	FMC HA Channel 22 Data N
K22	FMC_HA23_P	AC29	FMC HA 23rd Channel Data P
K23	FMC_HA23_N	AD29	FMC HA Channel 23 Data N
K25	FMC_HB00_CC_P	U25	FMC HB Channel 0 Data (Clock) P
K26	FMC_HB00_CC_N	V26	FMC HB Channel 0 Data (Clock) N
J24	FMC_HB01_P	P21	FMC HB Channel 1 Data P
J25	FMC_HB01_N	R21	FMC HB Channel 1 Data N
F22	FMC_HB02_P	U22	FMC HB Channel 2 Data P
F23	FMC_HB02_N	V22	FMC HB 2nd channel data N
E21	FMC_HB03_P	R22	FMC HB Channel 3 Data P
E22	FMC_HB03_N	R23	FMC HB Channel 3 Data N
F25	FMC_HB04_P	W25	FMC HB Channel 4 Data P
F26	FMC_HB04_N	W26	FMC HB Channel 4 Data N
E24	FMC_HB05_P	U24	FMC HB Channel 5 Data P
E25	FMC_HB05_N	V24	FMC HB Channel 5 Data N
K28	FMC_HB06_CC_P	U26	FMC HB Channel 6 Data P
K29	FMC_HB06_CC_N	U27	FMC HB Channel 6 Data N
J27	FMC_HB07_P	T22	FMC HB Channel 7 Data P
J28	FMC_HB07_N	T23	FMC HB Channel 7 Data N
F28	FMC_HB08_P	V28	FMC HB Channel 8 Data P
F29	FMC_HB08_N	V29	FMC HB Channel 8 Data N
E27	FMC_HB09_P	V27	FMC HB Channel 9 Data P
E28	FMC_HB09_N	W28	FMC HB Channel 9 Data N
K31	FMC_HB10_P	W29	FMC HB Channel 10 Data P

K32	FMC_HB10_N	W30	FMC HB Channel 10 Data N
J30	FMC_HB11_P	T24	FMC HB Channel 11 Data P
J31	FMC_HB11_N	T25	FMC HB Channel 11 Data N
F31	FMC_HB12_P	T30	FMC HB Channel 12 Data P
F32	FMC_HB12_N	U30	FMC HB Channel 12 Data N
E30	FMC_HB13_P	T29	FMC HB Channel 13 Data P
E31	FMC_HB13_N	U29	FMC HB Channel 13 Data N
K34	FMC_HB14_P	N29	FMC HB Channel 14 Data P
K35	FMC_HB14_N	P29	FMC HB Channel 14 Data N
J33	FMC_HB15_P	R28	FMC HB Channel 15 Data P
J34	FMC_HB15_N	T28	FMC HB Channel 15 Data N
F34	FMC_HB16_P	P30	FMC HB Channel 16 Data P
F35	FMC_HB16_N	R30	FMC HB Channel 16 Data N
K37	FMC_HB17_CC_P	R27	FMC HB Channel 17 Data (Clock) P
K38	FMC_HB17_CC_N	T27	FMC HB Channel 17 Data (Clock) N
J36	FMC_HB18_P	P23	FMC HB Channel 18 Data P
J37	FMC_HB18_N	P24	FMC HB 18th channel data N
E33	FMC_HB19_P	P25	FMC HB Channel 19 Data P
E34	FMC_HB19_N	P26	FMC HB Channel 19 Data N
F37	FMC_HB20_P	N26	FMC HB Channel 20 Data P
F38	FMC_HB20_N	N27	FMC HB Channel 20 Data N
E36	FMC_HB21_P	N28	FMC HB Channel 21 Data P
E37	FMC_HB21_N	P28	FMC HB Channel 21 Data N
D4	FMC_GBTCLK0_M2C_P	AD10	Transceiver Reference Clock 0 Input P
D5	FMC_GBTCLK0_M2C_N	AD9	Transceiver Reference Clock 0 Input N
B20	FMC_GBTCLK1_M2C_P	AA8	Transceiver Reference Clock 1 Input P
B21	FMC_GBTCLK1_M2C_N	AA7	Transceiver Reference Clock 1 Input N
C6	FMC_DP0_M2C_P	AH10	Transceiver Data 0 Input P
C7	FMC_DP0_M2C_N	AH9	Transceiver Data 0 Input N
A2	FMC_DP1_M2C_P	AJ8	Transceiver Data 1 Input P
A3	FMC_DP1_M2C_N	AJ7	Transceiver Data 1 Input N
A6	FMC_DP2_M2C_P	AG8	Transceiver Data 2 Input P
A7	FMC_DP2_M2C_N	AG7	Transceiver Data 2 Input N
A10	FMC_DP3_M2C_P	AE8	Transceiver Data 3 Input P
A11	FMC_DP3_M2C_N	AE7	Transceiver Data 3 Input N
A14	FMC_DP4_M2C_P	AH6	Transceiver Data 4 Input P
A15	FMC_DP4_M2C_N	AH5	Transceiver Data 4 Input N
A18	FMC_DP5_M2C_P	AG4	Transceiver Data 5 Input P
A19	FMC_DP5_M2C_N	AG3	Transceiver Data 5 Input N
B16	FMC_DP6_M2C_P	AF6	Transceiver Data 6 Input P
B17	FMC_DP6_M2C_N	AF5	Transceiver Data 6 Input N
B12	FMC_DP7_M2C_P	AD6	Transceiver Data 7 Input P
B13	FMC_DP7_M2C_N	AD5	Transceiver Data 7 Input N
C2	FMC_DP0_C2M_P	AK10	Transceiver Data 0 Output P
C3	FMC_DP0_C2M_N	AK9	Transceiver Data 0 Output N
A22	FMC_DP1_C2M_P	AK6	Transceiver Data 1 Output P
A23	FMC_DP1_C2M_N	AK5	Transceiver Data 1 Output N
A26	FMC_DP2_C2M_P	AJ4	Transceiver Data 2 Output P

A27	FMC_DP2_C2M_N	AJ3	Transceiver Data 2 Output N
A30	FMC_DP3_C2M_P	AK2	Transceiver Data 3 Output P
A31	FMC_DP3_C2M_N	AK1	Transceiver Data 3 Output N
A34	FMC_DP4_C2M_P	AH2	Transceiver Data 4 Output P
A35	FMC_DP4_C2M_N	AH1	Transceiver Data 4 Output N
A38	FMC_DP5_C2M_P	AF2	Transceiver data 5 output P
A39	FMC_DP5_C2M_N	AF1	Transceiver Data 5 Output N
B36	FMC_DP6_C2M_P	AE4	Transceiver Data 6 Output P
B37	FMC_DP6_C2M_N	AE3	Transceiver Data 6 Output N
B32	FMC_DP7_C2M_P	AD2	Transceiver Data 7 Output P
B33	FMC_DP7_C2M_N	AD1	Transceiver Data 7 Output N

Table 19: FMC connector pin assignment

Part 13: LED Light

The AX7450B development board has 9 monochrome LED lights and 1 two-color LED light. The monochrome LED light contains 1 power indicator; 1 DONE configuration indicator; 2 serial communication indicators, 4 PL control indicators. The two-color LED light is assembled on the board side and controlled by the IO of the PL. 4 monochrome LED lights are connected to the IO of the BANK10, and the two-color LED light is connected to the IO of the BANK9. A schematic diagram of the hardware connection of the user LED light is shown in Figure 19:

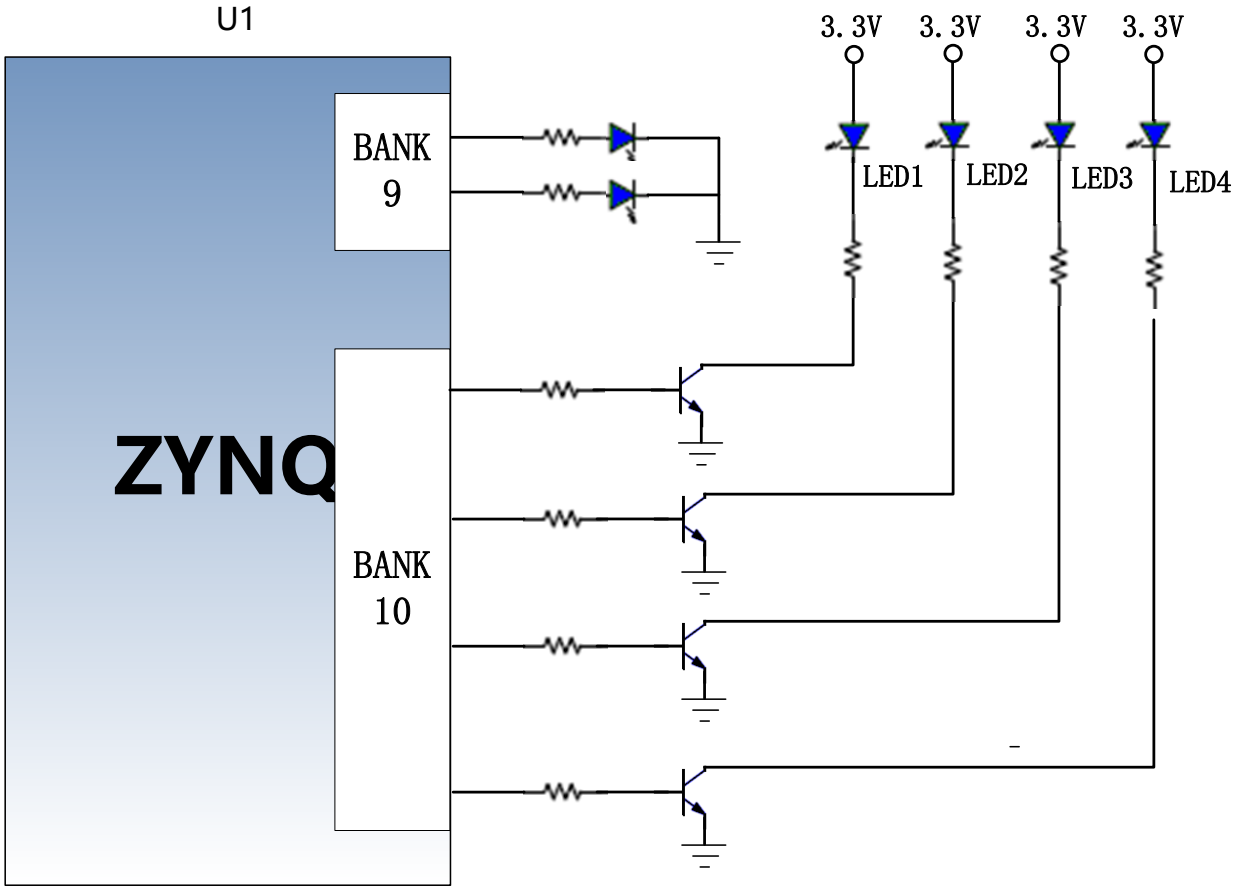


Figure 19: Hardware connection diagram of user LED light

Pin assignment for user LED:

Signal name	ZYNQ pin name	ZYNQ pin number	Remark
PL_LED1	IO_L23P_T3_10	AC16	User monochrome PL LED 1 light
PL_LED2	IO_L23N_T3_10	AB17	User monochrome PL LED 2 light
PL_LED3	IO_L24P_T3_10	AB16	User monochrome PL LED3 light
PL_LED4	IO_L24N_T3_10	AA17	User monochrome PL LED4 light
TEST_LED1	IO_L11N_T1_SRCC_9	AC19	Consumer Bi-Color PL LED 1 Light
TEST_LED2	IO_L12P_T1_MRCC_9	AD18	Consumer Bi-Color PL LED 2 Light

Table 20: User LED pin assignment

Part 14: Reset key and User keys

The AX7450B development board has a reset button, RESET, and a user button. The reset signal is connected to the PS reset pin of the ZYNQ chip. The user can use this reset button to reset the ZYNQ system. One user button is connected to the IO of the PL. Both the reset button and the user button are valid at low level, and the connection diagram of the reset button and the user button is shown in Figure 20:

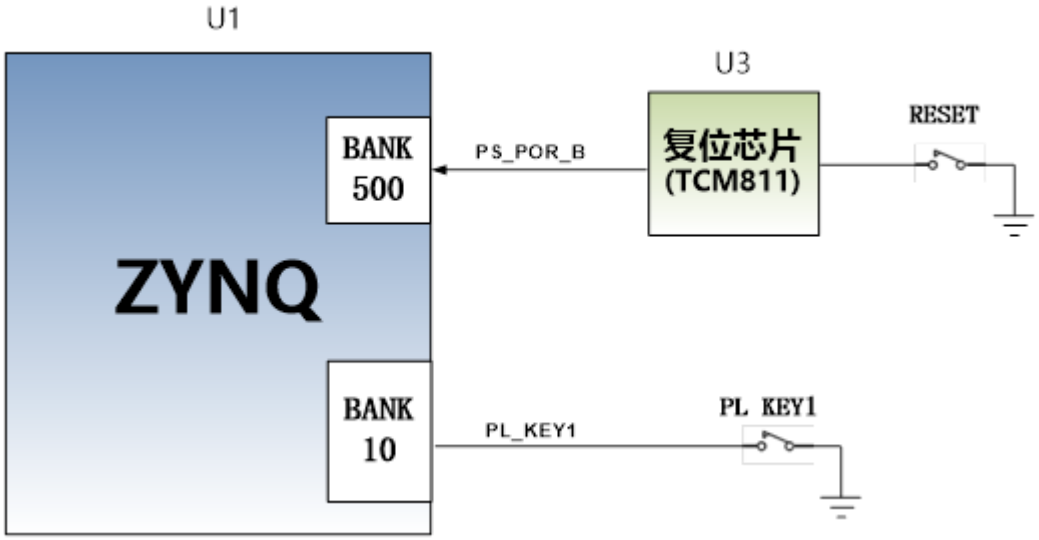


Figure 20: Connection diagram of reset button

ZYNQ pin assignment for key:

Signal name	ZYNQ pin name	ZYNQ pin number	Remark
PS_POR_B	PS_POR_B_500	D21	ZYNQ system reset signal
PL_KEY1	IO_L21N_T3_DQS_10	AC12	PL key 1 input

Table 21: Key pin assignment

Part 15: SMA interface

There are two SMA interfaces on the AX7450B development board, which is convenient for users to input or output differential clock signals or individual clock signals through the SMA line. The signal of the SMA interface is connected to the IO of BANK9, and the default standard level is 3.3V. The schematic diagram of SMA connection is shown in Figure 21:

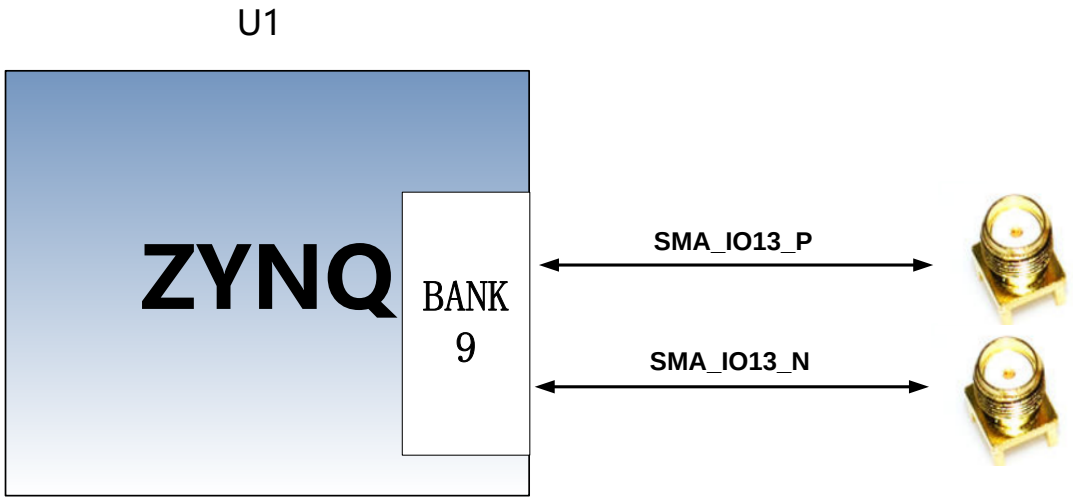


Figure 21: Schematic diagram of SMA connection

ZYNQ pin assignment for SMA interface:

Signal name	ZYNQ pin name	ZYNQ pin number	Remark
SMA_IO13_P	IO_L13P_T2_MRCC_9	AA18	SMA Interface Input 1
SMA_IO13_N	IO_L13N_T2_MRCC_9	AA19	SMA Interface Input 2

Table 22: Pin assignment for SMA interface

Part 16: JTAG Debugging interface

A JTAG interface is reserved on the AX7450B board to download the ZYNQ program or the curing program to FLASH. In order to avoid the damage to the ZYNQ chip caused by hot plug, we add a protection diode on the JTAG signal to ensure that the voltage of the signal is within the range accepted by the FPGA, so as to avoid the damage to the ZYNQ chip.

The following figure is the physical picture of the JTAG interface on the base board. The user can connect the PC and JTAG interface through the USB downloader provided by us to debug the system of ZYNQ. Be careful not to plug and unplug the JTAG cable.

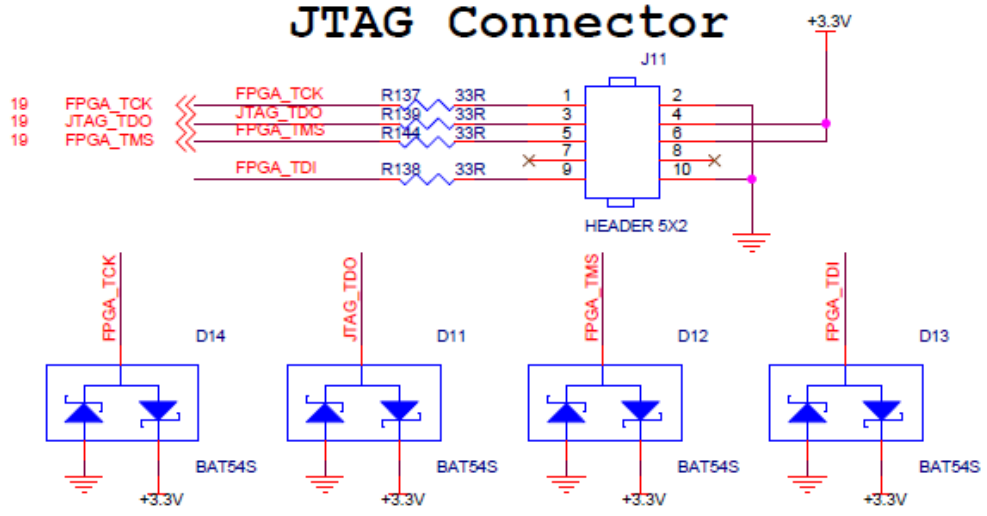


Figure 22: JTAG Interface Section of the Schematic

Part 17: Dip switch Configuration

There is a 2-bit dial switch SW1 on the development board to configure the boot mode of the ZYNQ system. The AX7450B system development platform supports three boot modes. The three boot modes are JTAG debug mode, QSPI FLASH and SD card boot mode. After the XC7Z100 chip is powered on, it will detect the level of the response MIO ports (MIO5 and MIO4) to determine the startup mode. The user can select different starting modes through the dial switch SW1 on the core board. The SW1 startup mode configuration is shown in Table 23 below.

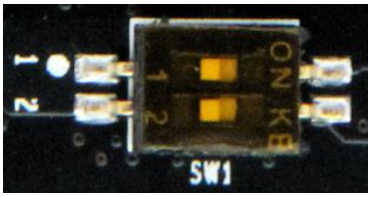
SW1	Dial position (1,2)	MIO5, MIO4 level	Start mode
	ON、ON	0、0	JTAG
	OFF、OFF	1、1	SD card
	OFF、ON	1、0	QSPI FLASH

Table 23: SW1 Startup Mode Configuration

Part 18: Power source

The power input voltage of the development board is DC12V, and the external + 12V power supply or PCIe supplies power to the board. Please use the power supply of the development board when supplying power from the external power supply. Do not use the power supply of other specifications to avoid damaging the development board. The + 12V input power supply generates the ZYNQ core power supply of + 1.0V through the DCDC power supply chip MYMGK1R820ERSR. In addition, +12V generates +5V, +3.3V, +1.8V, MGTAVTT, VADJ and VIO_B through DC/DC power supply chip ETA1471FT2G. Power chip ETA8156FT2G generates +1.5V and MGTAVCC power supplies.

The schematic diagram of the power supply design on the board is shown in Figure 23 below:

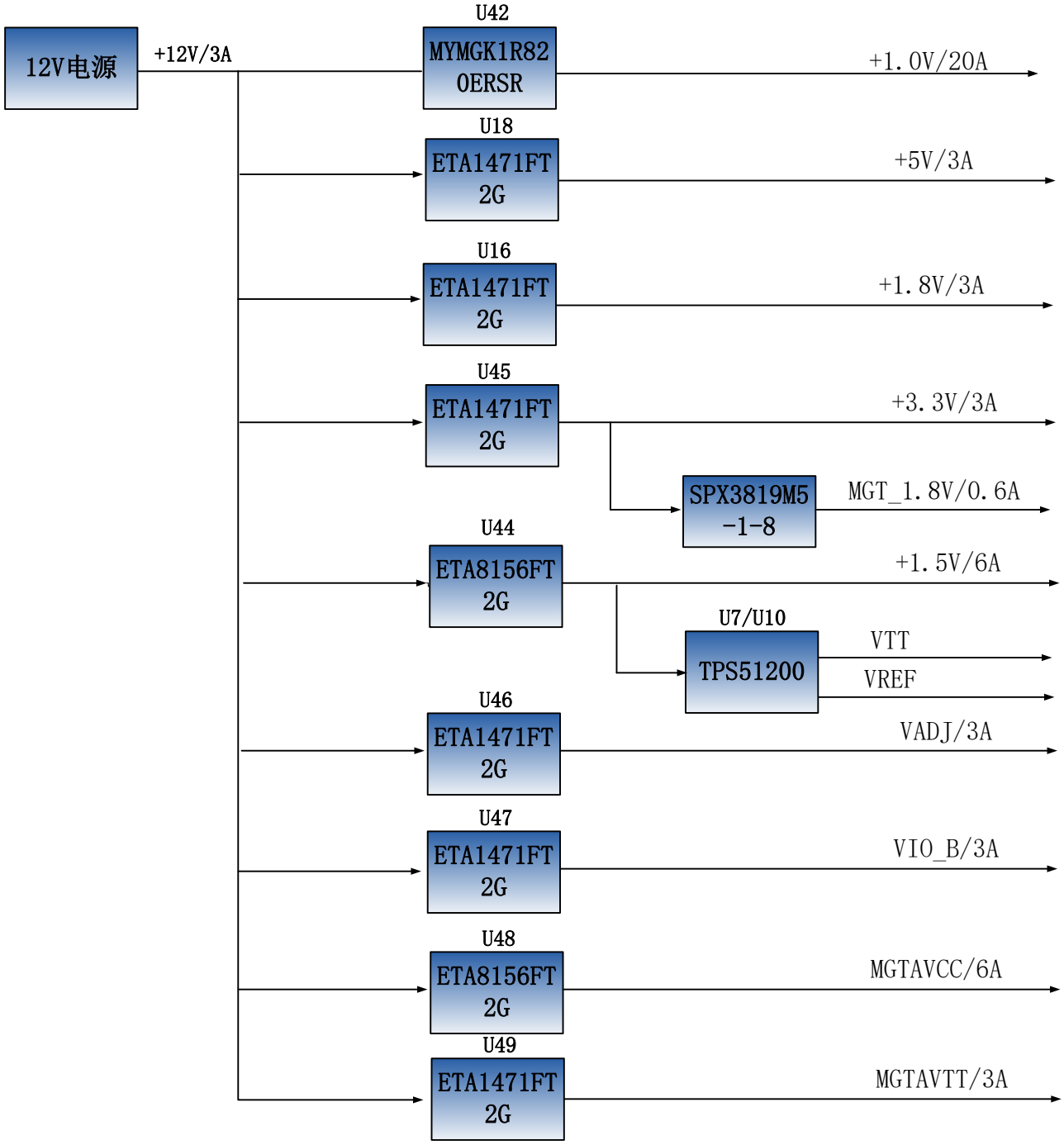


Figure 23: Power Interface Part in the Schematic Diagram

The function of each power distribution is shown in the following table:

Power source	Function
+1.0V	Core voltage of ZYNQ PS and PL sections
+1.8V	ZYNQ PS and PL part auxiliary voltage, BANK501 IO voltage, eMMC, HDMI
+3.3V	ZYNQ Bank0, Bank500, QSIP FLASH, Clock crystal, SD card, SFP optical module
+1.5V	DDR3, ZYNQ Bank501, Bank33,Bank34，Bank35
VADJ	ZYNQ Bank10, Bank11, Bank12, FMC
VIO_B	ZYNQ Bank13, FMC
VREF, VTT（+0.75V）	PS DDR3，PL DDR3

MGTAVCC(+1.0V)	ZYNQ Bank109,110，111, Bank112
MGTAVTT(+1.2V)	ZYNQ Bank109,110，111, Bank112

Table 24: function of each power distribution

Because the power supply of ZYNQ FPGA has the requirement of power-on sequence, in the circuit design, we have designed according to the power supply requirements of the chip, the power-on sequence is +1.0V-> +1.8V-> (+1.5V, +3.3V, VCCIO) circuit design to ensure the normal operation of the chip.

Part 19: Fan

Because the ZYNQ7100 generates a lot of heat when it works properly, we added a heat sink and fan to the board to prevent the chip from overheating. The fan is controlled by the ZYNQ chip. The control pin is connected to the IO of BANK11. If the IO level output is high, the MOSFET is turned on and the fan works. If the IO level output is low, the fan stops. The fan design on the board is shown in Figure 24 below:

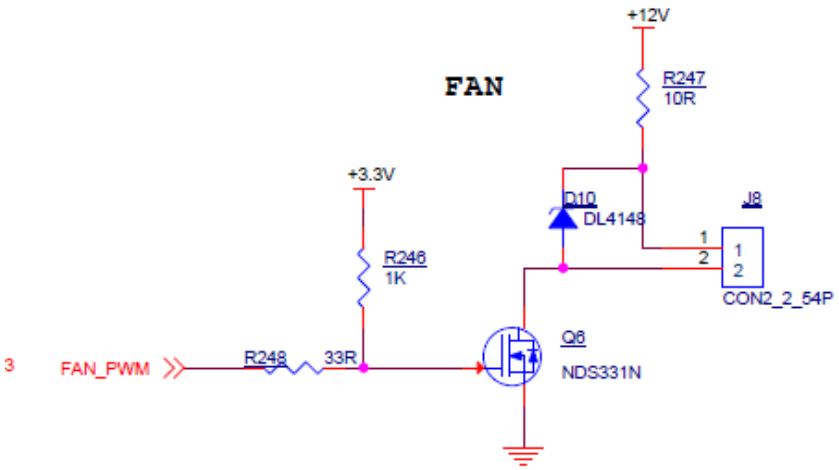


Figure 24: Fan design in the schematic diagram of the development board

The fan has been fixed on the development board with screws before leaving the factory. The power supply of the fan is connected to the socket of J8. The red one is the positive pole and the black one is the negative pole.

Part 20: Structure Size Figure

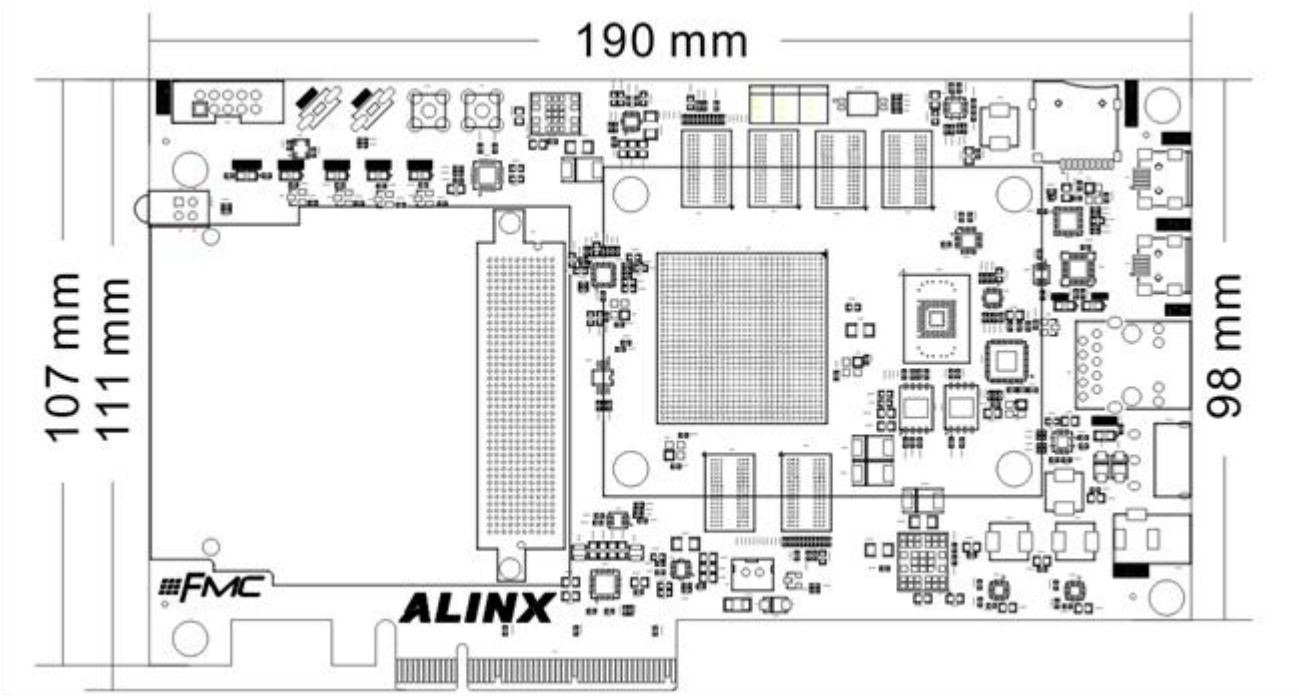


Figure 25: Front View (Top View)