ARTIX-7 FPGA

Development Board

AX7A200B

User Manual

REV 1.0

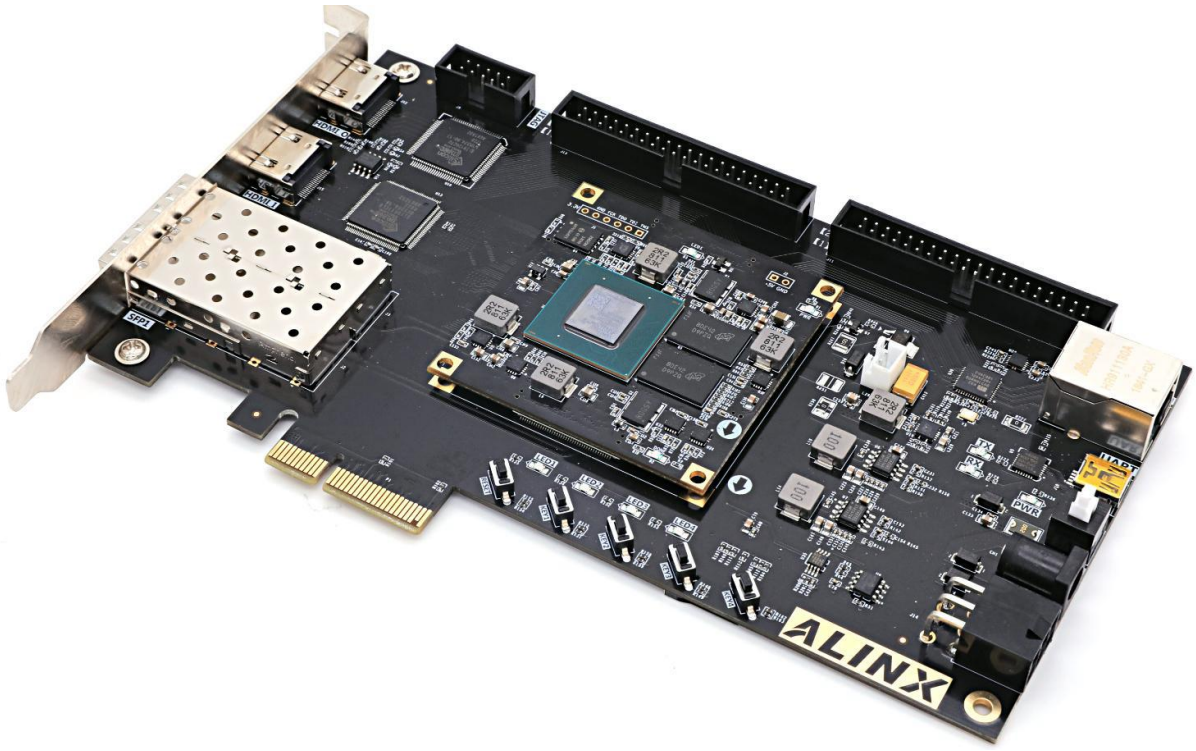
ALINX

Table of Content

1. AX7A200B Introduction 4
2. FPGA Core Board 7
2.1 Introduction 7
2.2 FPGA Chip 9
2.3 Active Differential Crystal 10
2.4 DDR3 12
2.5 QSPI Flash 15
2.6 LED 16
2.7 JTAG Interface 17
2.8 Power Interface 18
2.9 Expansion Ports 18
2.10 Power Supply 25
2.11 Size Dimension 28
3. Carrier Board 29
3.1 Introduction 29
3.2 Gigabit Ethernet Interface 30
3.3 SFP Interface 32
3.4 PCIe x4 Interface 33
3.5 HDMI Output Interface 35
3.6 HDMI Input Interface 37
3.7 SD Card Slot 38
3.8 USB-to-serial Port 39
3.9 EEPROM 24LC04 41
3.10 Temperature Sensor 41
3.11 Expansion Port 42
3.12 JTAG Interface 45
3.13 Keys 46
3.14 LED 47
3.15 Power Supply 48
3.16 Fan Interface (Reserved) 49
3.17 Carrier Board Size Dimension 50

This ARTIX-7 FPGA development platform AX7A200B adopts the core board + carrier board mode, which is convenient for users to use the core board for secondary development.

In the design of carrier board, we have extended a wealth of interfaces for users, such as 1 PCIex2 interface, 2 SFP interfaces, 1 HDMI output interface, 1 HDMI Input interface, 1 Gigabit Ethernet interface, Uart interface, SD card slot etc. It meets user's requirements for PCIe high-speed data transmission, video image processing and industrial control. It is a "Versatile" ARTIX-7 FPGA development platform. It provides the possibility for high-speed video transmission, pre-validation and post-application of network, fiber and PCIe communication and data processing. This product is very suitable for students, engineers and other groups engaged in ARTIX-7 FPGA development



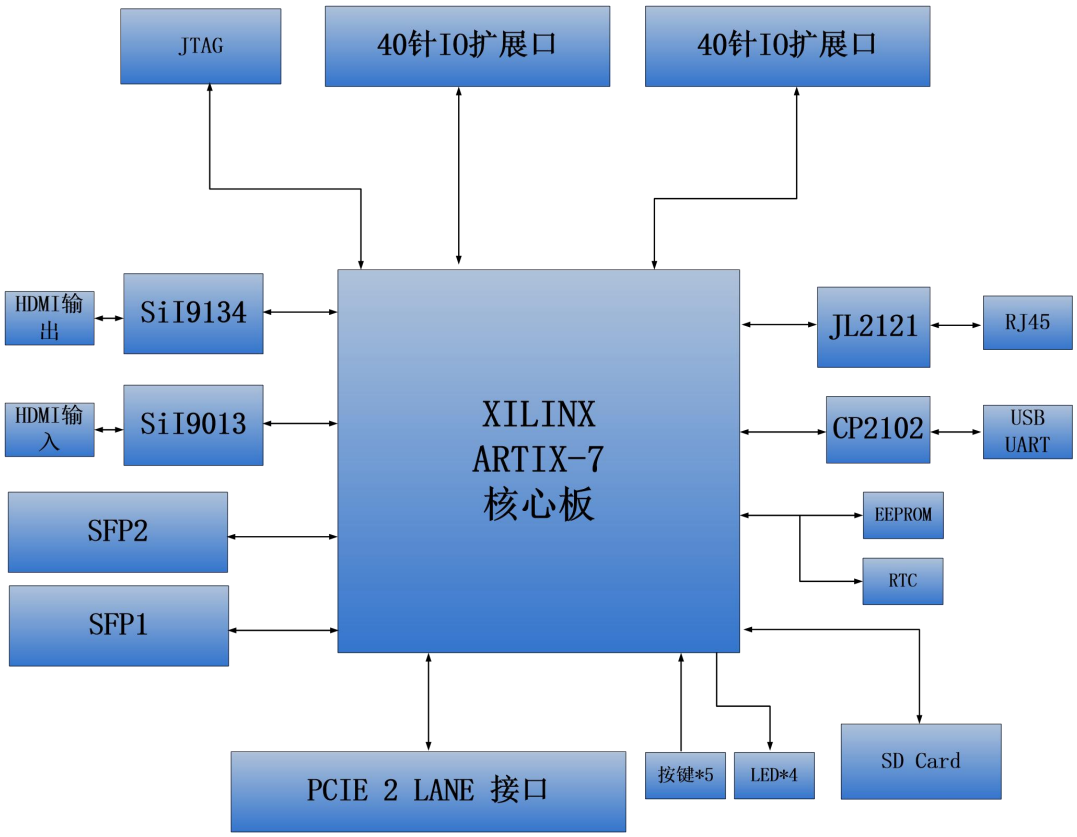
1. AX7A200B Introduction

The entire structure of the AX7A200 FPGA development board is inherited from our consistent core board + carrier board model. High-speed inter-board connectors are used to connect the core board and the carrier board.

The core board is mainly composed of FPGA + 2 DDR3 + QSPI FLASH, which undertakes the functions of high-speed data processing and storage of FPGA, high-speed data reading and writing between FPGA and two DDR3s, data bit width is 32 bits, and the bandwidth of the whole system is up to 25Gb/s (800M*32bit); The two DDR3 capacities are up to 8Gbit, which meets the need for high buffers during data processing. The selected FPGA is the XC7A200T chip of XILINX's ARTIX-7 series, in BGA 484 package. The communication clock frequency between the XC7A200T and DDR3 reaches 400Mhz and the data rate is 800Mhz, which fully meets the needs of high-speed multi-channel data processing. In addition, the XC7A200T FPGA features four GTP high-speed transceivers with speeds up to 6.6Gb/s per channel, making it ideal for fiber-optic communications and PCIe data communications.

The AX7A200B carrier board has rich peripheral interfaces, including 1 PCIex2 interface, 2 SFP interfaces, 1 HDMI output interface, 1 HDMI input interface, 1 Uart interface, 1 Gigabit Ethernet interface,1 SD card slot, 2-way 40-pin expansion header, some buttons, LED and EEPROM circuit.

The following is the structure diagram of the whole development system:



Through this diagram, you can see the interfaces and functions that the AX7A200B FPGA Development Board contains:

- Artix-7 FPGA Core Board

The core board consists of XC7A200T + 8Gb DDR3 + 128Mb QSPI FLASH. There are two high-precision Sitime LVDS differential crystals, one at 200MHz and the other at 125MHz, providing stable clock input for FPGA systems and GTP modules.

- 1 PCIe x2 Interface

Supports PCI Express 2.0 standard, provides PCIex2 high-speed data transmission interface, single channel communication rate up to 5Gbaud.

- 2 High-speed SFP Interfaces

The two high-speed transceivers of the GTP transceiver of ARTIX-7 FPGA are connected to the transmission and reception of two optical modules to realize 2-channel high-speed optical fiber communication interfaces. Each fiber optic data communication receives and transmits at speeds up to 6.6 Gb/s.

- 1 Gigabit Ethernet Interface RJ-45 Interface

Gigabit Ethernet interface chip adopts JL2121 industrial grade GPHY chip

from JL Semiconductor company. The JL2121 chip supports 10/100/1000 Mbps network transmission rate; supports full duplex and self-adaptive.

- 1 HDMI Output Interface

  Silion Image's SIL9134 HDMI encoding chip is selected to support up to 1080P@60Hz output and support 3D output.

- 1 HDMI Input Interface

  Silion Image's SIL9011/SIL9013 HDMI decoder chip is selected, which supports up to 1080P@60Hz input and supports data output in different formats.

- 1 USB-to-Uart Interface

  1-channel USB-to-Uart interface for communication with the computer for user debugging. The serial port chip is the USB-UAR chip of Silicon Labs CP2102GM, and the USB interface is the MINI USB interface.

- Micro SD Card Holder

  Supports SD mode and SPI mode.

- EEPROM

  EEPROM 24LC04 with an on-board IIC interface;

- 2-channel 40-pin Expansion Ports

  Reserve two 40-pin 2.54mm pitch expansion ports, which can be connected to various Alinx modules, such as binocular camera, TFT LCD screen, high-speed AD module, etc. The expansion ports contain one 5V power supply, two 3.3V power supplies, three ground power supplies, and 34 I/O ports.

- JTAG Port

  10-pin 2.54mm standard JTAG port for FPGA program downloading and debugging;

- Keys

  Four user keys and one reset key;

- LEDs

  5 user LEDs (1 on the core board and 4 on the carrier board)

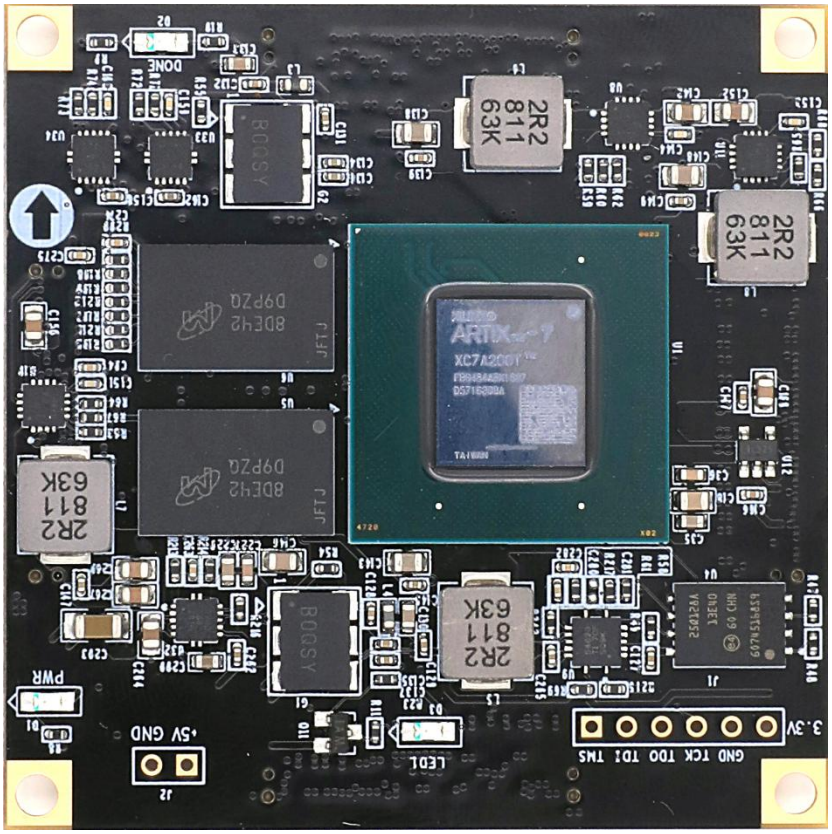
2. FPGA Core Board

2.1 Introduction

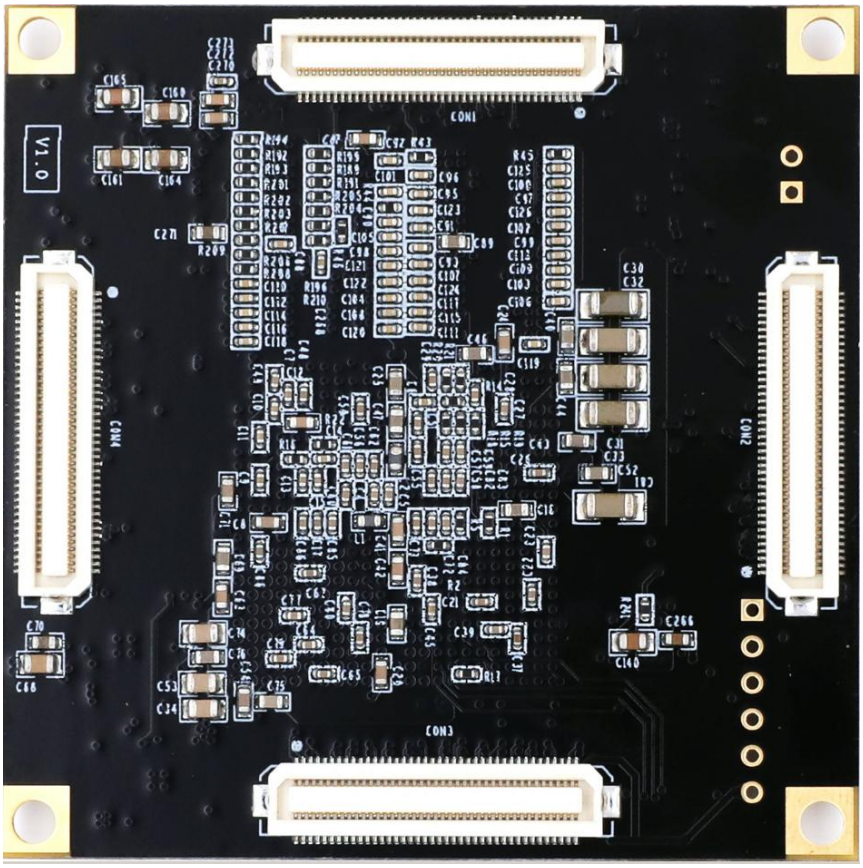
AC7A200 (core board model, the same below) FPGA core board is based on XILINX's ARTIX-7 series 100T XC7A200T-2FBG484I. It is a high-performance core board with high speed, high bandwidth and high capacity. It is suitable for high-speed data communication, video image processing, high-speed data acquisition etc.

This AC7A200 core board uses two pieces of MICRON's MT41J256M16HA-125 DDR3 chip, each DDR has a capacity of 4Gbit; two DDR chips form a 32-bit data bus width, and the read/write data bandwidth between FPGA and DDR3 is up to 25Gb; such configuration can meet the needs of high bandwidth data processing.

The AC7A200 core board expands 180 standard IO ports with 3.3V level, 15 standard IO ports with 1.5V level, and 4 pairs of GTP high speed RX/TX differential signals. For users who need a lot of IO, this core board will be a good choice. Moreover, lines between the FPGA chip and the interface are processed in equal length and differential length, and the core board size is only 2.36 inch *2.36 inch, which is very suitable for secondary development.



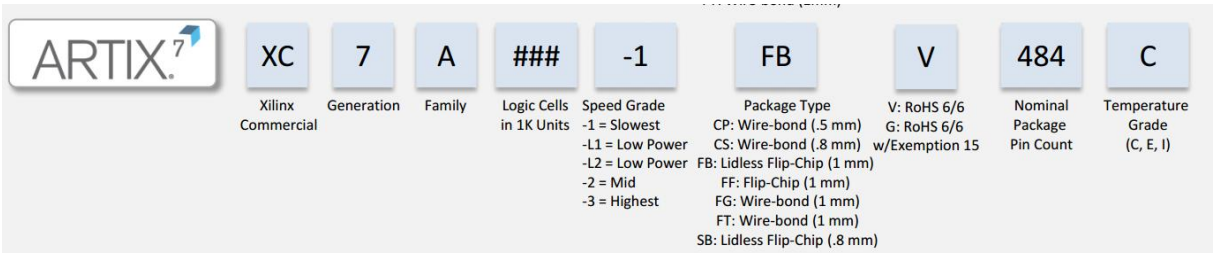
AC7A200 Front View



AC7A200 Back view

2.2 FPGA Chip

As mentioned before, the FPGA model used is XC7A200T-2FBG484I, which belongs to Xilinx Company's Artix-7 series, with speed grade 2 and temperature grade of industrial grade. This model is in FBG484 package with 484 pins. The chip naming rules of Xilinx ARTIX-7 FPGA are as follows:



The main parameters of the FPGA chip XC7A200T are as follows:

Name	Parameters
Logic Cells	215360
Slices	33650
CLB flip-flops	269200
Block RAM（kb)	13140
DSP Slices	740
PCIe Gen2	1
XADC	12bit, 1Mbps AD
GTP Transceiver	4 个，6.6Gb/s max
Speed Grade	-2
Temperature Grade	Industrial grade

FPGA power supply system

Artix-7 FPGA power supplies are V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, V_{CCO}, $V_{MGTAVCC}$ and $V_{MGTAVTT}$. V_{CCINT} is the FPGA core power supply pin, which needs to be connected to 1.0V; V_{CCBRAM} is the power supply pin of FPGA Block RAM, should be connected to 1.0V; V_{CCAUX} is FPGA auxiliary power supply pin, should be connected to 1.8V; V_{CCO} is the voltage of each BANK of FPGA, including BANK0, BANK13~16, BANK34~35. On AC7A200 FPGA core board, the voltage of BANK34 and BANK35 is 1.5V because they need to be connected to DDR3 and

the voltage of other BANKs is 3.3V. The V_{CCO} of BANK15 and BANK16 is powered by the LDO, and can be changed by replacing the LDO chip. $V_{MGTAVCC}$ is the supply voltage of the FPGA internal GTP transceiver, connected to 1.0V; $V_{MGTAVTT}$ is the termination voltage of the GTP transceiver, connected to 1.2V.

The Artix-7 FPGA system requires that the power-up sequence be V_{CCINT}→ V_{CCBRAM}→V_{CCAUX}→V_{CCO}. If V_{CCINT} and V_{CCBRAM} have the same voltage, they can be powered up at the same time. The power-off sequence is reversed. The power-up sequence of the GTP transceiver is V_{CCINT}→$V_{MGTAVCC}$→$V_{MGTAVTT}$. If V_{CCINT} and $V_{MGTAVCC}$ have the same voltage, they can be powered up at the same time. The power-off sequence is just the opposite of the power-on sequence

2.3 Active Differential Crystal

The AC7A200 core board is equipped with two Sitime active differential crystals, one is 200MHz, the model is SiT9102-200.00MHz, for the FPGA system master clock and for generating DDR3 control clock; the other is 125MHz, model is SiT9102 -125MHz, for reference clock input of GTP transceivers.

2.3.1 200Mhz deferential clock

G1 in Figure 2-3-1 is the 200M active differential crystal that provides the development board system clock source. The crystal output is connected to the BANK34 global clock pin MRCC (R4 and T4) of the FPGA. This 200Mhz differential clock can be used to drive the user logic in the FPGA. Users can configure the PLLs and DCMs inside the FPGA to generate clocks of different frequencies.

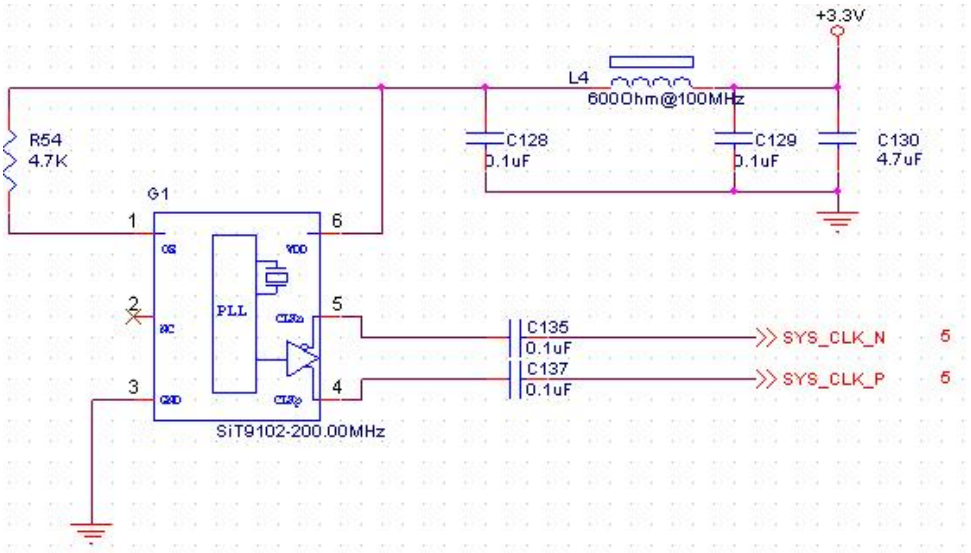


Figure 2-3-1: 200Mhz Active Differential Crystal Schematic

Clock Pin Assignment:

Signal Name	FPGA Pin
SYS_CLK_P	R4
SYS_CLK_N	T4

2.3.2 125Mhz deferential clock

G2 in Figure 2-3-2 is the 125MHz active differential crystal, which is the reference input clock provided to the GTP module inside the FPGA. The crystal output is connected to the GTP BANK216 clock pins MGTREFCLK0P (F6) and MGTREFCLK0N (E6) of the FPGA.

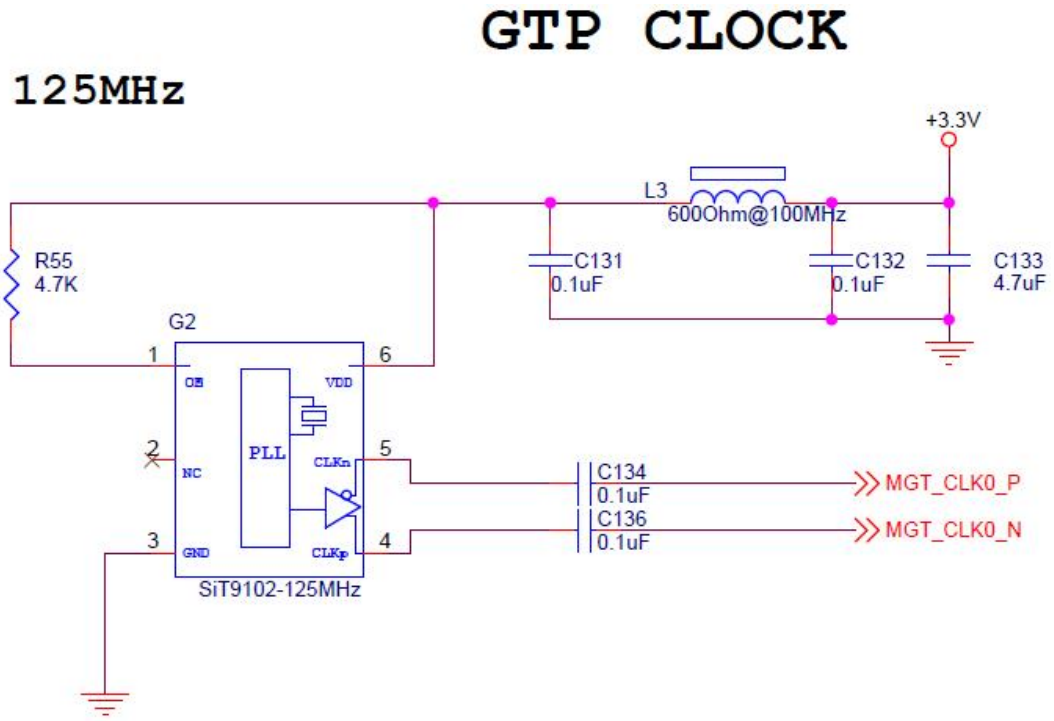


Figure 2-3-2: 125Mhz Active Differential Crystal Schematic

Clock Pin Assignment:

Signal Name	FPGA Pin
MGT_CLK0_P	F6
MGT_CLK0_N	E6

2.4 DDR3

The FPGA core board AC7A200 is equipped with two Micron 4Gbit (512MB) DDR3 chips (8Gbit in total), model is MT41J256M16HA-125 (compatible with MT41K256M16HA-125). The total bus width of DDR is 32bit. The DDR3 SDRAM has a maximum operating speed of 400MHz (data rate 800Mbps). The DDR3 memory system is directly connected to the memory interfaces of the BANK 34 and BANK35 of the FPGA. The specific configuration of DDR3 SDRAM is shown in Table 2-4-1.

Bit Number	Model	Capacity	Manufacturer
U5,U6	MT41J256M16HA-125	256M x 16bit	micron

Table 2-4-1: DDR3 SDRAM Configuration

The hardware design of DDR3 requires strict consideration of signal integrity. We have fully considered the matching resistor/terminal resistance, line impedance control, and line length control in circuit design and PCB design to ensure high-speed and stable operation of DDR3. Figure 2-4-1 details the hardware connection of DDR3 DRAM

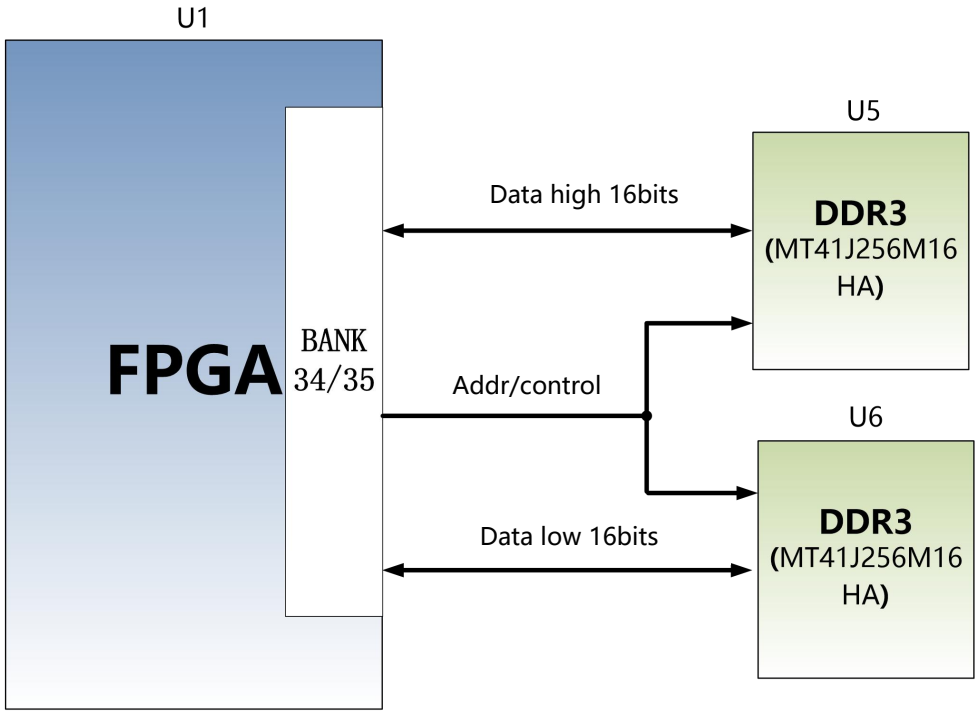


Figure 2-4-1: The DDR3 DRAM Schematic

DDR3 DRAM Pin Assignment:

Signal Name	FPGA Pin Name	FPGA Pin No.
DDR3_DQS0_P	IO_L3P_T0_DQS_AD5P_35	E1
DDR3_DQS0_N	IO_L3N_T0_DQS_AD5N_35	D1
DDR3_DQS1_P	IO_L9P_T1_DQS_AD7P_35	K2
DDR3_DQS1_N	IO_L9N_T1_DQS_AD7N_35	J2
DDR3_DQS2_P	IO_L15P_T2_DQS_35	M1
DDR3_DQS2_N	IO_L15N_T2_DQS_35	L1
DDR3_DQS3_P	IO_L21P_T3_DQS_35	P5
DDR3_DQS3_N	IO_L21N_T3_DQS_35	P4
DDR3_DQ[0]	IO_L2P_T0_AD12P_35	C2
DDR3_DQ [1]	IO_L5P_T0_AD13P_35	G1
DDR3_DQ [2]	IO_L1N_T0_AD4N_35	A1
DDR3_DQ [3]	IO_L6P_T0_35	F3
DDR3_DQ [4]	IO_L2N_T0_AD12N_35	B2
DDR3_DQ [5]	IO_L5N_T0_AD13N_35	F1
DDR3_DQ [6]	IO_L1P_T0_AD4P_35	B1
DDR3_DQ [7]	IO_L4P_T0_35	E2
DDR3_DQ [8]	IO_L11P_T1_SRCC_35	H3
DDR3_DQ [9]	IO_L11N_T1_SRCC_35	G3
DDR3_DQ [10]	IO_L8P_T1_AD14P_35	H2
DDR3_DQ [11]	IO_L10N_T1_AD15N_35	H5
DDR3_DQ [12]	IO_L7N_T1_AD6N_35	J1
DDR3_DQ [13]	IO_L10P_T1_AD15P_35	J5
DDR3_DQ [14]	IO_L7P_T1_AD6P_35	K1
DDR3_DQ [15]	IO_L12P_T1_MRCC_35	H4
DDR3_DQ [16]	IO_L18N_T2_35	L4
DDR3_DQ [17]	IO_L16P_T2_35	M3
DDR3_DQ [18]	IO_L14P_T2_SRCC_35	L3
DDR3_DQ [19]	IO_L17N_T2_35	J6
DDR3_DQ [20]	IO_L14N_T2_SRCC_35	K3

DDR3_DQ [21]	IO_L17P_T2_35	K6
DDR3_DQ [22]	IO_L13N_T2_MRCC_35	J4
DDR3_DQ [23]	IO_L18P_T2_35	L5
DDR3_DQ [24]	IO_L20N_T3_35	P1
DDR3_DQ [25]	IO_L19P_T3_35	N4
DDR3_DQ [26]	IO_L20P_T3_35	R1
DDR3_DQ [27]	IO_L22N_T3_35	N2
DDR3_DQ [28]	IO_L23P_T3_35	M6
DDR3_DQ [29]	IO_L24N_T3_35	N5
DDR3_DQ [30]	IO_L24P_T3_35	P6
DDR3_DQ [31]	IO_L22P_T3_35	P2
DDR3_DM0	IO_L4N_T0_35	D2
DDR3_DM1	IO_L8N_T1_AD14N_35	G2
DDR3_DM2	IO_L16N_T2_35	M2
DDR3_DM3	IO_L23N_T3_35	M5
DDR3_A[0]	IO_L11N_T1_SRCC_34	AA4
DDR3_A[1]	IO_L8N_T1_34	AB2
DDR3_A[2]	IO_L10P_T1_34	AA5
DDR3_A[3]	IO_L10N_T1_34	AB5
DDR3_A[4]	IO_L7N_T1_34	AB1
DDR3_A[5]	IO_L6P_T0_34	U3
DDR3_A[6]	IO_L5P_T0_34	W1
DDR3_A[7]	IO_L1P_T0_34	T1
DDR3_A[8]	IO_L2N_T0_34	V2
DDR3_A[9]	IO_L2P_T0_34	U2
DDR3_A[10]	IO_L5N_T0_34	Y1
DDR3_A[11]	IO_L4P_T0_34	W2
DDR3_A[12]	IO_L4N_T0_34	Y2
DDR3_A[13]	IO_L1N_T0_34	U1
DDR3_A[14]	IO_L6N_T0_VREF_34	V3
DDR3_BA[0]	IO_L9N_T1_DQS_34	AA3

DDR3_BA[1]	IO_L9P_T1_DQS_34	Y3
DDR3_BA[2]	IO_L11P_T1_SRCC_34	Y4
DDR3_S0	IO_L8P_T1_34	AB3
DDR3_RAS	IO_L12P_T1_MRCC_34	V4
DDR3_CAS	IO_L12N_T1_MRCC_34	W4
DDR3_WE	IO_L7P_T1_34	AA1
DDR3_ODT	IO_L14N_T2_SRCC_34	U5
DDR3_RESET	IO_L15P_T2_DQS_34	W6
DDR3_CLK_P	IO_L3P_T0_DQS_34	R3
DDR3_CLK_N	IO_L3N_T0_DQS_34	R2
DDR3_CKE	IO_L14P_T2_SRCC_34	T5

2.5 QSPI Flash

The FPGA core board is equipped with one 128Mbit QSPI FLASH, and the model is N25Q128, which uses the 3.3V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, it can be used as a boot device for the system to store the boot image of the system. These images mainly include FPGA bit files, ARM application code, soft-core application code and other user data files. The specific models and related parameters of SPI FLASH are shown in Table 2-5-1.

Bit Number	Model	Capacity	Manufacturer
U8	N25Q128	128M Bit	Numonyx

Table 2-5-1: Model and parameters of QSPI FLASH

QSPI FLASH is connected to the dedicated pins of BANK0 and BANK14 of the FPGA chip, of which the clock pin is connected to CCLK0 of BANK0, and other data and chip-selected signals are connected to D00~D03 and FCS pins of BANK14 respectively. Figure 2-5-1 shows the hardware connection of QSPI Flash.

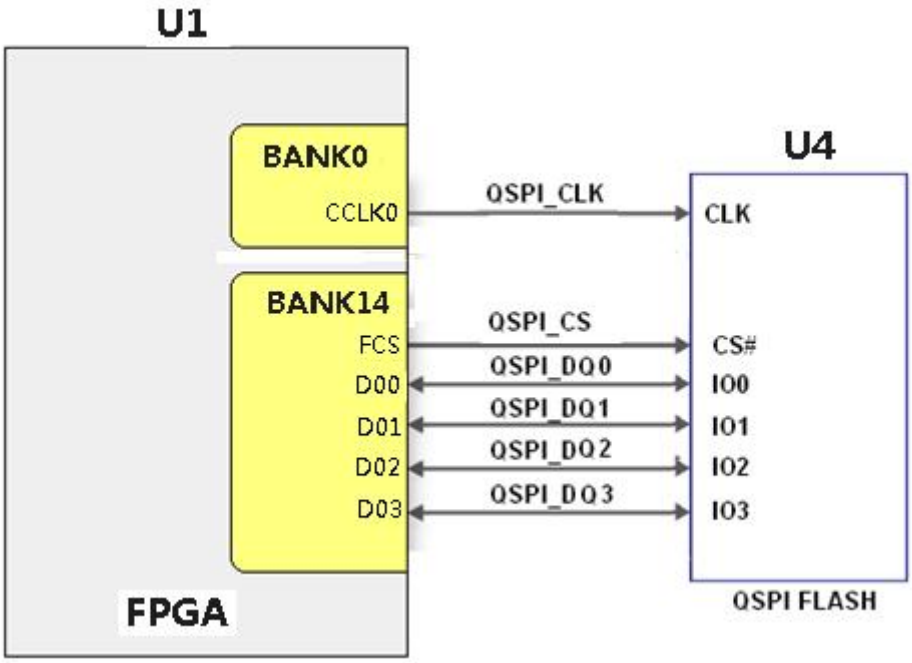


Figure 2-5-1: QSPI Flash connection diagram

Configuration chip pin assignment:

Signal Name	FPGA Pin Name	FPGA Pin No.
QSPI_CLK	CCLK_0	L12
QSPI_CS	IO_L6P_T0_FCS_B_14	T19
QSPI_DQ0	IO_L1P_T0_D00_MOSI_14	P22
QSPI_DQ1	IO_L1N_T0_D01_DIN_14	R22
QSPI_DQ2	IO_L2P_T0_D02_14	P21
QSPI_DQ3	IO_L2N_T0_D03_14	R21

2.6 LED

There are 3 red LED lights on the AC7A200 FPGA core board, one of which is the power indicator light (PWR), one is the configuration LED light (DONE), and one is the user LED light. When the core board is powered, the power indicator will light up; when the FPGA is programmed, the configuration LED will light up. The user LED light is connected to the IO of the BANK34, users can control the light on and off by the program. When the IO voltage connected to the user LED is high, the user LED will light up. When the IO voltage connected is low, the

user LED will be off. The schematic diagram of the LED light hardware connection is shown in Figure 2-6-1:

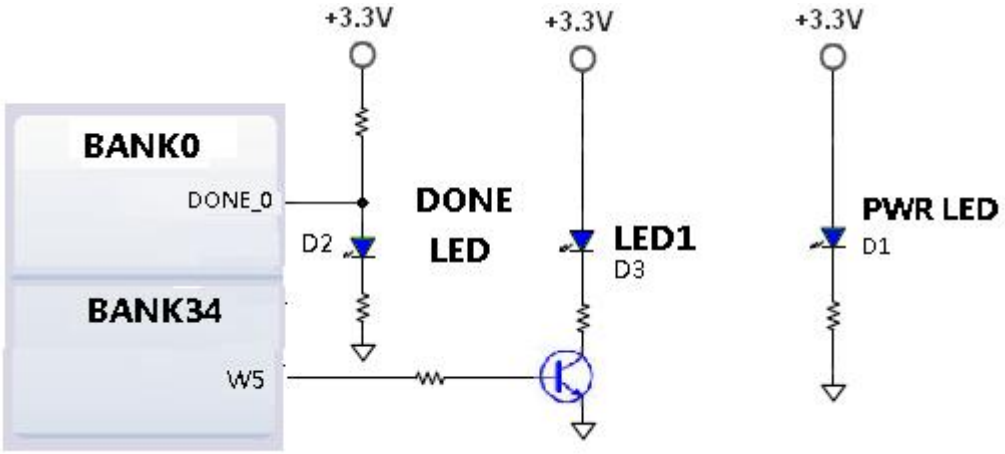


Figure 2-6-1: Hardware connection of LEDs on the Core Board

User LEDs Pin Assignment:

Signal Name	FPGA Pin Name	FPGA Pin No.	Remark
LED1	IO_L15N_T2_DQS_34	W5	User LED light

2.7 JTAG Interface

The JTAG test socket J1 is reserved on the AC7A200 core board for JTAG downloading and debugging when the core board is used alone. Figure 2-7-1 is the schematic of the JTAG interface, which involves six signals: TMS, TDI, TDO, TCK, GND and +3.3V.

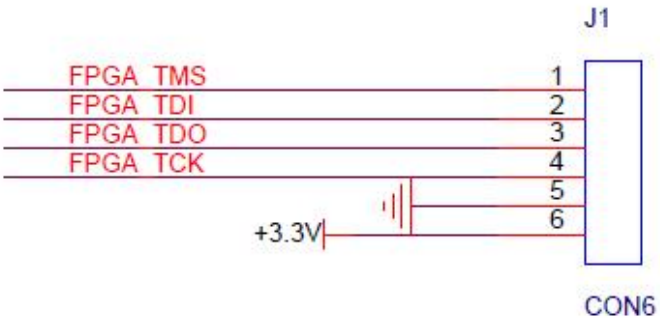


Figure 2-7-1: JTAG Interface Schematic

The JTAG interface J1 on core board uses a 6-pin 2.54mm pitch single-row test hole. If the user needs to use JTAG connection and debugging on the core

board, a single row of 6-pin pins needs to be welded.

2.8 Power Interface

In order to enable the core board to work independently, we reserve a 2-Pin power interface J2 for the core board. If you want to debug the function of the core board independently (without the carrier board), you need to provide +5V externally to power the core board.

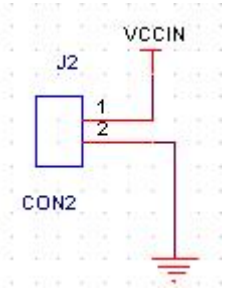


Figure 2-8-1: Power Interface schematic

2.9 Expansion Ports

A total of four high-speed expansion ports are extended on the back of the core board, using four 80Pin inter-board connectors to connect to carrier board, the connectors use Panasonic AXK580137YG, the model of the connector correspond to the carrier board is AXK680337YG. The I/O ports of the FPGA are connected to the four expansion ports through differential wiring. The PIN spacing of connectors is 0.5mm, which can realize high-speed data communication configured with the female connectors on the carrier board.

Expansion port CON1

The 80-Pin connector CON1 is used to connect the VCCIN power supply (+5V) of the carrier board, the ground power supply and the normal IOs of the FPGA. It should be noted here that 15 pins of the CON1 are connected to the IO port of the BANK34, because the BANK34 connection is connected to the DDR3. Therefore, the voltage standard of all IOs of this BANK34 is 1.5V. Pin assignment of the CON1 expansion port is shown in Table 2-9-1:

Table 2-9-1: Pin Assignment of Expansion Port CON1

CON1 Pin	Signal Name	FPGA Pin No.	Level Standard	CON1 Pin	Signal Name	FPGA Pin No.	Level Standard
PIN1	VCCIN	-	+5V	PIN2	VCCIN	-	+5V
PIN3	VCCIN	-	+5V	PIN4	VCCIN	-	+5V
PIN5	VCCIN	-	+5V	PIN6	VCCIN	-	+5V
PIN7	VCCIN	-	+5V	PIN8	VCCIN	-	+5V
PIN9	GND	-	GND	PIN10	GND	-	GND
PIN11	NC	-	-	PIN12	NC	-	-
PIN13	NC	-	-	PIN14	NC	-	-
PIN15	NC	-	-	PIN16	B13_L4_P	AA15	3.3V
PIN17	NC	-	-	PIN18	B13_L4_N	AB15	3.3V
PIN19	GND	-	GND	PIN20	GND	-	GND
PIN21	B13_L5_P	Y13	3.3V	PIN22	B13_L1_P	Y16	3.3V
PIN23	B13_L5_N	AA14	3.3V	PIN24	B13_L1_N	AA16	3.3V
PIN25	B13_L7_P	AB11	3.3V	PIN26	B13_L2_P	AB16	3.3V
PIN27	B13_L7_N	AB12	3.3V	PIN28	B13_L2_N	AB17	3.3V
PIN29	GND	-	GND	PIN30	GND	-	GND
PIN31	B13_L3_P	AA13	3.3V	PIN32	B13_L6_P	W14	3.3V
PIN33	B13_L3_N	AB13	3.3V	PIN34	B13_L6_N	Y14	3.3V
PIN35	B34_L23_P	Y8	1.5V	PIN36	B34_L20_P	AB7	1.5V
PIN37	B34_L23_N	Y7	1.5V	PIN38	B34_L20_N	AB6	1.5V
PIN39	GND	-	GND	PIN40	GND	-	GND
PIN41	B34_L18_N	AA6	1.5V	PIN42	B34_L21_N	V8	1.5V
PIN43	B34_L18_P	Y6	1.5V	PIN44	B34_L21_P	V9	1.5V
PIN45	B34_L19_P	V7	1.5V	PIN46	B34_L22_P	AA8	1.5V
PIN47	B34_L19_N	W7	1.5V	PIN48	B34_L22_N	AB8	1.5V
PIN49	GND	-	GND	PIN50	GND	-	GND
PIN51	XADC_VN	M9	Analog	PIN52	NC		
PIN53	XADC_VP	L10	Analog	PIN54	B34_L25	U7	1.5V
PIN55	NC	-	-	PIN56	B34_L24_P	W9	1.5V

PIN57	NC	-	-	PIN58	B34_L24_N	Y9	1.5V
PIN59	GND	-	GND	PIN60	GND	-	GND
PIN61	B16_L1_N	F14	3.3V	PIN62	NC	-	-
PIN63	B16_L1_P	F13	3.3V	PIN64	NC	-	-
PIN65	B16_L4_N	E14	3.3V	PIN66	NC	-	-
PIN67	B16_L4_P	E13	3.3V	PIN68	NC	-	-
PIN69	GND	-	GND	PIN70	GND	-	GND
PIN71	B16_L6_N	D15	3.3V	PIN72	NC	-	-
PIN73	B16_L6_P	D14	3.3V	PIN74	NC	-	-
PIN75	B16_L8_P	C13	3.3V	PIN76	NC	-	-
PIN77	B16_L8_N	B13	3.3V	PIN78	NC	-	-
PIN79	NC	-	-	PIN80	NC	-	-

Expansion port CON2

The 80-pin connector CON2 is used to extend the normal IO of the BANK13 and BANK14 of the FPGA. The voltage standards of both BANKs are 3.3V. Pin assignment of the CON2 expansion port is shown in Table 2-9-2:

Table 2-9-2: Pin Assignment of CON2

CON2 Pin	Signal Name	FPGA Pin No.	Level Standard	CON2 Pin	Signal Name	FPGA Pin No.	Level Standard
PIN1	B13_L16_P	W15	3.3V	PIN2	B14_L16_P	V17	3.3V
PIN3	B13_L16_N	W16	3.3V	PIN4	B14_L16_N	W17	3.3V
PIN5	B13_L15_P	T14	3.3V	PIN6	B13_L14_P	U15	3.3V
PIN7	B13_L15_N	T15	3.3V	PIN8	B13_L14_N	V15	3.3V
PIN9	GND	-	GND	PIN10	GND	-	GND
PIN11	B13_L13_P	V13	3.3V	PIN12	B14_L10_P	AB21	3.3V
PIN13	B13_L13_N	V14	3.3V	PIN14	B14_L10_N	AB22	3.3V
PIN15	B13_L12_P	W11	3.3V	PIN16	B14_L8_N	AA21	3.3V
PIN17	B13_L12_N	W12	3.3V	PIN18	B14_L8_P	AA20	3.3V
PIN19	GND	-	GND	PIN20	GND	-	GND
PIN21	B13_L11_P	Y11	3.3V	PIN22	B14_L15_N	AB20	3.3V

PIN23	B13_L11_N	Y12	3.3V	PIN24	B14_L15_P	AA19	3.3V
PIN25	B13_L10_P	V10	3.3V	PIN26	B14_L17_P	AA18	3.3V
PIN27	B13_L10_N	W10	3.3V	PIN28	B14_L17_N	AB18	3.3V
PIN29	GND	-	GND	PIN30	GND	-	GND
PIN31	B13_L9_N	AA11	3.3V	PIN32	B14_L6_N	T20	3.3V
PIN33	B13_L9_P	AA10	3.3V	PIN34	B13_IO0	Y17	3.3V
PIN35	B13_L8_N	AB10	3.3V	PIN36	B14_L7_N	W22	3.3V
PIN37	B13_L8_P	AA9	3.3V	PIN38	B14_L7_P	W21	3.3V
PIN39	GND	-	GND	PIN40	GND	-	GND
PIN41	B14_L11_N	V20	3.3V	PIN42	B14_L4_P	T21	3.3V
PIN43	B14_L11_P	U20	3.3V	PIN44	B14_L4_N	U21	3.3V
PIN45	B14_L14_N	V19	3.3V	PIN46	B14_L9_P	Y21	3.3V
PIN47	B14_L14_P	V18	3.3V	PIN48	B14_L9_N	Y22	3.3V
PIN49	GND	-	GND	PIN50	GND	-	GND
PIN51	B14_L5_N	R19	3.3V	PIN52	B14_L12_N	W20	3.3V
PIN53	B14_L5_P	P19	3.3V	PIN54	B14_L12_P	W19	3.3V
PIN55	B14_L18_N	U18	3.3V	PIN56	B14_L13_N	Y19	3.3V
PIN57	B14_L18_P	U17	3.3V	PIN58	B14_L13_P	Y18	3.3V
PIN59	GND	-	GND	PIN60	GND	-	GND
PIN61	B13_L17_P	T16	3.3V	PIN62	B14_L3_N	V22	3.3V
PIN63	B13_L17_N	U16	3.3V	PIN64	B14_L3_P	U22	3.3V
PIN65	B14_L21_N	P17	3.3V	PIN66	B14_L20_N	T18	3.3V
PIN67	B14_L21_P	N17	3.3V	PIN68	B14_L20_P	R18	3.3V
PIN69	GND	-	GND	PIN70	GND	-	GND
PIN71	B14_L22_P	P15	3.3V	PIN72	B14_L19_N	R14	3.3V
PIN73	B14_L22_N	R16	3.3V	PIN74	B14_L19_P	P14	3.3V
PIN75	B14_L24_N	R17	3.3V	PIN76	B14_L23_P	N13	3.3V
PIN77	B14_L24_P	P16	3.3V	PIN78	B14_L23_N	N14	3.3V
PIN79	B14_IO0	P20	3.3V	PIN80	B14_IO25	N15	3.3V

Expansion port CON3

The 80-pin connector CON3 is used to extend the normal IO of the BANK15

and BANK16 of the FPGA. In addition, four JTAG signals are also connected to the carrier board via the CON3 connector. The voltage standards of BANK15 and BANK16 can be adjusted by an LDO chip. The default installed LDO is 3.3V, if you want to output other standard levels, you can replace it with a suitable LDO. Pin assignment of the CON3 expansion port is shown in Table 2-9-3:

Table 2-9-3: Pin Assignment of CON3

CON3 Pin	Signal Name	FPGA Pin No.	Level Standard	CON3 Pin	Signal Name	FPGA Pin No.	Level Standard
PIN1	B15_IO0	J16	3.3V	PIN2	B15_IO25	M17	3.3V
PIN3	B16_IO0	F15	3.3V	PIN4	B16_IO25	F21	3.3V
PIN5	B15_L4_P	G17	3.3V	PIN6	B16_L21_N	A21	3.3V
PIN7	B15_L4_N	G18	3.3V	PIN8	B16_L21_P	B21	3.3V
PIN9	GND	-	GND	PIN10	GND	-	GND
PIN11	B15_L2_P	G15	3.3V	PIN12	B16_L23_P	E21	3.3V
PIN13	B15_L2_N	G16	3.3V	PIN14	B16_L23_N	D21	3.3V
PIN15	B15_L12_P	J19	3.3V	PIN16	B16_L22_P	E22	3.3V
PIN17	B15_L12_N	H19	3.3V	PIN18	B16_L22_N	D22	3.3V
PIN19	GND	-	GND	PIN20	GND	-	GND
PIN21	B15_L11_P	J20	3.3V	PIN22	B16_L24_P	G21	3.3V
PIN23	B15_L11_N	J21	3.3V	PIN24	B16_L24_N	G22	3.3V
PIN25	B15_L1_N	G13	3.3V	PIN26	B15_L8_N	G20	3.3V
PIN27	B15_L1_P	H13	3.3V	PIN28	B15_L8_P	H20	3.3V
PIN29	GND	-	GND	PIN30	GND	-	GND
PIN31	B15_L5_P	J15	3.3V	PIN32	B15_L7_N	H22	3.3V
PIN33	B15_L5_N	H15	3.3V	PIN34	B15_L7_P	J22	3.3V
PIN35	B15_L3_N	H14	3.3V	PIN36	B15_L9_P	K21	3.3V
PIN37	B15_L3_P	J14	3.3V	PIN38	B15_L9_N	K22	3.3V
PIN39	GND	-	GND	PIN40	GND	-	GND
PIN41	B15_L19_P	K13	3.3V	PIN42	B15_L15_N	M22	3.3V
PIN43	B15_L19_N	K14	3.3V	PIN44	B15_L15_P	N22	3.3V
PIN45	B15_L20_P	M13	3.3V	PIN46	B15_L6_N	H18	3.3V

PIN47	B15_L20_N	L13	3.3V	PIN48	B15_L6_P	H17	3.3V
PIN49	GND	-	GND	PIN50	GND	-	GND
PIN51	B15_L14_P	L19	3.3V	PIN52	B15_L13_N	K19	3.3V
PIN53	B15_L14_N	L20	3.3V	PIN54	B15_L13_P	K18	3.3V
PIN55	B15_L21_P	K17	3.3V	PIN56	B15_L10_P	M21	3.3V
PIN57	B15_L21_N	J17	3.3V	PIN58	B15_L10_N	L21	3.3V
PIN59	GND	-	GND	PIN60	GND	-	GND
PIN61	B15_L23_P	L16	3.3V	PIN62	B15_L18_P	N20	3.3V
PIN63	B15_L23_N	K16	3.3V	PIN64	B15_L18_N	M20	3.3V
PIN65	B15_L22_P	L14	3.3V	PIN66	B15_L17_N	N19	3.3V
PIN67	B15_L22_N	L15	3.3V	PIN68	B15_L17_P	N18	3.3V
PIN69	GND	-	GND	PIN70	GND	-	GND
PIN71	B15_L24_P	M15	3.3V	PIN72	B15_L16_P	M18	3.3V
PIN73	B15_L24_N	M16	3.3V	PIN74	B15_L16_N	L18	3.3V
PIN75	NC	-		PIN76	NC	-	
PIN77	FPGA_TCK	V12	3.3V	PIN78	FPGA_TDI	R13	3.3V
PIN79	FPGA_TDO	U13	3.3V	PIN80	FPGA_TMS	T13	3.3V

Expansion port CON4

The 80-Pin connector CON4 is used to extend the normal IO of the FPGA BANK16 and high-speed data and clock signals of GTP. The voltage standard of the IO port of BANK16 can be adjusted by an LDO chip, and the default installed LDO is 3.3V. If you want to output other standard levels, you can replace it with a suitable LDO. The high-speed data and clock signals of the GTP are strictly differentially lined on the core board. The data lines are equal in length and kept at a certain interval to prevent signal interference. Pin assignment of the CON4 expansion port is shown in Table 2-9-4:

Table 2-9-4: Pin Assignment of CON4

CON4 Pin	Signal Name	FPGA Pin No.	Level Standard	CON4 Pin	Signal Name	FPGA Pin No.	Level Standard
PIN1	NC		-	NC		-	NC

PIN3	NC		-	NC		-	NC
PIN5	NC		-	NC		-	NC
PIN7	NC		-	NC		-	NC
PIN9	GND	-	GND	PIN10	GND	-	GND
PIN11	NC		-	PIN12	MGT_TX2_P	B6	Diff
PIN13	NC		-	PIN14	MGT_TX2_N	A6	Diff
PIN15	GND	-	GND	PIN16	GND	-	GND
PIN17	MGT_TX3_P	D7	Diff	PIN18	MGT_RX2_P	B10	Diff
PIN19	MGT_TX3_N	C7	Diff	PIN20	MGT_RX2_N	A10	Diff
PIN21	GND	-	GND	PIN22	GND	-	GND
PIN23	MGT_RX3_P	D9	Diff	PIN24	MGT_TX0_P	B4	Diff
PIN25	MGT_RX3_N	C9	Diff	PIN26	MGT_TX0_N	A4	Diff
PIN27	GND	-	GND	PIN28	GND	-	GND
PIN29	MGT_TX1_P	D5	Diff	PIN30	MGT_RX0_P	B8	Diff
PIN31	MGT_TX1_N	C5	Diff	PIN32	MGT_RX0_N	A8	Diff
PIN33	GND	-	GND	PIN34	GND	-	GND
PIN35	MGT_RX1_P	D11	Diff	PIN36	MGT_CLK1_P	F10	Diff
PIN37	MGT_RX1_N	C11	Diff	PIN38	MGT_CLK1_N	E10	Diff
PIN39	GND	-	GND	PIN40	GND	-	GND
PIN41	B16_L5_P	E16	3.3V	PIN42	B16_L2_P	F16	3.3V
PIN43	B16_L5_N	D16	3.3V	PIN44	B16_L2_N	E17	3.3V
PIN45	B16_L7_P	B15	3.3V	PIN46	B16_L3_P	C14	3.3V
PIN47	B16_L7_N	B16	3.3V	PIN48	B16_L3_N	C15	3.3V
PIN49	GND	-	GND	PIN50	GND	-	GND
PIN51	B16_L9_P	A15	3.3V	PIN52	B16_L10_P	A13	3.3V
PIN53	B16_L9_N	A16	3.3V	PIN54	B16_L10_N	A14	3.3V
PIN55	B16_L11_P	B17	3.3V	PIN56	B16_L12_P	D17	3.3V
PIN57	B16_L11_N	B18	3.3V	PIN58	B16_L12_N	C17	3.3V
PIN59	GND	-	GND	PIN60	GND	-	GND
PIN61	B16_L13_P	C18	3.3V	PIN62	B16_L14_P	E19	3.3V
PIN63	B16_L13_N	C19	3.3V	PIN64	B16_L14_N	D19	3.3V

PIN65	B16_L15_P	F18	3.3V	PIN66	B16_L16_P	B20	3.3V
PIN67	B16_L15_N	E18	3.3V	PIN68	B16_L16_N	A20	3.3V
PIN69	GND	-	GND	PIN70	GND	-	GND
PIN71	B16_L17_P	A18	3.3V	PIN72	B16_L18_P	F19	3.3V
PIN73	B16_L17_N	A19	3.3V	PIN74	B16_L18_N	F20	3.3V
PIN75	B16_L19_P	D20	3.3V	PIN76	B16_L20_P	C22	3.3V
PIN77	B16_L19_N	C20	3.3V	PIN78	B16_L20_N	B22	3.3V
PIN79	NC	-		PIN80	NC	-	

2.10 Power Supply

The power supply voltage of the AC7A200 core board is DC5V. The AC7A200 core board is powered by the J2 interface when it is used separately, and is powered by the carrier board when it is connected to the carrier board. Please do not use J2 interface and carrier board to supply power at the same time to avoid damage.The power supply design diagram on the board is shown in Figure 2-10-1 below:

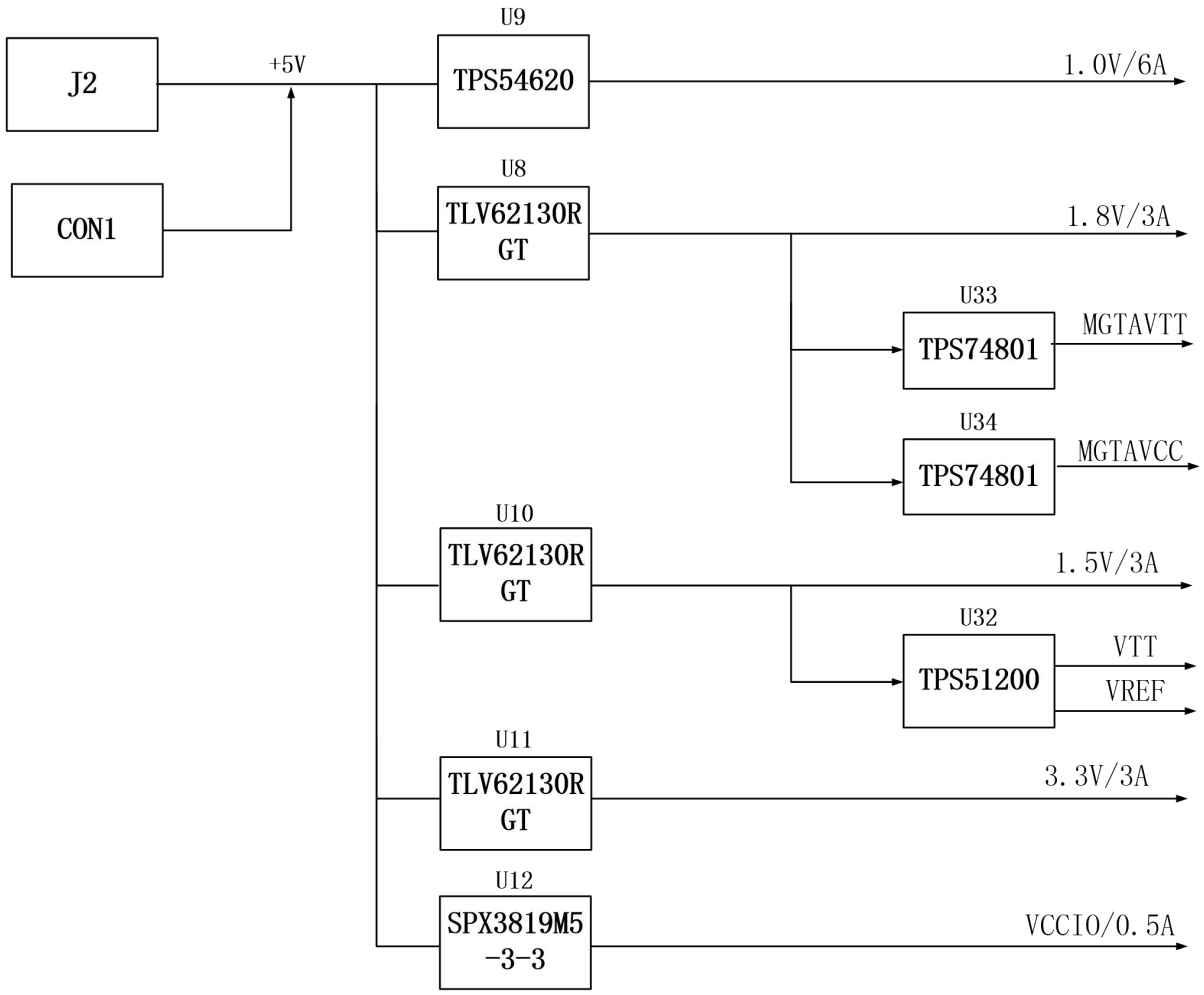


Figure 2-10-1: Power Supply on core board schematic

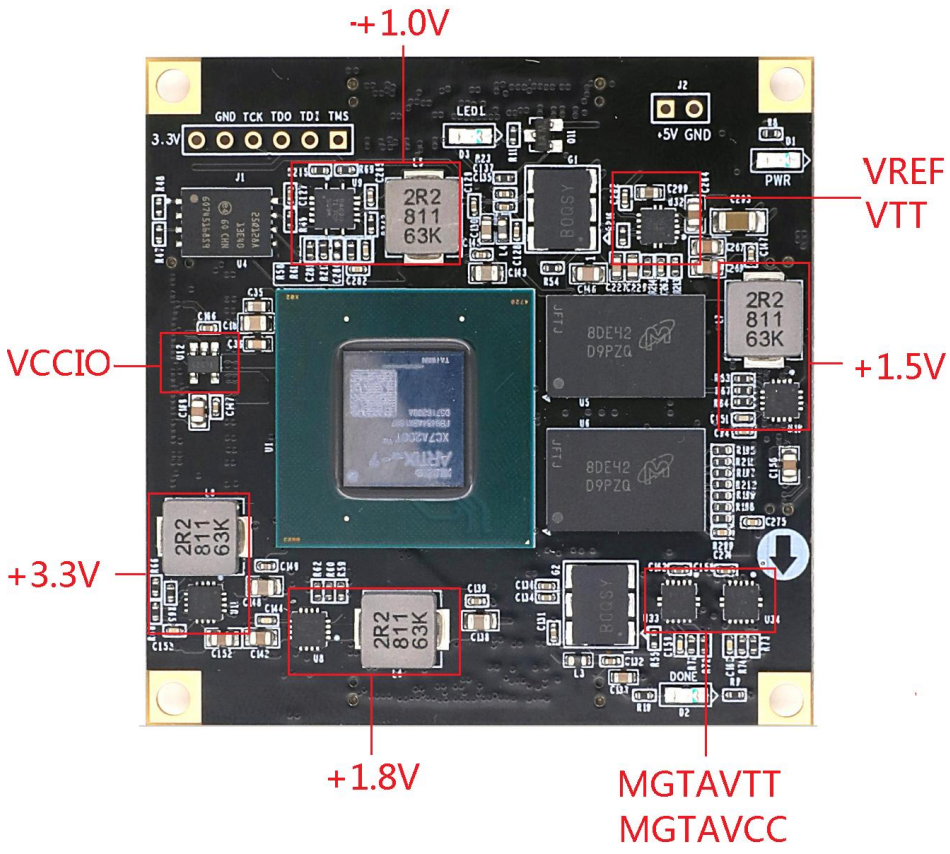
The core board is powered by +5V, and converted into +3.3V, +1.5V, +1.8V, +1.0V power supplies through the 3-way DC/DC power supply chip TLV62130RGT and TPS54620, in which the current of +1.0V can be up to 6A and the output current of the other 3 power supplies can be up to 3A. In addition, through one LDO SPX3819M5-3-3 to generate VCCIO power supply, VCCIO mainly supplies power for FPGA BANK15 and BANK16. Users can adapt the IO of the BANK15 and BANK16 to different voltage standards by replacing SPX3819M5-3-3 with other LDO chips. 1.5V generates the VTT and VREF voltage required for DDR3 through TI's TPS51200. The 1.8V generates the power supply MGTAVTT and MGTAVCC for the GTP transceiver through TI's TPS74801 chip. The functions of each power distribution are shown in the following table:

Power Supply	Function

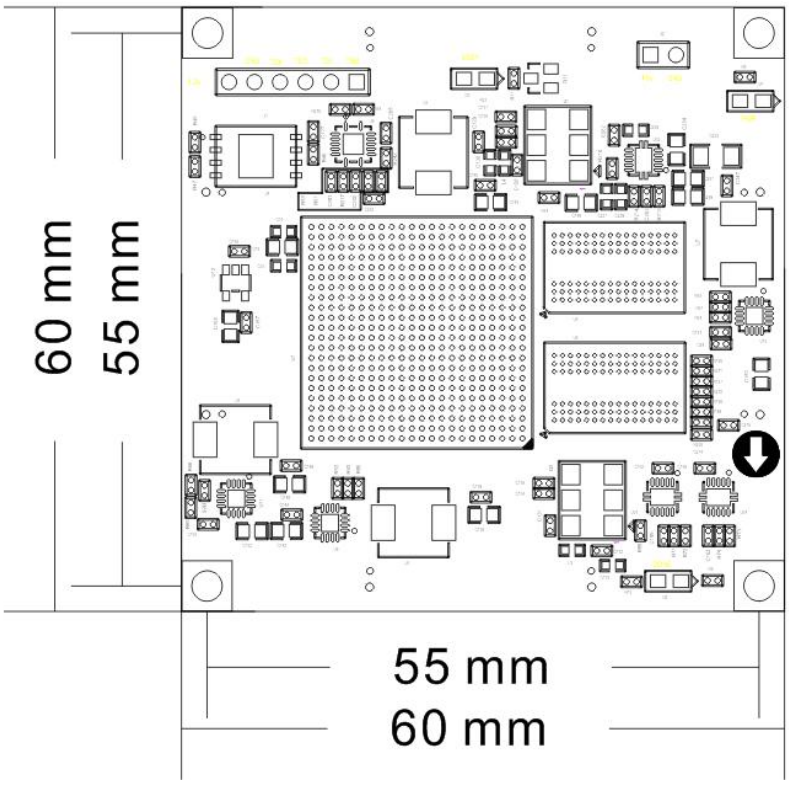
+3.3V	FPGA Bank0,Bank13，Bank14 的 VCCIO, QSIP FLASH, Clock crystal oscillator
+1.8V	FPGA auxiliary voltage, TPS74801 power supply
+1.0V	The core voltage of the FPGA
+1.5V	DDR3, FPGA Bank34 and Bank35
VREF, VTT （+0.75V）	DDR3
VCCIO(+3.3V)	FPGA Bank15, Bank16
MGTAVTT(+1.2V)	FPGA GTP transceiver Bank216
MGTAVCC(+1.0V)	FPGA GTP transceiver Bank216

Because the power supply of Artix-7 FPGA has the power-on sequence requirement, in the circuit design, we have designed according to the power requirements of the chip, and the power-on sequence is 1.0V->1.8V->(1.5 V, 3.3V, VCCIO) and 1.0V-> MGTAVCC -> MGTAVTT to ensure the normal operation of the chip.

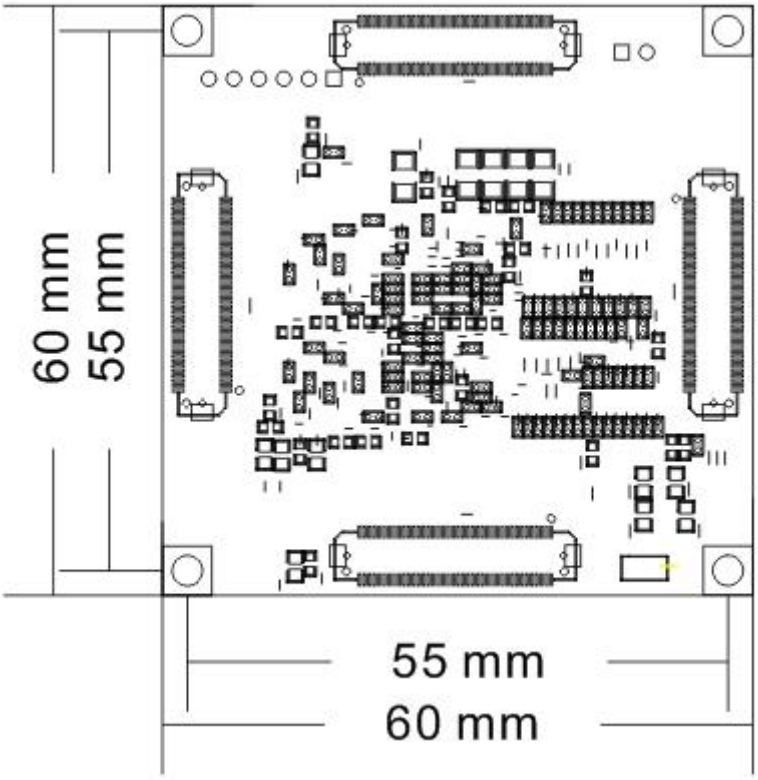
Power circuits on the AC7A200 FPGA core board are shown in Figure 2-10-2:



2.11 Size Dimension

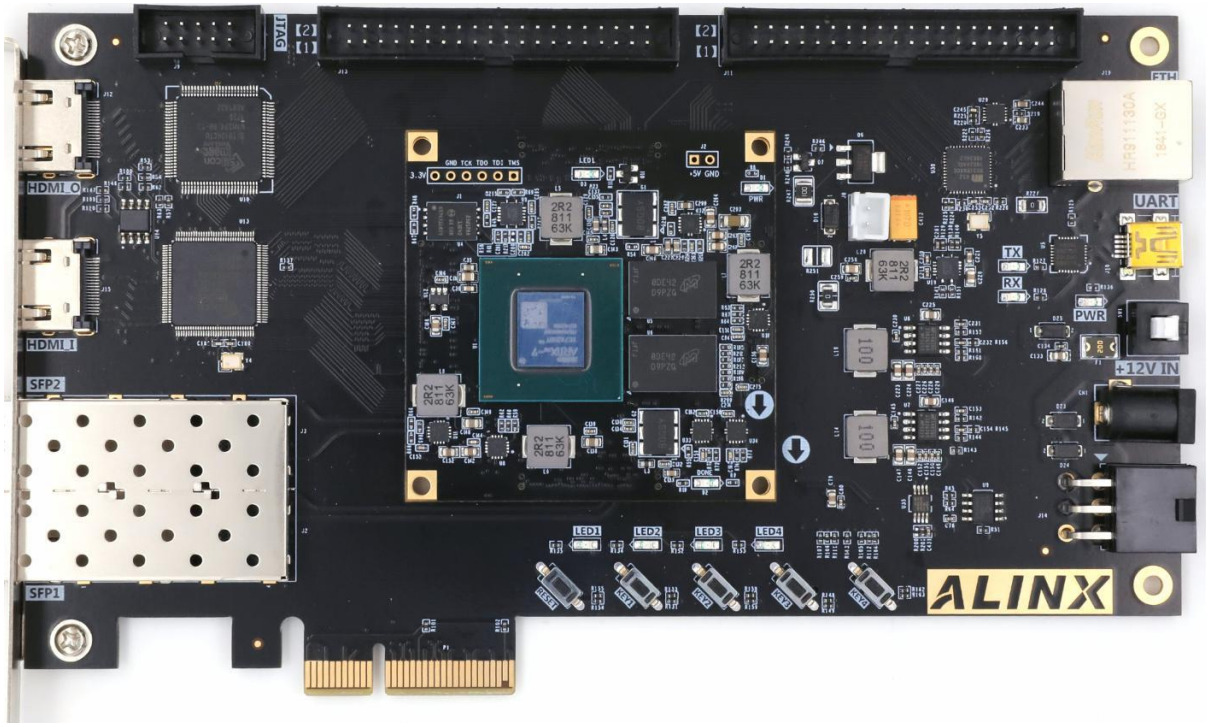


Front View



Back View

3. Carrier Board



3.1 Introduction

Through the previous function introduction, you can know the function of the carrier board:

- 1 PCIe x2 high-speed data transmission interface
- 2 SFP high-speed optical fiber interfaces
- 1 HDMI video input interface
- 1 HDMI video output interface
- 1 10/100M/1000M Ethernet RJ-45 interface
- 1 USB Uart communication interface
- 1 SD card interface
- 2 40-pin expansion ports
- EEPROM
- JTAG debugging interface
- 5 individual keys
- 4 user LED lights

3.2 Gigabit Ethernet Interface

The AX7A200B development board provides network communication services for users through a JL2121-N040I Ethernet PHY chip from JLSemi company. The Ethernet PHY chip is connected to the IO interface of the ARTIX7 FPGA. The JL2121-N040I chip supports 10/100/1000 Mbps network transmission rate and communicates with the FPGA through the RGMII interface. JL2121-N040I supports MDI/MDX self-adaptive, various speed self-adaptive, Master/Slave self-adaptive, supports MDIO bus for PHY register management.

When the JL2121 is powered on, it detects some specific IO level states to determine its own working mode. Table 3-2-1 describes the default Settings of the GPHY chip after it is powered on.

Configuration Pin	Instructions	Configuration Value
RXD3_ADR0 RXC_ADR1 RXCTL_ADR2	MDIO/MDC 模式的 PHY 地址	PHY Address is 001
RXD1_TXDLY	TX clock 2ns delay	Delay
RXD0_RXDLY	RX clock 2ns delay	Delay

Table 3-2-1: Default configuration of the PHY chip

When the network is connected to Gigabit Ethernet, the data transmission of FPGA and PHY chip JL2121 is communicated through the RGMII bus with a 125Mhz transmission clock, and the data is sampled on the rising and falling edge of the clock.

When the network is connected to 100M Ethernet, the data transmission of FPGA and PHY chip JL2121 is communicated through the RMII bus with a 25Mhz transmission clock, and the data is sampled on the rising and falling edge of the clock.

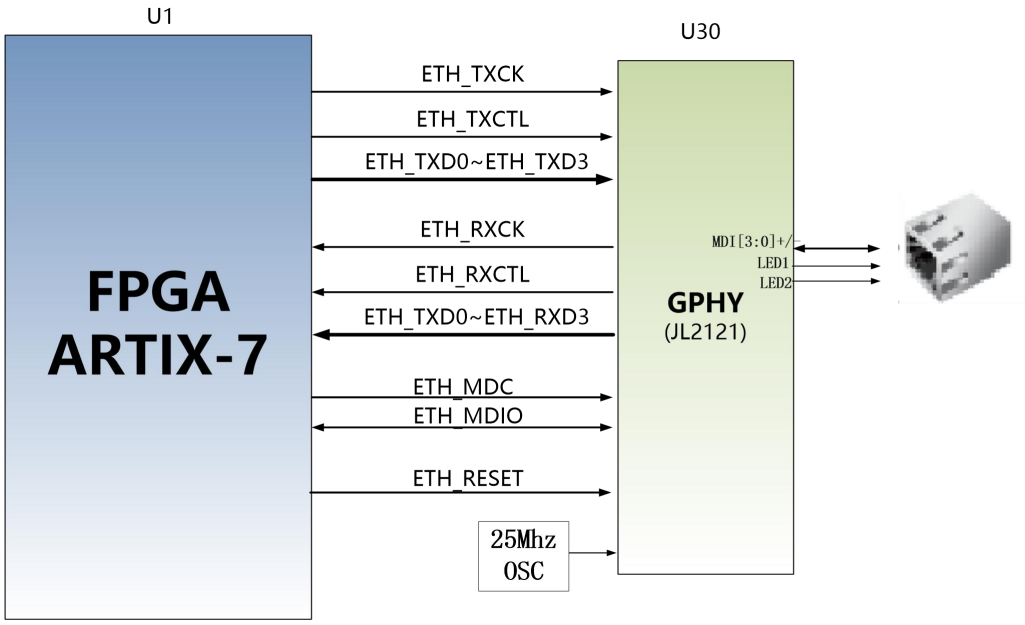


Figure 3-2-1: Connection diagram between FPGA and Ethernet PHY chip

FPGA pin assignment of Ethernet PHY is as follows:

Signal Name	FPGA Pin Number	Description
ETH_TXCK	P15	RGMII sends the clock
ETH_TXD0	N14	Send data bit0
ETH_TXD1	P16	Send data bit1
ETH_TXD2	R17	Send data bit2
ETH_TXD3	R16	Send data bit3
ETH_TXCTL	N17	Send the enable signal
ETH_RXCK	V18	RGMII receives the clock
ETH_RXD0	P19	Receive data Bit0
ETH_RXD1	U18	Receive data Bit1
ETH_RXD2	U17	Receive data Bit2
ETH_RXD3	P17	Receive data Bit3
ETH_RXCTL	R19	Receive data valid signal
ETH_MDC	N13	MDIO manages the clock
ETH_MDIO	P14	MDIO manages the data
ETH_RESET	R14	PHY chip reset

3.3 SFP Interface

The AX7A200B carrier board has two optical fiber interfaces. You can purchase optical modules (1.25G or 2.5G optical modules in the market) and insert them into the two interfaces for optical fiber data communication. The two optical fiber interfaces are respectively connected to the two RX/TX channels of the FPGA GTP transceiver, and the TX signal and RX signal are connected to the FPGA and optical module in differential signal mode through the straight separation capacitor, and the data rate of each TX transmission and RX reception is up to 6.6Gb/s. The reference clock of the GTP transceiver is provided by a 125M differential crystal oscillator on the core board.

The schematic diagram of FPGA and optical fiber design is shown in Figure 3-3-1 below:

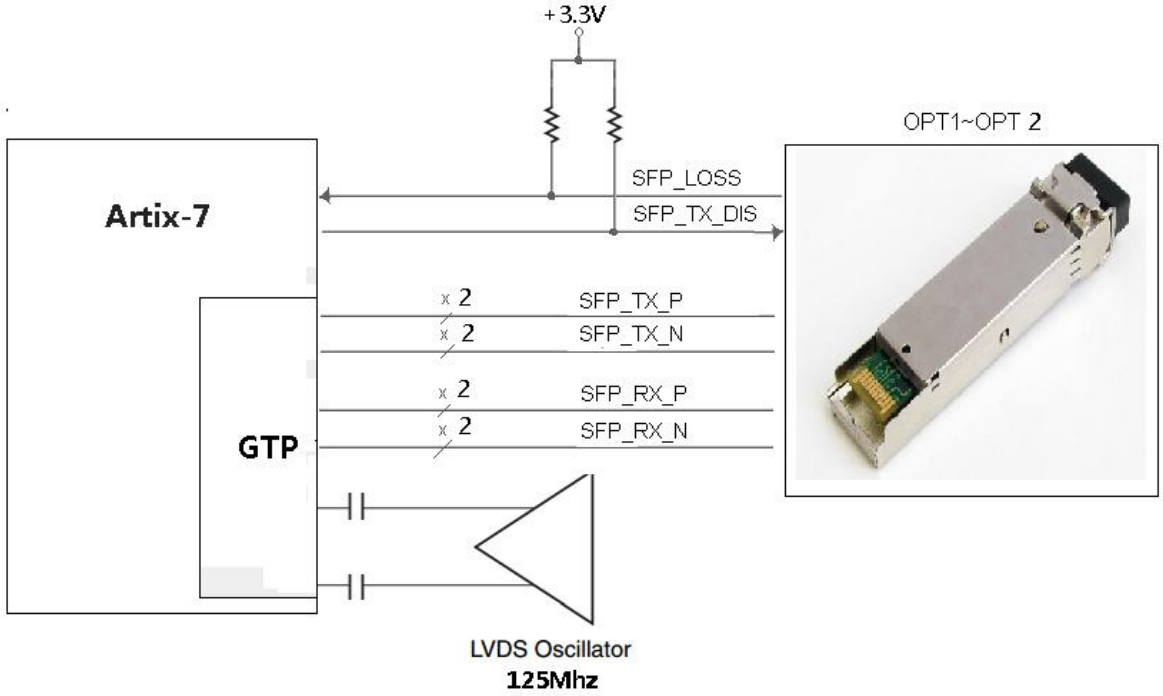


Figure 3-3-1 Schematic diagram of optical fiber design

FPGA pin assignment of the first-channel optical fiber interface:

Network Name	FPGA Pin	Description
SFP1_TX_P	B4	SFPSFP optical module data transmission Positive
SFP1_TX_N	A4	SFP optical module data transmission

		Negative
SFP1_RX_P	B8	SFP optical module data reception Positive
SFP1_RX_P	A8	SFP optical module data reception Negative
SFP1_TX_DIS	J15	SFP optical module disables optical emission and has high validity
SFP1_LOSS	H15	SFP optical reception LOSS signal. High indicates that no optical signal is received

FPGA pin assignment of the second-channel optical fiber interface:

Network Name	FPGA Pin	Description
SFP2_TX_P	D5	SFP optical module data transmission Positive
SFP2_TX_N	C5	SFP optical module data transmission Negative
SFP2_RX_P	D11	SFP optical module data reception Positive
SFP2_RX_P	C11	SFP optical module data reception Negative
SFP2_TX_DIS	H14	SFP optical module disables optical emission and has high validity
SFP2_LOSS	J14	SFP optical reception LOSS signal. High indicates that no optical signal is received

3.4 PCIe x4 Interface

The AX7A200B carrier board provides an industrial-grade high-speed data transmission PCIe x4 interface. The PCIE card dimensions meet the electrical requirements of standard PCIe cards and can be used directly in the x4 PCIe

slots of normal PC.

The receiving and sending signals of the PCIe interface are directly connected to the GTP transceiver of the FPGA, and the four-channel TX signals and RX signals are connected to the FPGA in differential signal mode, and the single-channel communication rate can be up to 5G bit bandwidth. The PCIe reference clock is provided to the development board by the PCIe slot on the PC. The reference clock frequency is 100Mhz.

The design diagram of the PCIe interface of the development board is shown in Figure 3-4-1, where the TX sending signal and the reference clock CLK signal are connected in AC coupling mode.

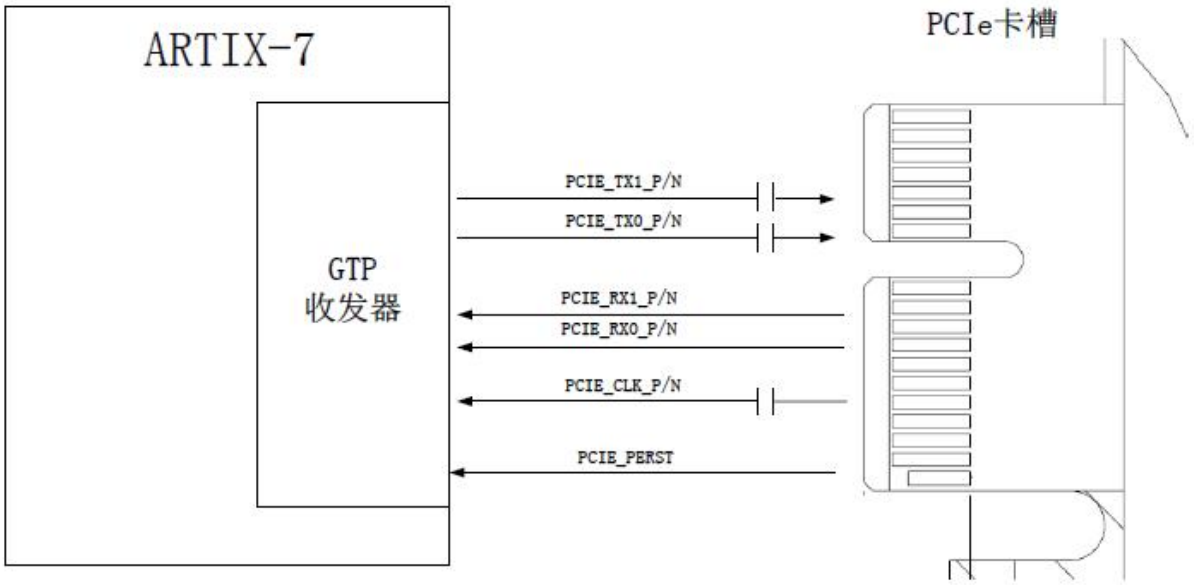


Figure 3-3-1: PCIe x2 design diagram

FPGA pin assignment of PCIe x2 interface is as follows:

Network Name	FPGA Pin	Description
PCIE_RX0_P	D9	PCIE channel 0 data reception Positive
PCIE_RX0_N	C9	PCIE channel 0 data reception Negative
PCIE_RX1_P	B10	PCIE channel 1 data reception Positive
PCIE_RX1_N	A10	PCIE channel 1 data reception Negative
PCIE_TX0_P	D7	PCIE channel 0 data transmission Positive
PCIE_TX0_N	C7	PCIE channel 0 data transmission Negative

PCIE_TX1_P	B6	PCIE channel 1 data transmission Positive
PCIE_TX1_N	A6	PCIE channel 1 data transmission Negative
PCIE_CLK_P	F10	PCIE's reference clock Positive
PCIE_CLK_N	E10	PCIE's reference clock Negative

3.5 HDMI Output Interface

The HDMI output interface is implemented by Silion Image's SIL9134 HDMI (DVI) coding chip, which supports the highest output 1080P@60Hz and 3D output.

Among them, the IIC configuration interface of SIL9134 is also connected to the IO of FPGA, and initialization and control operations are performed on SIL9134 through FPGA programming. The hardware connection of the HDMI output interface is shown in Figure 3-5-1.

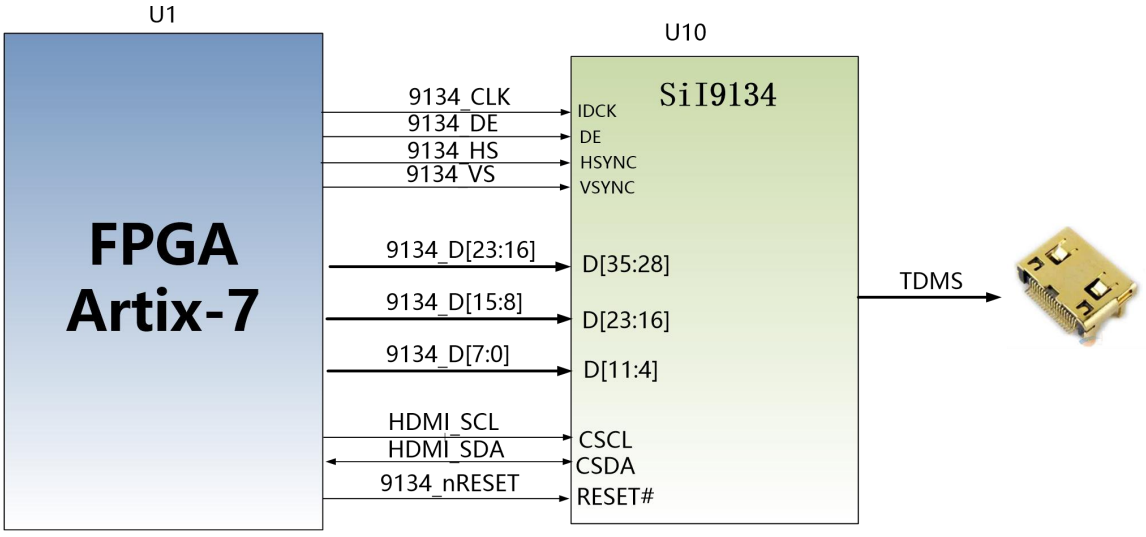


Figure 3-5-1: Design diagram of HDMI Interface

FPGA Pin Assignment:

Signal Name	FPGA Pin
9134_NRESET	Y17
9134_CLK	Y22
9134_HS	T18
9134_VS	R18

9134_DE	U22
9134_D0	V22
9134_D1	Y18
9134_D2	Y19
9134_D3	W19
9134_D4	W20
9134_D5	Y21
9134_D6	U21
9134_D7	T21
9134_D8	W21
9134_D9	W22
9134_D10	T20
9134_D11	AB18
9134_D12	AA18
9134_D13	AA19
9134_D14	AB20
9134_D15	AA20
9134_D16	AA21
9134_D17	AB22
9134_D18	AB21
9134_D19	W17
9134_D20	V17
9134_D21	V20
9134_D22	U20
9134_D23	V19
HDMI_SCL	H13
HDMI_SDA	G13

3.6 HDMI Input Interface

We use Silion Image's SIL9013 HDMI decoding chip, which supports the highest input 1080P@60Hz and supports data output in different formats.

Among them, the IIC configuration interface of SIL9013 is also connected to the IO of FPGA, and initialization and control operations are carried out on SIL9013 through FPGA programming. The hardware connection of the HDMI input interface is shown in Figure 3-6-1.

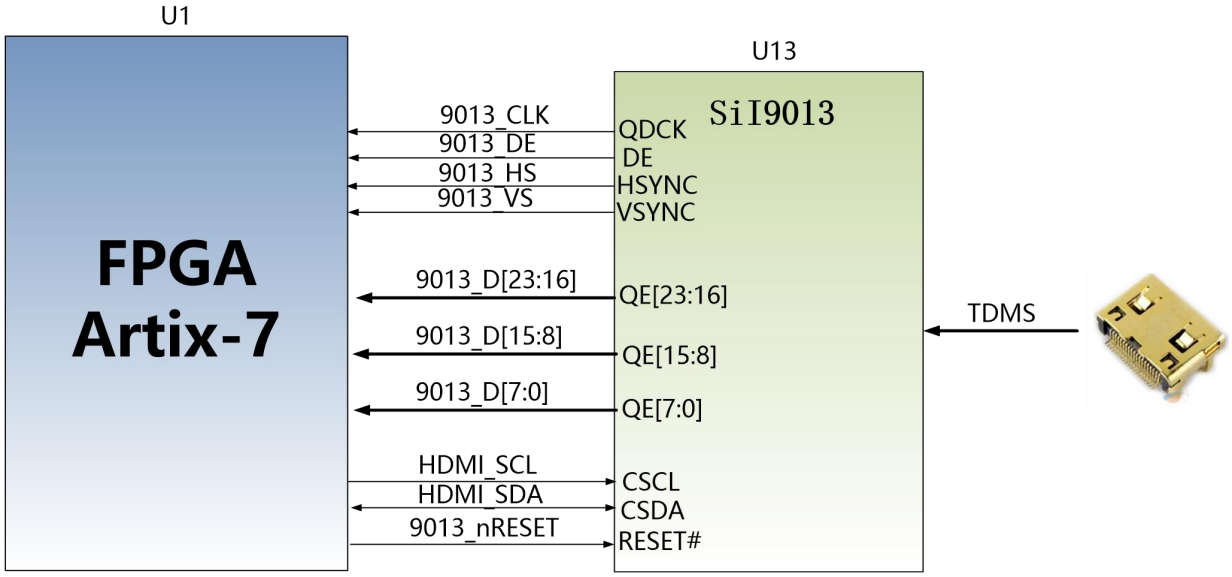


Figure 3-6-1: HDMI input schematic

FPGA pin assignment:

Signal Name	FPGA Pin
9013_NRESET	J21
9013_CLK	K18
9013_HS	N18
9013_VS	M18
9013_DE	N19
9013_D0	M20
9013_D1	N20
9013_D2	L21
9013_D3	M21

9013_D4	K19
9013_D5	H17
9013_D6	H18
9013_D7	N22
9013_D8	M22
9013_D9	K22
9013_D10	K21
9013_D11	J22
9013_D12	H22
9013_D13	H20
9013_D14	G20
9013_D15	M17
9013_D16	J16
9013_D17	G17
9013_D18	G18
9013_D19	G15
9013_D20	G16
9013_D21	J19
9013_D22	H19
9013_D23	J20
HDMI_SCL	H13
HDMI_SDA	G13

3.7 SD Card Slot

SD Card (Secure Digital Memory Card) is a memory card based on semiconductor flash memory process. The concept was led by Japan's Panasonic in 1999, and accomplished under the substantial research and development by participants Toshiba and the United States SanDisk company. In 2000, the three companies launched the Secure Digital Association (SDA), which attracted a large number of manufacturers to join in, including IBM, Microsoft, Motorola, NEC, Samsung and others. Driven by these leaders, SD

cards have become the most widely used memory card in consumer digital devices.

Now, SD card is a very common storage device. The SD card we extend out uses MicroSD card and supports SPI mode and SD mode. The schematic diagram is shown in Figure 3-7-1 below.

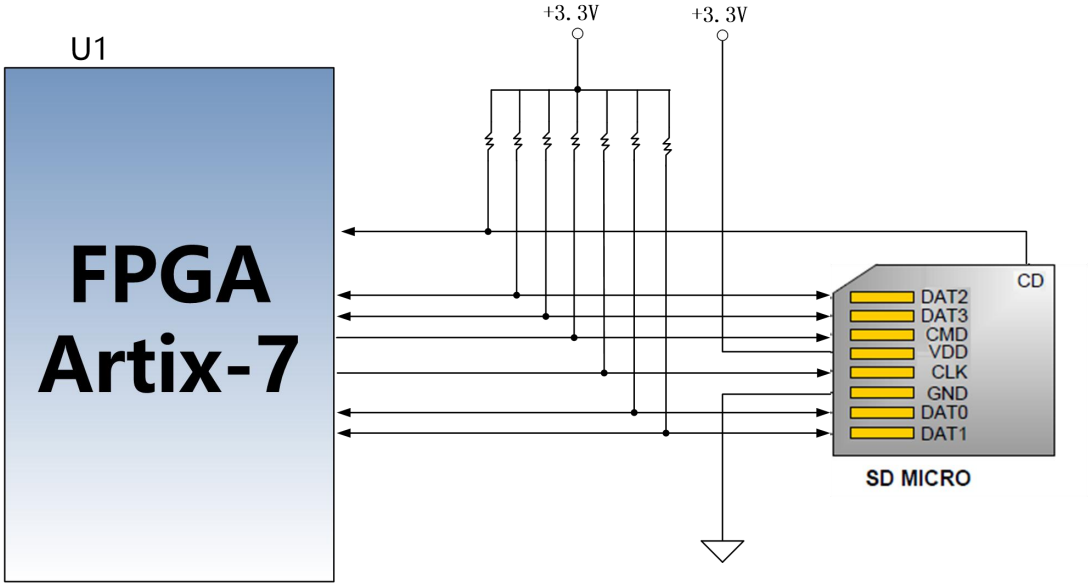


Figure 3-7-1 SD card slot schematic

SD card slot pin assignment:

SD mode	
Signal Name	**FPGA Pin**
SD_CLK	E13
SD_CMD	E14
SD_CD_N	C13
SD_DAT0	D15
SD_DAT1	D14
SD_DAT2	F14
SD_DAT3	F13

3.8 USB-to-serial Port

The AX7A200B development board contains the USB-UAR chip of Silicon

Labs CP2102GM. The USB interface adopts the MINI USB interface, which can be connected to the USB port of the PC with a USB cable for serial data communication.

The schematic diagram of USB Uart circuit design is shown in the following figure:

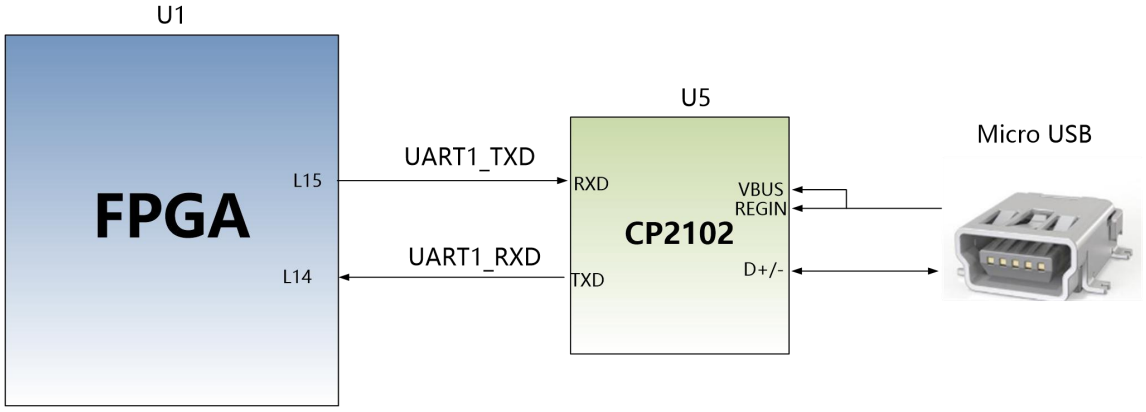


Figure 3-8-1: schematic diagram of USB-to-serial port

Two LED lights (LED3 and LED4) with silk-screen TX and RX on the PCB are set for the serial signal. The TX and RX LED lights will indicate whether the serial port has data transmission or data reception, as shown in the following figure.

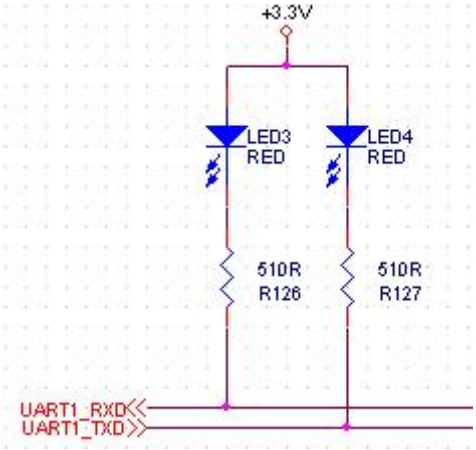


Figure 3-8-2 USB-to-serial port signal indicators

Pin assignment of UART-to-serial port:

Signal Name	FPGA Pin
UART1_RXD	L14
UART1_TXD	L15

3.9 EEPROM 24LC04

The AX7A200B development board carries an EEPROM (model: 24LC04), the capacity is: 4Kbit (2*256*8bit), consists of two 256byte blocks, and communicates through the IIC bus. EEPROM is set to learn the communication mode of IIC bus. The I2C signal of the EEPROM is connected to the BANK15 IO port of the FPGA end. Figure 3-9-1 shows the design diagram of EEPROM:

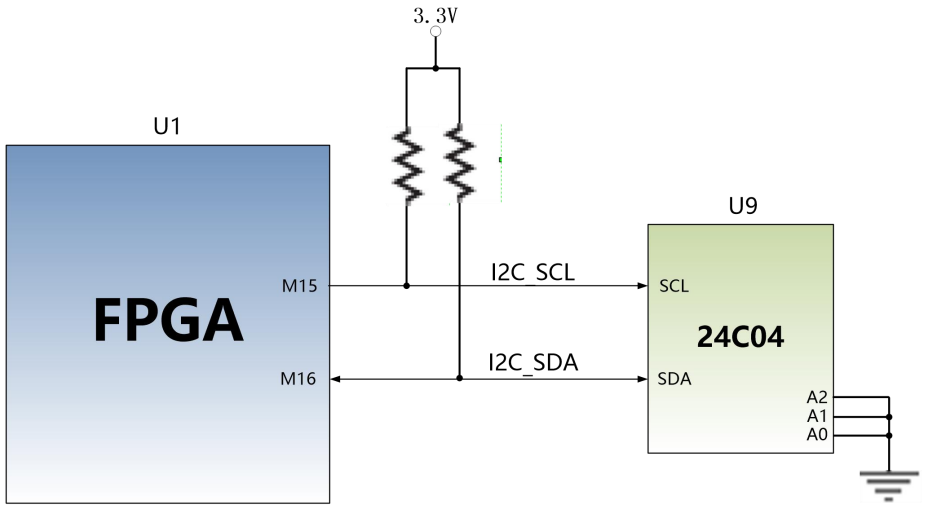


Figure 3-9-1: EEPROM schematic

EEPROM pin assignment:

Signal Name	FPGA Pin
I2C_SCL	M15
I2C_SDA	M16

3.10 Temperature Sensor

The AX7A200B development board is equipped with a high-precision, low-power, digital temperature sensor chip (model: LM75) from ON Semiconductor. The temperature accuracy of LM75 chip is 0.5 degrees, and the sensor and FPGA are directly I2C digital interface, and the FPGA reads the temperature near the current development board through the I2C interface. Figure 3-10-1 shows the design diagram of the LM75 sensor chip.

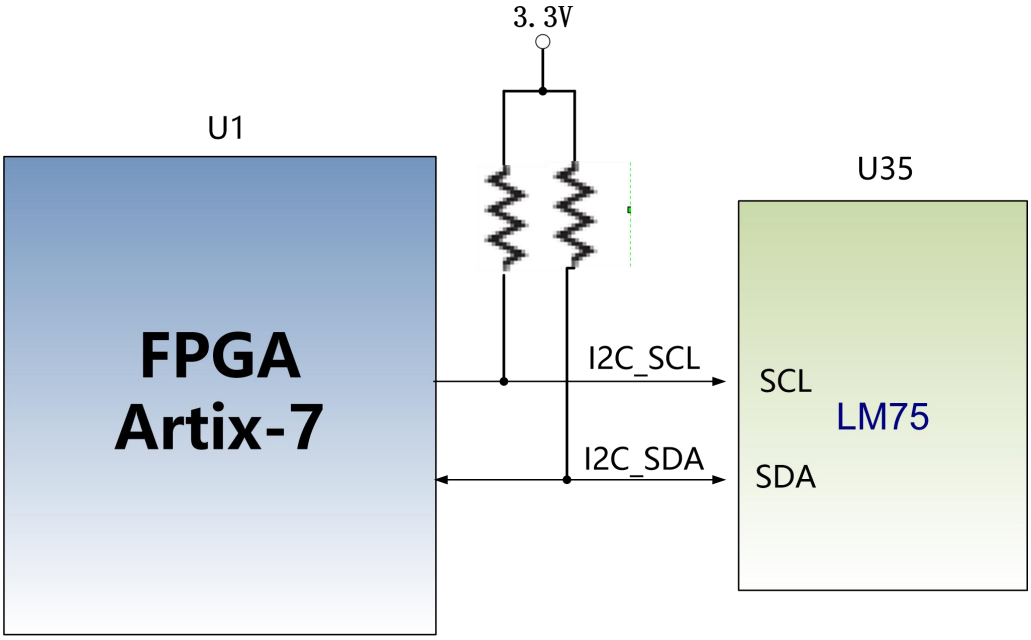


Figure 3-10-1: LM75 Sensor Schematic

LM75 sensor pin assignment:

Signal Name	FPGA Pin
I2C_SCL	M15
I2C_SDA	M16

3.11 Expansion Port

The carrier board is reserved with two 0.1inch spacing standard 40-pin expansion ports J11 and J13, which are used to connect the ALINX modules or the external circuit designed by the user. The expansion port has 40 signals, including one 5V power supply, two 3.3V power supplies, three ground channels, and 34 IO ports. **Do not connect IO directly to a 5V device to avoid damaging the FPGA. If you want to connect a 5V device, you need to connect the level conversion chip.**

A 33 ohm Network Resistor is placed in series between the expansion port and the FPGA connection to protect the FPGA from damage caused by excessive external voltage or current. The circuit of the expansion port (J11) is shown in Figure 3-11-1 below:

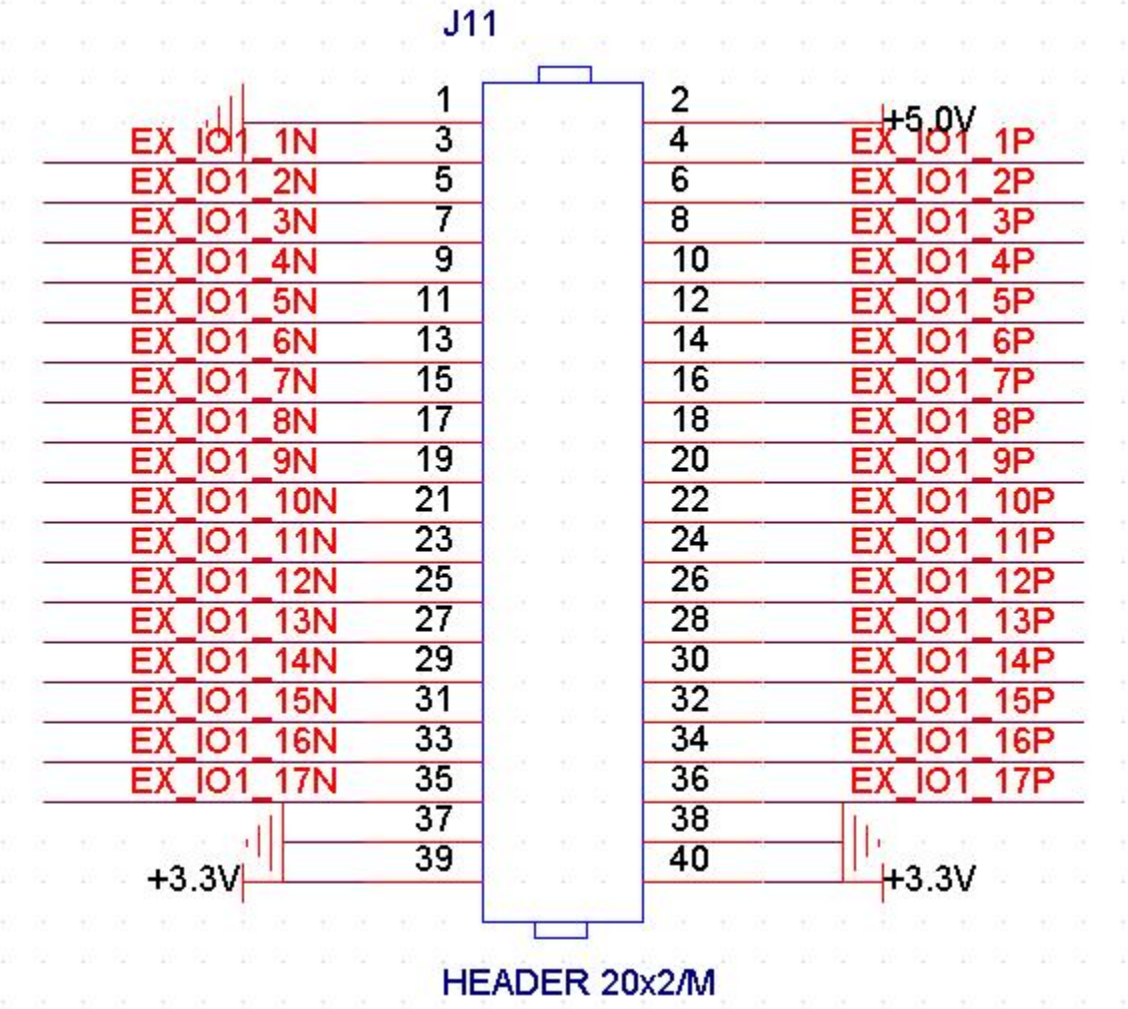


Figure 3-11-1: Schematic of expansion port J11

FPGA pin assignment of J11:

Pin No.	FPGA Pin	Pin No.	FPGA Pin
1	GND	**2**	+5V
3	G21	**4**	G22
5	C22	**6**	B22
7	F19	**8**	F20
9	D20	**10**	C20
11	A18	**12**	A19
13	B20	**14**	A20
15	F18	**16**	E18
17	E19	**18**	D19

19	C18	**20**	C19
21	B17	**22**	B18
23	D17	**24**	C17
25	A15	**26**	A16
27	B15	**28**	B16
29	A13	**30**	A14
31	E16	**32**	D16
33	C14	**34**	C15
35	F16	**36**	E17
37	GND	**38**	GND
39	+3.3V	**40**	+3.3V

The circuit of the expansion port (J13) is shown in Figure 3-11-2 below:

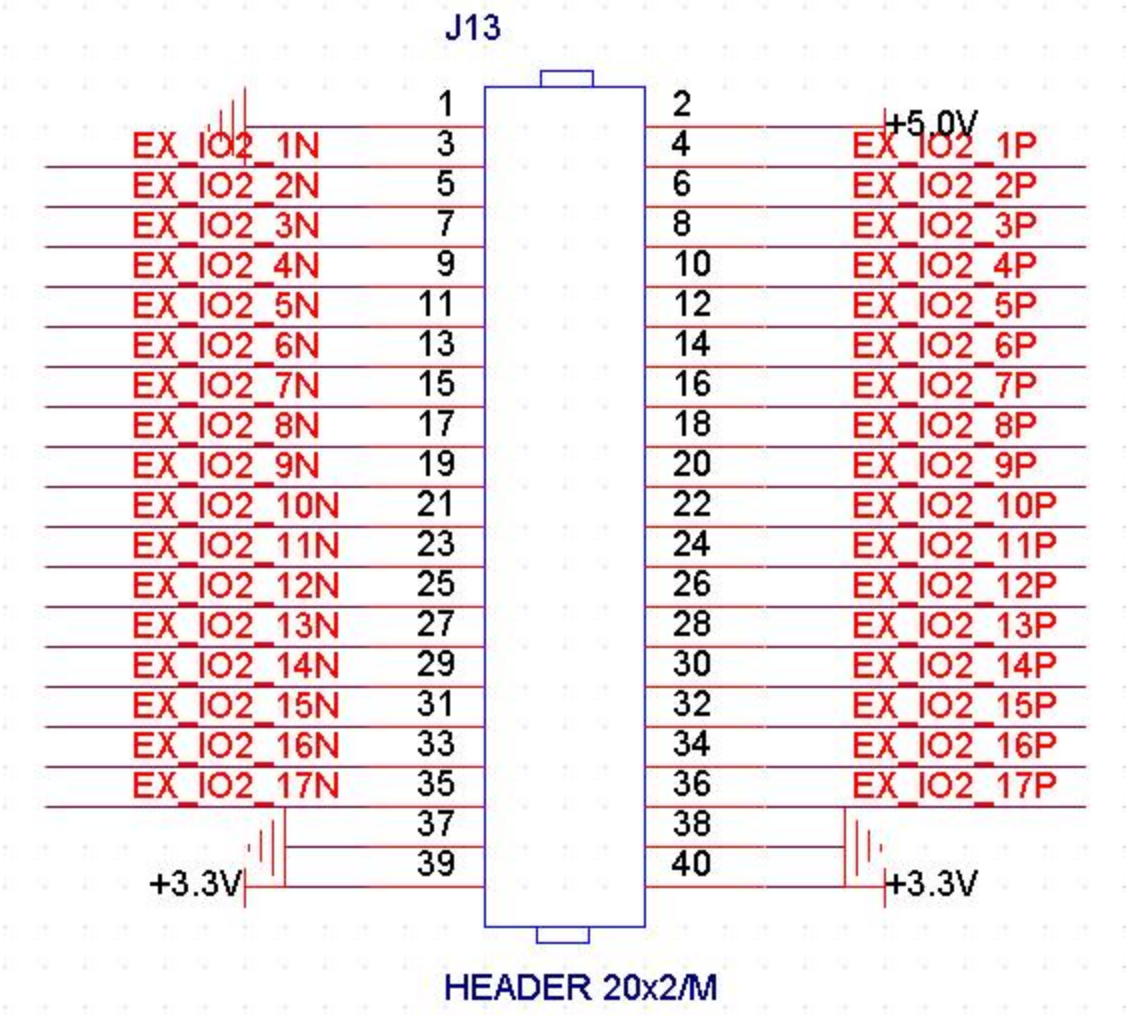


Figure 3-11-2: Schematic of expansion port J13

FPGA pin assignment of J13

Pin No.	FPGA Pin	Pin No.	FPGA Pin
1	GND	**2**	+5V
3	W16	**4**	W15
5	T15	**6**	T14
7	V15	**8**	U15
9	V14	**10**	V13
11	W12	**12**	W11
13	Y12	**14**	Y11
15	W10	**16**	V10
17	AA10	**18**	AA11
19	AA9	**20**	AB10
21	U16	**22**	T16
23	AA13	**24**	AB13
25	AB11	**26**	AB12
27	Y13	**28**	AA14
29	W14	**30**	Y14
31	Y16	**32**	AA16
33	AB16	**34**	AB17
35	AA15	**36**	AB15
37	GND	**38**	GND
39	+3.3V	**40**	+3.3V

3.12 JTAG Interface

The development board reserves a JTAG interface for downloading FPGA programs or curing programs to FLASH. In order to prevent the damage to the FPGA chip caused by hot plugging, we add a protection diode to the JTAG signal to ensure that the voltage of the signal is in the range accepted by the FPGA to avoid the damage of the FPGA.

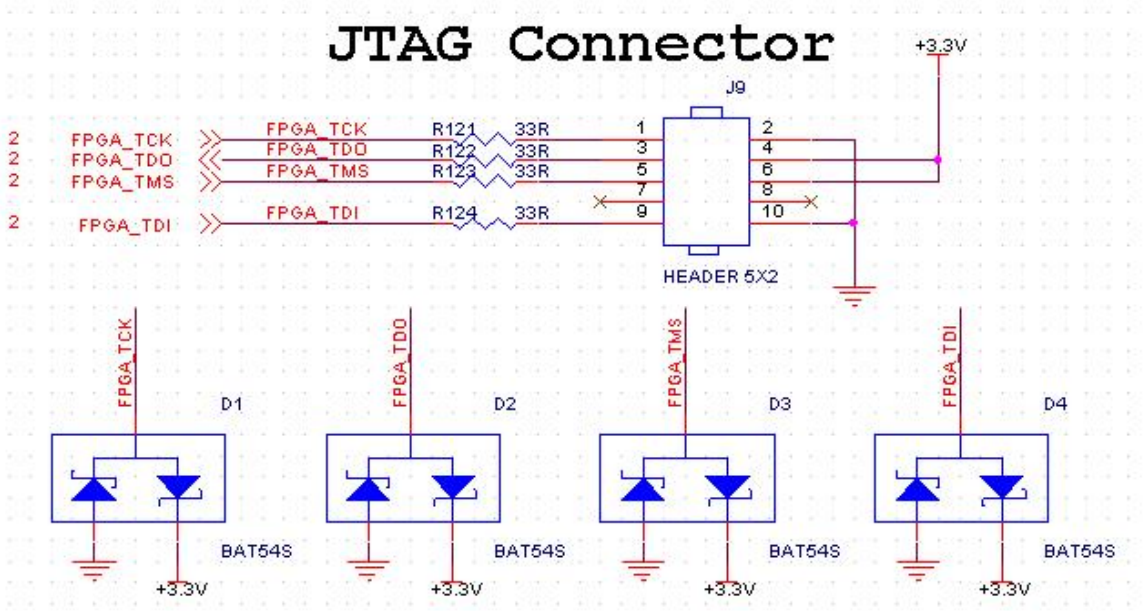


Figure 3-12-1: Schematic of JTAG interface

The following figure shows the actual JTAG port on the carrier board. Do not hot-plug the JTAG cable.

3.13 Keys

The carrier board contains five user keys RESET, KEY1 to KEY4, which are connected to the normal IOs of the FPGA. The low level of the key is set to be valid. When the key is pressed, the FPGA IO input voltage is low; when the key is not pressed, the FPGA IO input voltage is high. The key circuit is shown in Figure 3-13-1 below:

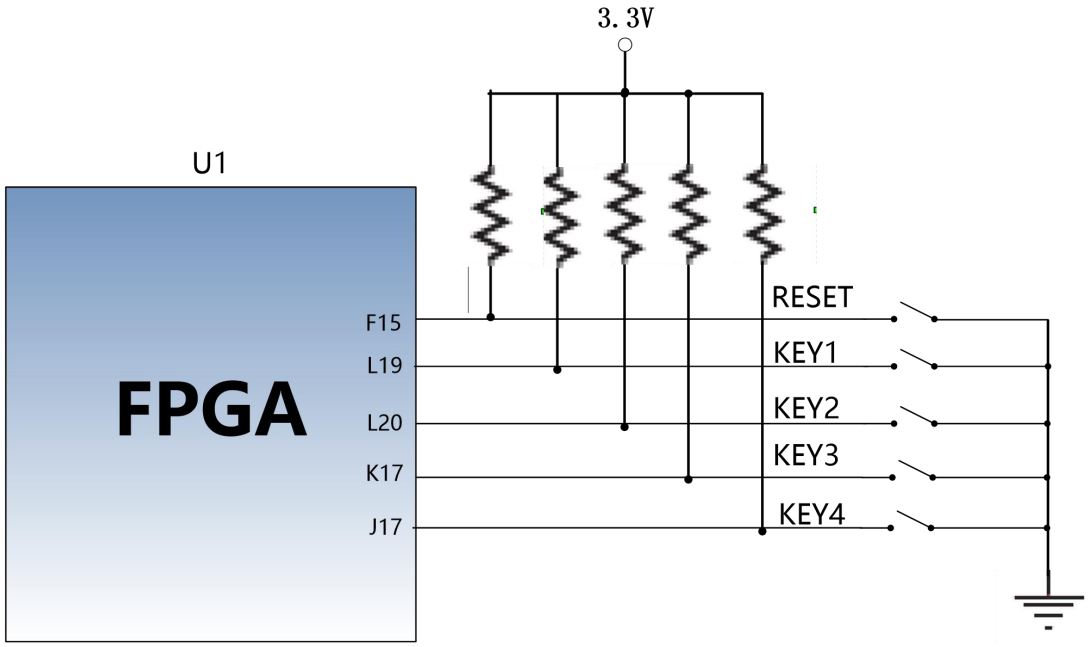


Figure 3-13-1: Design diagram of key hardware

Keys FPGA pin assignment:

Signal Name	FPGA Pin
RESET	F15
KEY1	L19
KEY2	L20
KEY3	K17
KEY4	J17

3.14 LED

There are 7 red LED lights on the carrier board, of which 1 is the power indicator (PWR), 2 are the data receiving and sending indicators of the USB Uart, and 4 are the user LED lights (LED1~LED4). When the development board is powered, the power indicator will light up. User LED1 to LED4 connect to the normal IOs of the FPGA. When the voltage of IO connected to the user LED light is set to be low level, the user LED will light up. When the voltage of IO connected to the user LED light is set to high level, the user LED will turn off.

Figure 3-14-1 shows the diagram of hardware connection of LED lights:

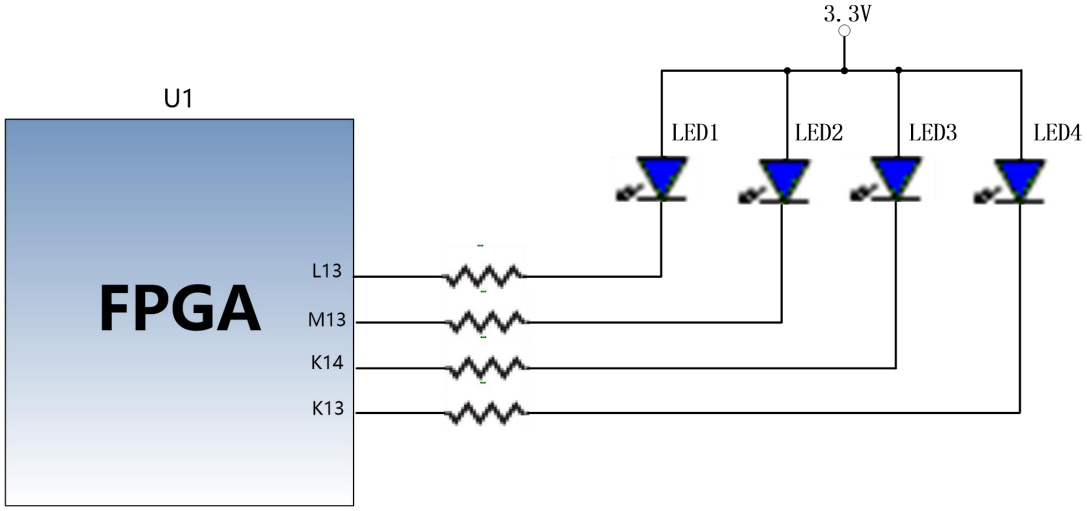


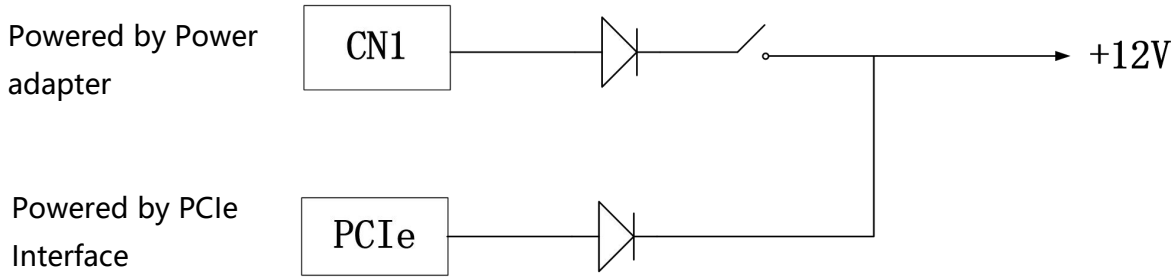
Figure 3-14-1: Hardware design diagram of LEDs

FPGA pin assignment of LED lights:

Signal Name	FPGA Pin
LED1	L13
LED2	M13
LED3	K14
LED4	K13

3.15 Power Supply

The power input voltage of the development board is DC12V, please use the power supply of the development board, do not use other power supplies with different specifications, so as to avoid damage to the development board. The development board can also support power from the PCIe interface or the 12V power supply from the ATX chassis.



The +12V voltage is converted to +5V, +3.3V and +1.8V by three DC/DC power chips on the carrier board. The power supply design on the carrier board is shown in Figure 3-15-1 below:

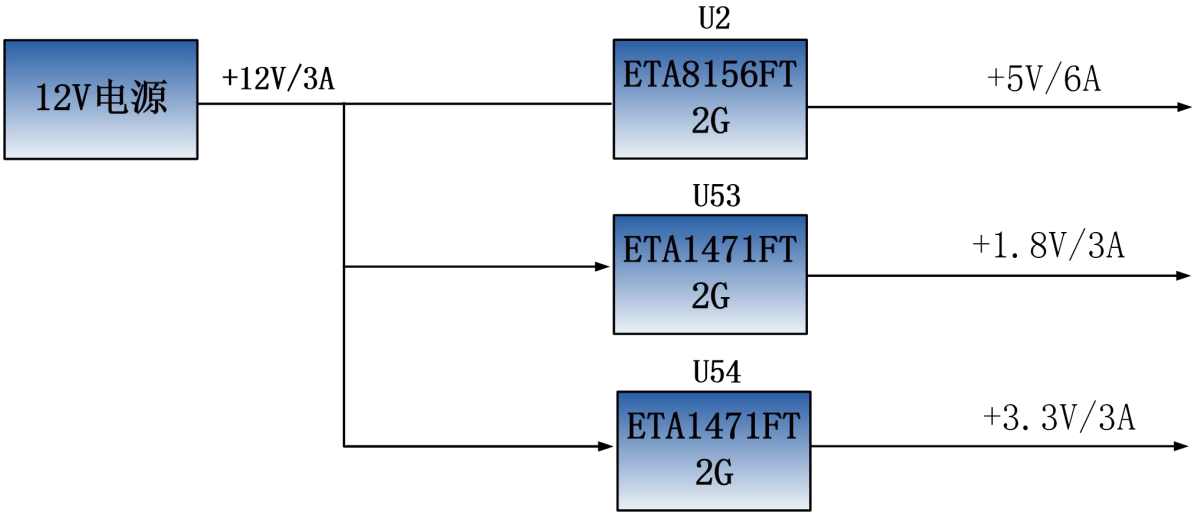


Figure 3-15-1: Power schematic diagram of the carrier board

3.16 Fan Interface (Reserved)

Because the FPGA chip generates heat during normal operation, we reserve a fan interface on the board (the fan is not installed by default). The the fan is controlled by the FPGA chip, and the control pin is connected to the IO of the BANK16. If the IO level output is low, the MOSFET tube will be on and the fan will work. If the IO level output is high, the fan will stop working. The fan design diagram on the board is shown in figure 3-16-1 below:

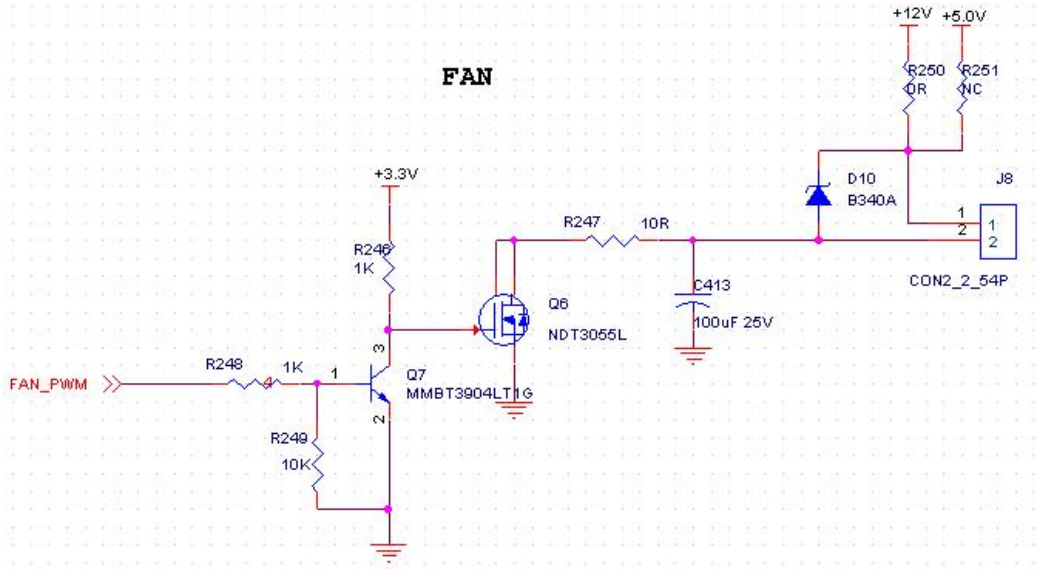
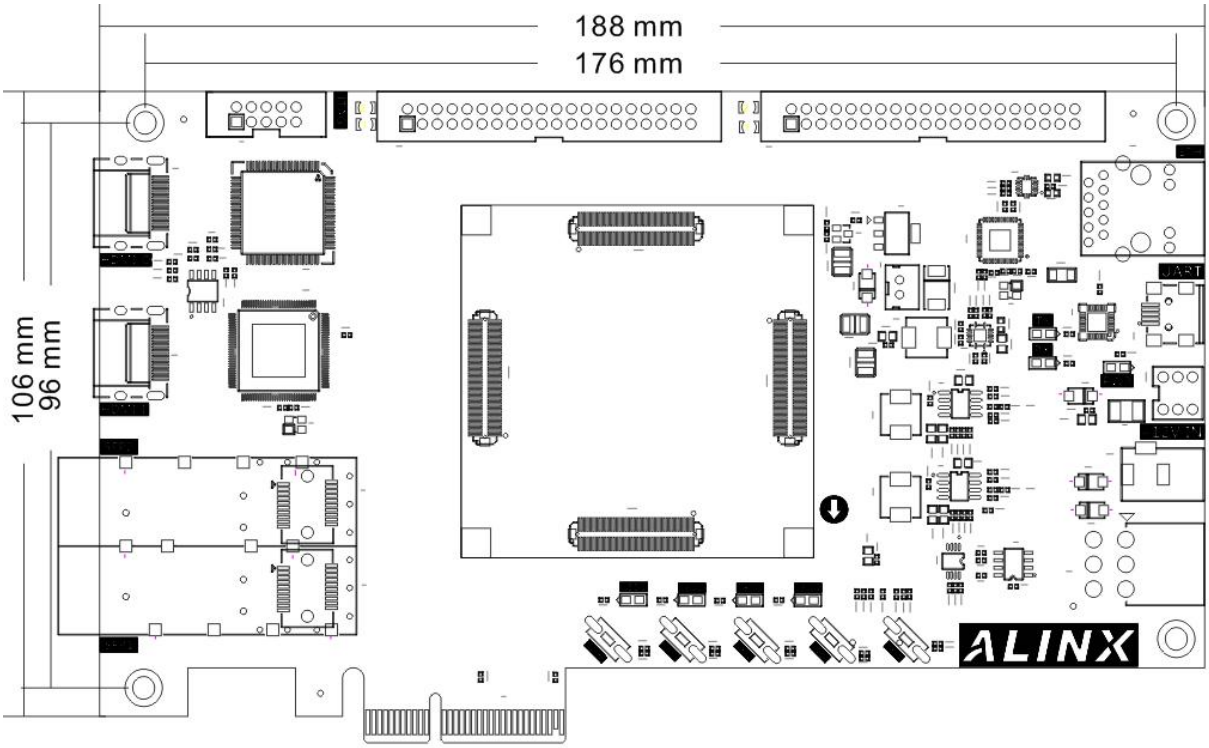


Figure 3-16-1: Fan design in the development board schematic

The fan has been fixed on the development board with screws before leaving the factory. The power supply of the fan is connected to the socket of the J8. The red one is positive and the black one is negative.

3.17 Carrier Board Size Dimension



Top View