ZYNQ7000 FPGA

Development Board

AX7Z010B

User Manual

ALINX

Version Rescord

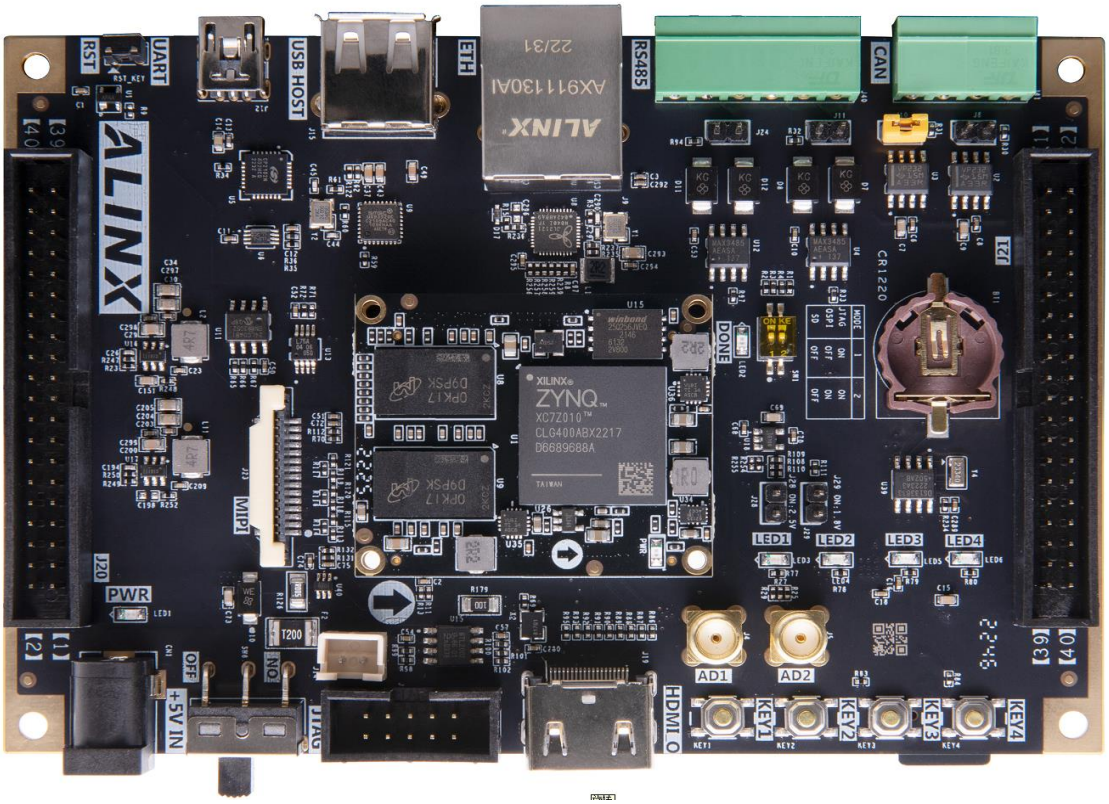
Version	Date	Release By	Description
REV1.0	2019-12-15	Rachel Zhou	First Release

Table of Contents

Alinx AX7Z010B FPGA board based on XILINX ZYNQ7000 series released in 2022. We wrote this user manual to let you quickly understand this development platform.

The ZYNQ7000 FPGA development platform adopts the mode of "core board+ carrier board", which is convenient for users to develop and utilize the core board twice. The core board uses XILINX's Zynq7000 SOC chip solution, which uses ARM+FPGA SOC technology to integrate dual-core ARM Cortex-A9 and FPGA programmable logic on a single chip. In addition, the core board contains two high-speed DDR3 SDRAM chips with a total of 512MB and one 256Mb QSPI FLASH chip.

In the design of the carrier board, we have extended a rich external interface for users, such as 2x CAN communication interfaces, 2x 485 communication interfaces, 2x XADC input interfaces, 1x Gigabit Ethernet interface, 1x USB2.0 HOST interface, 1x HDMI output interface, 1x Uart communication interface, SD card holder, 40-pin expansion port and so on. It is a "professional" ZYNQ development platform that can meet the user's various Ethernet high-speed data exchange, data storage, video transmission processing and industrial control requirements, providing the possibility for high-speed Ethernet data transmission and exchange, data processing in the early verification and later application. It is believed that such a product is very suitable for students, engineers and other groups engaged in the development of ZYNQ.



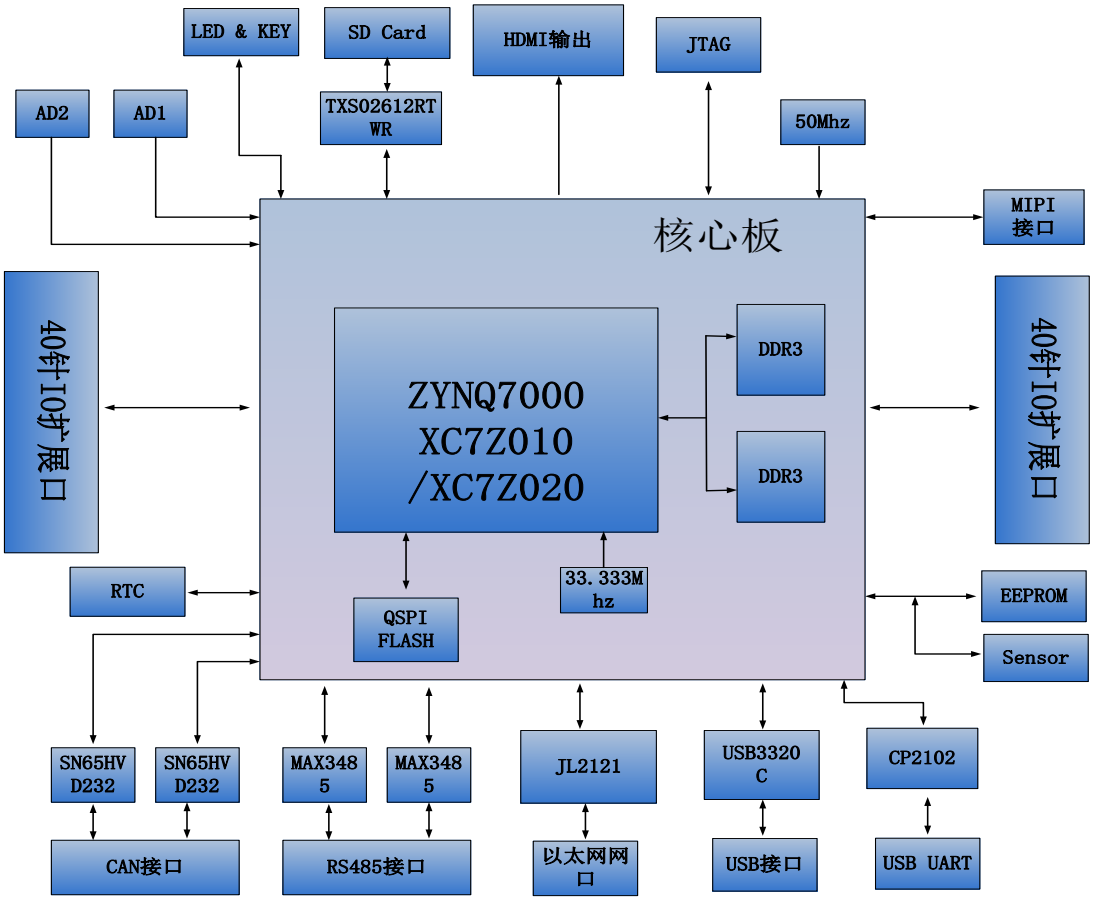
1. AX7Z010B Introduction

The entire structure of the development board designed by inheriting Alinx consistent "core board + carrier board" model. The core board and carrier board are connected using high-speed interboard connectors.

The core board minimum system is mainly composed of the XC7Z010 + 2 DDR3 + QSPI FLASH, which is responsible for the high-speed data processing and storage functions of the ZYNQ system. The data bit width between ZYNQ7010 and two DDR3 chips is 32 bits, and the capacity of two DDR3 chips is up to 512MB. The ZYNQ7010 is based on Xilinx's Zynq7000 series chip, model XC7Z010-1CLG400I. The ZYNQ7010 chip can be divided into a Processor System (PS) and a Programmable Logic (PL).

The carrier board extends the rich peripheral interfaces for the core board, including 1x Gigabit Ethernet interface, 1x USB2.0 HOST interface, 1x HDMI output interface, 1x SD Card interface, and 1x UART USB interface, 1x SD card interface, 1x MIPI interface, 2x CAN bus interfaces, 2x RS485 bus interfaces, 2x AD input interfaces, 2x 40-pin expansion ports and some keys and LEDs.

The following is the structure diagram of the whole development system:



Through this diagram, we can see the interfaces and functions that our development platform contains:

- ZYNQ7000 Core Board
  It is composed of XC7Z010+512MB DDR3 + 256Mb QSPI FLASH and has a 33.333333MHz crystal oscillator to provide the clock to the PS system.
- CAN Communication Interface
  2x CAN bus interface based on TI company's SN65HVD232 chip.
- 485 Communication Interface
  2x 485 communication interface based on MAXIM company's MAX3485 chip.
- Gigabit Ethernet Interface
  1x 10/100M/1000M Ethernet RJ45 interface for Ethernet data exchange with computers or other network devices. The network interface chip uses JLSemi's JL2121 industrial-grade GPHY chip.
- USB2.0 HOST Interface
  1x high-speed USB2.0 HOST interface, which can be used to connect the development board to USB peripherals such as mouse, keyboard, and U disk.
- USB Uart Interface
  1x Uart to USB interface, which can be used to communicate with the computer and is convenient for debugging. The serial chip uses the USB-UAR chip of Silicon Labs CP2102GM, and the USB interface uses the MINI USB interface.
- Micro SD Card Holder
  1x MicroSD card used to store operating system images and file systems.
- AD Analog Input Interface
  2x AD analog input interfaces, in SMA interface form, can be used for analog signal input and voltage conversion. Analog signal voltage input range is 0~10V (Do not input voltage beyond this range).
- 1x HDMI image-video output interface, can achieve 1080P video image transmission.
- One IIC interface EEPROM 24LC04.
- One on-board temperature sensor chip LM75 is used to detect the ambient temperature of the board.
- One MIPI camera interface can be used to connect the ALINX OV5640 camera with MIPI interface (used only by the AX7Z020).
- 1x JTAG Debugging Interface
- 40-pin Expansion Port
  2x 40-pin 0.1-inch pitch expansion ports can be connected to various ALINX modules (binocular camera, TFT LCD screen, high-speed AD module, etc.). The expansion port

contains 1-channel 5V power supply, 2-channel 3.3V power supplies, 3-channel ground, 34 IO ports.

- LED
  7 LEDs (1 on core board, 6 on carrier board). Core board: 1 power LED; Carrier board: 1 power LED, 1 DONE configuration LED, 4 user LEDs.
- 4 User Keys on carrier board.

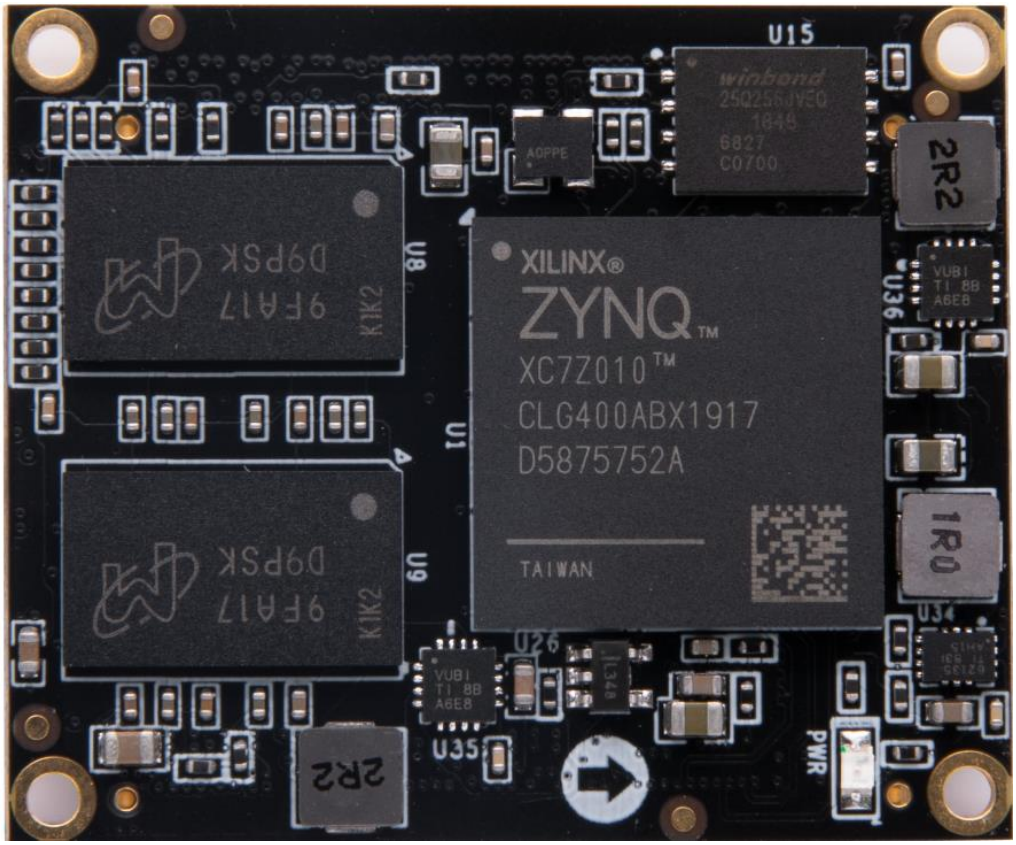
2. AC7Z010 Core Board

2.1 Introduction

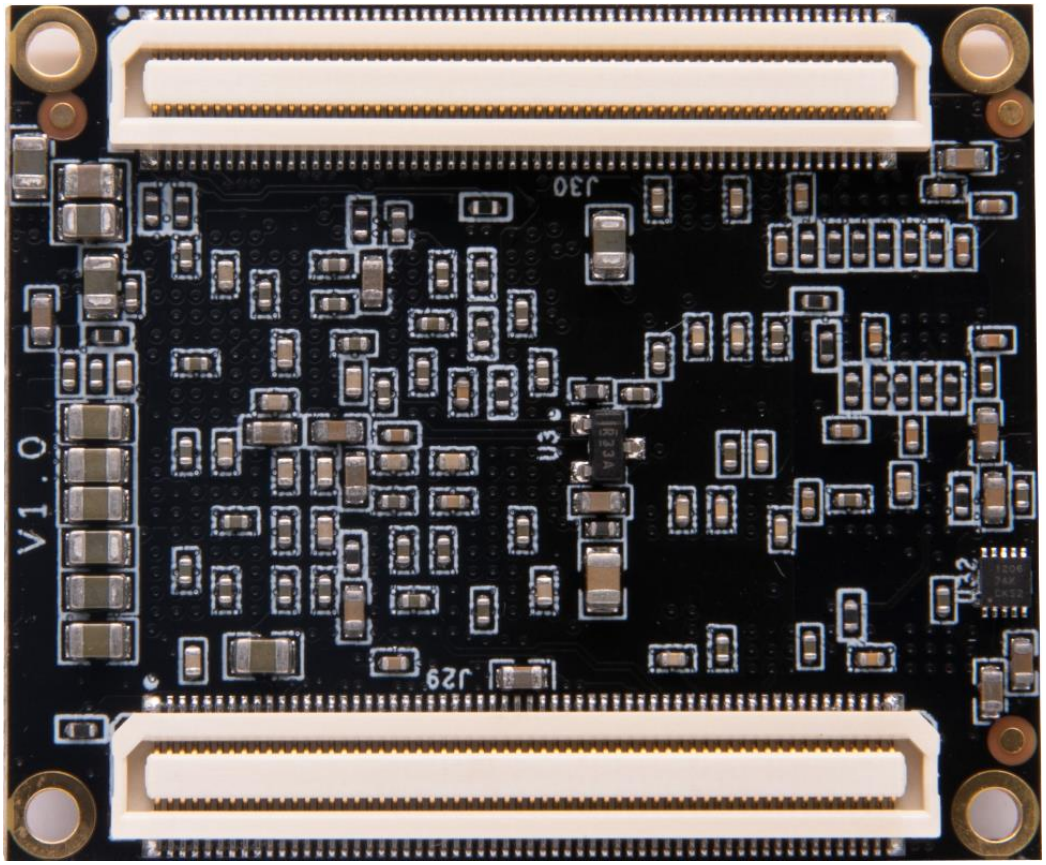
AC7Z010 (core board model, the same below) FPGA core board, ZYNQ chip is based on XC7Z010-1CLG400I of XILINX ZYNQ7000 series. The ZYNQ chip's PS system integrates two ARM CortexTM-A9 processors, AMBA® interconnects, internal memory, external memory interfaces and peripherals. The FPGA of the ZYNQ chip contains a wealth of programmable logic cells, DSP and internal RAM.

This core board uses two Micron's MT41K128M16TW-107 DDR3 chips, each of which has a capacity of 256MB; two DDR chips combine to form a 32-bit data bus width, and the clock frequency of read and write data between ZYNQ and DDR3 can up to 533Mhz. Such configuration can meet the requirements for system's high-bandwidth data processing.

To connect with the carrier board, the two board-to-board connectors on the core board have expanded USB interfaces, Gigabit Ethernet interfaces, SD card slot, and other remaining MIO ports (48) on PS side; and almost all IO ports (100) of BAN34 and BANK35 on the PL side, the IO levels of BANK34 and BANK35 can be provided through the carrier board to meet users' requirements for different level interfaces. For users who need a lot of IO, this core board will be a good choice. And as for the IO connection, the lines between ZYNQ chip and interfaces are processed in equal length and differential length. What's more, the core board size is only 35 * 42 (mm), which is very suitable for secondary development.



AC7Z010 Core Board Front View



AC7Z010 Core Board Back View

2.2 ZYNQ Chip

Based on Xilinx's Zynq7000 series chip XC7Z010-1CLG400I, AC7Z010's PS system integrates two ARM Cortex™-A9 processors, AMBA® interconnects, internal memory, external memory interfaces and peripherals. These peripherals mainly include USB bus interface, Ethernet interface, SD/SDIO interface, I2C bus interface, CAN bus interface, UART interface, GPIO etc. The PS can operate independently and can start up in power-on or reset condition. Figure 2-2-1 detailed the Overall Block Diagram of the ZYNQ7000 Chip.

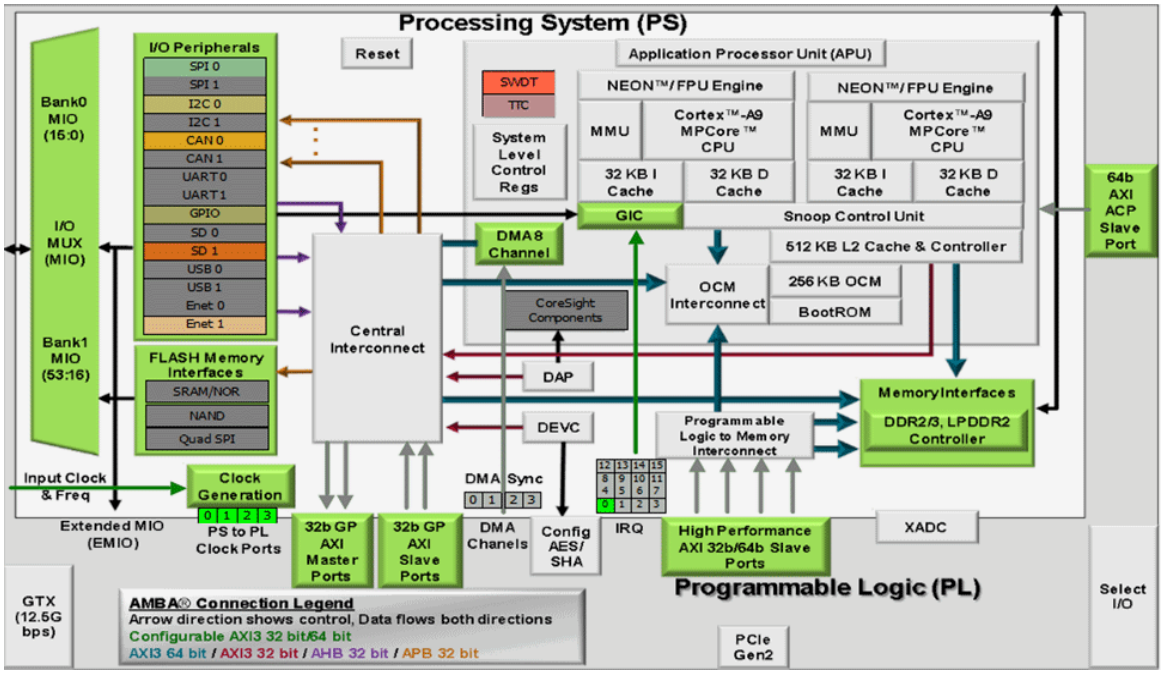


Figure 2-2-1: Overall Block Diagram of the ZYNQ7000 Chip

The main parameters of the PS system are as follows:

- ARM dual-core CortexA9-based application processor, ARM-v7 architecture, up to 1GHz.
- 32KB level-1 instruction and data cache per CPU, 512KB level-2 cache shared by 2 CPUs.
- On-chip boot ROM and 256KB on-chip RAM.
- External storage interface, support 16 / 32bit DDR2, DDR3 interfaces.
- Two Gigabit NIC, support divergent-aggregate DMA, GMII, RGMII, SGMII interfaces.
- Two USB2.0 OTG interfaces, each supporting up to 12 nodes.
- Two CAN2.0B bus interfaces.
- Two SD card, SDIO, MMC compatible controllers.
- Two SPIs, two UARTs, two I2C interfaces.
- 4 pairs of 32bit GPIO, 54 (32 + 22) as PS system IOs, 64 Ios are connected to PL.
- High bandwidth connection within PS and PS to PL.

The main parameters of the PL logic are as follows:

- Logic Cells: 28K;
- LUTs:17600
- Flip-flops: 35200
- 18x25MACCs: 80;
- Block RAM: 240KB;
- Two AD converters for on-chip voltage and temperature sensing and up to 17 external differential input channels, 1MBPS

XC7Z100-1CLG400I chip speed grade is-1, industrial grade, package is BGA400, pin pitch is 0.8mm. The specific chip model naming rule of ZYNQ7000 series is shown in Figure 2-2-2:

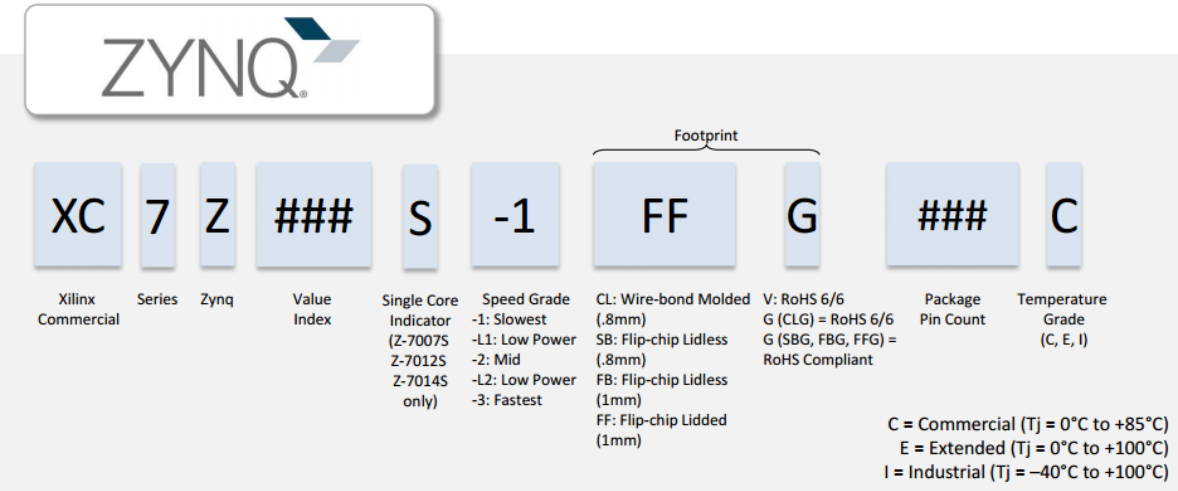


Figure 2-2-2: ZYNQ model naming rules

2.3 DDR3 DRAM

The FPGA core board AC7Z010 is equipped with two Micron DDR3 SDRAM chips (1GB in total), model MT41K128M16TW-107 (Compatible with Hynix H5TQ2G63AFR-PBI). The total bus width of DDR3 SDRAM is 32bit. DDR3 SDRAM can operate at a maximum speed of 533MHz (data rate 1066Mbps). The DDR3 memory system is directly connected to the memory interface of the BANK 502 of the ZYNQ Processing System (PS). The specific configuration of DDR3 SDRAM is shown in Table 2-3-1 below:

Table 2-3-1 DDR3 SDRAM Configuration

Bit Number	Chip Model	Capacity	Manufacturer
U8, U9	MT41K128M16TW-107	256M x 16bit	Micron

The hardware design of DDR3 requires strict consideration of signal integrity. We have fully

considered the matching resistor/terminal resistance, trace impedance control, and trace length control in circuit design and PCB design to ensure high-speed and stable operation of DDR3.

The hardware connection of DDR3 DRAM is shown in Figure 2-3-1:

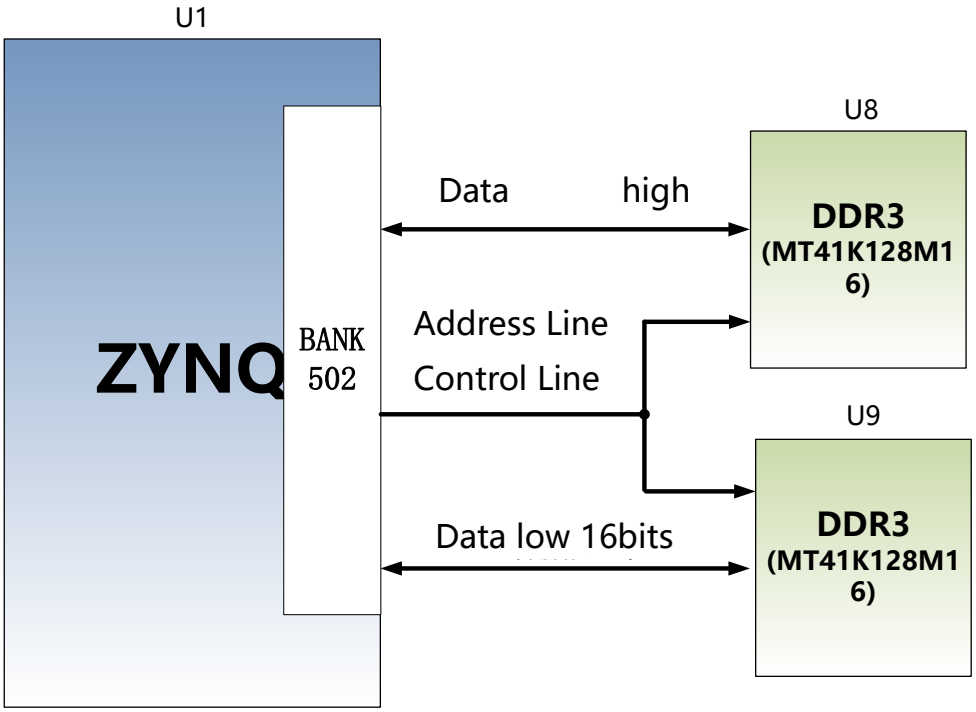


Figure 2-3-1: DDR3 DRAM schematic

DDR3 DRAM pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin No.
DDR3_DQS0_P	PS_DDR_DQS_P0_502	C2
DDR3_DQS0_N	PS_DDR_DQS_N0_502	B2
DDR3_DQS1_P	PS_DDR_DQS_P1_502	G2
DDR3_DQS1_N	PS_DDR_DQS_N1_502	F2
DDR3_DQS2_P	PS_DDR_DQS_P2_502	R2
DDR3_DQS2_N	PS_DDR_DQS_N2_502	T2
DDR3_DQS3_P	PS_DDR_DQS_P3_502	W5
DDR3_DQS4_N	PS_DDR_DQS_N3_502	W4
DDR3_D0	PS_DDR_DQ0_502	C3
DDR3_D1	PS_DDR_DQ1_502	B3
DDR3_D2	PS_DDR_DQ2_502	A2
DDR3_D3	PS_DDR_DQ3_502	A4
DDR3_D4	PS_DDR_DQ4_502	D3

DDR3_D5	PS_DDR_DQ5_502	D1
DDR3_D6	PS_DDR_DQ6_502	C1
DDR3_D7	PS_DDR_DQ7_502	E1
DDR3_D8	PS_DDR_DQ8_502	E2
DDR3_D9	PS_DDR_DQ9_502	E3
DDR3_D10	PS_DDR_DQ10_502	G3
DDR3_D11	PS_DDR_DQ11_502	H3
DDR3_D12	PS_DDR_DQ12_502	J3
DDR3_D13	PS_DDR_DQ13_502	H2
DDR3_D14	PS_DDR_DQ14_502	H1
DDR3_D15	PS_DDR_DQ15_502	J1
DDR3_D16	PS_DDR_DQ16_502	P1
DDR3_D17	PS_DDR_DQ17_502	P3
DDR3_D18	PS_DDR_DQ18_502	R3
DDR3_D19	PS_DDR_DQ19_502	R1
DDR3_D20	PS_DDR_DQ20_502	T4
DDR3_D21	PS_DDR_DQ21_502	U4
DDR3_D22	PS_DDR_DQ22_502	U2
DDR3_D23	PS_DDR_DQ23_502	U3
DDR3_D24	PS_DDR_DQ24_502	V1
DDR3_D25	PS_DDR_DQ25_502	Y3
DDR3_D26	PS_DDR_DQ26_502	W1
DDR3_D27	PS_DDR_DQ27_502	Y4
DDR3_D28	PS_DDR_DQ28_502	Y2
DDR3_D29	PS_DDR_DQ29_502	W3
DDR3_D30	PS_DDR_DQ30_502	V2
DDR3_D31	PS_DDR_DQ31_502	V3
DDR3_DM0	PS_DDR_DM0_502	A1
DDR3_DM1	PS_DDR_DM1_502	F1
DDR3_DM2	PS_DDR_DM2_502	T1
DDR3_DM3	PS_DDR_DM3_502	Y1
DDR3_A0	PS_DDR_A0_502	N2
DDR3_A1	PS_DDR_A1_502	K2
DDR3_A2	PS_DDR_A2_502	M3
DDR3_A3	PS_DDR_A3_502	K3

DDR3_A4	PS_DDR_A4_502	M4
DDR3_A5	PS_DDR_A5_502	L1
DDR3_A6	PS_DDR_A6_502	L4
DDR3_A7	PS_DDR_A7_502	K4
DDR3_A8	PS_DDR_A8_502	K1
DDR3_A9	PS_DDR_A9_502	J4
DDR3_A10	PS_DDR_A10_502	F5
DDR3_A11	PS_DDR_A11_502	G4
DDR3_A12	PS_DDR_A12_502	E4
DDR3_A13	PS_DDR_A13_502	D4
DDR3_A14	PS_DDR_A14_502	F4
DDR3_BA0	PS_DDR_BA0_502	L5
DDR3_BA1	PS_DDR_BA1_502	R4
DDR3_BA2	PS_DDR_BA2_502	J5
DDR3_S0	PS_DDR_CS_B_502	N1
DDR3_RAS	PS_DDR_RAS_B_502	P4
DDR3_CAS	PS_DDR_CAS_B_502	P5
DDR3_WE	PS_DDR_WE_B_502	M5
DDR3_ODT	PS_DDR_ODT_502	N5
DDR3_RESET	PS_DDR_DRST_B_502	B4
DDR3_CLK0_P	PS_DDR_CKP_502	L2
DDR3_CLK0_N	PS_DDR_CKN_502	M2
DDR3_CKE	PS_DDR_CKE_502	N3

2.4 QSPI Flash

The FPGA core board AC7Z010 is equipped with one 256Mb Quad-SPI FLASH chip, model is W25Q256FVEI, which uses the 3.3V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, it can be used as a boot device for the system to store the boot image of the system. These images mainly include FPGA bit files, ARM application code, and other user data files. The specific models and related parameters of QSPI FLASH are shown in Table2-4-1:

Bit Number	Chip Model	Capacity	Manufacturer
U15	W25Q256FVEI	32M Byte	Winbond

Table 2-4-1: QSPI Flash models and parameters

QSPI FLASH is connected to the GPIO port of the BANK500 in the PS of the ZYNQ chip. In the system design, the GPIO port functions of these PS ports need to be configured as the QSPI FLASH interface. Figure 2-4-1 shows the QSPI Flash in the schematic.

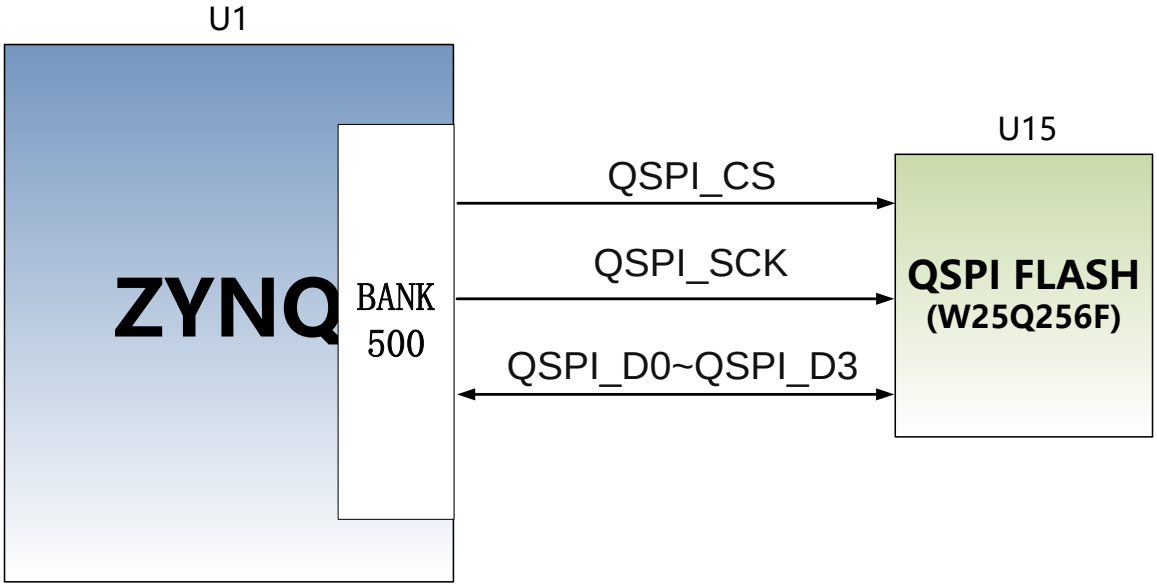


Figure 2-4-1: QSPI Flash connection diagram

Configuration chip pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin No.
QSPI_SCK	PS_MIO6_500	A5
QSPI_CS	PS_MIO1_500	A7
QSPI_D0	PS_MIO2_500	B8
QSPI_D1	PS_MIO3_500	D6
QSPI_D2	PS_MIO4_500	B7
QSPI_D3	PS_MIO5_500	A6

2.5 Clock Configuration

The AC7Z010 core board provides an active clock for the PS system, so that the PS system can work independently. The reference clock on the PL side is provided by the carrier board.

PS system clock source

The ZYNQ chip provides 33.333333MHz clock input for the PS through the X1 crystal on the core board. The clock input is connected to the PS_CLK_500 pin of the ZYNQ chip BANK500. Its schematic diagram is shown in Figure 2-5-1:

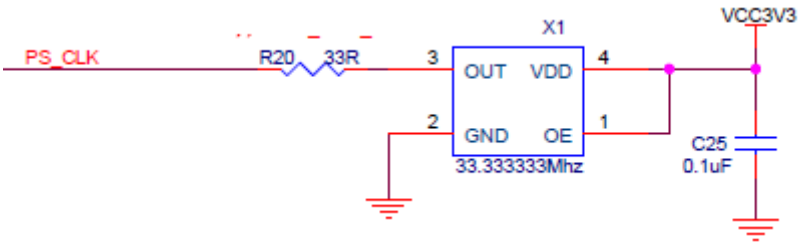


Figure 2-5-1: PS active crystal

Clock pin assignment:

Signal Name	ZYNQ Pin
PS_CLK_500	E7

PL clock source

The PL clock needs to be provided by the carrier board, and there is a 50Mhz clock on the AX7Z010B carrier board to provide a clock reference for the PL. The input of the clock is connected to the U18 pin of BANK34 of ZYNQ chip. Its schematic diagram is shown in Figure 2-5-2:

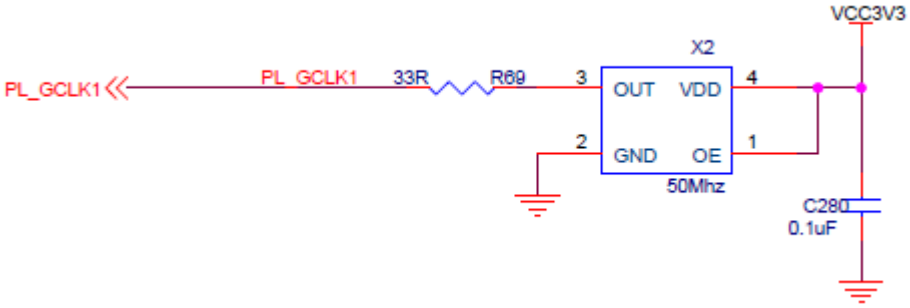


Figure 2-5-2: PL crystal oscillator on carrier board

Clock pin assignment:

Signal Name	ZYNQ Pin
PL_GCLK1	U18

2.6 Power Supply

The power supply voltage of AC7Z010 core board is DC5V, which is supplied by connecting the carrier board. In addition, the power supply of BANK34 and BANK35 is also provided by the carrier board. The power supply design diagram on the board is shown in Figure 2-6-1 below:

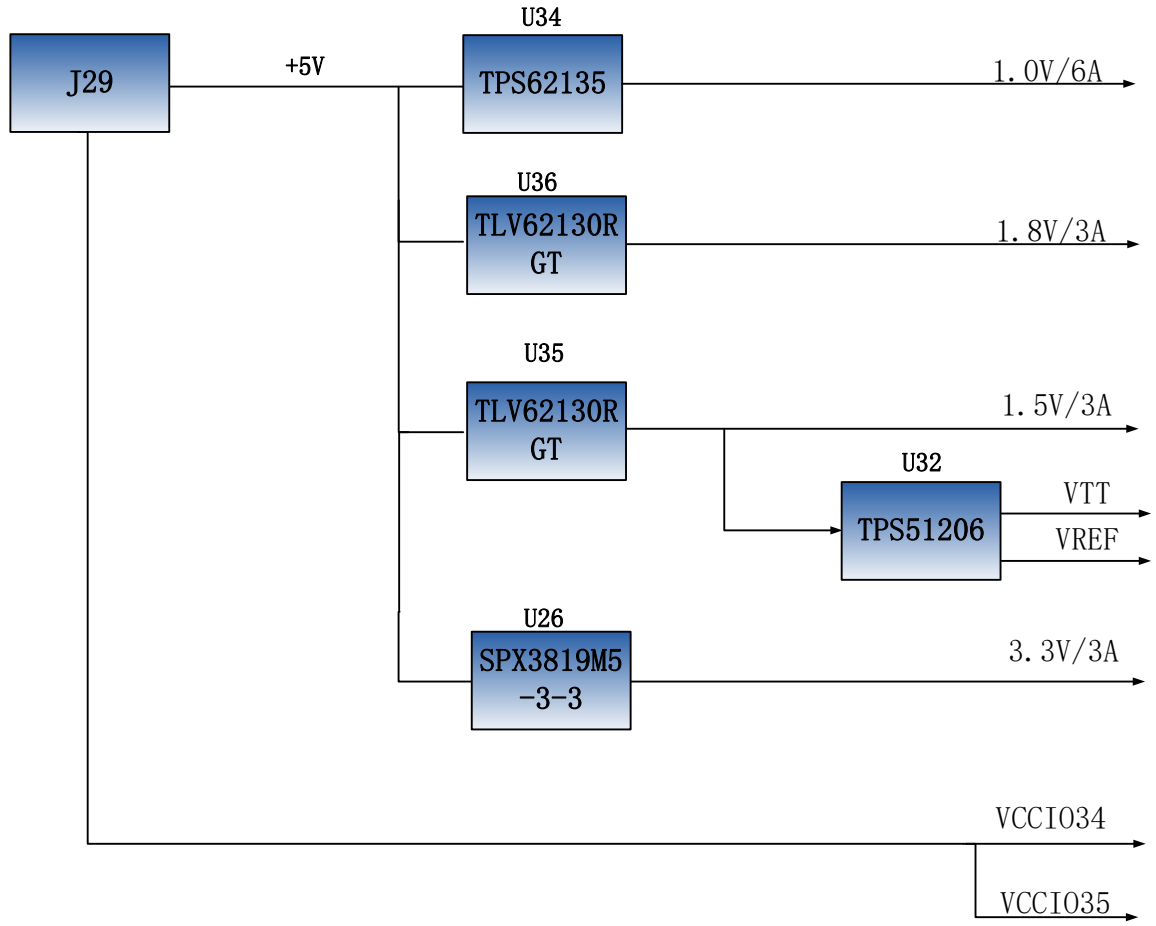


Figure 2-6-1: Power interface in the schematic diagram

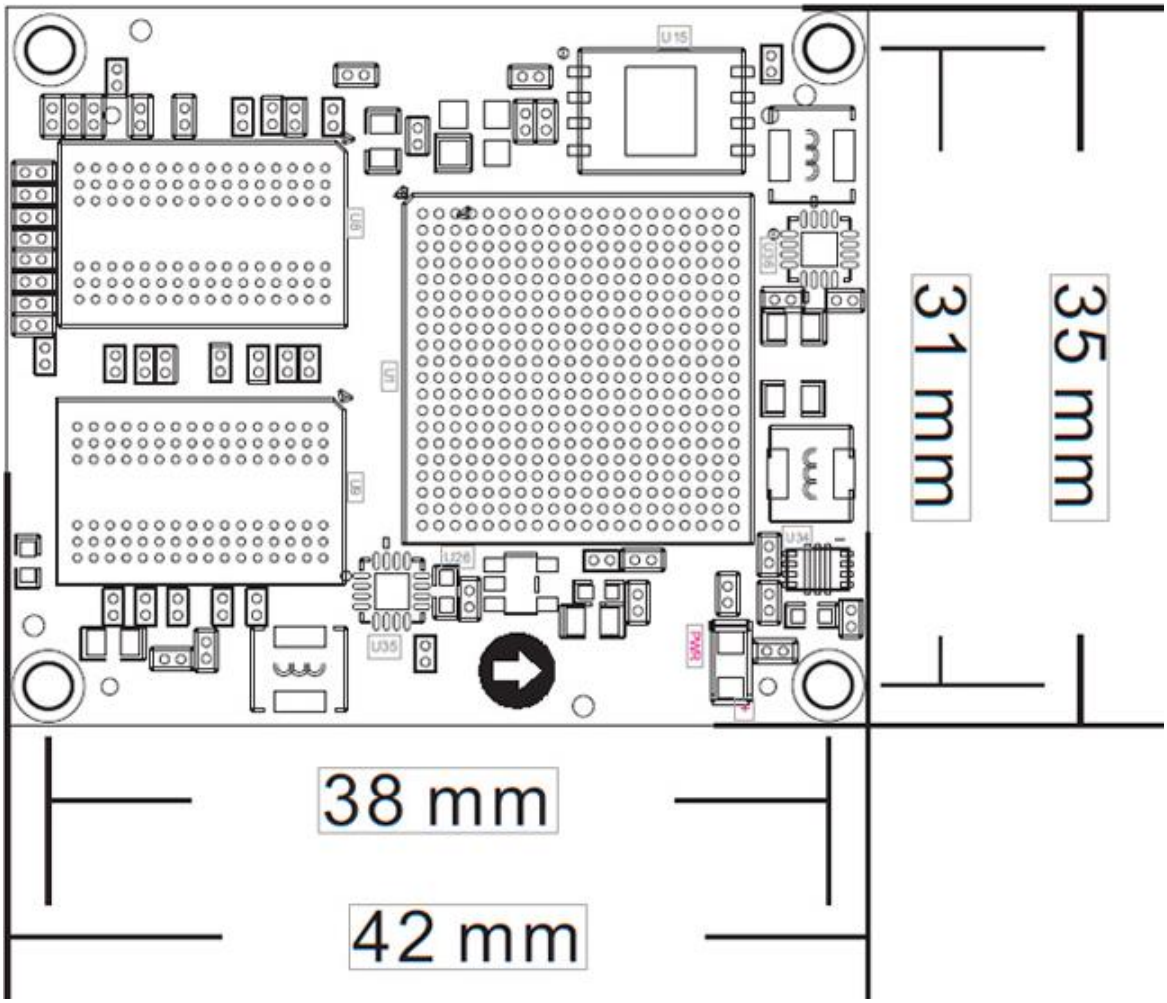
The development board is powered by +5V, converted into +1.0V, +1.8V, +1.5V, +3.3V through the four-channel DC/DC power chip. +1.0V output current can be up to 6A, +1.8V and +1.5V power supplies are 3A, +3.3V is 500mA. The J29 also has four pins each to supply power to the BANK34 and BANK35 of the FPGA, the default is 3.3V, and users can change the power supply of the BANK34 and BANK35 by changing the VCCIO34 and VCCIO35 on the carrier board. 1.5V generates the VTT and VREF voltages required for DDR3 through TI's TPS51206. The functions of each power distribution are shown in the following table:

Power Supply	Function
+1.0V	kernel voltage of ZYNQ PS and PL
+1.8V	ZYNQ PS and PL auxiliary voltage,

	BANK501 IO voltage
+3.3V	ZYNQ Bank0,Bank500，QSIP FLASH, Clock Crystal
+1.5V	DDR3, ZYNQ Bank501
VREF, VTT（+0.75V）	DDR3
VCCIO34/35	Bank34, Bank35

Because the power supply of the ZYNQ FPGA has the power-on sequence requirements, in the circuit design, we have designed according to the power requirements of the chip. The power-on sequence is +1.0V->+1.8V-> (+1.5 V, +3.3V, VCCIO) circuit design to ensure the normal operation of the chip. **Because the level standards of BANK34 and BANK35 are determined by the power supply provided by the carrier board, the highest is 3.3V. When you design the carrier board to provide the VCCIO34 and VCCIO35 powers for the core board, the power-on sequence should be slower than +5V.**

2.7 Size Dimension



Top View

2.8 Connectors Pin Assignment

The core board has a total of two high-speed expansion ports. It uses two 120-pin connectors (J29/J30) to connect to the carrier board. The PIN spacing of the board-to-board connector is 0.5mm, among them, J29 is connected to 5V power, VCCIO power input, some IO signals and JTAG signals, while J30 is connected to the remaining IO signals and MIO. The IO level of BANK34 and BANK35 can be changed by adjusting the VCCIO input on the connector, the highest level does not exceed 3.3V. The AX7Z010B carrier board we designed is 3.3V by default. **Note that the IO of BANK13 is not available for AC7Z010 core board.**

J29 pin assignment:

J29 Pin	Signal Name	ZYNQ Pin Number	J29 Pin	Signal Name	ZYNQ Pin Number
1	VCC5V	-	2	VCC5V	-
3	VCC5V	-	4	VCC5V	-
5	VCC5V	-	6	VCC5V	-
7	VCC5V	-	8	VCC5V	-
9	GND	-	10	GND	-
11	VCCIO_34	-	12	VCCIO_35	-
13	VCCIO_34	-	14	VCCIO_35	-
15	VCCIO_34	-	16	VCCIO_35	-
17	VCCIO_34	-	18	VCCIO_35	-
19	GND	-	20	GND	-
21	IO34_L10P	V15	22	IO34_L7P	Y16
23	IO34_L10N	W15	24	IO34_L7N	Y17
25	IO34_L15N	U20	26	IO34_L17P	Y18
27	IO34_L15P	T20	28	IO34_L17N	Y19
29	GND	-	30	GND	-
31	IO34_L9N	U17	32	IO34_L8P	W14
33	IO34_L9P	T16	34	IO34_L8N	Y14
35	IO34_L12N	U19	36	IO34_L3P	U13
37	IO34_L12P	U18	38	IO34_L3N	V13
39	GND	-	40	GND	-
41	IO34_L14N	P20	42	IO34_L21N	V18
43	IO34_L14P	N20	44	IO34_L21P	V17
45	IO34_L16N	W20	46	IO34_L18P	V16
47	IO34_L16P	V20	48	IO34_L18N	W16

49	GND	-	50	GND	-
51	IO34_L22N	W19	52	IO34_L23P	N17
53	IO34_L22P	W18	54	IO34_L23N	P18
55	IO34_L20N	R18	56	IO34_L13N	P19
57	IO34_L20P	T17	58	IO34_L13P	N18
59	GND	-	60	GND	-
61	IO34_L19N	R17	62	IO34_L11N	U15
63	IO34_L19P	R16	64	IO34_L11P	U14
65	IO34_L24P	P15	66	IO34_L5N	T15
67	IO34_L24N	P16	68	IO34_L5P	T14
69	GND	-	70	GND	-
71	IO34_L4P	V12	72	IO34_L2N	U12
73	IO34_L4N	W13	74	IO34_L2P	T12
75	IO34_L1P	T11	76	IO34_L6N	R14
77	IO34_L1N	T10	78	IO34_L6P	P14
79	GND	-	80	GND	-
81	IO13_L13P	Y7	82	IO13_L21P	V11
83	IO13_L13N	Y6	84	IO13_L21N	V10
85	IO13_L11N	V7	86	IO13_L14N	Y8
87	IO13_L11P	U7	88	IO13_L14P	Y9
89	GND	-	90	GND	-
91	IO13_L19N	U5	92	IO13_L22N	W6
93	IO13_L19P	T5	94	IO13_L22P	V6
95	IO13_L16P	W10	96	IO13_L15P	V8
97	IO13_L16N	W9	98	IO13_L15N	W8
99	GND	-	100	GND	-
101	IO13_L17P	U9	102	IO13_L20P	Y12
103	IO13_L17N	U8	104	IO13_L20N	Y13
105	IO13_L18P	W11	106	IO13_L12N	U10
107	IO13_L18N	Y11	108	IO13_L12P	T9
109	GND	-	110	GND	-
111	FPGA_TCK	F9	112	VP	K9
113	FPGA_TMS	J6	114	VN	L10
115	FPGA_TDO	F6	116	PS_POR_B	C7
117	FPGA_TDI	G6	118	FPGA_DONE	R11
119	NC	-	120	NC	-

J30 pin assignment:

J30 Pin	Signal Name	ZYNQ Pin Number	J30 Pin	Signal Name	ZYNQ Pin Number
1	IO35_L1P	C20	2	IO35_L15N	F20
3	IO35_L1N	B20	4	IO35_L15P	F19
5	IO35_L18N	G20	6	IO35_L5P	E18
7	IO35_L18P	G19	8	IO35_L5N	E19
9	GND	T13	10	GND	T13
11	IO35_L10N	J19	12	IO35_L3N	D18
13	IO35_L10P	K19	14	IO35_L3P	E17
15	IO35_L2N	A20	16	IO35_L4P	D19
17	IO35_L2P	B19	18	IO35_L4N	D20
19	GND	T13	20	GND	T13
21	IO35_L8P	M17	22	IO35_L9N	L20
23	IO35_L8N	M18	24	IO35_L9P	L19
25	IO35_L7P	M19	26	IO35_L6P	F16
27	IO35_L7N	M20	28	IO35_L6N	F17
29	GND	T13	30	GND	T13
31	IO35_L17N	H20	32	IO35_L16N	G18
33	IO35_L17P	J20	34	IO35_L16P	G17
35	IO35_L19N	G15	36	IO35_L13N	H17
37	IO35_L19P	H15	38	IO35_L13P	H16
39	GND	T13	40	GND	T13
41	IO35_L12N	K18	42	IO35_L14N	H18
43	IO35_L12P	K17	44	IO35_L14P	J18
45	IO35_L24N	J16	46	IO35_L20P	K14
47	IO35_L24P	K16	48	IO35_L20N	J14
49	GND	T13	50	GND	T13
51	IO35_L21N	N16	52	IO35_L11P	L16
53	IO35_L21P	N15	54	IO35_L11N	L17
55	IO35_L22N	L15	56	IO35_L23P	M14
57	IO35_L22P	L14	58	IO35_L23N	M15
59	GND	T13	60	GND	T13
61	PS_MIO22	B17	62	PS_MIO50	B13
63	PS_MIO27	D13	64	PS_MIO45	B15
65	PS_MIO23	D11	66	PS_MIO46	D16

67	PS_MIO24	A16	68	PS_MIO41	C17
69	GND	T13	70	GND	T13
71	PS_MIO25	F15	72	PS_MIO7	D8
73	PS_MIO26	A15	74	PS_MIO12	D9
75	PS_MIO21	F14	76	PS_MIO10	E9
77	PS_MIO16	A19	78	PS_MIO11	C6
79	GND	T13	80	GND	T13
81	PS_MIO20	A17	82	PS_MIO9	B5
83	PS_MIO19	D10	84	PS_MIO14	C5
85	PS_MIO18	B18	86	PS_MIO8	D5
87	PS_MIO17	E14	88	PS_MIO0	E6
89	GND	T13	90	GND	T13
91	PS_MIO39	C18	92	PS_MIO13	E8
93	PS_MIO38	E13	94	PS_MIO47	B14
95	PS_MIO37	A10	96	PS_MIO48	B12
97	PS_MIO28	C16	98	PS_MIO49	C12
99	GND	T13	100	GND	T13
101	PS_MIO35	F12	102	PS_MIO52	C10
103	PS_MIO34	A12	104	PS_MIO51	B9
105	PS_MIO33	D15	106	PS_MIO40	D14
107	PS_MIO32	A14	108	PS_MIO44	F13
109	GND	T13	110	GND	T13
111	PS_MIO31	E16	112	PS_MIO15	C8
113	PS_MIO36	A11	114	PS_MIO42	E12
115	PS_MIO29	C13	116	PS_MIO43	A9
117	PS_MIO30	C15	118	PS_MIO53	C11
119	QSPI_D3_PS_MIO5	A6	120	QSPI_D2_PS_MIO4	B7

3. Carrier Board

3.1 Introduction

Through the previous function introduction, you can understand the function of the carrier board:

- 2x CAN communication interfaces
- 2x 485 communication interfaces
- 1x 10/100M/1000M Ethernet RJ-45 interface
- 1x USB HOST interface
- 1x USB Uart communication interface
- 1x SD card slot
- 2x 40-pin expansion port
- 2x AD input interfaces
- 1x HDMI output interface
- 1x MIPI camera interface (only for AX7Z020)
- 1x RTC real-time clock
- 1x EEPROM
- 1x temperature sensor
- JTAG debugging interface
- 4x keys
- 4x user LED lights

3.2 CAN Communication Interface

There are 2 CAN communication interfaces on the AX7Z010B carrier board, which are connected to the GPIO interface of the BANK500 on the PS system side. The CAN transceiver chip uses TI company's SN65HVD232C chip for user CAN communication services.

Figure 3-2-1 shows the connection diagram of the PS CAN transceiver chip:

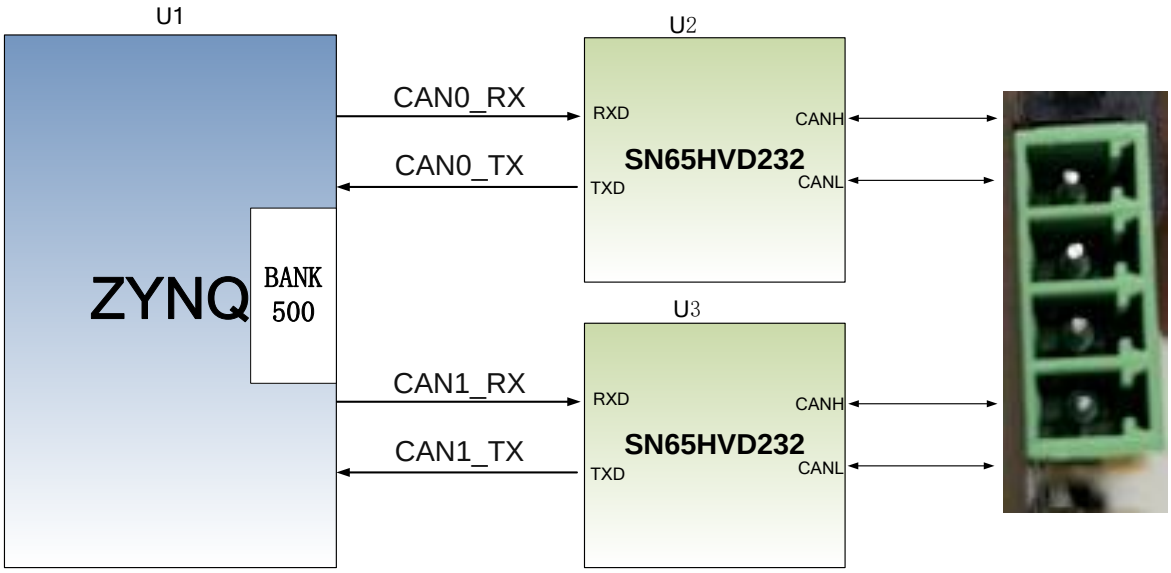


Figure 3-2-1: Connection diagram of PS CAN transceiver chip

CAN communication pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin No.	Description
CAN0_RX	PS_MIO10	E9	CAN0 Receiver
CAN0_TX	PS_MIO11	C6	CAN0 Transmitter
CAN1_RX	PS_MIO13	E8	CAN1 Receiver
CAN1_TX	PS_MIO12	D9	CAN1 Transmitter

3.3 485 Communication Interface

There are two 485 communication interfaces on the AX7Z010B carrier board. Among them, interface 1 is connected to the GPIO interface of BANK500 on the PS system, and interface 2 is connected to the GPIO interface of BANK34 on the PL system.

The 485-transceiver chip uses the MAX3485 chip from MAXIM for the user's 485 communication service.

Figure 3-3-1 shows the connection diagram of PL 485 transceiver chip:

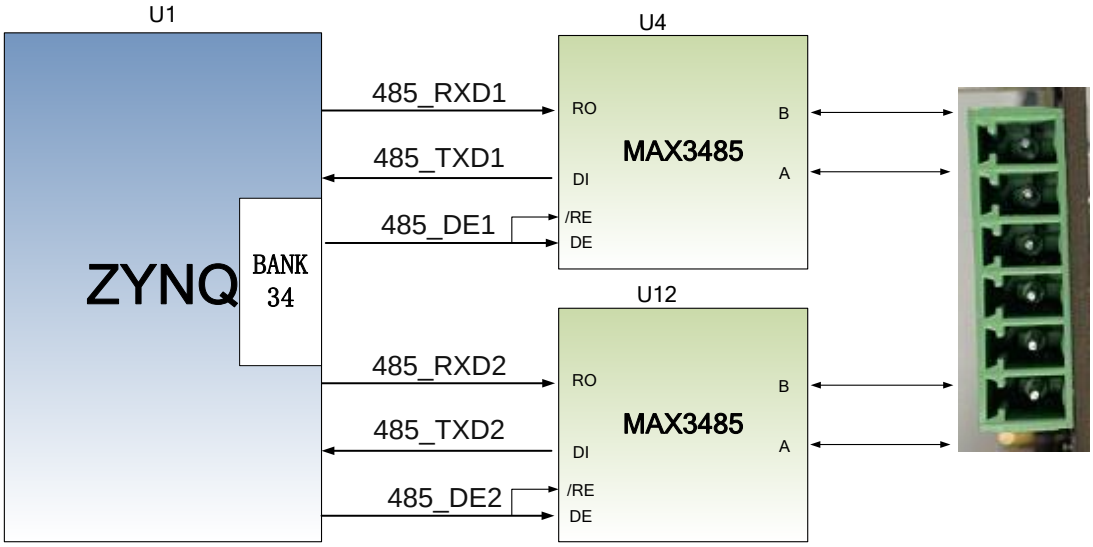


Figure 3-3-1: RS485 chip and interface connection diagram

485 communication pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin No.	Description
485_TXD1	PS_MIO15	C8	485 Receiver 1
485_RXD1	PS_MIO14	C5	485 Transmitter 1
485_DE1	PS_MIO9	B5	485 Receive launch enable 1
485_TXD2	IO34_L4N	W13	485 Transmitter 2
485_RXD2	IO34_L4P	V12	485 Receiver 2
485_DE2	IO34_L12N	U19	485 Receive launch enable 2

3.4 Gigabit Ethernet Interface

The AX7Z010B carrier board has one Gigabit Ethernet interface, which is connected to the GPIO interface of BANK501 on the PS system side. The Ethernet chip uses industrial-grade Ethernet GPHY chip (JL2121-N040I) from JLSemi to provide users with network communication services. The Ethernet PHY chip on the PS side is connected to the MIO interface of PS BANK502 on ZYNQ. The Ethernet PHY chip on the PL side is connected to the IO of BANK66. The JL2121 chip supports 10/100/1000 Mbps network transmission rate and communicates with the MAC layer of MPSOC system through the RGMII interface. JL2121D supports MDI/MDX self-adaption, various speed self-adaption, Master/Slave self-adaption, and supports MDIO bus for PHY register management.

When the JL2121 is powered on, it will detect the level states of some specific IOs to determine its own operating mode. Table 3-4-1 describes the default settings of the GPHY chip after it is powered on.

Table 3-4-1: Default configuration value of GPHY chip

Configuration Pin	Description	Configuration Value
RXD3_ADR0 RXC_ADR1 RXCTL_ADR2	PHY address in MDIO/MDC mode	PHY Address is 001
RXD1_TXDLY	TX clock 2ns delay	Delay
RXD0_RXDLY	RX clock 2ns delay	Delay

When the network is connected to Gigabit Ethernet, the MPSOC and PHY chip JL2121 transmit data via the RGMII bus with a transmission clock of 125Mhz. Data is sampled on the rising edge and falling edge of the clock.

When the network is connected to 100 Gigabit Ethernet, the MPSOC and PHY chip JL2121 transmit data the RMII bus with a transmission clock of 25Mhz. Data is sampled on the rising edge and falling edge of the clock.

Figure 3-4-1 shows the connection diagram of the PS-side Ethernet PHY chip:

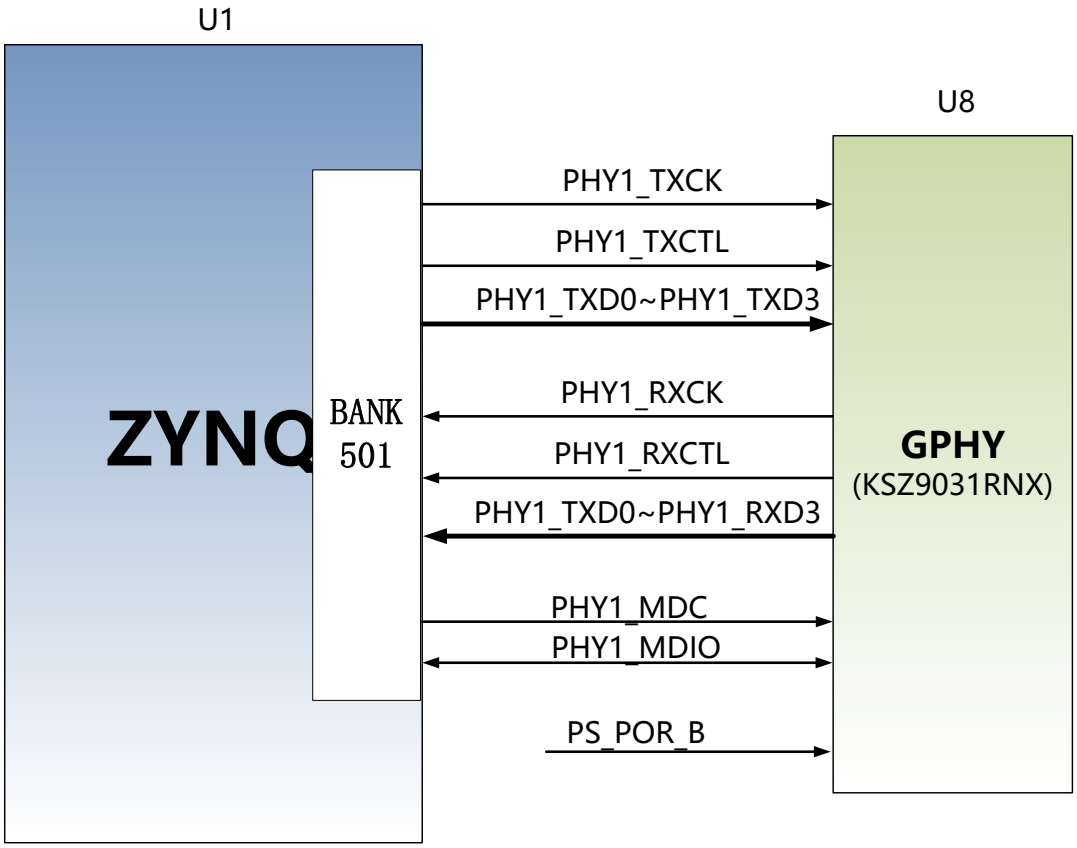


Figure 3-4-1: ZYNQ PS system and GPHY connection diagram

Gigabit Ethernet pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin No.	Description
ETH_TXCK	PS_MIO16	A19	RGMII Transmit Clock
ETH_TXD0	PS_MIO17	E14	Transmit data bit0
ETH_TXD1	PS_MIO18	B18	Transmit data bit1
ETH_TXD2	PS_MIO19	D10	Transmit data bit2
ETH_TXD3	PS_MIO20	A17	Transmit data bit3
ETH_TXCTL	PS_MIO21	F14	Transmit enable signal
ETH_RXCK	PS_MIO22	B17	RGMII Receive Clock
ETH_RXD0	PS_MIO23	D11	Receive data Bit0
ETH_RXD1	PS_MIO24	A16	Receive data Bit1
ETH_RXD2	PS_MIO25	F15	Receive data Bit2
ETH_RXD3	PS_MIO26	A15	Receive data Bit3
ETH_RXCTL	PS_MIO27	D13	Receive data valid signal
ETH_MDC	PS_MIO52	C10	MDIO Management clock
ETH_MDIO	PS_MIO53	C11	MDIO Management data
PS_POR_B	PS_POR_B	C7	Reset signal

3.5 USB2.0 Host Interface

The AX7Z010B has a USB2.0 HOST interface on the carrier board. The USB2.0 transceiver uses a 1.8V, high-speed USB3320C-EZK chip that supports the ULPI standard interface. The USB bus interface of ZYNQ is connected to the USB3320C-EZK transceiver to realize high-speed USB2.0 Host mode data communication. The USB data and control signals of the USB3320C are connected to the IO port of PS BANK501 of the ZYNQ chip. The 24MHz crystal oscillator provides the system clock for the USB3320C chip.

The USB interface is flat-type USB (USB Type A), which allows users to connect different USB Slave peripherals (such as USB mouse and USB keyboard) at the same time. In addition, the carrier board provides+5V power for the USB interface.

The connection diagram between the ZYNQ processor and the USB3320C-EZK chip is shown in 3-5-1:

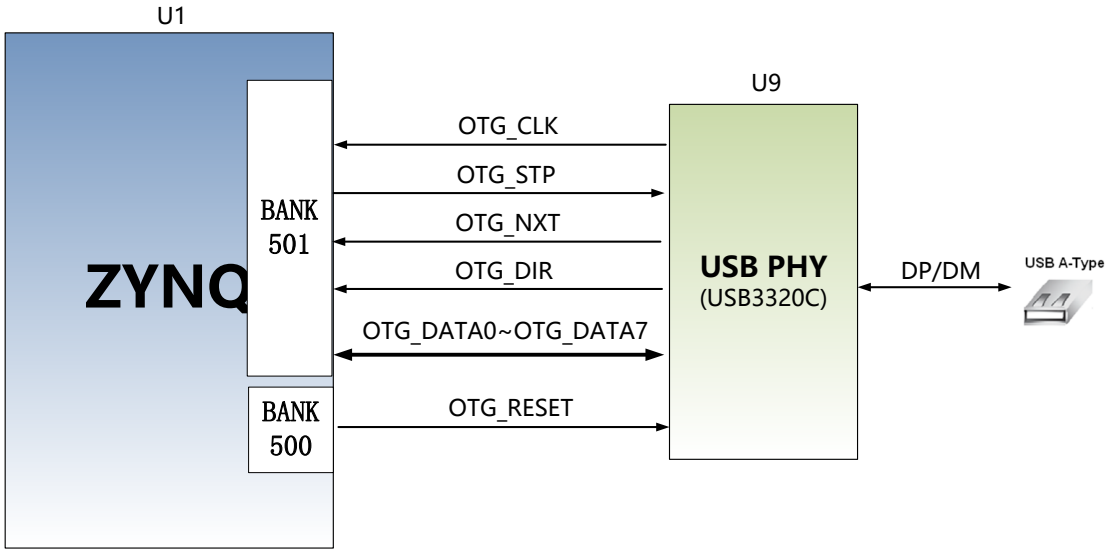


Figure 3-5-1: Connection between Zynq7000 and USB chip

USB2.0 pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin No.	Description
OTG_DATA4	PS_MIO28	C16	USB Data Bit4
OTG_DIR	PS_MIO29	C13	USB Data Direction Signal
OTG_STP	PS_MIO30	C15	USB Stop Signal
OTG_NXT	PS_MIO31	E16	USB Next Data Signal
OTG_DATA0	PS_MIO32	A14	USB Data Bit0
OTG_DATA1	PS_MIO33	D15	USB Data Bit1
OTG_DATA2	PS_MIO34	A12	USB Data Bit2
OTG_DATA3	PS_MIO35	F12	USB Data Bit3

OTG_CLK	PS_MIO36	A11	USB Clock Signal
OTG_DATA5	PS_MIO37	A10	USB Data Bit5
OTG_DATA6	PS_MIO38	E13	USB Data Bit6
OTG_DATA7	PS_MIO39	C18	USB Data Bit7
OTG_RESETN	PS_MIO46	D16	USB Reset Signal

3.6 Uart to USB Interface

The AX7Z010B FPGA carrier board is equipped with a Uart to USB interface for overall debugging of ZYNQ7000 system. The conversion chip uses the USB-UAR chip of Silicon Labs CP2102GM. The USB interface uses the MINI USB interface, and can be connected to the USB port of the upper PC with a USB cable for separate power supply and serial data communication of the core board.

The schematic diagram of USB Uart circuit design is shown in Figure 3-6-1:

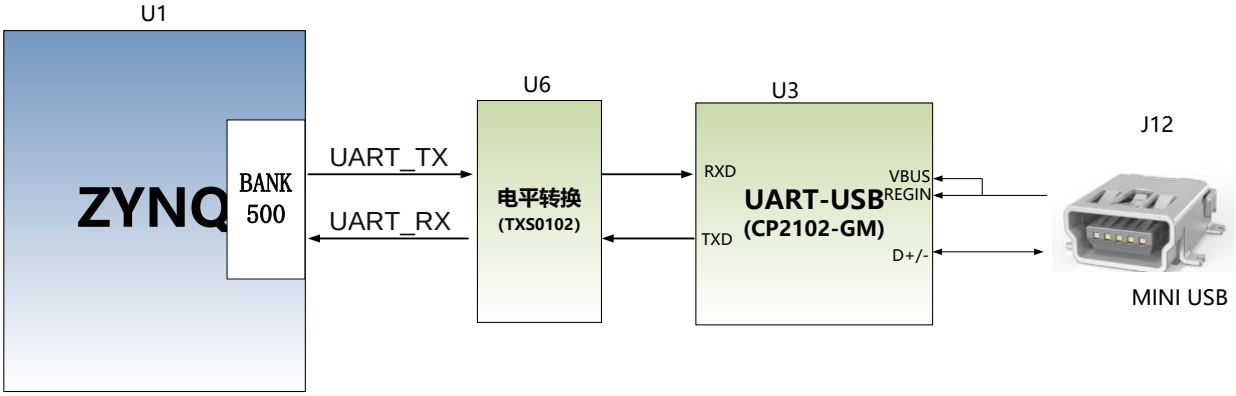


Figure 3-6-1: USB to serial port diagram

UART-USB ZYNQ pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin No.	Description
UART_RX	PS_MIO49	C12	Uart data input
UART_TX	PS_MIO48	B12	Uart data output

3.7 AD Input Interface

The AX7Z010B carrier board is equipped with four AD input interfaces, two of which are used to collect external analog signals for AD conversion, and the other two are used to measure the power supply voltage and current of the development board. The 2-channel analog signal used to collect the external analog signals use the SMA connector as the input, converts the input signal into a differential signal, and then inputs them into ZYNQ. Power

current measurement is connected to ZYNQ's dedicated AD input pins VP and VN.

The schematic diagram of AD acquisition circuit design is shown in Figure 3-7-1:

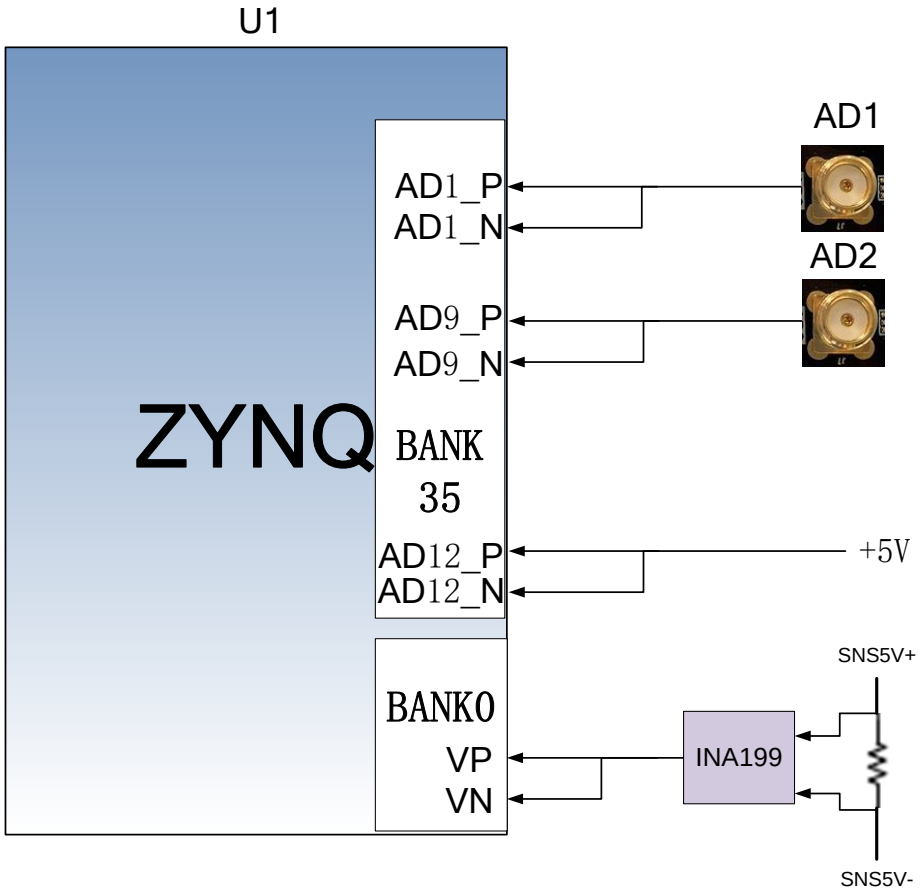


Figure 3-7-1: Acquisition circuit design schematic diagram

ZYNQ pin assignment for AD acquisition circuit:

Signal Name	ZYNQ Pin Name	ZYNQ Pin No.	Description
XADC_AD1P	IO35_L3P	E17	AD_IN_P
XADC_AD1N	IO35_L3N	D18	AD_IN_N
XADC_AD9P	IO35_L5P	E18	AD_IN_P
XADC_AD9N	IO35_L5N	E19	AD_IN_N
XADC_AD12P	IO35_L15P	F19	AD_IN_P
XADC_AD12N	IO35_L15N	F20	AD_IN_N
VP	VP	K9	AD_IN_P
VN	VN	L10	AD_IN_N

3.8 HDMI Output Interface

HDMI (High-Definition Multimedia Video Output Interface). The AX7Z010B development board directly connects to the differential signal and clock of the HDMI interface through the differential IO of ZYNQ, implements the differential conversion of HMDI signals into parallel and then codec in ZYNQ, and implements the transmission solution of DMI digital video input and output, supports up to 1080P@60Hz input and output functions.

The HDMI signal is connected to the PL BANK34 of ZYNQ, the design schematic is shown in Figure 3-8-1 below:

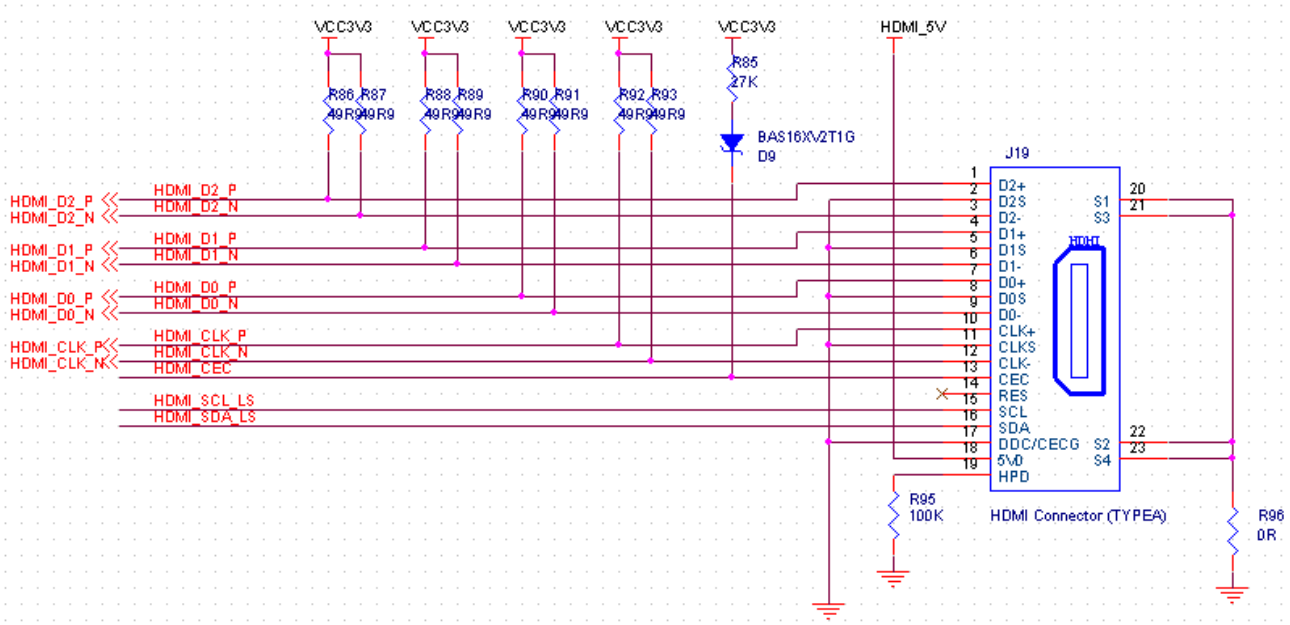


Figure 3-8-1: Design schematic of HDMI interface

ZYNQ pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin No.	Description
HDMI_CLK_P	IO34_L3P	U13	HDMI clock signal, Positive
HDMI_CLK_N	IO34_L3N	V13	HDMI clock signal, Negative
HDMI_D0_P	IO34_L8P	W14	HDMI data 0, Positive
HDMI_D0_N	IO34_L8N	Y14	HDMI data 0, Negative
HDMI_D1_P	IO34_L17P	Y18	HDMI data 1, Positive
HDMI_D1_N	IO34_L17N	Y19	HDMI data 1, Negative
HDMI_D2_P	IO34_L7P	Y16	HDMI data 2, Positive
HDMI_D2_N	IO34_L7N	Y17	HDMI data 2, Negative
HDMI_SCL	IO34_L21N	V18	HDMI IIC Clock
HDMI_SDA	IO34_L21P	V17	HDMI IIC Data

3.9 MIPI Camera Interface (Only for AX7Z020B)

The AX7Z010B has a MIPI camera interface on the carrier board, which can be used to connect to ALINX MIPI OV5640 camera module. The circuit schematic diagram of the MIPI interface part is shown in Figure 3-9-1 below:

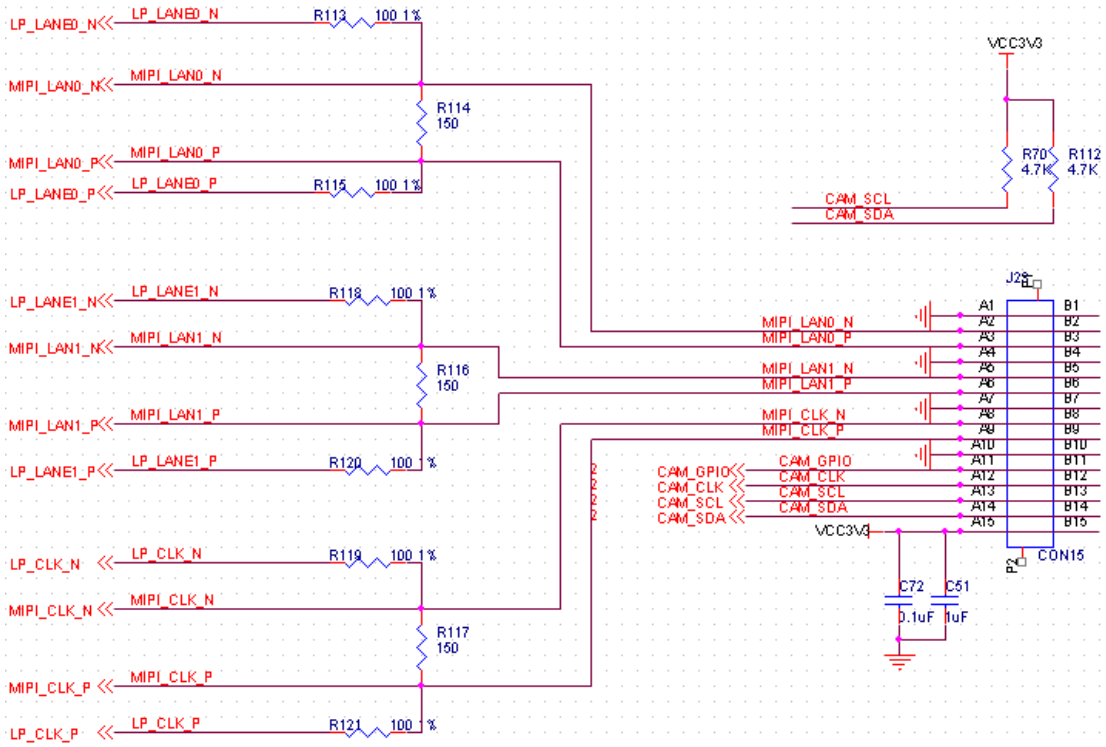


Figure 3-9-1: HDMI interface design schematic

MIPI interface pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin No.	Description
LP_CLK_P	IO13_L15P	V8	Clock in Low Power mode, Positive
LP_CLK_N	IO13_L15N	W8	Clock in Low Power mode, Negative
LP_LANE0_P	IO13_L12P	T9	LANE0 in Low Power mode, Positive
LP_LANE0_N	IO13_L12N	U10	LANE0 in Low Power mode, Negative
LP_LANE1_P	IO13_L20P	Y12	LANE1 in Low Power mode, Positive
LP_LANE1_N	IO13_L20N	Y13	LANE1 in Low Power mode, Negative
MIPI_CLK_P	IO13_L13P	Y7	Clock in High Speed mode, Positive
MIPI_CLK_N	IO13_L13N	Y6	Clock in High Speed mode, Negative
MIPI_LAN0_P	IO13_L18P	W11	LANE0 in High Speed mode, Positive
MIPI_LAN0_N	IO13_L18N	Y11	LANE0 in High Speed mode, Negative
MIPI_LAN1_P	IO13_L17P	U9	LANE1 in High Speed mode, Positive
MIPI_LAN1_N	IO13_L17N	U8	LANE1 in High Speed mode, Negative

CAM_GPIO	IO13_L11P	U7	GPIO control for camera
CAM_CLK	IO13_L11N	V7	clock input for camera
CAM_SCL	IO13_L19P	T5	I2C clock for camera
CAM_SDA	IO13_L19N	U5	I2C data for camera

3.10 SD Card Slot

The AX7Z010B has a Micro-type SD card interface to provide users access to the SD card memory for storing ZYNQ chip BOOT programs, Linux operating system kernel, file system, and other user data files.

The SDIO signal is connected to the IO signal of ZYNQ's PS BANK501. Because the BANK's VCCMIO is set to 1.8V, while the SD card's data level is 3.3V, so here, we use the TXS02612 level converter to connect them. The schematic diagram of Zynq7000 PS and SD card connectors is shown in Figure 3-10-1:

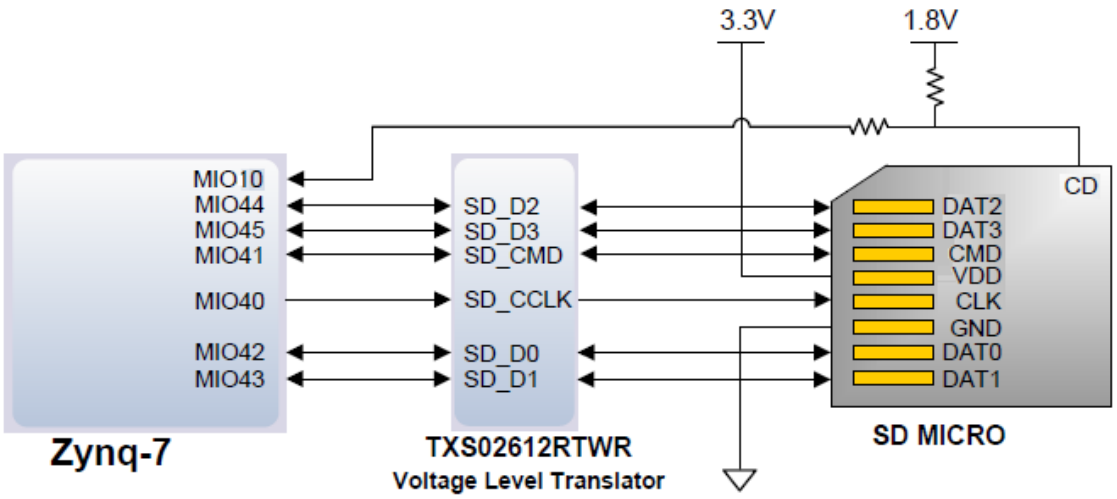


Figure 3-10-1: SD card connection diagram

SD card slot pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin No.	Description
SD_CLK	PS_MIO40	D14	SD clock signal
SD_CMD	PS_MIO41	C17	SD command signal
SD_D0	PS_MIO42	E12	SD data Data0
SD_D1	PS_MIO43	A9	SD data Data1
SD_D2	PS_MIO44	F13	SD data Data2
SD_D3	PS_MIO45	B15	SD Data Data3
SD_CD	PS_MIO47	B14	SD card insertion signal

3.11 EEPROM

The AX7Z010B development board carries an EEPROM on board. The EEPROM model is 24LC04 with a capacity of 4 Kbit (2 * 256 * 8 bit) and consists of two 256byte blocks that communicate via the IIC bus. EEPROM is set to learn the communication mode of IIC bus. The I2C signal of the EEPROM is connected to the I2C interface of the ZYNQ PS. Figure 3-11-1 shows the connection diagram of EEPROM.

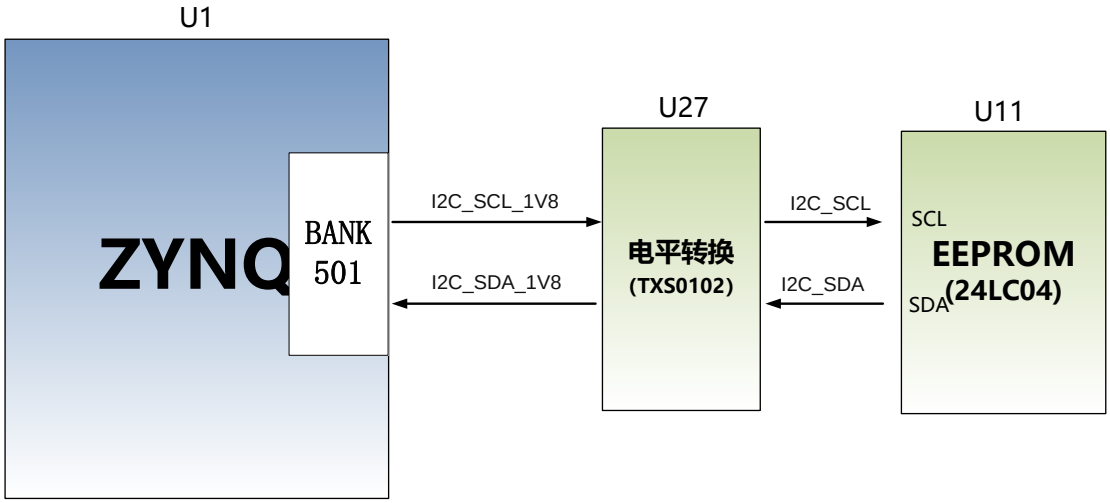


Figure 3-11-1: EEPROM connection diagram

EEPROM pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin No.	Description
I2C_SCL_1V8	MIO50	B13	IIC clock signal
I2C_SDA_1V8	MIO51	B9	IIC data signal

3.12 Real-time Clock

The AX7Z010B carries a real-time clock RTC chip, model DS1338, whose function is to provide calendar (including year, month, day, minute, second and week) till 2099. If time is needed in the system, then RTC needs to be involved in the production. It needs to connect a 32.768KHz passive clock externally to provide an accurate clock source to the clock chip, so that RTC can accurately provide clock information to the product.

At the same time, in order to ensure the normal operation of the real-time clock after the power failure of the product, it is generally necessary to equip another battery to supply power to the clock chip. BT1 is the battery holder. After we put the button battery (model CR1220, voltage is 3V) into the system, the button battery can also supply power to DS1338 when the system loses its own battery. In such way, whether the product is powered or not, the DS1302 will operate without interruption, providing continuous time information. The interface signals of the RTC and EEPORM share the I2C bus. Figure 3-12-1 shows the connection diagram of DS1338:

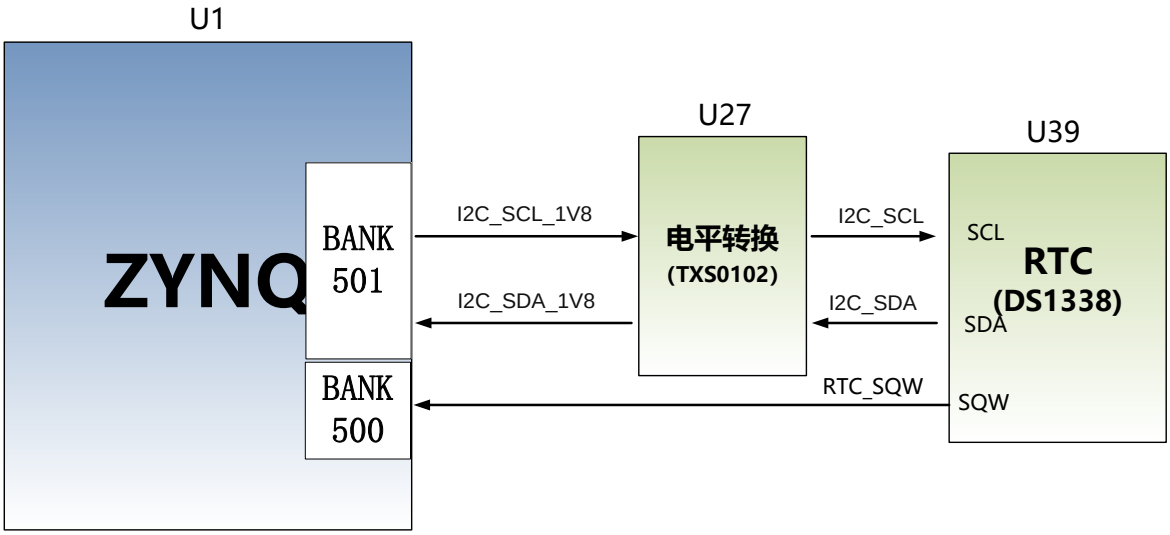


Figure 3-12-1: DS1338 schematic diagram

DS1338 interface pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin No.	Description
I2C_SCL_1V8	MIO50	B13	RTC clock signal
I2C_SDA_1V8	MIO51	B9	RTC reset signal
RTC_SQW	MIO7	D8	Square wave output signal

3.13 Temperature Sensor

The AX7Z010B development board is equipped with a high-precision, low-power, digital temperature sensor chip, model LM75 from ON Semiconductor company. The temperature accuracy of the LM75 chip is 0.5 degrees, the sensor and FPGA are directly use I2C digital interfaces, and ZYNQ7010 reads the temperature near the development board through the I2C interface. The interface signals of the LM75 sensor share the I2C bus with the EEPORM. Figure 3-13-1 shows the connection diagram of the LM75 sensor:

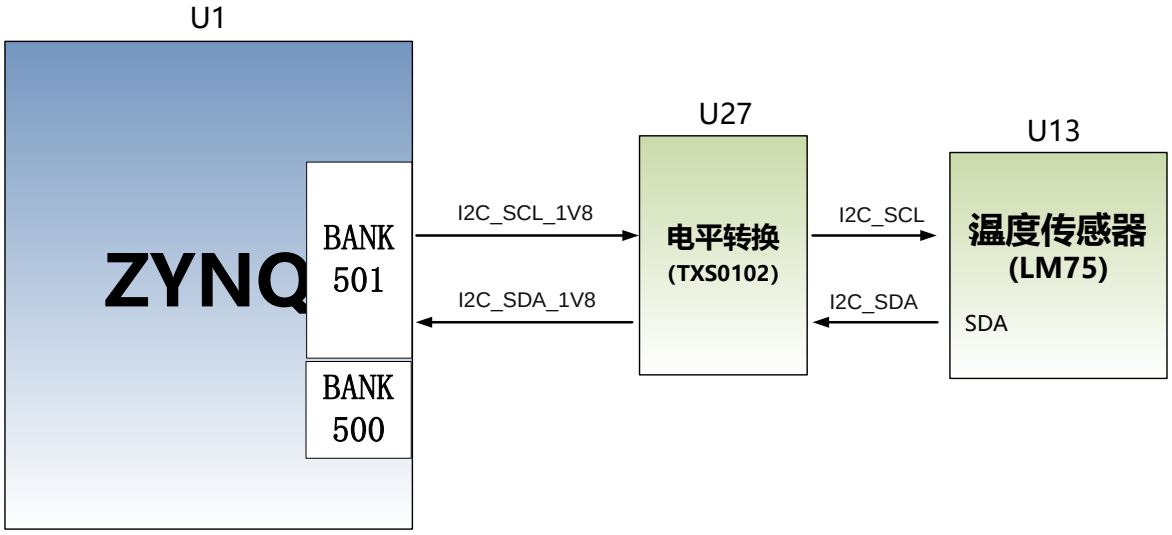


Figure 3-13-1: LM75 sensor connection diagram

3.14 JTAG Interface

The downloading and debugging circuit of JTAG is reserved on the AX7Z010B carrier board to extract JTAG debugging signals, TCK, TDO, TMS, and TDI. Figure 3-14-1 is the schematic diagram of the JTAG port on the development board:

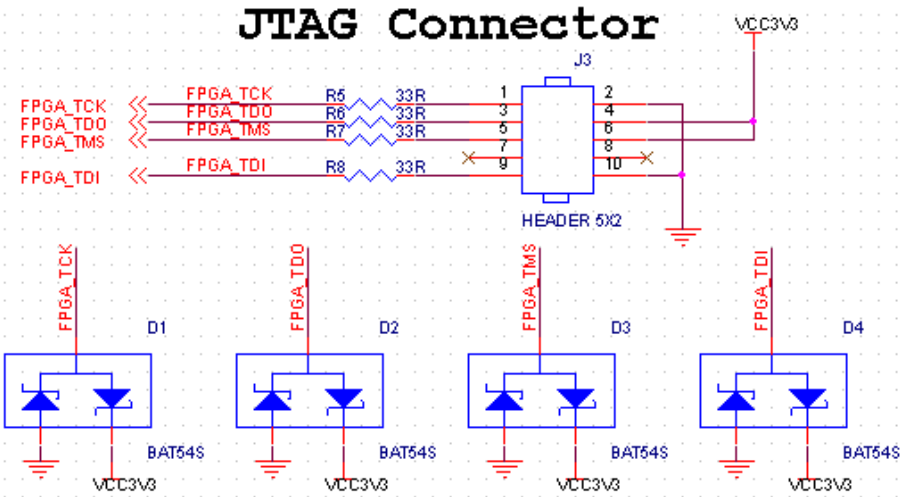


Figure 3-14-1: JTAG interface in schematic diagram

3.15 User LED

The AX7Z010B carrier board has 4 user LED lights (LED1~LED4), which are all connected to the IO of PL BANK35. Users can control the on and off of LEDs through the program. When the IO voltage of the connected user LED is high, the user LED light will be turned off, when the IO voltage is low, the user LED will be turned on. The schematic diagram of LED light hardware connection is shown in Figure 3-15-1:

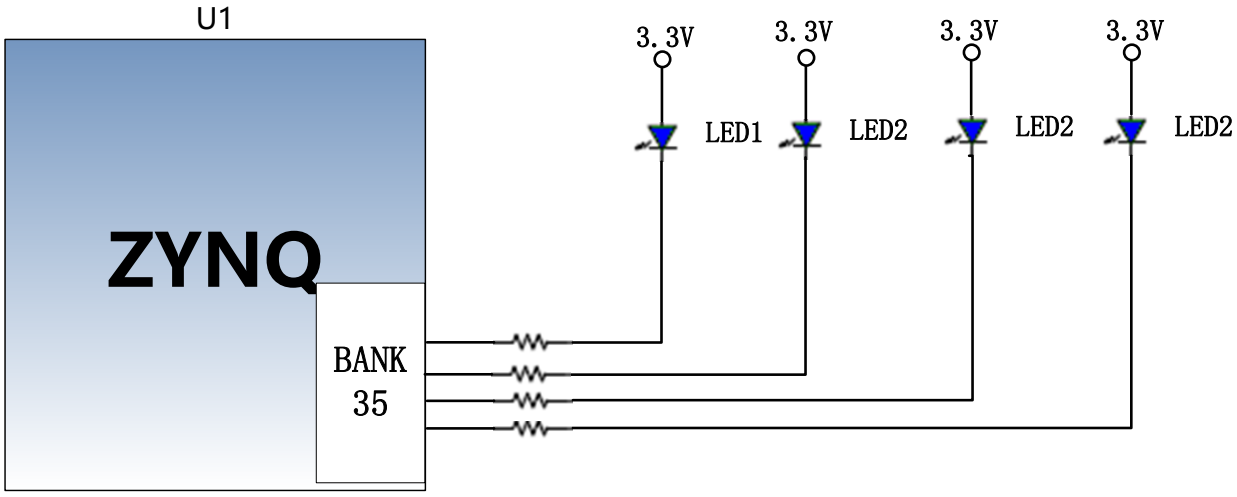


Figure 3-15-1: LED light hardware connection diagram

User LED light pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin No.	Description
LED1	IO35_L20N	J14	User LED1
LED2	IO35_L20P	K14	User LED2
LED3	IO35_L14P	J18	User LED3
LED4	IO35_L14N	H18	User LED4

3.16 User Keys

There are four user keys (KEY1 to KEY4) on the AX7Z010B carrier board. All four user keys are connected to the IO of BANK35 on the PL side. When the key is pressed, the signal will be low. The ZYNQ chip will determine whether the key is pressed by detecting whether the level is low. The diagram of user key connection is shown in Figure 3-16-1:

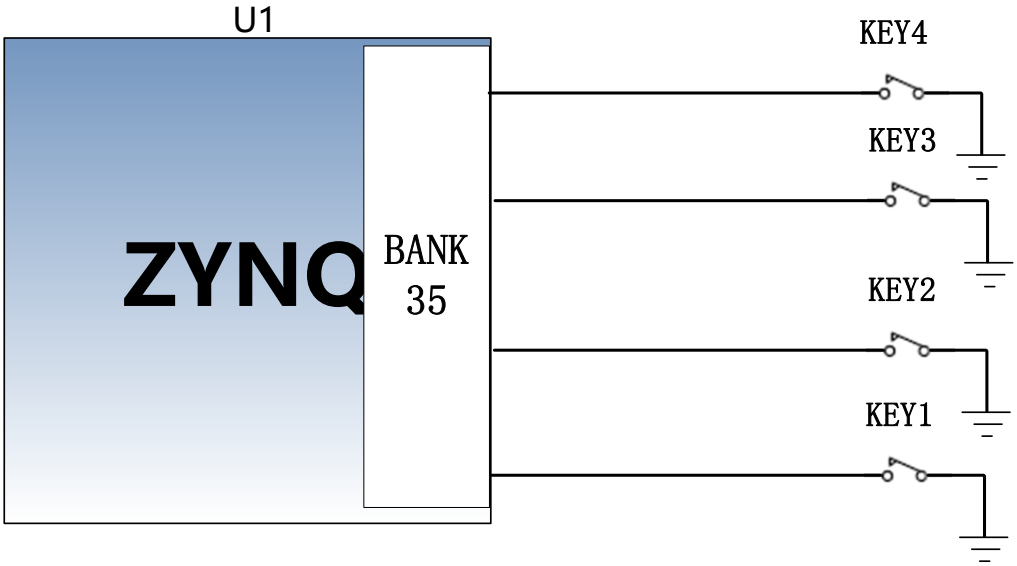


Figure 3-16-1: User key connection diagram

User key ZYNQ pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin No.	Description
KEY1	IO35_L23N	M15	User KEY1
KEY2	IO35_L23P	M14	User KEY2
KEY3	IO35_L11N	L17	User KEY3
KEY4	IO35_L11P	L16	User KEY4

3.17 Expansion Port

The AX7Z010B carrier board reserves two 40-pin expansion ports J20 and J21 with 2.54mm standard pitch, which are used to connect AlLINX modules or the external circuit designed by the user. The expansion port has 40 signals, including one 5V power supply, two 3.3V power supplies, three ground channels, and 34 IO ports. **Do not connect IO directly to a 5V device to avoid burning the ZYNQ7000 chip. If you want to connect a 5V device, you need to connect the level conversion chip.**

The circuit of the expansion port (J20) is shown in Figure 3-17-1 below:

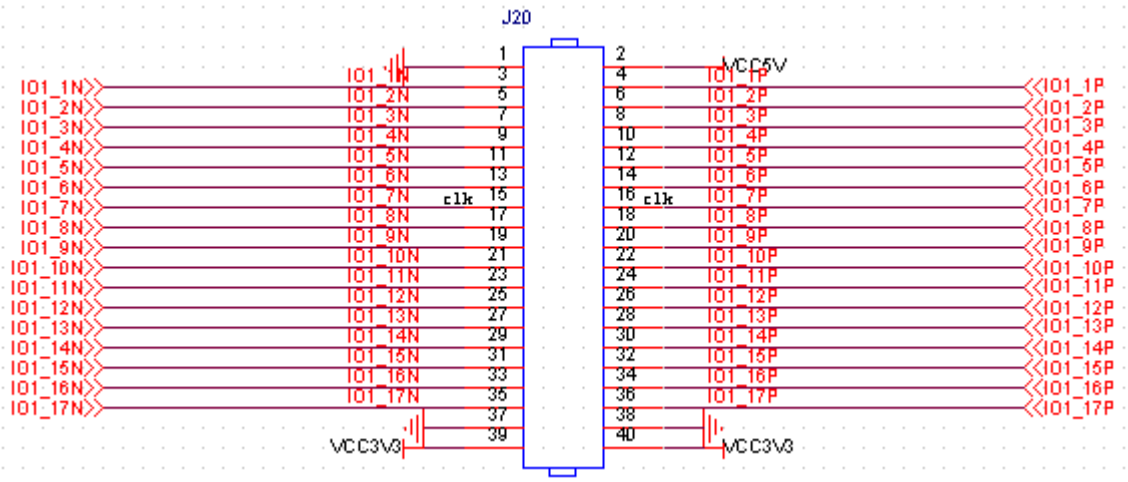


Figure 3-17-1: J20 schematic diagram

J20 ZYNQ pin assignment:

Pin No.	ZYNQ Pin	Pin No.	ZYNQ Pin
1	GND	**2**	+5V
3	R14	**4**	P14
5	U12	**6**	T12
7	T15	**8**	T14
9	T11	**10**	T10
11	U15	**12**	U14
13	P19	**14**	N18
15	R17	**16**	R16
17	P15	**18**	P16
19	N17	**20**	P18
21	V16	**22**	W16
23	R18	**24**	T17
25	W19	**26**	W18
27	W20	**28**	V20
29	P20	**30**	N20
31	U17	**32**	T16
33	U20	**34**	T20
35	V15	**36**	W15
37	GND	**38**	GND
39	+3.3V	**40**	+3.3V

The circuit of the expansion port (J21) is shown in Figure 3-17-2 below:

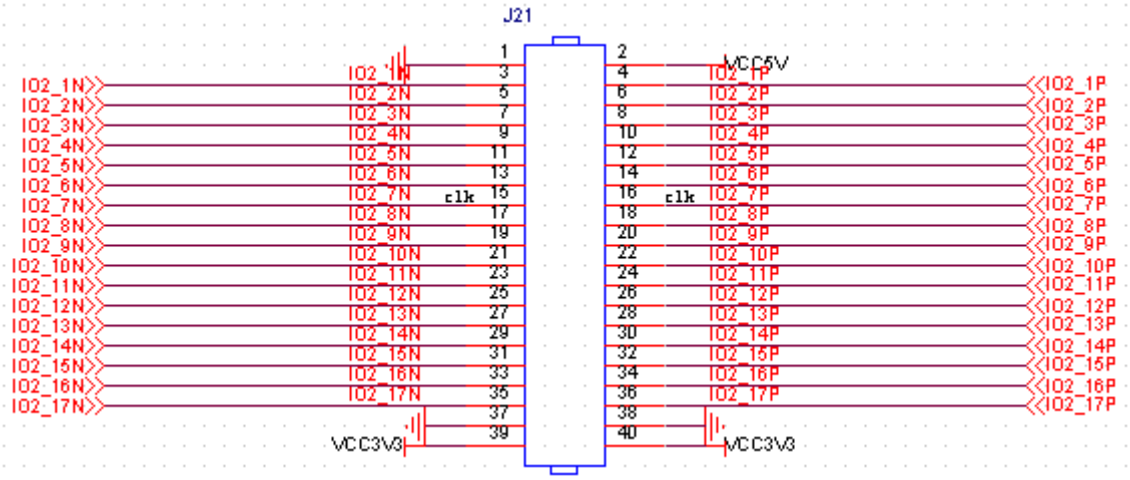


Figure 3-17-2: J21 schematic diagram

J21 ZYNQ pin assignment:

Pin No.	ZYNQ Pin	Pin No.	ZYNQ Pin
1	GND	**2**	+5V
3	M18	**4**	M17
5	K19	**6**	J19
7	B19	**8**	A20
9	B20	**10**	C20
11	G19	**12**	G20
13	M19	**14**	M20
15	D20	**16**	D19
17	L20	**18**	L19
19	F16	**20**	F17
21	H20	**22**	J20
23	G18	**24**	G17
25	H17	**26**	H16
27	G15	**28**	H15
29	K18	**30**	K17
31	J16	**32**	K16
33	N16	**34**	N15
35	L15	**36**	L14
37	GND	**38**	GND
39	+3.3V	**40**	+3.3V

3.18 Power Supply

The power input voltage of the development board is DC5V, please use the power supply of the development board, do not use other power supplies to avoid damage to the development board. The power on the carrier board is converted into 1.8V, +3.3V and VCCIO35 power supplies through two-channel DC/DC power chip ETA1471 and the one-channel LDO power chip SPX3819M5-ADJ.

The IO level of the BANK35 on ZYNQ7010 can be adjusted by the jumper cap on the carrier board. By default, if no jumper cap is installed on J28 and J29, the IO level of the BANK35 is 3.3V. If the J29 has a jumper cap installed, the IO level of the BANK35 is 1.8V. If the J28 has a jumper cap installed, the IO level of the BANK35 is 2.5V.

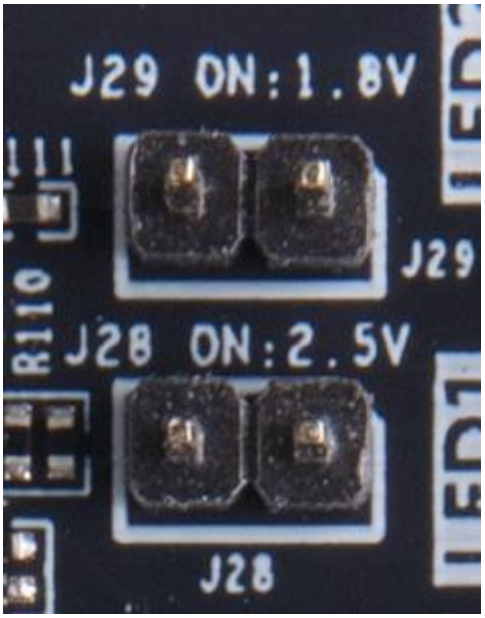
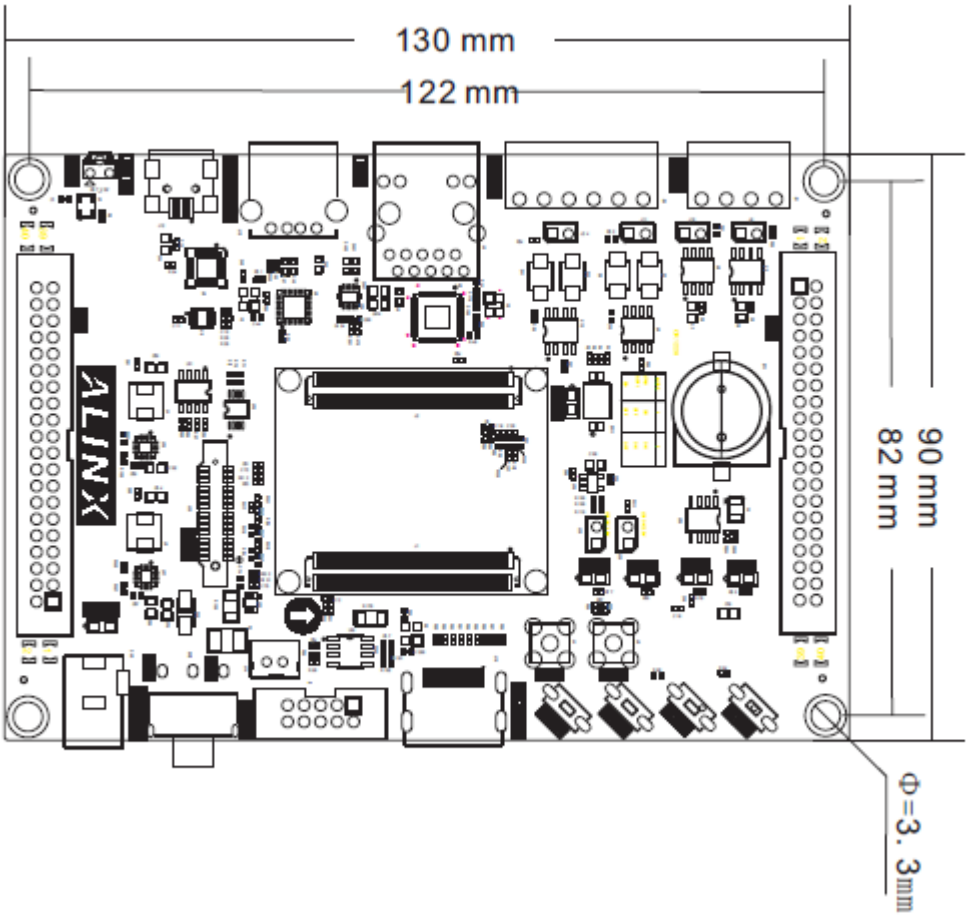


Figure 3-18-1: Voltage adjustment of VCCIO35

3.19 Carrier Board Size and Structure



Top View