ZYNQ7000 FPGA Development Board AX7Z035B User Manual

**ALINX**

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This ZYNQ7000 FPGA development platform adopts the core board + carrier board mode, which is convenient for users to use the core board for secondary development. The core board uses XILINX's Zynq7000 SOC chip XC7Z035 solution, uses ARM+FPGA SOC technology to integrate dual-core ARM Cortex-A9 and FPGA programmable logic on a single chip. In addition, the core board contains 4 pieces of 2GB high-speed DDR3 SDRAM chips, 1 piece of 8GB eMMC memory chip and 2 pieces of 256Mb QSPI FLASH chips.

In the design of carrier board, we have extended a wealth of interfaces for users, such as a PCIex4 interface, 4x fiber interfaces, 2x Gigabit Ethernet interfaces, 4x USB2.0 HOST interfaces, 1x HDMI output interface, 1x UART serial interface, 1x SD card interface, and 1x 40-pin expansion interface. It meets users' requirements for high-speed data exchange, data storage, video transmission processing and industrial control. It is a "professional" ZYNQ development platform. For high-speed data transmission and exchange, pre-verification and post-application of data processing is possible. This product is very suitable for students, engineers and other groups engaged in ZYNQ development.
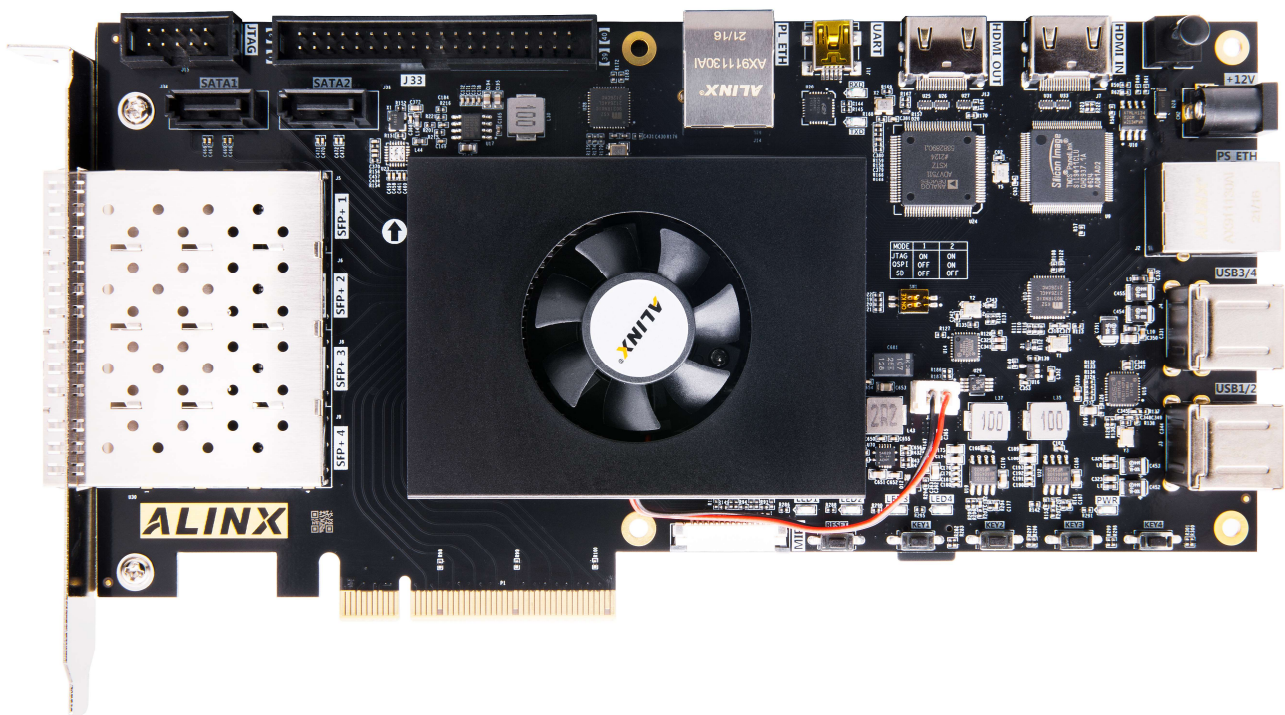
1. Development Board Introduction

The entire structure of AX7Z035B FPGA development board is inherited from our consistent core board+carrier board model. A high-speed inter-board connector is used between the core board and the carrier board.

The core board is mainly composed of ZYNQ7035 + 4x DDR3 + eMMC + QSPI FLASH. The ZYNQ7035 uses the Xilinx Zynq7000 series chips, model XC7Z035-2FFG676, which can be divided into Processor System (PS) and Programmable Logic (PL). On the PS and PL sides of the ZYNQ7350 chip, two DDR3s are mounted respectively, each DDR3 has a capacity of up to 512 Mbytes, so that ARM system and the FPGA system can independently process and store data. The PS-side 8GB eMMC FLASH memory chip and 256Mb QSPI FLASH are used to statically store ZYNQ's operating system, file system and user data.

The AX7Z035B carrier board has a wealth of peripheral interfaces, including 1x PCIex4 interface, 4x SFP interfaces, 2x Gigabit Ethernet interfaces (one for PS and one for PL), 4x USB2.0 HOST interfaces, 1x HDMI output interface, 1x UART serial interface, 1x SD card interface, 1x 40-pin expansion header and some key LEDs.

The following is the structure diagram of the whole development system:
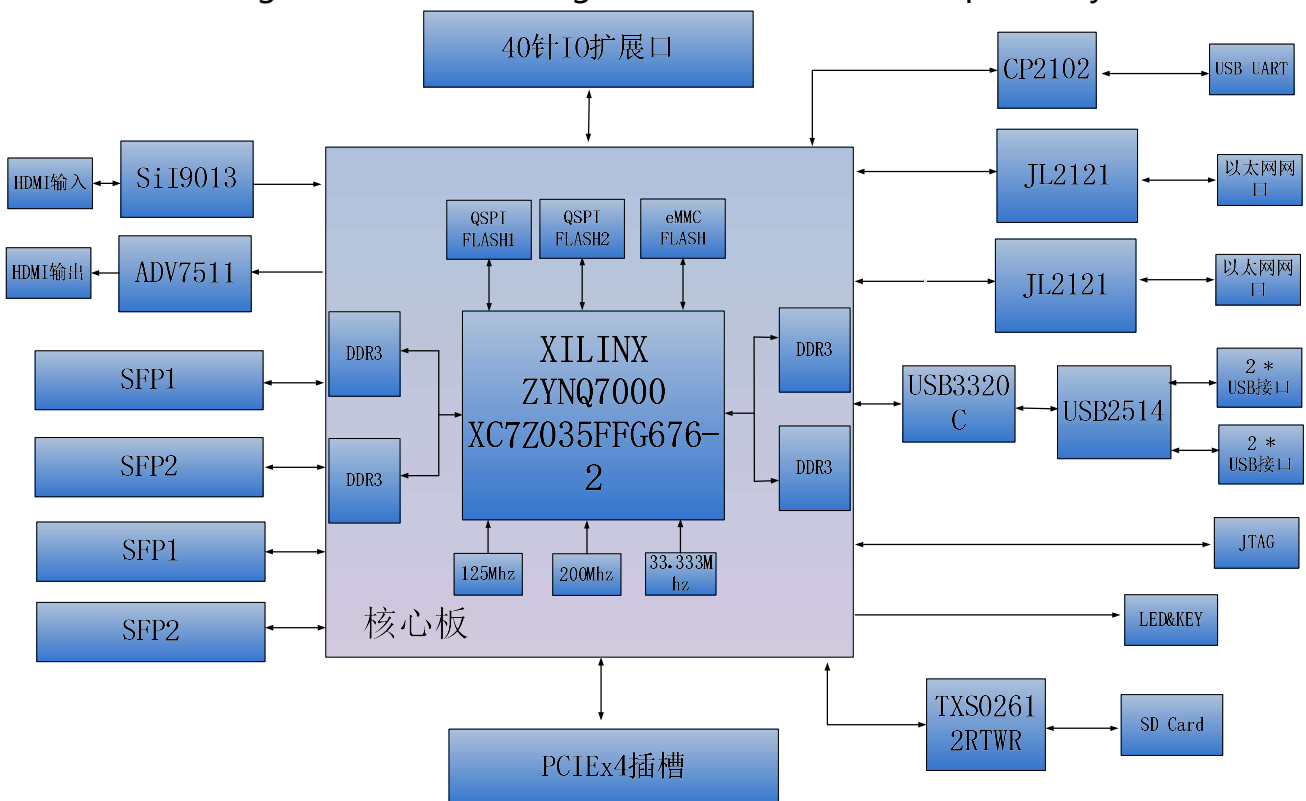
Through this diagram, you can see the interfaces and functions that the AX7Z035B FPGA Development Board contains:

● ZYNQ7035 core board

The core board consists of XC7Z035+2GB DDR3+8GB eMMC FLASH + 512Mb QSPI FLASH. In addition, three crystal oscillators provide clocks: one single-ended 33.3333MHz crystal oscillator to the PS system, one differential 200MHz crystal oscillator provides the PL logic DDR with reference clock, and one differential 125MHz crystal provides the GTX transceiver with reference clock.

● PCIe x4 Interface

Supports the PCI Express 2.0 standard and provides standard PCIe x4 high-speed data transfer interface and single-channel communication rate can up to 5GBaud.

● 4x SFP Interface

The 4-lane high-speed transceiver of ZYNQ's GTX transceiver is connected to the transmission and reception of four optical modules to realize 4-lane high-speed optical fiber communication interfaces. Each fiber optic data communication receives and transmits at speeds up to 10Gb/s.

● Gigabit Ethernet Interface

2-lane 10/100M/1000M Ethernet RJ45 interfaces for Ethernet data exchange with computers or other network devices. The network interface chip uses the JL2121 industrial GPHY chip from JL Semiconductor company. One Ethernet is connected to the PS end of the ZYNQ chip, and the other one is connected to the PL end of the ZYNQ chip.

● HDMI Video Output

1x HDMI video output interface, uses ANALOG DEVICE company's ADV7511 HDMI coding chip, supports the highest 1080P@60Hz output and supports 3D output.

● HDMI Video Input

1x HDMI video input interface, uses SIL9011/SIL9013 HDMI decoding chip from Silion Image company, supports the highest 1080P@60Hz output and supports 3D output.

● USB2.0 HOST Interface

Extend 4x USB HOST interfaces through the USB Hub chip for connecting

external USB slave devices, such as mouse, keyboard, USB flash drive and so on. The USB port uses flat-type USB port (USB Type A).

- USB Uart Interface

1x Uart to USB interface used for communication with the computer, convenient for user debugging. The serial port chip adopts the USB-UAR chip of Silicon Labs CP2102GM, and the USB interface adopts the MINI USB interface.

- Micro SD Card Holder

1x Micro SD card holder, used to store operating system images and file systems.

- 40-pin Expansion Port

A 40-pin 2.54mm pitch expansion port can be connected to various ALINX modules (binocular camera, TFT LCD screen, high-speed AD module, etc.). The expansion port contains 1x 5V power supply, 2x 3.3V power supply, 3x ground, 34x IO ports.

- JTAG Debugging Port

A 10-pin 2.54mm pitch standard JTAG port for FPGA program downloading and debugging. Users can debug and download the ZYNQ system through the XILINX downloader.

- LED Light

10 LEDs: 3 LEDs on the core board and 7 LEDs on the carrier board.

On Core board: 1 power indicator, 1 DONE configuration indicator, and 1 user indicator.

On Carrier board: 1 power indicator, 4 user indicators and 2 serial indicators.

- Key

5 keys: 1 reset key, 4 PL user keys.

2. AC7Z035B Core Board

2.1 Introduction

AC7Z035B (core board model, the same below) FPGA core board, ZYNQ chip is based on XC7Z035-2FFG676 of XILINX company ZYNQ7000 series. The ZYNQ chip's PS system integrates two ARM Cortex™-A9 processors, AMBA® interconnects, internal memory, external memory interfaces and peripherals. The FPGA of the ZYNQ chip contains a wealth of programmable logic cells, DSP and internal RAM.

The core board uses four Micron 512MB DDR3 chips MT41J256M16HA-125 for a total capacity of 2GB. PS and PL sides, each side has two DDR3 chips, which form a 32-bit bus width. The DDR3 SDRAM on the PS side can run at speed of up to 533MHz (data rate 1066Mbps), and the DDR3 SDRAM on the PL side can run at speed of up to 800MHz (data rate 1600Mbps). In addition, two 256MBit QSPI FLASH and 8GB eMMC FLASH chips are integrated on the core board to boot the storage configuration and system files.

To connect with the carrier board, the four board-to-board connectors of the core board expand the USB interface, the Gigabit Ethernet interface, the SD card interface, and other remaining MIO ports on the PS side; and extend 8-pair high-speed transceiver GTX interfaces of the ZYNQ, almost all IO ports (144) on the PL side. The level of IO of BANK12 and BANK13 can be modified by replacing the LDO chip on the core board to meet users' requirements for different level interfaces. For users who need a lot of IO, this core board will be a good choice. Moreover, as for the IO connection, lines between the ZYNQ chip and interface are processed in equal length and differential length, and the core board size is only 80*60 (mm), which is very suitable for secondary development.
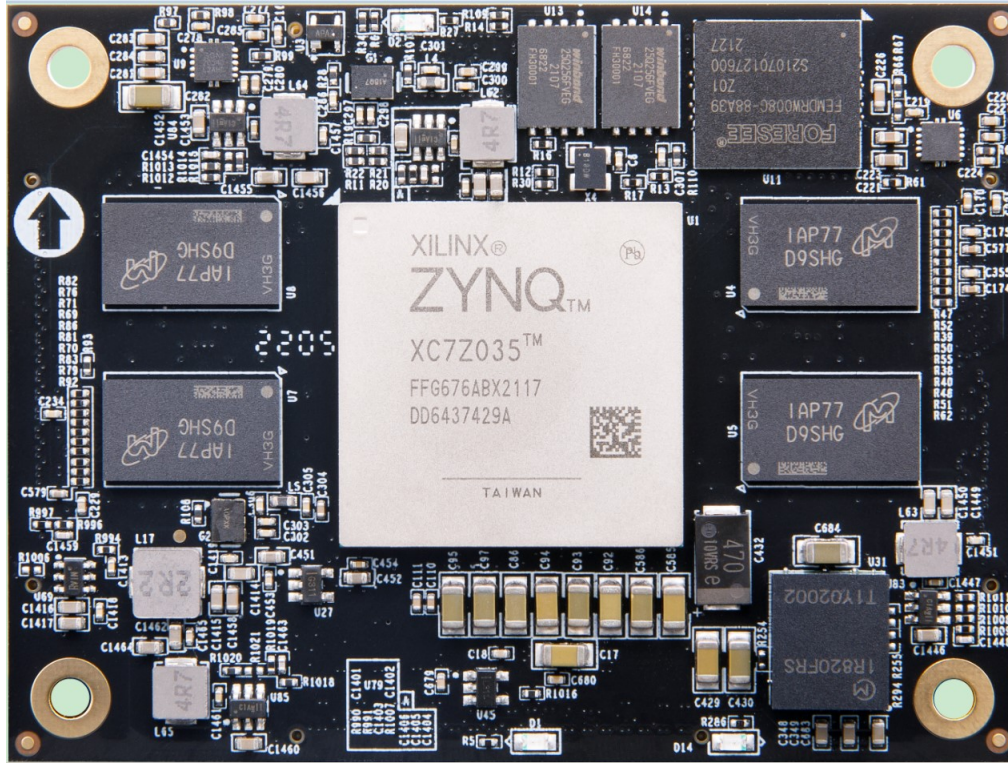
AC7Z035B Front View
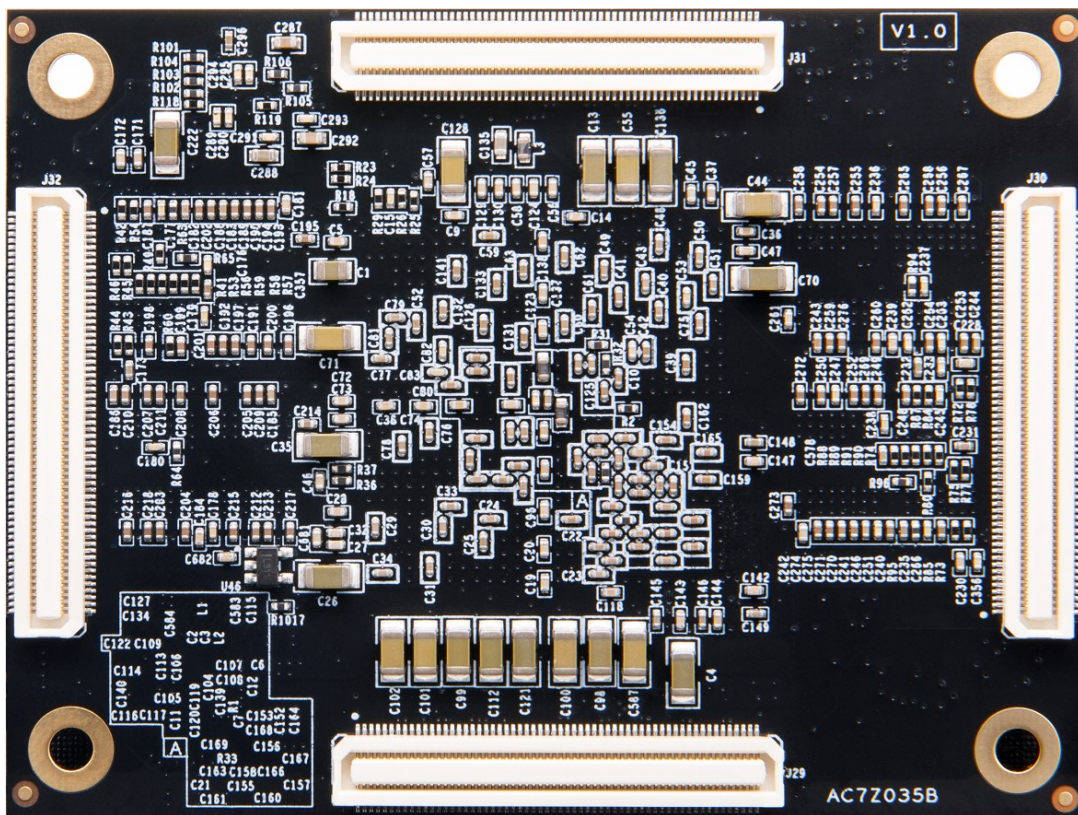
AC7Z035B Back View

2.2   ZYNQ Chip

The FPGA core board AC7Z035B uses Xilinx's Zynq7000 series chip, model XC7Z035-2FFG676. The chip's PS system integrates two ARM CortexTM-A9 processors, AMBA® interconnects, internal memory, external memory interfaces and peripherals. These peripherals mainly include USB bus interface, Ethernet interface, SD/SDIO interface, I2C bus interface, CAN bus interface, UART interface, GPIO etc. The PS can operate independently and start up at power on or reset. Figure 2-2-1 detailed the Overall Block Diagram of the ZYNQ7000 Chip.
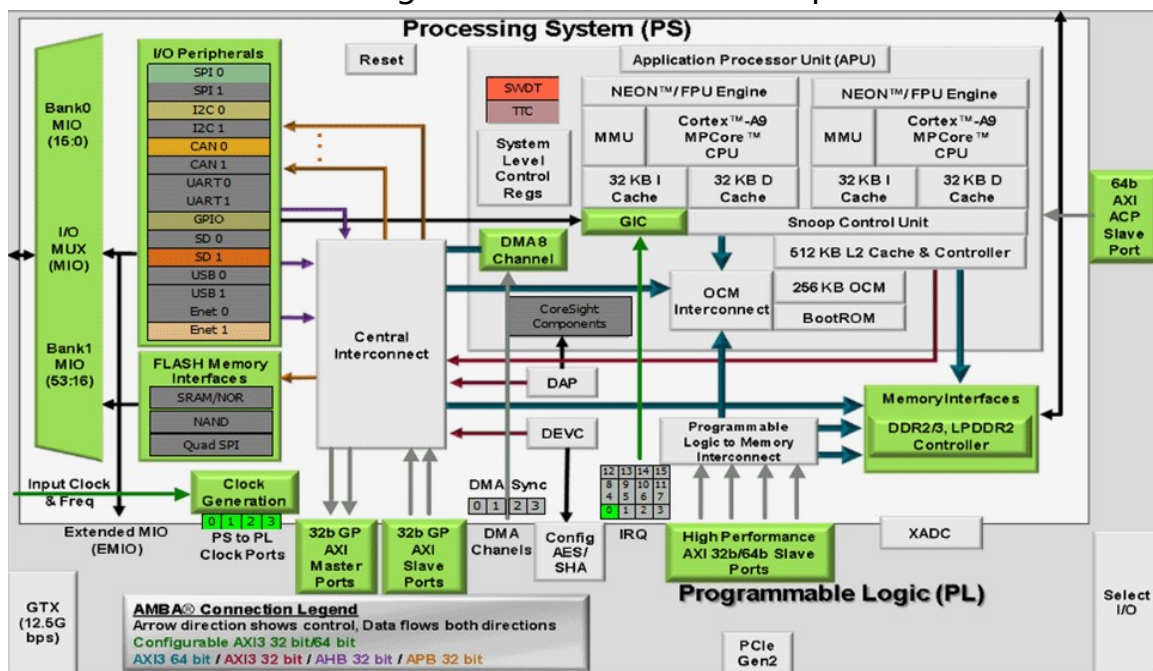
Figure 2-2-1: Overall Block Diagram of the ZYNQ7000 Chip

The main parameters of the PS system part are as follows:

- ARM dual-core CortexA9-based application processor, ARM-v7 architecture, up to 800MHz.

- 32KB level 1 instruction and data cache per CPU, 512KB level 2 cache, shared by 2 CPUs.

- On-chip boot ROM and 256KB on-chip RAM.

- External storage interface, support 16/32 bit DDR2, DDR3 interface.

- 2x Gigabit NIC, support divergent-aggregate DMA, GMII, RGMII, SGMII interface.

- 2x USB2.0 OTG interfaces, each supports up to 12 nodes.

- 2x CAN2.0B bus interfaces.

- 2x SD card, SDIO, MMC compatible controllers.
- 2x SPIs, 2x UARTs, 2x I2C interfaces.
- 54x multi-function Ios, which can be configured as normal IO or peripheral control interfaces.
- High bandwidth connection within PS and PS to PL.

The main parameters of the PL logic are as follows:

- Logic Cells: 275K;
- LUTs: 171,900
- Flip-flops: 343,800
- 18x25MACCs: 900;
- Block RAM: 17.6Mb;
- 8-lane high-speed GTX transceivers, support PCIE Gen2x8;
- 2x AD converters for on-chip voltage, temperature sensing and up to 17 external differential input channels, 1MBPS.

XC7Z035-2FFG676I chip speed grade is -2, industrial grade, package is FGG676, pin pitch is 1.0mm, the specific chip model naming definition of ZYNQ7000 series is shown in Figure 2-2-2:
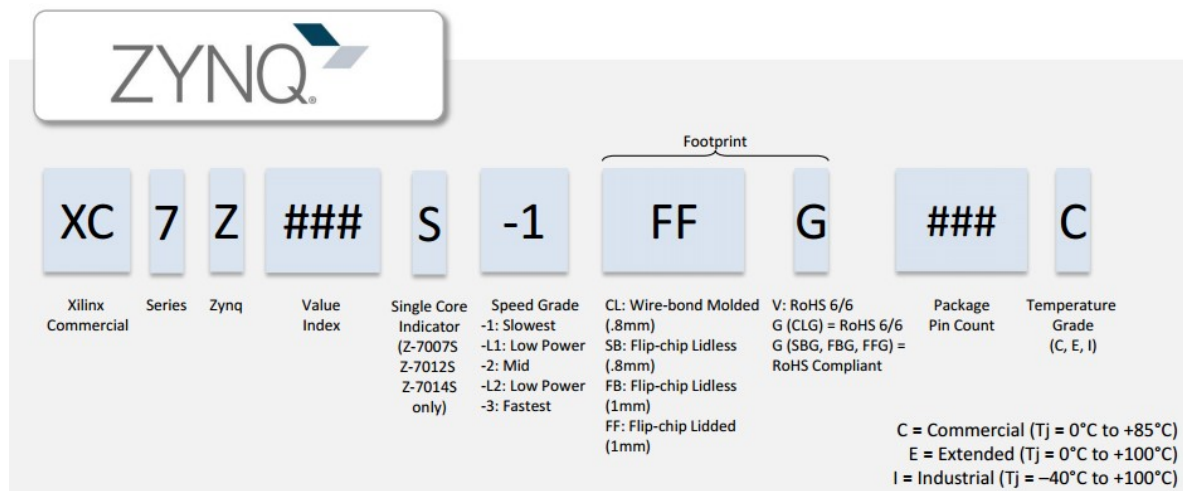
Figure 2-2-2: Specific Chip Model Definition of ZYNQ7000 Series

Figure 2-2-3: The XC7Z035 chip used on the Core Board

2.3 DDR3 DRAM

The FPGA board AX7Z035B is equipped with four Micron 512MB DDR3 chips, model MT41J256M16HA-125 (compatible with MT41K256M16HA-125), each side has 2 DDR3s mounted. Two DDR3 SDRAMs form a 32-bit bus width. The PS-side DDR3 SDRAM has a maximum operating speed of 533MHz (data rate 1066Mbps), and two DDR3 memory systems are directly connected to the memory interface of the ZYNQ PS BANK 502. The PL-side DDR3 SDRAM has a maximum operating speed of 800MHz (data rate 1600Mbps), and two DDR3 memory systems are connected to the BANK33 and BANK34 interfaces of the FPGA. The specific configuration of DDR3 SDRAM is shown in Table 2-3-1.

Table 2-3-1 DDR3 SDRAM Configuration

Bit Number	Model	Capacity	Manufacturer
U4, U5, U7, U8	MT41J256M16HA-125	256M x 16bit	Micron

The hardware design of DDR3 requires strict consideration of signal integrity. We have fully considered the matching resistor/terminal resistance, line impedance

control, and line length control in circuit design and PCB design to ensure high-speed and stable operation of DDR3.

　　The hardware connection of DDR3 DRAM on the PS side is shown in Figure 2-3-1:

U1

Upper 16bits data　　　　U4 DDR3 (MT41J256M16 HA-125)

BANK 502　Address line Control line

ZYNQ

U5 DDR3 (MT41J256M16 HA-125)

Lower 16bits data
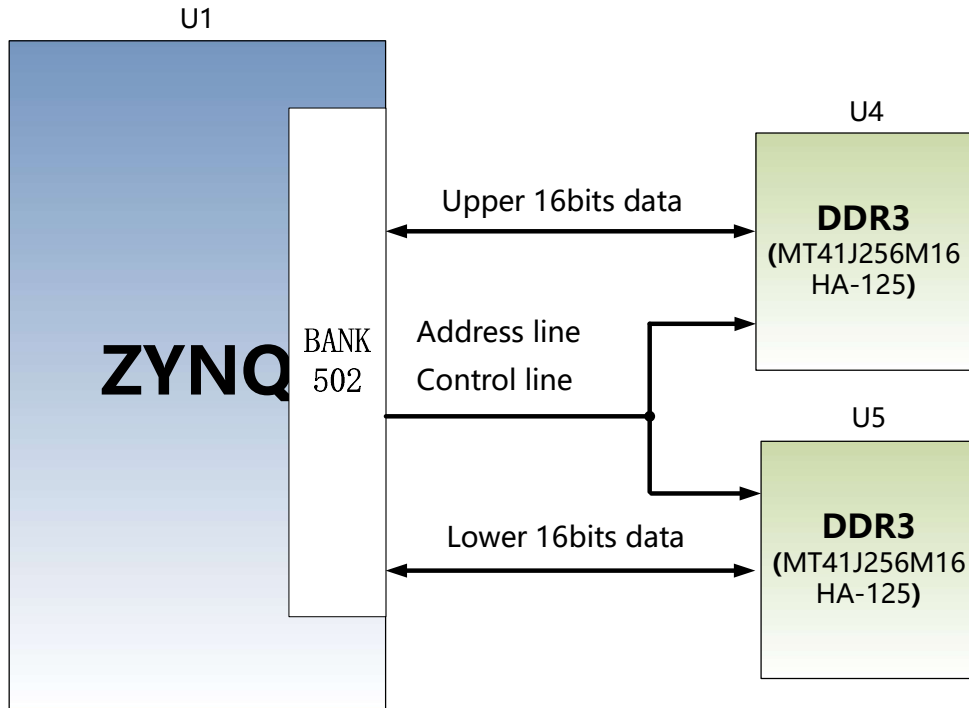
Figure 2-3-1: The Schematic of DDR3 DRAM on the PS side

U1

Upper 16bits data　　　　U7 DDR3 (MT41J256M16 HA-125)

BANK 33, 34　Address line Control line

ZYNQ

U8 DDR3 (MT41J256M16 HA-125)

Lower 16bits data
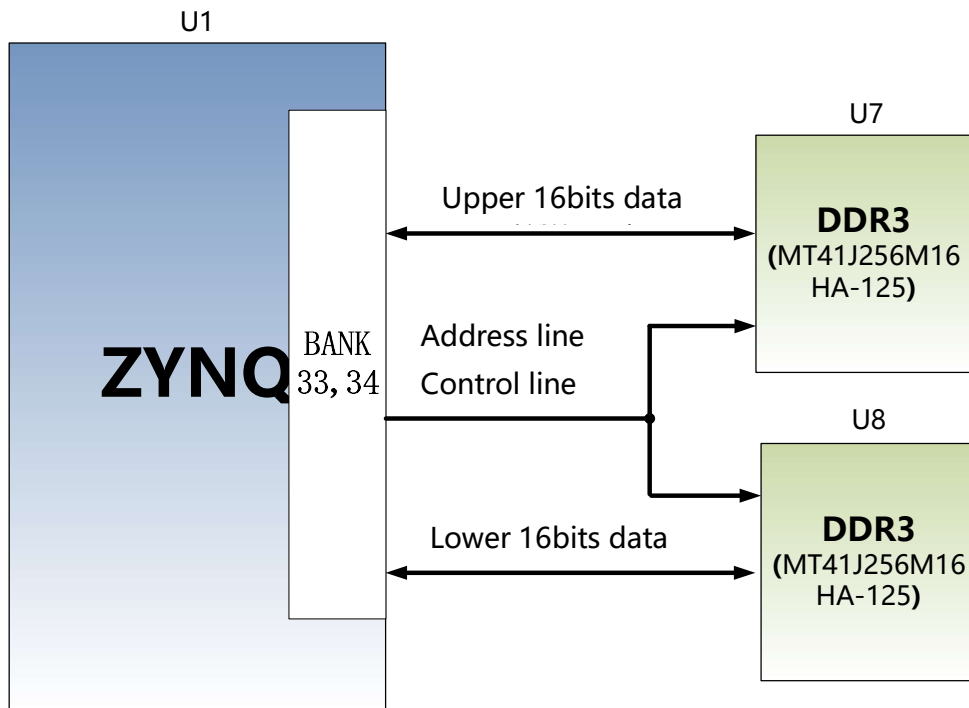
Figure 2-3-2: The Schematic of DDR3 DRAM on the PL side

PS DDR3 DRAM 拼 assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number
PS_DDR3_DQS0_P	PS_DDR_DQS_P0_502	H24
PS_DDR3_DQS0_N	PS_DDR_DQS_N0_502	G25
PS_DDR3_DQS1_P	PS_DDR_DQS_P1_502	L24
PS_DDR3_DQS1_N	PS_DDR_DQS_N1_502	L25
PS_DDR3_DQS2_P	PS_DDR_DQS_P2_502	P25
PS_DDR3_DQS2_N	PS_DDR_DQS_N2_502	R25
PS_DDR3_DQS3_P	PS_DDR_DQS_P3_502	W24
PS_DDR3_DQS4_N	PS_DDR_DQS_N3_502	W25
PS_DDR3_D0	PS_DDR_DQ0_502	J26
PS_DDR3_D1	PS_DDR_DQ1_502	F25
PS_DDR3_D2	PS_DDR_DQ2_502	J25
PS_DDR3_D3	PS_DDR_DQ3_502	G26
PS_DDR3_D4	PS_DDR_DQ4_502	H26
PS_DDR3_D5	PS_DDR_DQ5_502	H23
PS_DDR3_D6	PS_DDR_DQ6_502	J24
PS_DDR3_D7	PS_DDR_DQ7_502	J23
PS_DDR3_D8	PS_DDR_DQ8_502	K26
PS_DDR3_D9	PS_DDR_DQ9_502	L23
PS_DDR3_D10	PS_DDR_DQ10_502	M26
PS_DDR3_D11	PS_DDR_DQ11_502	K23
PS_DDR3_D12	PS_DDR_DQ12_502	M25
PS_DDR3_D13	PS_DDR_DQ13_502	N24
PS_DDR3_D14	PS_DDR_DQ14_502	M24
PS_DDR3_D15	PS_DDR_DQ15_502	N23
PS_DDR3_D16	PS_DDR_DQ16_502	R26
PS_DDR3_D17	PS_DDR_DQ17_502	P24
PS_DDR3_D18	PS_DDR_DQ18_502	N26
PS_DDR3_D19	PS_DDR_DQ19_502	P23
PS_DDR3_D20	PS_DDR_DQ20_502	T24
PS_DDR3_D21	PS_DDR_DQ21_502	T25

PS_DDR3_D22	PS_DDR_DQ22_502	T23
PS_DDR3_D23	PS_DDR_DQ23_502	R23
PS_DDR3_D24	PS_DDR_DQ24_502	V24
PS_DDR3_D25	PS_DDR_DQ25_502	U26
PS_DDR3_D26	PS_DDR_DQ26_502	U24
PS_DDR3_D27	PS_DDR_DQ27_502	U25
PS_DDR3_D28	PS_DDR_DQ28_502	W26
PS_DDR3_D29	PS_DDR_DQ29_502	Y25
PS_DDR3_D30	PS_DDR_DQ30_502	Y26
PS_DDR3_D31	PS_DDR_DQ31_502	W23
PS_DDR3_DM0	PS_DDR_DM0_502	G24
PS_DDR3_DM1	PS_DDR_DM1_502	K25
PS_DDR3_DM2	PS_DDR_DM2_502	P26
PS_DDR3_DM3	PS_DDR_DM3_502	V26
PS_DDR3_A0	PS_DDR_A0_502	K22
PS_DDR3_A1	PS_DDR_A1_502	K20
PS_DDR3_A2	PS_DDR_A2_502	N21
PS_DDR3_A3	PS_DDR_A3_502	L22
PS_DDR3_A4	PS_DDR_A4_502	M20
PS_DDR3_A5	PS_DDR_A5_502	N22
PS_DDR3_A6	PS_DDR_A6_502	L20
PS_DDR3_A7	PS_DDR_A7_502	J21
PS_DDR3_A8	PS_DDR_A8_502	T20
PS_DDR3_A9	PS_DDR_A9_502	U20
PS_DDR3_A10	PS_DDR_A10_502	M22
PS_DDR3_A11	PS_DDR_A11_502	H21
PS_DDR3_A12	PS_DDR_A12_502	P20
PS_DDR3_A13	PS_DDR_A13_502	J20
PS_DDR3_A14	PS_DDR_A14_502	R20
PS_DDR3_BA0	PS_DDR_BA0_502	U22
PS_DDR3_BA1	PS_DDR_BA1_502	T22
PS_DDR3_BA2	PS_DDR_BA2_502	R22

PS_DDR3_S0	PS_DDR_CS_B_502	Y21
PS_DDR3_RAS	PS_DDR_RAS_B_502	V23
PS_DDR3_CAS	PS_DDR_CAS_B_502	Y23
PS_DDR3_WE	PS_DDR_WE_B_502	V22
PS_DDR3_ODT	PS_DDR_ODT_502	Y22
PS_DDR3_RESET	PS_DDR_DRST_B_502	H22
PS_DDR3_CLK0_P	PS_DDR_CKP_502	R21
PS_DDR3_CLK0_N	PS_DDR_CKN_502	P21
PS_DDR3_CKE	PS_DDR_CKE_502	U21

PL DDR3 DRAM pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number
PL_DDR3_DQS0_P	IO_L3P_T0_DQS_33	G2
PL_DDR3_DQS0_N	IO_L3N_T0_DQS_33	F2
PL_DDR3_DQS1_P	IO_L9P_T1_DQS_33	K2
PL_DDR3_DQS1_N	IO_L9N_T1_DQS_33	K1
PL_DDR3_DQS2_P	IO_L15P_T2_DQS_33	N3
PL_DDR3_DQS2_N	IO_L15N_T2_DQS_33	N2
PL_DDR3_DQS3_P	IO_L21P_T3_DQS_33	M8
PL_DDR3_DQS4_N	IO_L21N_T3_DQS_33	L8
PL_DDR3_D0	IO_L5N_T0_33	E1
PL_DDR3_D1	IO_L1N_T0_33	F4
PL_DDR3_D2	IO_L4P_T0_33	D1
PL_DDR3_D3	IO_L1P_T0_33	G4
PL_DDR3_D4	IO_L2N_T0_33	D3
PL_DDR3_D5	IO_L5P_T0_33	E2
PL_DDR3_D6	IO_L2P_T0_33	D4
PL_DDR3_D7	IO_L4N_T0_33	C1
PL_DDR3_D8	IO_L7N_T1_33	H1
PL_DDR3_D9	IO_L10N_T1_33	G1
PL_DDR3_D10	IO_L7P_T1_33	J1
PL_DDR3_D11	IO_L8N_T1_33	H3

PL_DDR3_D12	IO_L11N_T1_SRCC_33	K3
PL_DDR3_D13	IO_L8P_T1_33	H4
PL_DDR3_D14	IO_L11P_T1_SRCC_33	L3
PL_DDR3_D15	IO_L10P_T1_33	H2
PL_DDR3_D16	IO_L18P_T2_33	N1
PL_DDR3_D17	IO_L14P_T2_SRCC_33	L5
PL_DDR3_D18	IO_L14N_T2_SRCC_33	L4
PL_DDR3_D19	IO_L13P_T2_MRCC_33	M6
PL_DDR3_D20	IO_L16P_T2_33	M2
PL_DDR3_D21	IO_L17P_T2_33	N4
PL_DDR3_D22	IO_L16N_T2_33	L2
PL_DDR3_D23	IO_L17N_T2_33	M4
PL_DDR3_D24	IO_L23P_T3_33	N7
PL_DDR3_D25	IO_L22N_T3_33	J6
PL_DDR3_D26	IO_L19P_T3_33	M7
PL_DDR3_D27	IO_L20N_T3_33	J5
PL_DDR3_D28	IO_L24P_T3_33	K8
PL_DDR3_D29	IO_L20P_T3_33	K5
PL_DDR3_D30	IO_L24N_T3_33	K7
PL_DDR3_D31	IO_L22P_T3_33	K6
PL_DDR3_DM0	IO_L6P_T0_33	F3
PL_DDR3_DM1	IO_L12P_T1_MRCC_33	J4
PL_DDR3_DM2	IO_L13N_T2_MRCC_33	M5
PL_DDR3_DM3	IO_L23N_T3_33	N6
PL_DDR3_A0	IO_L17N_T2_34	A8
PL_DDR3_A1	IO_L23P_T3_34	C2
PL_DDR3_A2	IO_L14P_T2_SRCC_34	D6
PL_DDR3_A3	IO_L15N_T2_DQS_34	B9
PL_DDR3_A4	IO_L10N_T1_34	D5
PL_DDR3_A5	IO_L17P_T2_34	A9
PL_DDR3_A6	IO_L11N_T1_SRCC_34	E7
PL_DDR3_A7	IO_L15P_T2_DQS_34	C9

PL_DDR3_A8	IO_L12N_T1_MRCC_34	F7
PL_DDR3_A9	IO_L18N_T2_34	A7
PL_DDR3_A10	IO_L24N_T3_34	A2
PL_DDR3_A11	IO_L11P_T1_SRCC_34	F8
PL_DDR3_A12	IO_L23N_T3_34	B1
PL_DDR3_A13	IO_L16P_T2_34	B10
PL_DDR3_A14	IO_L12P_T1_MRCC_34	G7
PL_DDR3_BA0	IO_L18P_T2_34	B7
PL_DDR3_BA1	IO_L19N_T3_VREF_34	C3
PL_DDR3_BA2	IO_L22N_T3_34	A3
PL_DDR3_S0	IO_L14N_T2_SRCC_34	C6
PL_DDR3_RAS	IO_L19P_T3_34	C4
PL_DDR3_CAS	IO_L20N_T3_34	B4
PL_DDR3_WE	IO_L20P_T3_34	B5
PL_DDR3_ODT	IO_L22P_T3_34	A4
PL_DDR3_RESET	IO_L16N_T2_34	A10
PL_DDR3_CLK0_P	IO_L21P_T3_DQS_34	B6
PL_DDR3_CLK0_N	IO_L21N_T3_DQS_34	A5
PL_DDR3_CKE	IO_L24P_T3_34	B2

2.4   QSPI Flash

The board is equipped with two 256MBit Quad-SPI FLASH chips to form an 8-bit bandwidth data bus, the FLASH model is W25Q256FVEI, which uses the 3.3V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, it can be used as a boot device for the system to store the boot image of the system. These images mainly include FPGA bit files, ARM application code, and other user data files. The specific models and related parameters of QSPI FLASH are shown in Table 2-4-1.

Bit Number	Model	Capacity	Manufacturer
U13, U14	W25Q256FVEI	256M bit	Winbond

Table 2-4-1: QSPI FLASH specification and parameters

QSPI FLASH is connected to the GPIO port of the PS BANK500 of the ZYNQ chip. In the system design, the functions of these PS GPIO ports need to be configured as the QSPI FLASH interfaces. Figure 2-4-1 shows the QSPI Flash in the schematic.

Figure 2-4-1: QSPI Flash connection diagram

Configuration chip pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin No.
QSPI0_SCK	PS_MIO6_500	F23
QSPI0_CS	PS_MIO1_500	D26
QSPI0_D0	PS_MIO2_500	E25
QSPI0_D1	PS_MIO3_500	D25
QSPI0_D2	PS_MIO4_500	F24
QSPI0_D3	PS_MIO5_500	C26
QSPI1_SCK	PS_MIO9_500	D24
QSPI1_CS	PS_MIO0_500	E26
QSPI1_D0	PS_MIO10_500	A25
QSPI1_D1	PS_MIO11_500	B26
QSPI1_D2	PS_MIO12_500	A23

QSPI1_D3	PS_MIO13_500	B25

2.5 eMMC Flash

The FPGA core board AC7Z035B is equipped with a large-capacity 8GB eMMC FLASH chip, model THGBMFG6C1LBAIL, which supports the JEDEC e-MMC V5.0 standard HS-MMC interface with level of 1.8V or 3.3V. The data width of the connection between eMMC FLASH and ZYNQ is 4 bits. Due to the large capacity and non-volatile nature of eMMC FLASH, it can be used as a large-capacity storage device for the ZYNQ system, such as ARM applications, system files and other user data files. The specific models and related parameters of eMMC FLASH are shown in Table 2-5-1.

Bit Number	Model	Capacity	Manufacturer
U11	THGBMFG6C1LBAIL	8G Byte	TOSHIBA

Table 2-5-1: eMMC FLASH specification and parameters

eMMC FLASH is connected to the GPIO port of the PS BANK501 of the ZYNQ chip. In the system design, the functions of these PS ports need to be configured as the SD interfaces. Figure 2-5-1 shows the eMMC Flash in the schematic.
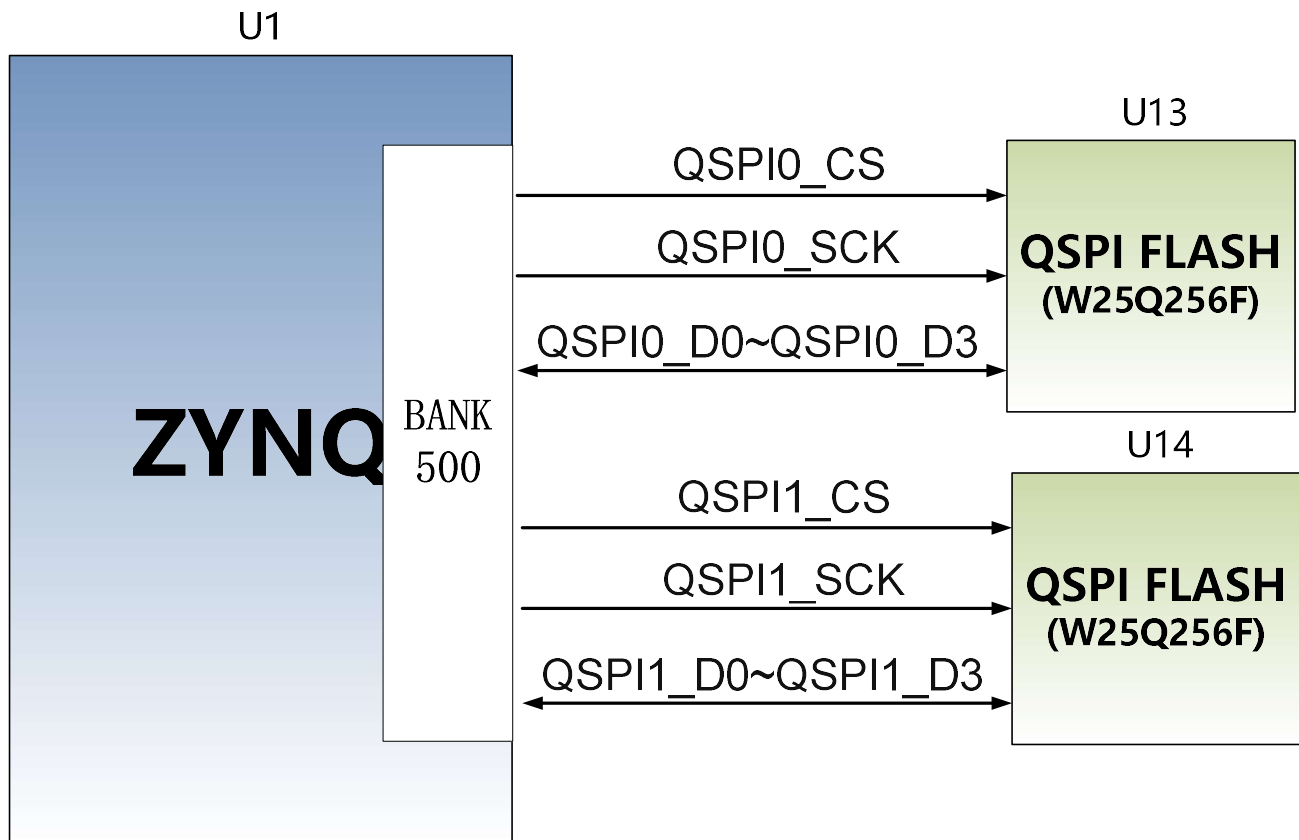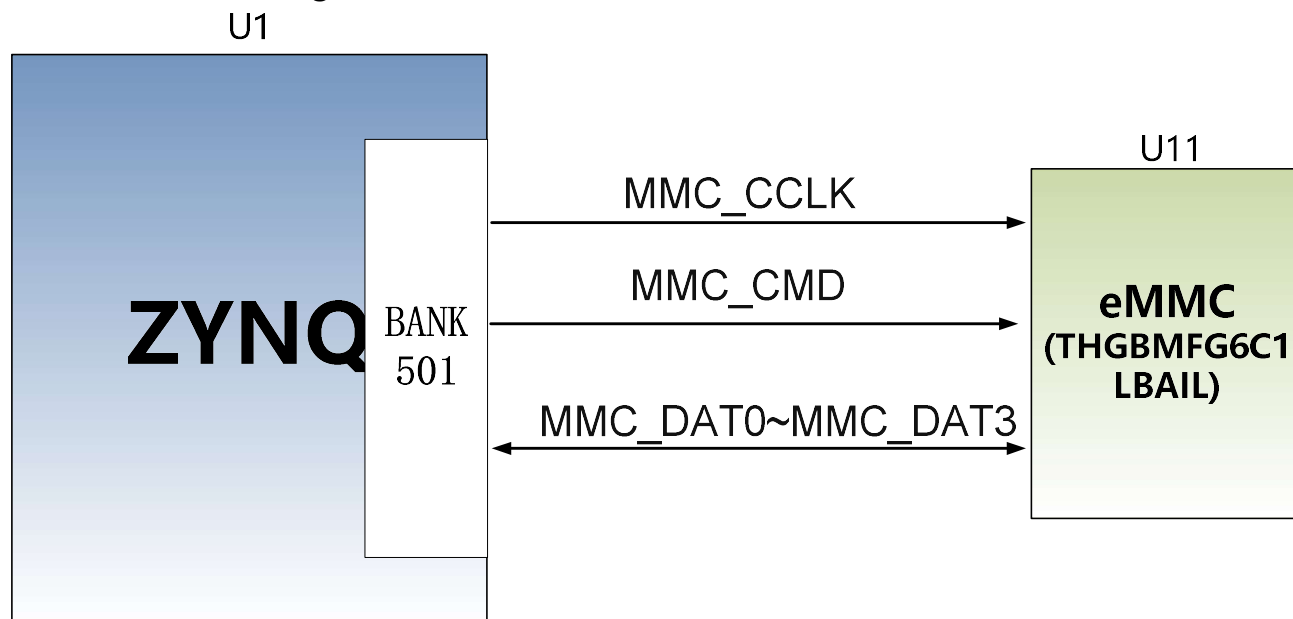

Figure 2-5-1: eMMC Flash connection diagram

Configuration chip pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number
MMC_CCLK	PS_MIO48_501	B21
MMC_CMD	PS_MIO47_501	B19
MMC_D0	PS_MIO46_501	E17
MMC_D1	PS_MIO49_501	A18
MMC_D2	PS_MIO50_501	B22
MMC_D3	PS_MIO51_501	B20

2.6   Clock Configuration

The core system respectively provides reference clocks for the PS system, the PL logic, and the GTX transceiver, allowing the PS system and PL logic to work independently. The schematic diagram of the clock circuit design is shown in Figure 2-6-1:
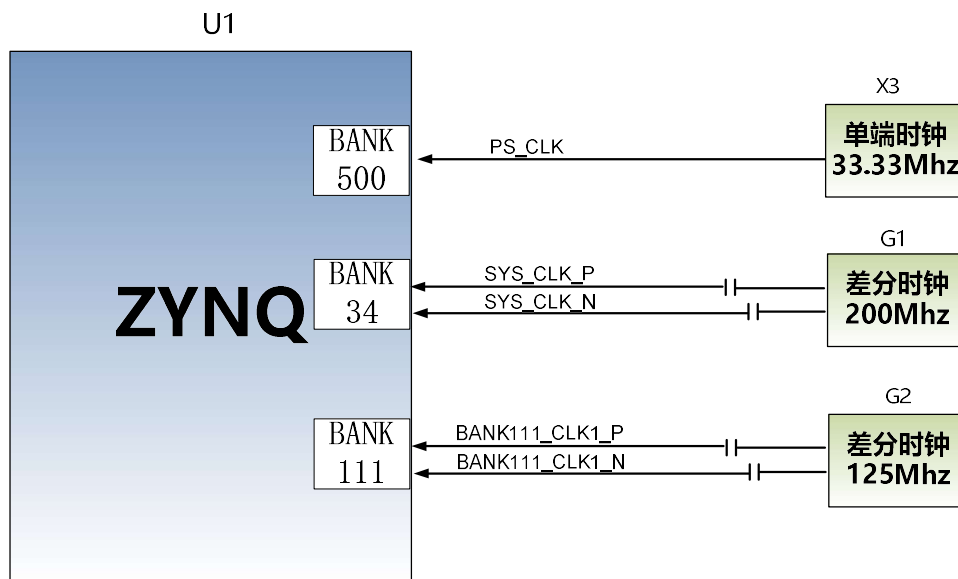
Figure 2-6-1: Core board clock source

PS system clock source

The ZYNQ chip provides a 33.333MHz clock input to the PS via the X4 crystal on the board. The input of the clock is connected to the pin of the BANK500 PS_CLK_500 of the ZYNQ chip. The schematic diagram is shown in Figure 2-6-2:
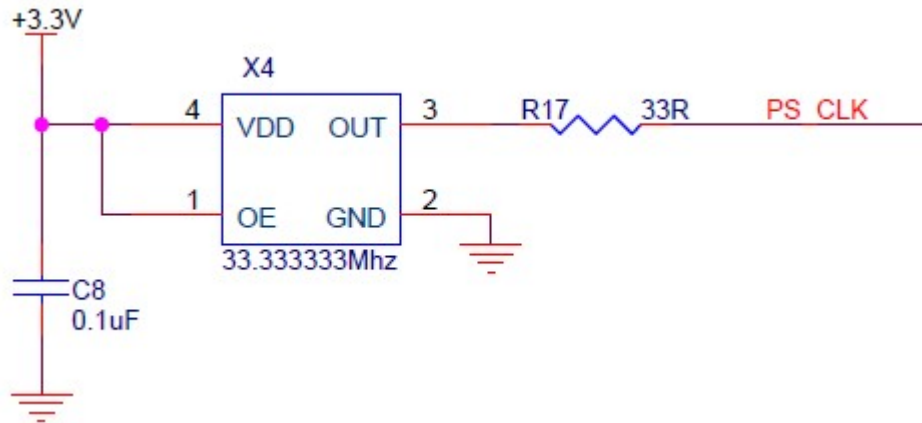
Figure 2-6-2: PS active crystal oscillator

Clock pin assignment:

Signal Name	ZYNQ Pin
PS_CLK	B24

PL system clock source

The board has a differential 200MHz PL system clock source for the reference clock of the DDR3 controller. The crystal output is connected to the MRCC of the FPGA BANK34, which can be used to drive the DDR3 controller and user logic in the FPGA. The schematic diagram of the clock source is shown in Figure 2-6-3:
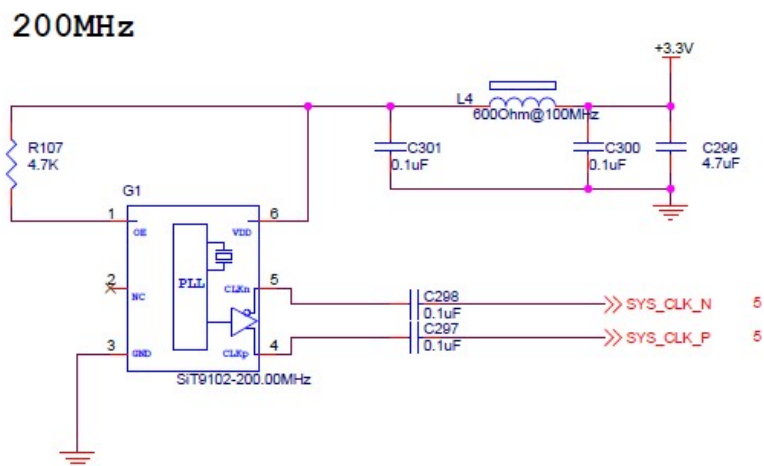
Figure 2-6-3: PL system clock source

PL clock pin assignment:

Signal Name	ZYNQ Pin
SYS_CLK_P	C8
SYS_CLK_N	C7

GTX reference clock

The FPGA core board provides a 125Mhz reference clock for the GTX transceiver. The reference clock is connected to the reference clock input REFCLK1P/REFCLK1N of the BANK111. The schematic diagram of the clock source is shown in Figure 2-6-4:
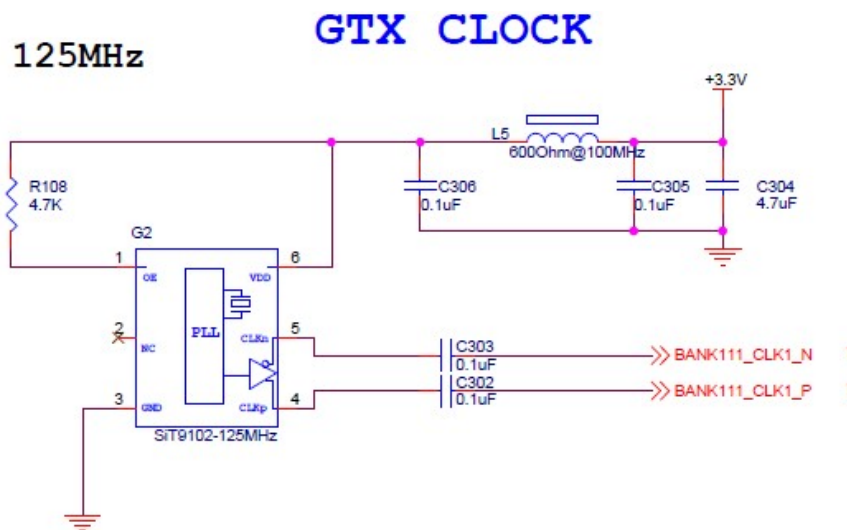
Figure 2-6-4: GTX clock source

Figure 2-6-5: Programmable clock source on the board

GTX clock source ZYNQ pin assignment:

Signal Name	ZYNQ Pin
BANK111_CLK1_P	AA6
BANK111_CLK1_N	AA5

2.7   LED Light

There are 3 red LED lights on the AC7Z035B FPGA core board, one of which is the power indicator light (PWR), one is the configuration LED light (DONE), and one is the user LED light. When the core board is powered, the power indicator will light up; when the FPGA is configured, the configuration LED will light up. The user LED light is connected to the IO of the PL. Users can control the light on and off by the program. When the IO voltage connected to the user LED is high, the user LED will off. When the IO voltage is low, the user LED will light up. The schematic diagram of the LED light hardware connection is shown in Figure 2-7-1:
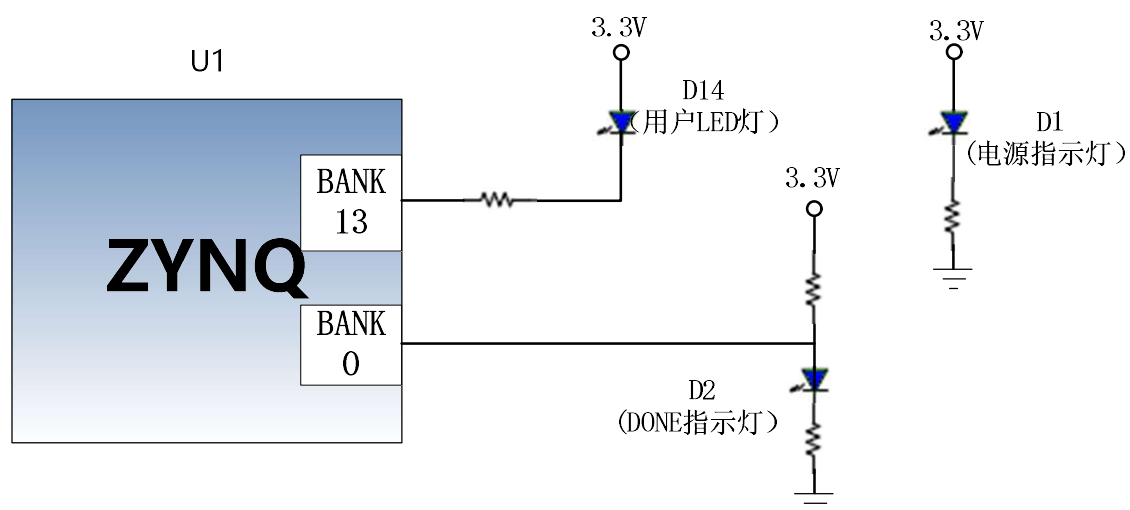
Figure 2-7-1: Core board LED light Hardware Connection

User LED light pin assignment:

LED	ZYNQ Pin Name	ZYNQ Pin Number	Description
D14	B13_IO25	V19	User LED light

2.8   Reset Circuit

There is a reset circuit on the AC7Z035B core board. The reset input signal is connected to the reset key on the carrier board. The reset output is connected to the PS reset pin of the ZYNQ chip. Users can use the key on the carrier board to reset the ZYNQ system. The schematic diagram of the reset connection is shown in Figure 2-8-1:
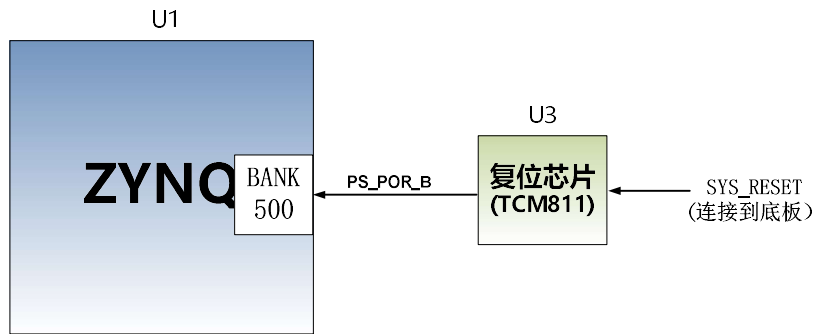
Figure 2-8-1: Reset connection diagram

Reset key ZYNQ pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin No.	Description
PS_POR_B	PS_POR_B_500	C23	ZYNQ System Reset Signal

2.9　Power Supply

The power supply voltage of the AC7Z035B core board is DC5V, which is supplied by connecting the carrier board. The schematic diagram of the power supply design on the board is shown in Figure 2-9-1:
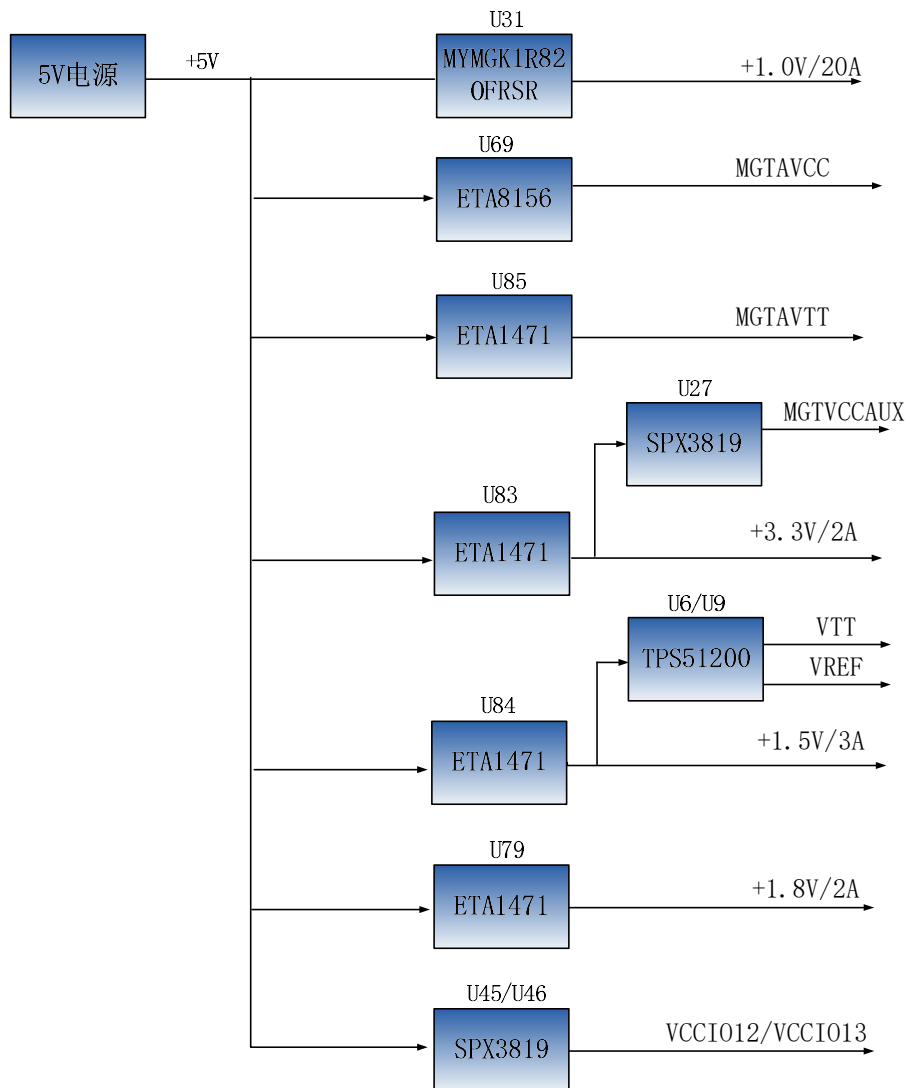
Figure 2-9-1: Schematic diagram of the power interface

+5V generates a+1.0V ZYNQ core power supply through the DCDC power chip MYMGK1R820FRSR, with an output current of up to 20A, which far meets the current requirements of ZYNQ's core voltage. Then, +5V generates MGTAVTT, +1.5V, +3.3V, and+1.5V through the DCDC chip ETA1471, generates the power supply of MGTAVTT via DCDC chip ETA8156. +3.3V generates GTX auxiliary power supply+1.8V through LDO chip SPX3819-1-8. The VTT and VREF voltages of DDR3 in the PS and PL parts are generated by TPS51200. In addition, the IO power supply for

BANK12 and BANK13 is generated through two SPX3819M5-3-3 channels. Users can replace the LDO chip to make the IO input and output of these two BANKs meet other voltage standards.

The functions of each power distribution are shown in the following table:

Power Supply	Function
+1.0V	Core voltage of ZYNQ PS and PL
+1.8V	ZYNQ PS and PL auxiliary voltage, BANK501，BANK35，eMMC
+3.3V	ZYNQ Bank0,Bank500，QSIP FLASH, Clock crystal oscillator
+1.5V	DDR3, ZYNQ Bank502, Bank33, Bank34
VCCIO12	ZYNQ Bank12
VCCIO13	ZYNQ Bank13
VREF, VTT (+0.75V)	PS DDR3，PL DDR3
MGTAVCC(+1.0V)	ZYNQ Bank111, Bank112
MGTAVTT(+1.2V)	ZYNQ Bank111, Bank112
MGTVCCAUX (+1.8V)	ZYNQ Bank111, Bank112

Because the power supply of the ZYNQ FPGA has the power-on sequence requirements, in the circuit design, we have designed according to the power requirements of the chip. The power-on sequence is +1.0V->+1.8V-> (+1.5 V, +3.3V, VCCIO12, VCCIO13) circuit design to ensure the normal operation of the chip.

2.10 Size Dimension
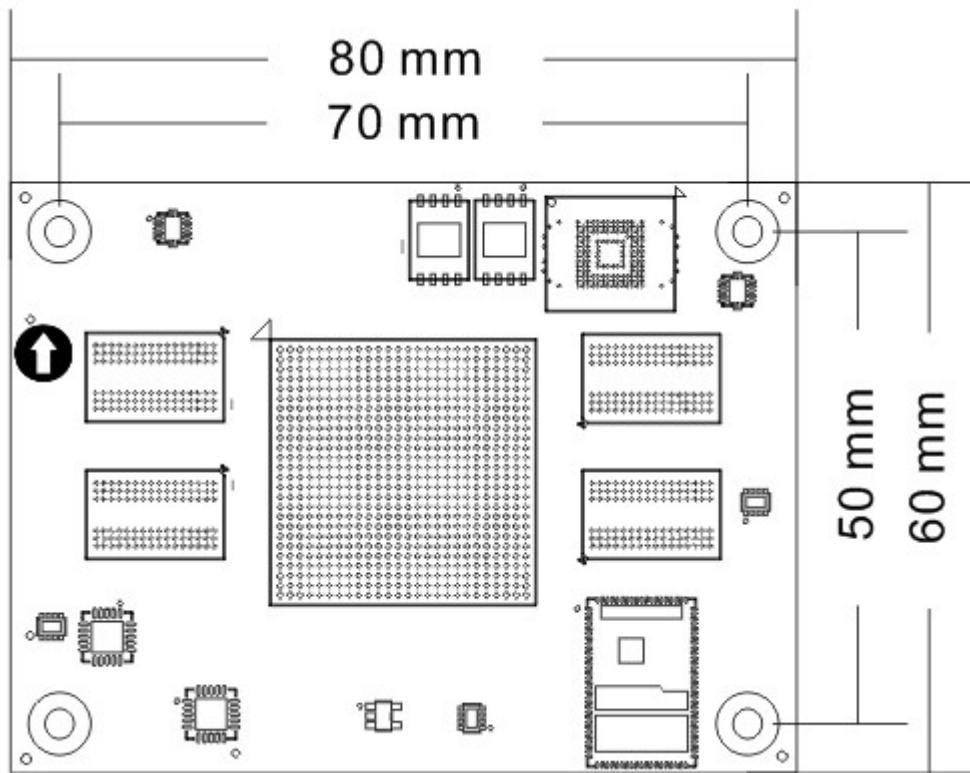
Top View

2.11 Connectors Pin Assignment

The core board has a total of 4 high-speed expansion ports, which are connected to the carrier board using four 120Pin board-to-board connectors (J29~J32). The connectors use Panasonic's AXK5A2137YG, and the corresponding connectors' model on the carrier board is AXK6A2337YG. J29 connects to BANK12's and BANK13's IO, J30 connects to GTX's transceiver signal, J31 connects to JTAG's and BANK35's IO (1.8V level standard), J32 connects to PS's MIO, BANK13's IO, and+5V power supply.

J29 connector pin assignment:

J29 Pin	Signal Name	ZYNQ Pin No.	J29 Pin	Signal Name	ZYNQ Pin No.
1	B13_L8_P	AE23	2	B13_L9_N	AB22
3	B13_L8_N	AF23	4	B13_L9_P	AB21
5	GND	-	6	GND	-

7	B13_L10_N	AA23	8	B13_L13_N	AD21
9	B13_L10_P	AA22	10	B13_L13_P	AD20
11	GND	-	12	GND	-
13	B13_L15_N	AF20	14	B13_L14_N	AC22
15	B13_L15_P	AF19	16	B13_L14_P	AC21
17	GND	-	18	GND	-
19	B13_L23_N	W19	20	B13_L7_P	AE22
21	B13_L23_P	W18	22	B13_L7_N	AF22
23	GND	-	24	GND	-
25	B13_L22_P	AA19	26	B13_L20_P	AA20
27	B13_L22_N	AB19	28	B13_L20_N	AB20
29	GND	-	30	GND	-
31	B13_L17_N	AD19	32	B13_L18_N	AF18
33	B13_L17_P	AD18	34	B13_L18_P	AE18
35	GND	-	36	GND	-
37	B13_L19_N	Y20	38	B13_L16_N	AE21
39	B13_L19_P	W20	40	B13_L16_P	AE20
41	GND	-	42	GND	-
43	B13_L24_N	AA18	44	B13_L21_N	AC19
45	B13_L24_P	Y18	46	B13_L21_P	AC18
47	GND	-	48	GND	-
49	B12_L23_P	Y16	50	B12_L18_N	AF17
51	B12_L23_N	Y15	52	B12_L18_P	AE17
53	GND	-	54	GND	-
55	B12_L15_P	AD16	56	B12_L16_P	AF15
57	B12_L15_N	AD15	58	B12_L16_N	AF14
59	GND	-	60	GND	-
61	B12_L14_P	AB15	62	B12_L13_N	AD14
63	B12_L14_N	AB14	64	B12_L13_P	AC14
65	GND	-	66	GND	-
67	B12_L10_N	AF13	68	B12_L19_P	Y17
69	B12_L10_P	AE13	70	B12_L19_N	AA17

71	GND	-	72	GND	-
73	B12_L4_P	AB11	74	B12_L20_P	AB17
75	B12_L4_N	AB10	76	B12_L20_N	AB16
77	GND	-	78	GND	-
79	B12_L7_P	AE10	80	B12_L8_N	AF12
81	B12_L7_N	AD10	82	B12_L8_P	AE12
83	GND	-	84	GND	-
85	B12_L24_P	W16	86	B12_L21_P	AC17
87	B12_L24_N	W15	88	B12_L21_N	AC16
89	GND	-	90	GND	-
91	B12_L3_N	AA10	92	B12_L17_P	AE16
93	B12_L3_P	Y10	94	B12_L17_N	AE15
95	GND	-	96	GND	-
97	B12_L11_P	AC12	98	B12_L22_P	AA15
99	B12_L11_N	AD11	100	B12_L22_N	AA14
101	GND	-	102	GND	-
103	B12_L12_N	AD13	104	B12_L5_P	W13
105	B12_L12_P	AC13	106	B12_L5_N	Y13
107	GND	-	108	GND	-
109	B12_L6_P	AA13	110	B12_L9_P	AE11
111	B12_L6_N	AA12	112	B12_L9_N	AF10
113	GND	-	114	GND	-
115	B12_L1_P	Y12	116	B12_L2_P	AB12
117	B12_L1_N	Y11	118	B12_L2_N	AC11
119	GND	-	120	GND	-

J30 connector pin assignment:

J30 Pin	Signal Name	ZYNQ Pin No.	J30 Pin	Signal Name	ZYNQ Pin No.
1			2		
3			4		
5	GND	-	6	GND	-

7			8		
9			10		
11	GND	-	12	GND	-
13			14		
15			16		
17	GND	-	18	GND	-
19			20		
21			22		
23	GND	-	24	GND	-
25			26		
27			28		
29	GND	-	30	GND	-
31	BANK112_TX0_N	AA1	32	BANK112_RX0_N	AB3
33	BANK112_TX0_P	AA2	34	BANK112_RX0_P	AB4
35	GND	R13	36	GND	R13
37	BANK112_TX1_N	W1	38	BANK112_RX1_N	Y3
39	BANK112_TX1_P	W2	40	BANK112_RX1_P	Y4
41	GND	R13	42	GND	R13
43	BANK112_TX2_N	U1	44	BANK112_RX2_N	V3
45	BANK112_TX2_P	U2	46	BANK112_RX2_P	V4
47	GND	R13	48	GND	R13
49	BANK112_TX3_N	R1	50	BANK112_RX3_N	T3
51	BANK112_TX3_P	R2	52	BANK112_RX3_P	T4
53	GND	R13	54	GND	R13
55	BANK112_CLK0_N	R5	56	BANK112_CLK1_N	U5
57	BANK112_CLK0_P	R6	58	BANK112_CLK1_P	U6
59	GND	-	60	GND	R13
61			62	BANK111_RX3_N	AD3
63			64	BANK111_RX3_P	AD4
65	GND	-	66	GND	R13
67			68	BANK111_TX3_N	AC1
69			70	BANK111_TX3_P	AC2

71	GND	-	72	GND	R13
73			74	BANK111_RX2_N	AC5
75			76	BANK111_RX2_P	AC6
77	GND	-	78	GND	R13
79			80	BANK111_TX2_N	AE1
81			82	BANK111_TX2_P	AE2
83	GND	-	84	GND	R13
85			86	BANK111_RX1_N	AE5
87			88	BANK111_RX1_P	AE6
89	GND	-	90	GND	R13
91			92	BANK111_TX1_N	AF3
93			94	BANK111_TX1_P	AF4
95	GND	-	96	GND	R13
97			98	BANK111_RX0_N	AD7
99			100	BANK111_RX0_P	AD8
101	GND	-	102	GND	R13
103			104	BANK111_TX0_N	AF7
105			106	BANK111_TX0_P	AF8
107	GND	-	108	GND	R13
109			110	BANK111_CLK0_N	W5
111			112	BANK111_CLK0_P	W6
113	GND	-	114	GND	-
115			116		
117			118		
119	GND	-	120	GND	-

J31 connector pin assignment:

J31 Pin	Signal Name	ZYNQ Pin No.	J31 Pin	Signal Name	ZYNQ Pin No.
1	FPGA_TCK	W12	2	FPGA_TDI	V11
3	FPGA_TMS	W11	4	FPGA_TDO	W10
5	GND	-	6	GND	-

7	B35_L3_P	G10	8	B35_L2_P	E10
9	B35_L3_N	F10	10	B35_L2_N	D10
11	GND	-	12	GND	-
13	B35_L7_N	H12	14	B35_L6_P	F13
15	B35_L7_P	H13	16	B35_L6_N	E13
17	GND	-	18	GND	-
19	B35_L4_P	E11	20	B35_L23_P	C11
21	B35_L4_N	D11	22	B35_L23_N	B11
23	GND	-	24	GND	-
25	B35_L5_N	G11	26	B35_L22_P	C12
27	B35_L5_P	G12	28	B35_L22_N	B12
29	GND	-	30	GND	-
31	B35_L8_P	K13	32	B35_L24_N	A12
33	B35_L8_N	J13	34	B35_L24_P	A13
35	GND	-	36	GND	-
37	B35_L12_P	J14	38	B35_L11_N	F14
39	B35_L12_N	H14	40	B35_L11_P	G14
41	GND	-	42	GND	-
43	B35_L9_P	K15	44	B35_L19_N	C13
45	B35_L9_N	J15	46	B35_L19_P	D13
47	GND	-	48	GND	-
49	B35_L1_N	E12	50	B35_L21_N	A14
51	B35_L1_P	F12	52	B35_L21_P	A15
53	GND	-	54	GND	-
55	B35_L17_N	B15	56	B35_L14_P	F15
57	B35_L17_P	B16	58	B35_L14_N	E15
59	GND	-	60	GND	-
61	B35_L20_N	B14	62	B35_L18_P	B17
63	B35_L20_P	C14	64	B35_L18_N	A17
65	GND	-	66	GND	-
67	B35_L10_N	G15	68	B35_L15_N	C16
69	B35_L10_P	G16	70	B35_L15_P	C17

71	GND	-	72	GND	-
73	B35_L13_N	D14	74		
75	B35_L13_P	D15	76		
77	GND	-	78	GND	-
79	B35_L16_N	D16	80		
81	B35_L16_P	E16	82		
83	GND	-	84	GND	-
85			86		
87			88		
89	GND	-	90	GND	-
91			92		
93			94		
95	GND	-	96	GND	-
97			98		
99			100		
101	GND	-	102	GND	-
103			104		
105			106		
107	GND	-	108	GND	-
109			110		
111			112		
113	GND	-	114	GND	-
115	PS_POR_B		116		
117	SYS_RESET	-	118		
119	GND	-	120	GND	-

J32 connector pin assignment:

J32 Pin	Signal Name	ZYNQ Pin No.	J32 Pin	Signal Name	ZYNQ Pin No.
1	PS_MIO5	C26	2	PS_MIO17	G17
3	PS_MIO4	F24	4	PS_MIO18	G20
5	GND	-	6	GND	-

7	PS_MIO14	D23	8	PS_MIO19	G19
9	PS_MIO15	C24	10	PS_MIO20	H19
11	GND	-	12	GND	-
13	PS_MIO52	A20	14	PS_MIO16	G21
15	PS_MIO53	A19	16	PS_MIO21	F22
17	GND	-	18	GND	-
19	PS_MIO7	E23	20	PS_MIO26	H17
21			22	PS_MIO25	F19
23	GND	-	24	GND	-
25	PS_MIO40	C22	26	PS_MIO24	J19
27	PS_MIO41	C19	28	PS_MIO23	F20
29	GND	-	30	GND	-
31	PS_MIO42	F17	32	PS_MIO27	F18
33	PS_MIO43	D18	34	PS_MIO22	G22
35	GND	-	36	GND	-
37	PS_MIO44	E18	38	PS_MIO30	K19
39	PS_MIO45	C18	40	PS_MIO29	E20
41	GND	-	42	GND	-
43			44	PS_MIO36	K16
45			46	PS_MIO31	E21
47	GND	-	48	GND	-
49			50	PS_MIO32	K17
51			52	PS_MIO33	E22
53	GND	-	54	GND	-
55			56	PS_MIO34	J16
57			58	PS_MIO35	D19
59	GND	-	60	GND	-
61			62	PS_MIO28	J18
63			64	PS_MIO37	D20
65	GND	-	66	GND	-
67			68	PS_MIO38	D21
69			70	PS_MIO39	C21

71	GND	-	72	GND	-
73			74		
75			76		
77	GND	-	78	GND	-
79			80		
81			82		
83	GND	-	84	GND	-
85	B13_L1_P	AA25	86	B13_L11_P	AD23
87	B13_L1_N	AB25	88	B13_L11_N	AD24
89	GND	-	90	GND	-
91	B13_L6_P	AA24	92	B13_L4_P	AD25
93	B13_L6_N	AB24	94	B13_L4_N	AD26
95	GND	-	96	GND	-
97	B13_L2_N	AC26	98	B13_L5_P	AF24
99	B13_L2_P	AB26	100	B13_L5_N	AF25
101	GND	-	102	GND	-
103	B13_L12_P	AC23	104	B13_L3_P	AE25
105	B13_L12_N	AC24	106	B13_L3_N	AE26
107	+5V	-	108	+5V	-
109	+5V	-	110	+5V	-
111	+5V	-	112	+5V	-
113	+5V	-	114	+5V	-
115	+5V	-	116	+5V	-
117	+5V	-	118	+5V	-
119	+5V	-	120	+5V	-

3. Carrier Board

3.1　Introduction

Through the previous function introduction, we can take a look at the function of the carrier board now:

- 1x PCIEx4 Interface
- 4x SFP Interface
- 2x 10/100M/1000M Ethernet RJ-45 Interface
- 1x HDMI Video Output Interface
- 1x HDMI Video Input Interface
- 4x USB HOST Interface
- 1x USB Uart Communication Interface
- 1x SD Card Interface
- 1x 40pin Expansion Port
- JTAG Debugging Interface
- 4x Independent keys
- 4x LED Lights

3.2　Uart to USB Interface

The AX7Z035B carrier board is equipped with a Uart to USB interface for system debugging. The conversion chip uses the USB-UAR chip of Silicon Labs CP2102GM. The USB interface uses the MINI USB interface. It can be connected to the USB port of the upper PC with a USB cable for separate power supply and serial data communication of the core board.

The schematic diagram of USB Uart circuit design is shown in the following figure:
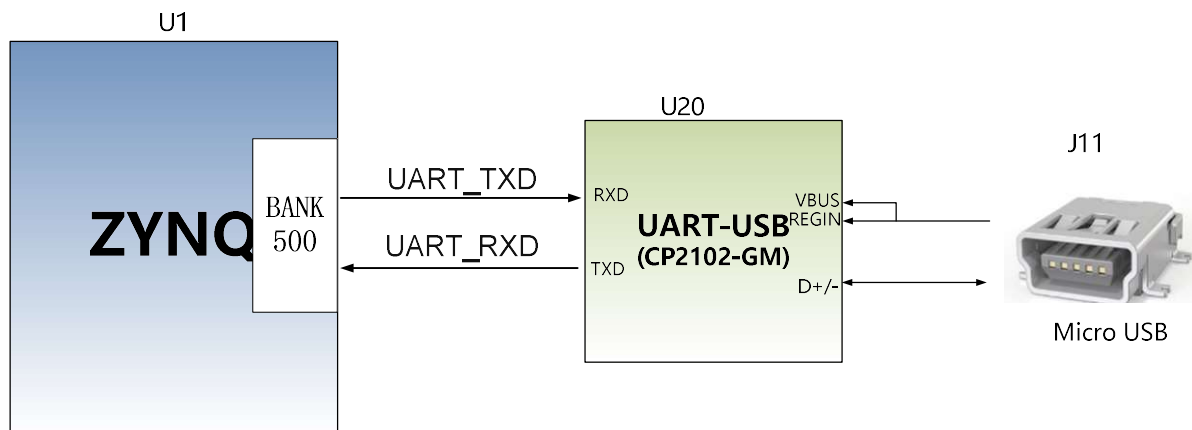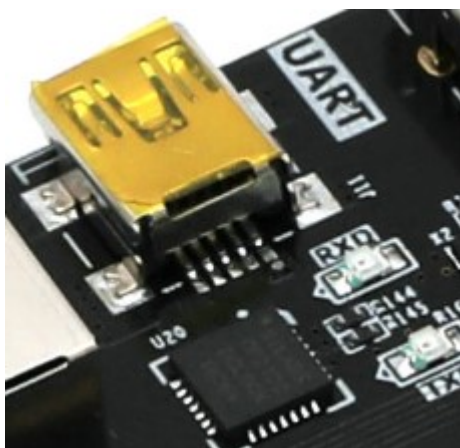
Figure 3-2-1: USB to serial port schematic

Figure 3-2-2: USB to serial port on the AX7Z035B Board

USB to serial port ZYNQ pin assignment:

Signal name	ZYNQ Pin	ZYNQ Pin Number	Description
UART_RXD	PS_MIO14_500	D23	Uart data input
UART_TXD	PS_MIO15_500	C24	Uart data output

3.3 Gigabit Ethernet Interface

The AX7Z035B development board has two Gigabit Ethernet interfaces, one of which is connected to the PS system, and the other one is connected to the logical IO ports of the PL. The Gigabit Ethernet interface connected to the PL side needs to be mounted to ZYNQ's AXI bus system via program calling IP.

The Ethernet chip adopts JL Semiconductor's industrial-grade Ethernet GPHY chip (JL2121-N040I) to provide network communication services for users. The Ethernet PHY chip on the PS end is connected to the GPIO interface of ZYNQ's PS

BANK501. The Ethernet PHY chip on the PL end is connected to the IO of BANK35. The JL2121 chip supports a 10/100/1000 Mbps network transmission rate and communicates data with the MAC layer of the Zynq7000 system through the RGMII interface. JL2121D supports MDI/MDX self-adaptation, various speed self-adaptations, Master/Slave self-adaptation, and supports MDIO bus for PHY register management.

JL2121 will detect the level status of specific IO when powered on to determine its own operating mode. Table 3-3-1 describes the default setting of the GPHY chip after power on.

Configuration Pin	Description	Configuration Value
RXD3_ADR0 RXC_ADR1 RXCTL_ADR2	PHY address in MDIO/MDC mode	PHY Address is 001
RXD1_TXDLY	TX clock 2ns delay	Delay
RXD0_RXDLY	RX clock 2ns delay	Delay

Table 3-3-1: PHY chip default configuration value

When the network is connected to a Gigabit Ethernet, ZYNQ and PHY chip JL2121 communicate over the RGMII bus for data transmission, the transmission clock is 125Mhz, and data is sampled on the rising edge and falling edge of the clock.

When the network is connected to 100 Gigabit Ethernet, ZYNQ and PHY chip JL2121 communicate over the RMII bus for data transmission, and the transmission clock is 25Mhz. Data is sampled on the rising edge and falling edge of the clock.

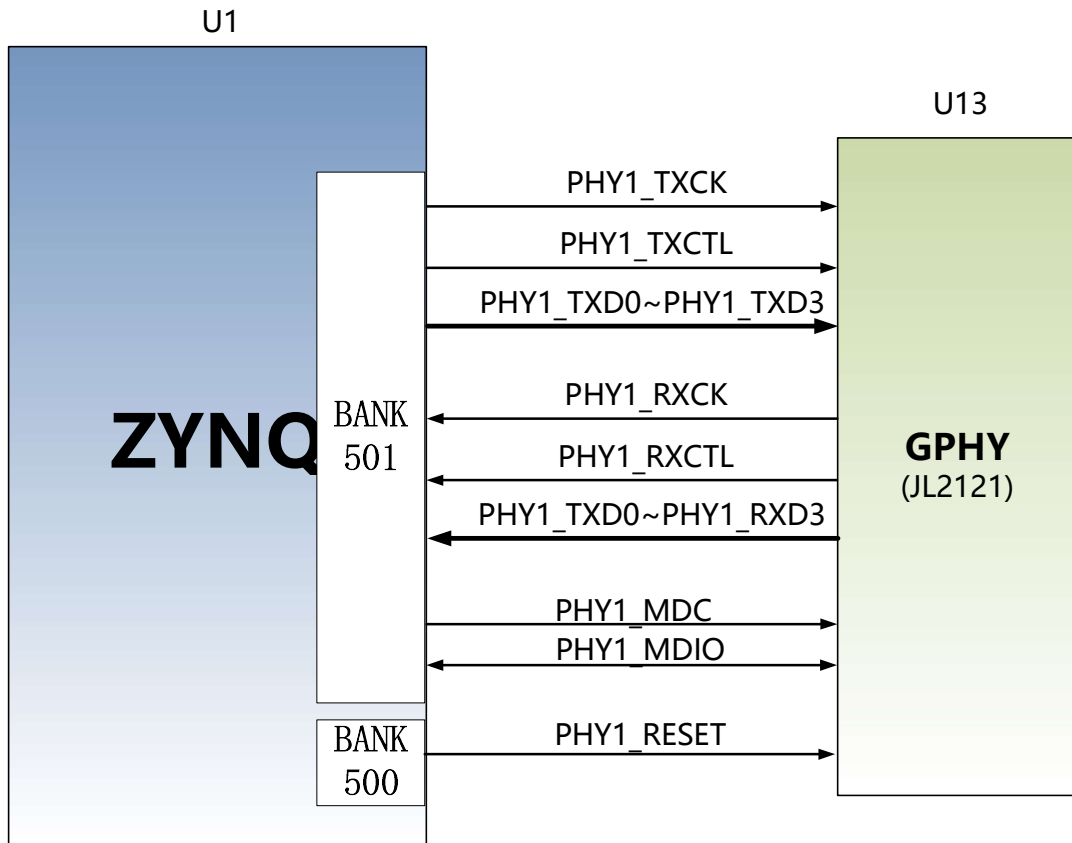Figure 3-3-1 shows the connection diagram of the PS Ethernet PHY chip.

U1

U13

ZYNQ

BANK
501

BANK
500

GPHY
(JL2121)

PHY1_TXCK

PHY1_TXCTL

PHY1_TXD0~PHY1_TXD3

PHY1_RXCK

PHY1_RXCTL

PHY1_TXD0~PHY1_RXD3

PHY1_MDC

PHY1_MDIO

PHY1_RESET

Figure 3-3-1: Connection between ZYNQ PS system and GPHY

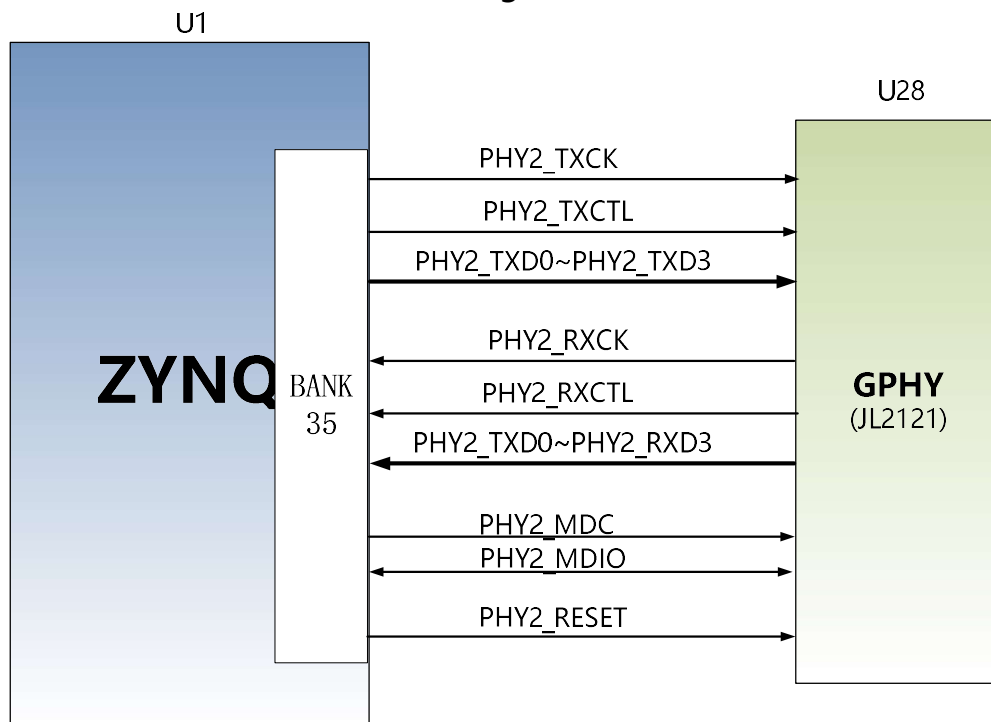Figure 3-3-2 shows the connection diagram of the ZYNQ PL Ethernet PHY chip:

U1

U28

ZYNQ

BANK
35

GPHY
(JL2121)

PHY2_TXCK

PHY2_TXCTL

PHY2_TXD0~PHY2_TXD3

PHY2_RXCK

PHY2_RXCTL

PHY2_TXD0~PHY2_RXD3

PHY2_MDC

PHY2_MDIO

PHY2_RESET

Figure 3-3-2: Connection between ZYNQ PL and GPHY

PS side Gigabit Ethernet pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
PHY1_TXCK	PS_MIO16_501	G21	RGMII Transmit Clock
PHY1_TXD0	PS_MIO17_501	G17	Transmit data bit0
PHY1_TXD1	PS_MIO18_501	G20	Transmit data bit1
PHY1_TXD2	PS_MIO19_501	G19	Transmit data bit2
PHY1_TXD3	PS_MIO20_501	H19	Transmit data bit3
PHY1_TXCTL	PS_MIO21_501	F22	Transmit enable signal
PHY1_RXCK	PS_MIO22_501	G22	RGMII Receive Clock
PHY1_RXD0	PS_MIO23_501	F20	Receive data Bit0
PHY1_RXD1	PS_MIO24_501	J19	Receive data Bit1
PHY1_RXD2	PS_MIO25_501	F19	Receive data Bit2
PHY1_RXD3	PS_MIO26_501	H17	Receive data Bit3
PHY1_RXCTL	PS_MIO27_501	F18	Receive data valid signal
PHY1_MDC	PS_MIO52_501	A20	MDIO Management clock
PHY1_MDIO	PS_MIO53_501	A19	MDIO Management data
PHY1_RESET	PS_MIO7_500	E23	Reset signal

PL side Gigabit Ethernet pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
PHY2_TXCK	B35_L23_P	C11	RGMII Transmit Clock
PHY2_TXD0	B35_L2_P	E10	Transmit data bit0
PHY2_TXD1	B35_L2_N	D10	Transmit data bit1
PHY2_TXD2	B35_L6_P	F13	Transmit data bit2
PHY2_TXD3	B35_L6_N	E13	Transmit data bit3
PHY2_TXCTL	B35_L23_N	B11	Transmit enable signal
PHY2_RXCK	B35_L11_P	G14	RGMII Receive Clock
PHY2_RXD0	B35_L24_P	A13	Receive data Bit0

PHY2_RXD1	B35_L24_N	A12	Receive data Bit1
PHY2_RXD2	B35_L22_N	B12	Receive data Bit2
PHY2_RXD3	B35_L22_P	C12	Receive data Bit3
PHY2_RXCTL	B35_L11_N	F14	Receive data valid signal
PHY2_MDC	B35_L19_N	C13	MDIO Management clock
PHY2_MDIO	B35_L19_P	D13	MDIO Management data
PHY2_RESET	B35_L21_N	A14	Reset signal

3.4   USB2.0 Host Interface

There are 4 USB2.0 HOST interfaces on the AX7Z035B FPGA development board. The USB2.0 transceiver uses a 1.8V, high-speed USB3320C-EZK chip that supports the ULPI standard interface, and then expands the 4-way USB HOST interfaces through a USB HUB chip USB2514. ZYNQ's USB bus interface is connected to the USB3320C-EZK transceiver for data communication in the high-speed USB2.0 Host mode. The USB3320C's USB data and control signals are connected to the IO port of PS BANK501 of the ZYNQ chip. The USB interface's differential signal (DP/DM) is connected to the USB2514 chip to extend four USB interfaces. Two 24MHz crystals provide clocks for USB3320C and USB2514 chips, respectively.

Four USB interfaces are flat-type USB interfaces (USB Type A), which allows users to connect different USB Slave peripherals (such as USB mouse and USB keyboard) at the same time. Each USB interface provides +5V power.

The schematic diagram of the connection among ZYNQ processor, USB3320C-EZK chip and USB2514 chip is shown as Figure 3-4-1:
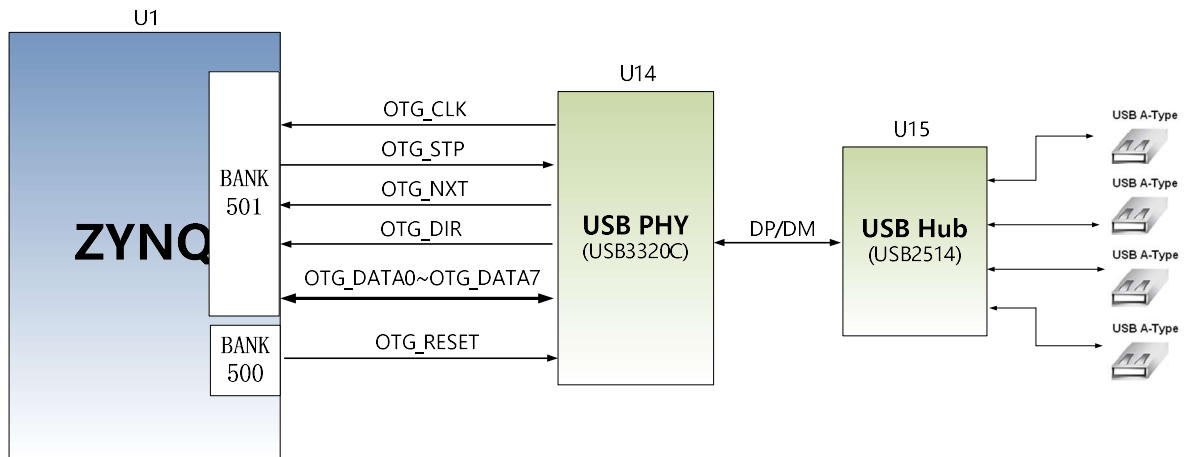
Figure 3-4-1: The connection between Zynq7000 and USB chips

USB2.0 pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
OTG_DATA4	PS_MIO28_501	J18	USB Data Bit4
OTG_DIR	PS_MIO29_501	E20	USB Data Direction Signal
OTG_STP	PS_MIO30_501	K19	USB Stop Signal
OTG_NXT	PS_MIO31_501	E21	USB Next Data Signal
OTG_DATA0	PS_MIO32_501	K17	USB Data Bit0
OTG_DATA1	PS_MIO33_501	E22	USB Data Bit1
OTG_DATA2	PS_MIO34_501	J16	USB Data Bit2
OTG_DATA3	PS_MIO35_501	D19	USB Data Bit3
OTG_CLK	PS_MIO36_501	K16	USB Clock Signal
OTG_DATA5	PS_MIO37_501	D20	USB Data Bit5
OTG_DATA6	PS_MIO38_501	D21	USB Data Bit6
OTG_DATA7	PS_MIO39_501	C21	USB Data Bit7
OTG_RESETN	PS_MIO7_500	E23	USB Reset Signal

3.5　HDMI Output Interface

The HDMI output interface is implemented by using ANALOG DEVICE's ADV7511 HDMI (DVI) encoding chip, which supports up to 1080P@60Hz output and supports 3D output.

Among them, the ADV7511's video digital interface, audio digital interface and

I2C configuration interface are connected to the PL BANK35 IO of the ZYNQ7000. The ZYNQ7000 system initializes and controls the ADV7511 through the I2C pin. The hardware connection diagram of ADV7511 chip and ZYNQ7000 is shown in Figure 3-5-1.
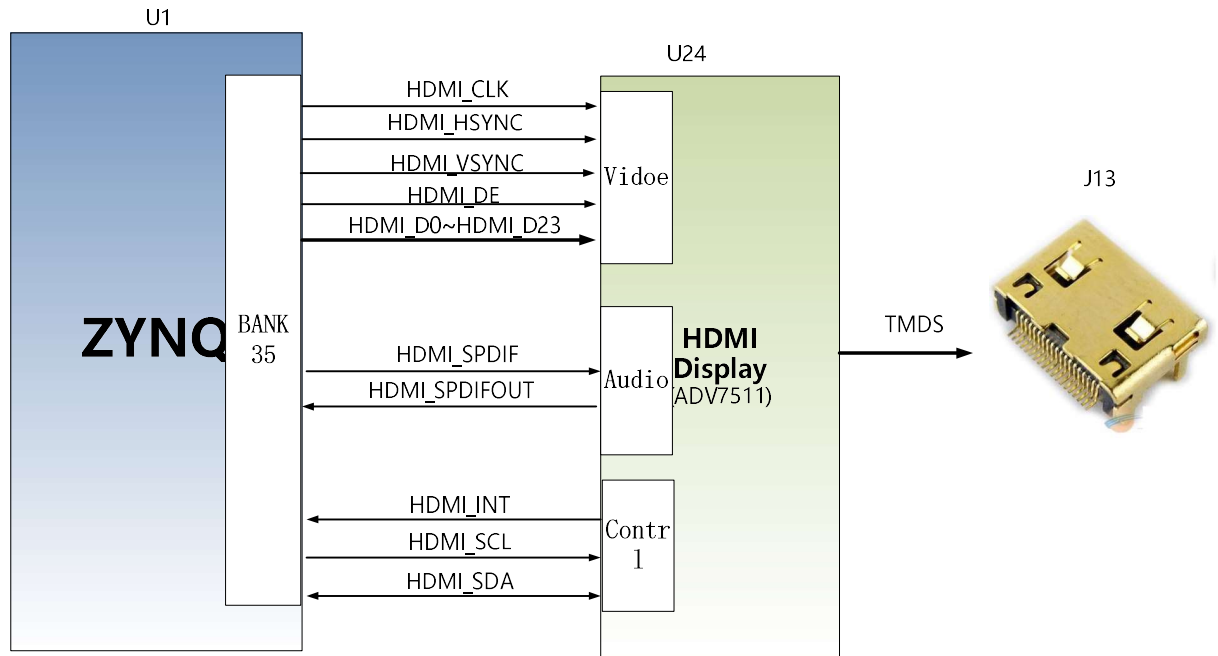

Figure 3-5-1: Schematic diagram of HDMI output interface design

ZYNQ pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
HDMI_CLK	B35_L9_P	K15	HDMI Video signal clock
HDMI_HSYNC	B35_L3_N	F10	HDMI Video signal line synchronization
HDMI_VSYNC	B35_L3_P	G10	HDMI Video signal column synchronization
HDMI_DE	B35_L7_N	H12	HDMI video signal is valid
HDMI_D0	B35_L7_P	H13	HDMI video signal data 0
HDMI_D1	B35_L4_P	E11	HDMI video signal data 1
HDMI_D2	B35_L4_N	D11	HDMI video signal data 2
HDMI_D3	B35_L5_N	G11	HDMI video signal data 3
HDMI_D4	B35_L5_P	G12	HDMI video signal data 4
HDMI_D5	B35_L8_P	K13	HDMI video signal data 5

HDMI_D6	B35_L8_N	J13	HDMI video signal data 6
HDMI_D7	B35_L12_P	J14	HDMI video signal data 7
HDMI_D8	B35_L12_N	H14	HDMI video signal data 8
HDMI_D9	B35_L9_N	J15	HDMI video signal data 9
HDMI_D10	B35_L1_N	E12	HDMI video signal data 10
HDMI_D11	B35_L1_P	F12	HDMI video signal data 11
HDMI_D12	B35_L17_N	B15	HDMI video signal data 12
HDMI_D13	B35_L17_P	B16	HDMI video signal data 13
HDMI_D14	B35_L20_N	B14	HDMI video signal data 14
HDMI_D15	B35_L20_P	C14	HDMI video signal data 15
HDMI_D16	B35_L10_N	G15	HDMI video signal data 16
HDMI_D17	B35_L10_P	G16	HDMI video signal data 17
HDMI_D18	B35_L13_N	D14	HDMI video signal data 18
HDMI_D19	B35_L13_P	D15	HDMI video signal data 19
HDMI_D20	B35_L16_N	D16	HDMI video signal data 20
HDMI_D21	B35_L16_P	E16	HDMI video signal data 21
HDMI_D22	B35_L15_P	C17	HDMI video signal data 22
HDMI_D23	B35_L15_N	C16	HDMI video signal data 23
HDMI_INT	B35_L21_P	A15	HDMI Interrupt signal
HDMI_SCL	B35_L18_P	B17	HDMI IIC control clock
HDMI_SDA	B35_L18_N	A17	HDMI IIC control data

3.6 HDMI Input Interface

The HDMI input interface uses Silion Image's SIL9011/SIL9013 HDMI decoder chip, which supports up to 1080P@60Hz input and supports data output in different formats.

Among them, the IIC configuration interface of SIL9011/SIL9013 is also connected with the IO of BANK13 of FPGA. ZYNQ initializes and controls SIL9013 by programming I2C bus. The hardware connection of HDMI input interface is shown in Figure 3-6-1.
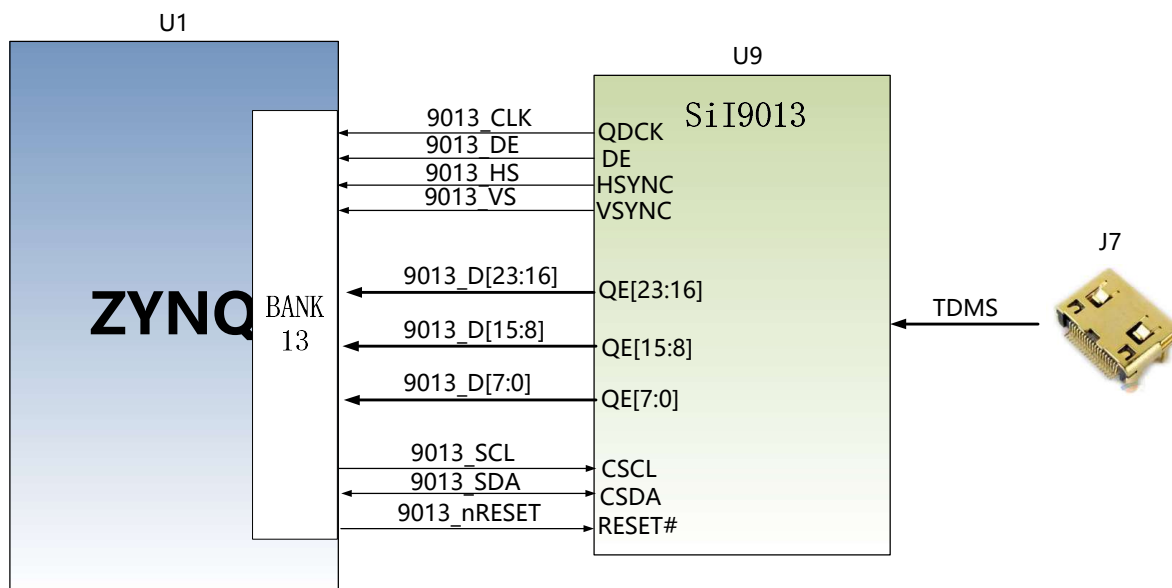
Figure 3-6-1: HDMI input schematic diagram

ZYNQ pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
9013_nRESET	B13_L24_N	AA18	9013 Reset Signal
9013_CLK	B13_L11_P	AD23	9013 video signal clock
9013_HS	B13_L5_P	AF24	9013 video signal line synchronization
9013_VS	B13_L5_N	AF25	9013 video signal column synchronization
9013_DE	B13_L4_N	AD26	9013 video signal valid
9013_D[0]	B13_L4_P	AD25	9013 video signal data 0
9013_D[1]	B13_L11_N	AD24	9013 video signal data 1
9013_D[2]	B13_L12_N	AC24	9013 video signal data 2
9013_D[3]	B13_L12_P	AC23	9013 video signal data 3
9013_D[4]	B13_L2_P	AB26	9013 video signal data 4
9013_D[5]	B13_L2_N	AC26	9013 video signal data 5
9013_D[6]	B13_L6_N	AB24	9013 video signal data 6
9013_D[7]	B13_L6_P	AA24	9013 video signal data 7
9013_D[8]	B13_L1_N	AB25	9013 video signal data 8
9013_D[9]	B13_L1_P	AA25	9013 video signal data 9

9013_D[10]	B13_L8_P	AE23	9013 video signal data 10
9013_D[11]	B13_L8_N	AF23	9013 video signal data 11
9013_D[12]	B13_L10_N	AA23	9013 video signal data 12
9013_D[13]	B13_L10_P	AA22	9013 video signal data 13
9013_D[14]	B13_L15_N	AF20	9013 video signal data 14
9013_D[15]	B13_L15_P	AF19	9013 video signal data 15
9013_D[16]	B13_L23_N	W19	9013 video signal data 16
9013_D[17]	B13_L23_P	W18	9013 video signal data 17
9013_D[18]	B13_L22_P	AA19	9013 video signal data 18
9013_D[19]	B13_L22_N	AB19	9013 video signal data 19
9013_D[20]	B13_L17_N	AD19	9013 video signal data 20
9013_D[21]	B13_L17_P	AD18	9013 video signal data 21
9013_D[22]	B13_L19_N	Y20	9013 video signal data 22
9013_D[23]	B13_L19_P	W20	9013 video signal data 23
9013_SCL	B13_L3_N	AE26	9013 IIC control clock
9013 _SDA	B13_L3_P	AE25	9013　control data

3.7 SFP Interface

The AX7Z035B carrier board has four SFP interfaces. Users can purchase SFP optical modules (1.25G, 2.5G, 10G optical modules on the market) and insert them into these four interfaces for optical data communication. The four SFP interfaces are connected to the two RX/TX of the GNK transceiver of ZYNQ BANK111. The TX signal and the RX signal are connected to the ZYNQ and the optical module through the DC blocking capacitor in differential signal mode. The TX and RX data rates are up to 10Gb/s per channel. The reference clock for the GTX transceiver of BANK111 is provided by the 125M differential clock of AC7Z035B FPGA core board.

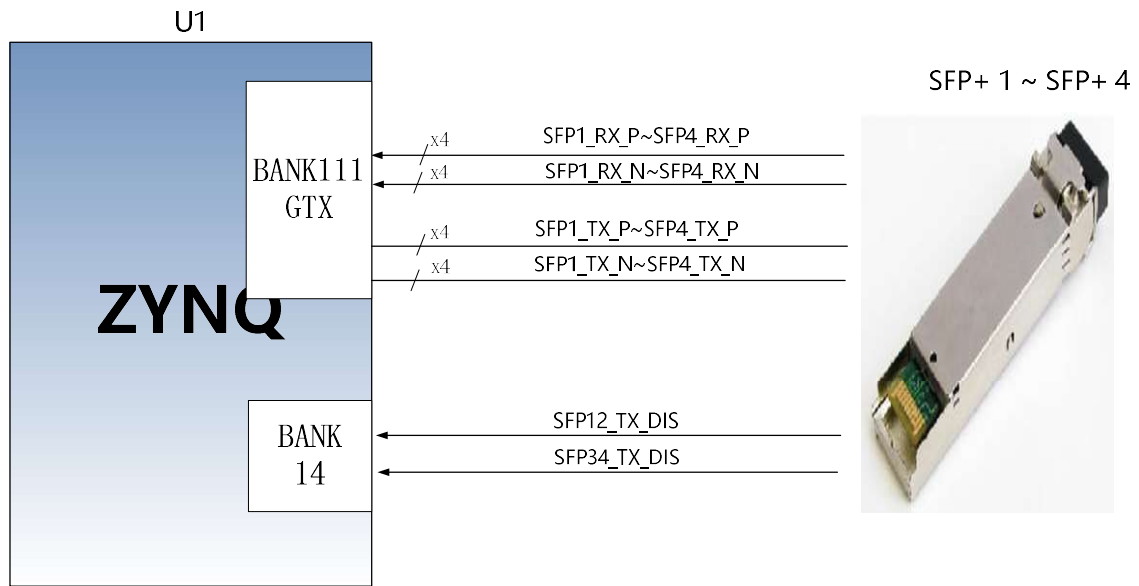The schematic diagram of FPGA and fiber optic design is shown in Figure 3-7-1:

Figure 3-7-1: Schematic diagram of fiber optic design

Pin assignment of 4 SFP interfaces:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
SFP1_TX_P	BANK111_TX0_P	AF8	Optical module 1 transmit data positive
SFP1_TX_N	BANK111_TX0_N	AF7	Optical module 1 transmit data negative
SFP1_RX_P	BANK111_RX0_P	AD8	Optical module 1 receive data positive
SFP1_RX_N	BANK111_RX0_N	AD7	Optical module 1 receive data negative
SFP2_TX_P	BANK111_TX1_P	AF4	Optical module 2 transmit data positive
SFP2_TX_N	BANK111_TX1_N	AF3	Optical module 2 transmit data negative
SFP2_RX_P	BANK111_RX1_P	AE6	Optical module 2 receive data positive
SFP2_RX_N	BANK111_RX1_N	AE5	Optical module 2 receive data negative
SFP3_TX_P	BANK111_TX2_P	AE2	Optical module 3 transmit data

			positive
SFP3_TX_N	BANK111_TX2_N	AE1	Optical module 3 transmit data negative
SFP3_RX_P	BANK111_RX2_P	AC6	Optical module 3 receive data positive
SFP3_RX_N	BANK111_RX2_N	AC5	Optical module 3 receive data negative
SFP4_TX_P	BANK111_TX3_P	AC2	Optical module 4 transmit data positive
SFP4_TX_N	BANK111_TX3_N	AC1	Optical module 4 transmit data negative
SFP4_RX_P	BANK111_RX3_P	AD4	Optical module 4 receive data positive
SFP4_RX_N	BANK111_RX3_N	AD3	Optical module 4 receive data negative
SFP12_TX_DIS	B12_L18_N	AF17	Optical module 12 Light emission prohibited, high effective
SFP34_TX_DIS	B12_L18_P	AE17	Optical module 34 Light emission prohibited, high effective

3.8   PCIe Slot

The AX7Z035B carrier board has a PCIe x4 interface. In order to be compatible with the AC7Z100 core board, the PCB is physically made into a PCIE x8 interface. In the electrical connection, we only have 4 pairs of transceivers connected to the PCIEx8 slot, so only PCIEex4, PCIex2, PCIex1 data communication can be realized.

The transmit and receive signals of the PCIe interface are directly connected to the GTX transceiver of the ZYNQ BANK112. Four-channel TX signals and the RX signals are connected to the BANK112 in differential signal mode, and the single-channel communication rate can up to 5G bit bandwidth.

The PCIe interface design diagram of the FPGA development board is shown in Figure 3-8-1, where the TX transmission signal is connected in AC coupling mode.
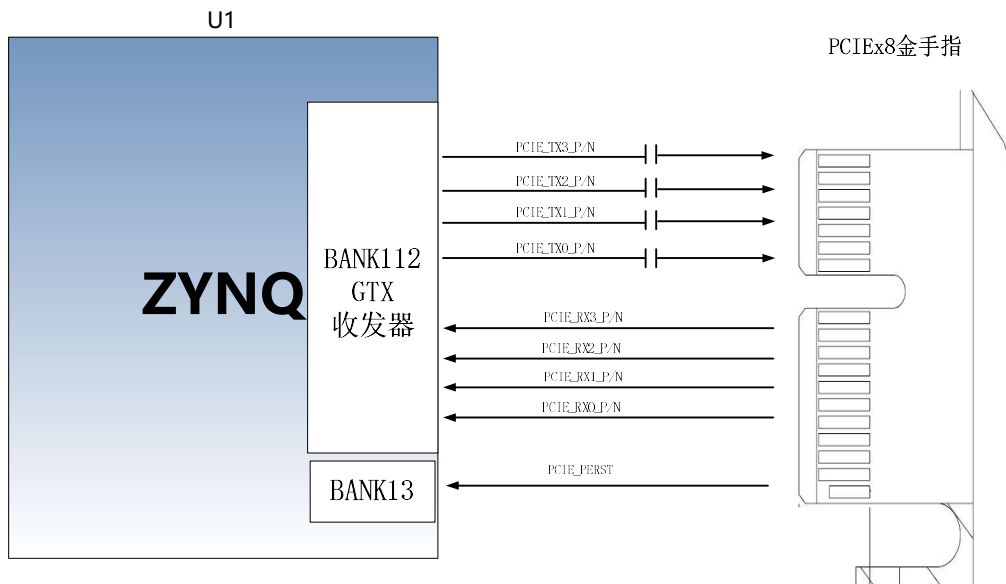
Figure 3-8-1: PCIe slot design schematic

PCIe x4 interface ZYNQ pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
PCIE_RX0_P	BANK112_RX3_P	T4	PCIE Channel 0 Data Receive Positive
PCIE_RX0_N	BANK112_RX3_N	T3	PCIE Channel 0 Data Receive Negative
PCIE_RX1_P	BANK112_RX2_P	V4	PCIE Channel 1 Data Receive Positive
PCIE_RX1_N	BANK112_RX2_N	V3	PCIE Channel 1 Data Receive Negative
PCIE_RX2_P	BANK112_RX1_P	Y4	PCIE Channel 2 Data Receive Positive
PCIE_RX2_N	BANK112_RX1_N	Y3	PCIE Channel 2 Data Receive Negative
PCIE_RX3_P	BANK112_RX0_P	AB4	PCIE Channel 3 Data Receive Positive
PCIE_RX3_N	BANK112_RX0_N	AB3	PCIE Channel 3 Data Receive Negative
PCIE_TX0_P	BANK112_TX3_P	R2	PCIE Channel 0 Data Transmit

			Positive
PCIE_TX0_N	BANK112_TX3_N	R1	PCIE Channel 0 Data Transmit Negative
PCIE_TX1_P	BANK112_TX2_P	U2	PCIE Channel 1 Data Transmit Positive
PCIE_TX1_N	BANK112_TX2_N	U1	PCIE Channel 1 Data Transmit Negative
PCIE_TX2_P	BANK112_TX1_P	W2	PCIE Channel 2 Data Transmit Positive
PCIE_TX2_N	BANK112_TX1_N	W1	PCIE Channel 2 Data Transmit Negative
PCIE_TX3_P	BANK112_TX0_P	AA2	PCIE Channel 3 Data Transmit Positive
PCIE_TX3_N	BANK112_TX0_N	AA1	PCIE Channel 3 Data Transmit Negative
PCIE_CLK_P	BANK112_CLK0_P	R6	PCIE Channel Reference Clock Positive
PCIE_CLK_N	BANK112_CLK0_N	R5	PCIE Channel Reference Clock Negative
PCIE_PERST	B13_L24_P	Y18	PCIE board reset signal

3.9   SD Card Slot

The AX7Z035B FPGA board contains a Micro SD card interface to provide user access to the SD card memory, the BOOT program for storing the ZYNQ chip, the Linux operating system kernel, the file system and other user data files.

The SDIO signal is connected to the IO signal of the PS BANK501 of ZYNQ. Since the VCCMIO of the BANK is set to 1.8V, but the data level of the SD card is 3.3V, so here we use the TXS02612 level converter to realize the connection. The schematic of the Zynq7000 PS and SD card connector is shown in Figure 3-9-1:
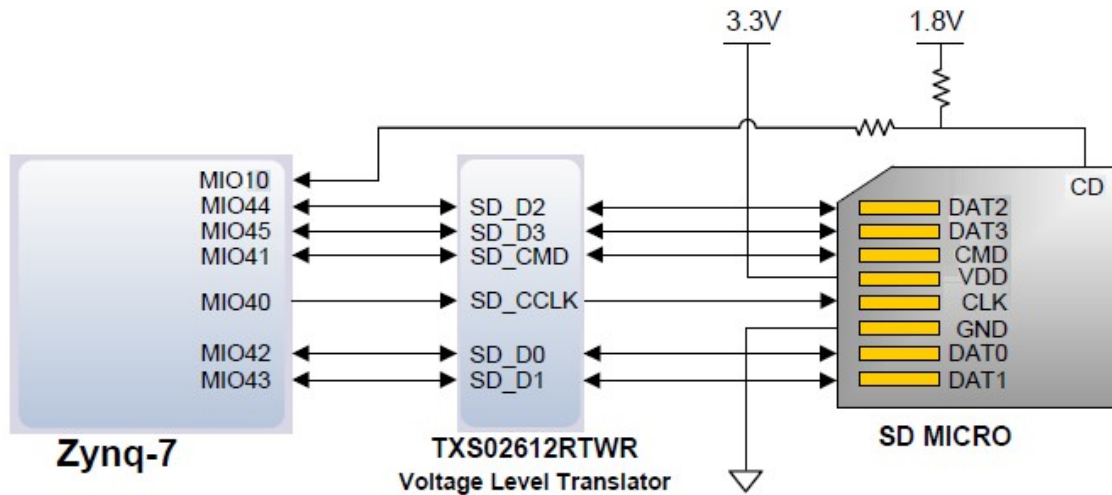
Figure 3-9-1: SD Card Connection Diagram

SD card slot pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
SD_CLK	PS_MIO40	C22	SD Clock Signal
SD_CMD	PS_MIO41	C19	SD Command Signa
SD_D0	PS_MIO42	F17	SD Data0
SD_D1	PS_MIO43	D18	SD Data1
SD_D2	PS_MIO44	E18	SD Data2
SD_D3	PS_MIO45	C18	SD Data3

3.10 40Pin Expansion Port

The carrier board is reserved with one 2.54-mm standard 40-pin expansion ports J33, which are used to connect the ALINX modules or the external circuit designed by the user himself. The expansion port has 40 signals with 1x 5V power supply, 2x 3.3 V power supply, 3x ground and 34x IO. IO of expansion port is connected to the IO of BANK12 of ZYNQ chip, the default is 3.3V. Do not directly connect the IO to 5V devices to avoid burning the FPGA. If you want to connect 5V devices, you need to connect a level conversion chip first.

The circuit of the expansion port (J33) is shown in Figure 3-10-1:

Figure 3-10-1: J33 schematic diagram
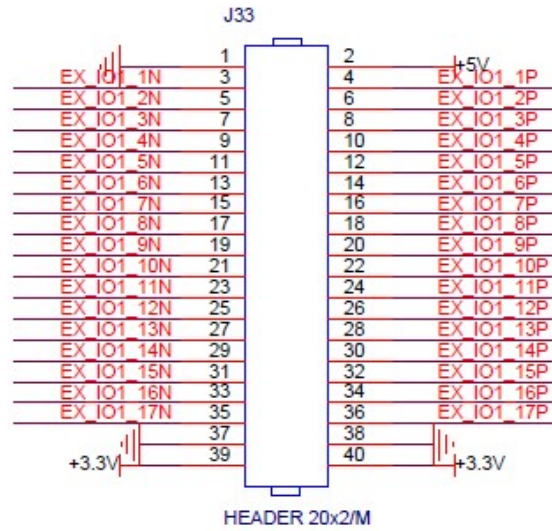
J33 ZYNQ pin assignment:

J33 Pin	Signal Name	ZYNQ Pin No.	J33 Pin	Signal Name	ZYNQ Pin No.
1	GND	-	2	+5V	-
3	IO1_1N	Y11	4	IO1_1P	Y12
5	IO1_2N	AC11	6	IO1_2P	AB12
7	IO1_3N	AA12	8	IO1_3P	AA13
9	IO1_4N	AF10	10	IO1_4P	AE11
11	IO1_5N	AC13	12	IO1_5P	AD13
13	IO1_6N	Y13	14	IO1_6P	W13
15	IO1_7N	AD11	16	IO1_7P	AC12
17	IO1_8N	AA14	18	IO1_8P	AA15
19	IO1_9N	Y10	20	IO1_9P	AA10
21	IO1_10N	AE15	22	IO1_10P	AE16
23	IO1_11N	W15	24	IO1_11P	W16
25	IO1_12N	AC16	26	IO1_12P	AC17
27	IO1_13N	AD10	28	IO1_13P	AE10

29	IO1_14N	AE12	30	IO1_14P	AF12
31	IO1_15N	AB10	32	IO1_15P	AB11
33	IO1_16N	AB16	34	IO1_16P	AB17
35	IO1_17N	AA17	36	IO1_17P	Y17
37	GND	-	38	GND	-
39	+3.3V	-	40	+3.3V	-

3.11 LED Light

There are 7 LEDs on the carrier board, including 1x power indicator, 2x serial communication indicators and 4x PL control indicators. When the board is powered on, the power indicator will light up; 4 LEDs are connected to the IO of the PL, users can control their on and off by programming. When the voltage of IO connected to the user LED is low, the user LED will off. When the voltage is high, the user LED will light up. Figure 3-11-1 shows the hardware connection of the user LED light:
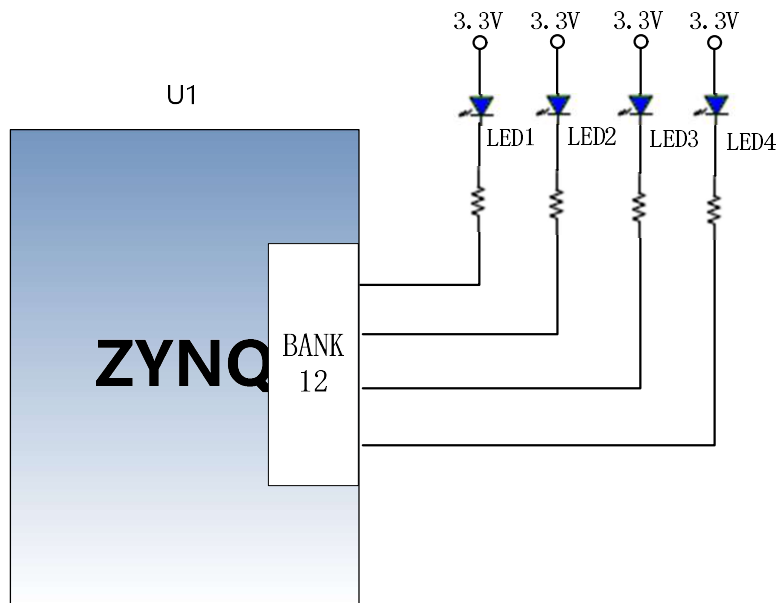
Figure 3-11-1: User LED Hardware Connection Diagram

User LED pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
PL_LED1	B12_L14_P	AB15	User PL LED1
PL_LED2	B12_L14_N	AB14	User PL LED2
PL_LED3	B12_L10_N	AF13	User PL LED3

PL_LED4	B12_L10_P	AE13	User PL LED4

3.12 Reset Key and User Key

The AX7Z035B has a reset key "RESET" and 4 user keys on the carrier board. The reset signal is connected to the reset chip input of the core board. Users can use this reset key to reset the ZYNQ system. The other four keys are connected to the IO of the PL. All the reset key and user keys are active in low level. The connection among the reset key and user keys is shown in Figure 3-12-1:

U1
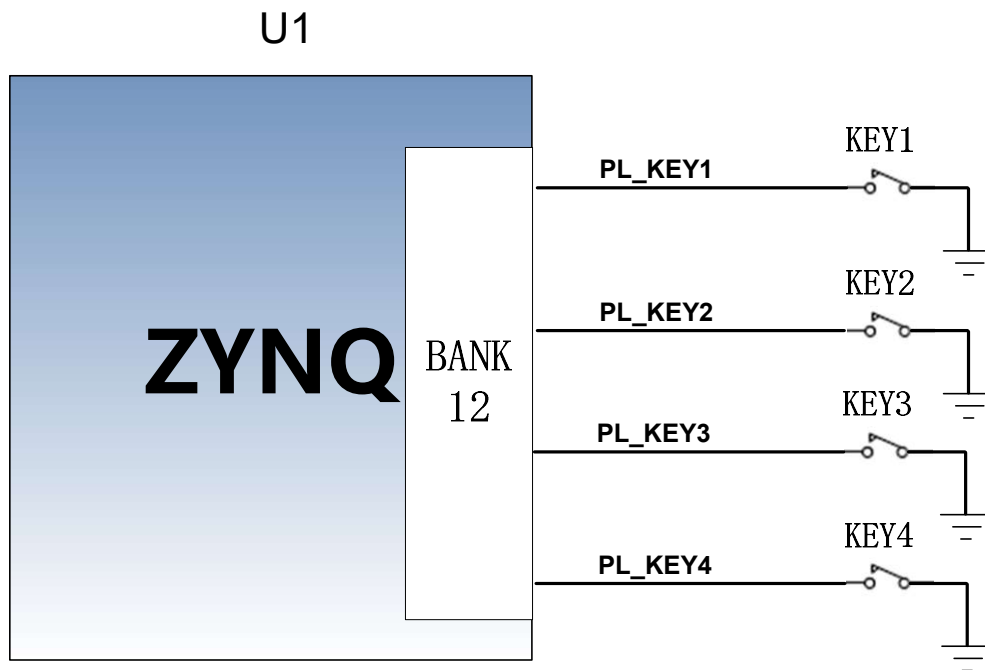
Figure 3-12-1: Schematic diagram of reset key connection

Key ZYNQ pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin No.	Description
PL_KEY1	B12_L16_P	AF15	PL key1 input
PL_KEY2	B12_L16_N	AF14	PL key2 input
PL_KEY3	B12_L13_N	AD14	PL key3 input
PL_KEY4	B12_L13_P	AC14	PL key4 input

3.13 JTAG Debugging Port

A JTAG interface is reserved on the carrier board for downloading ZYNQ programs or solidifying programs to FLASH. To prevent damage to the ZYNQ chip caused by hot-plugging or unplugging, we have added protective diodes to the JTAG signal to ensure that the signal voltage is within the range accepted by the FPGA and avoid damage to the ZYNQ chip.
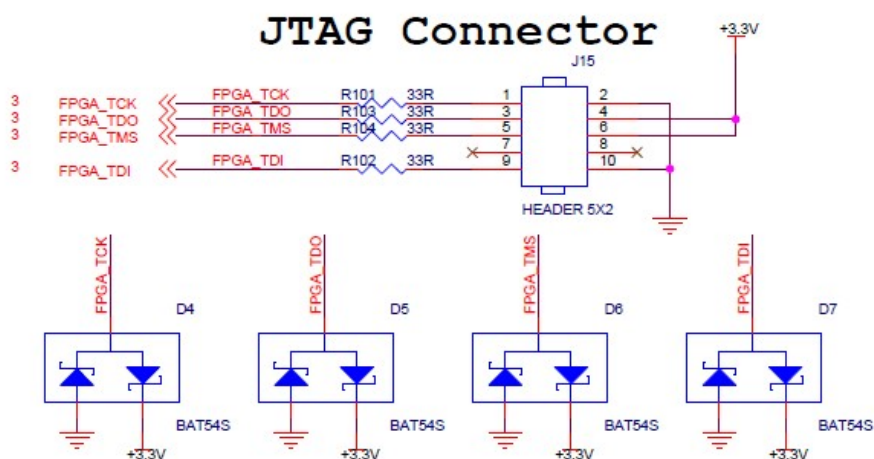

Figure 3-13-1: JTAG Interface Schematic

Users can connect the PC and JTAG interface through the USB downloader provided by us for ZYNQ system debugging. When plugging and unplugging JTAG cables, be careful not to hot plug and unplug them.

3.14 DIP Switch Configuration

There is a dip switch SW1 on the development board to configure the boot mode of the ZYNQ system. The board has three boot modes: JTAG debug mode, QSPI FLASH and SD card boot mode. When powered on, the XC7Z035 chip detects the level of the responding MIO ports (MIO5 and MIO4) to determine the boot mode. Users can select different boot modes through the dip switch SW1 on the core board. Table 3-14-1 lists the boot mode configuration of SW1.
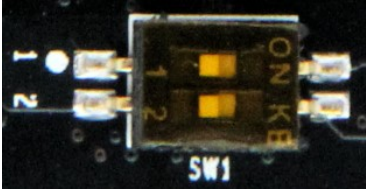
SW1	Dip Position （1, 2）	MIO5, MIO4 Level	Boot Mode
	ON、ON	0、0	JTAG
	OFF、OFF	1、1	SD Card
	OFF、ON	1、0	QSPI FLASH

Figure 3-14-1: SW1 boot mode configuration

3.15 Power Supply

The power input voltage of the development board is DC12V. You can supply power to the development board through the PCIE slot or external +12V power supply. When use external power supply, use the power supply equipped on the board instead of using other power supplies, to avoid damage to the development board. The power supply on the carrier board can convert into +5V, +3.3V and 1.8V through the 1-channel DC/DC power chip ETA8156FT2G and 2-channel DC/DC power chip ETA1471FT2G. Because the +5V power supply supplies the core board through connectors, the current output of the DCDC power supply is 6A, and the current output of the other 2 power supplies is 3A.

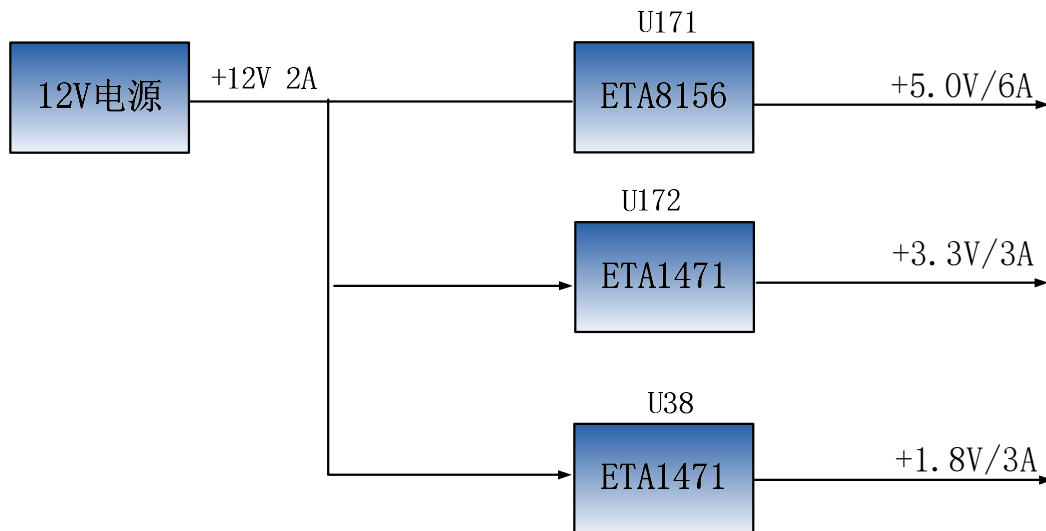The power supply design diagram on the board is shown in Figure 3-15-1 below:

Figure 3-15-1 Schematic diagram of the power interface

The functions of each power distribution are shown in the following table:

Power Supply	Function
+5.0V	Core board power supply

+1.8V	Ethernet，HDMI，USB
+3.3V	Ethernet，HDMI，USB，SD，SFP，PCIE

3.16 Fan

Because ZYNQ7035 generates a lot of heat when it is working properly, we added a heat sink and fan to the board to prevent the chip from overheating. Fan control is controlled by ZYNQ chip, the control pin is connected to the IO of BANK12. If the IO level output is low, the MOSFET tube is on, the fan will work; if the IO level output is high, the fan will stop. The fan design drawing on the board is shown in Figure 3-16-1 below:
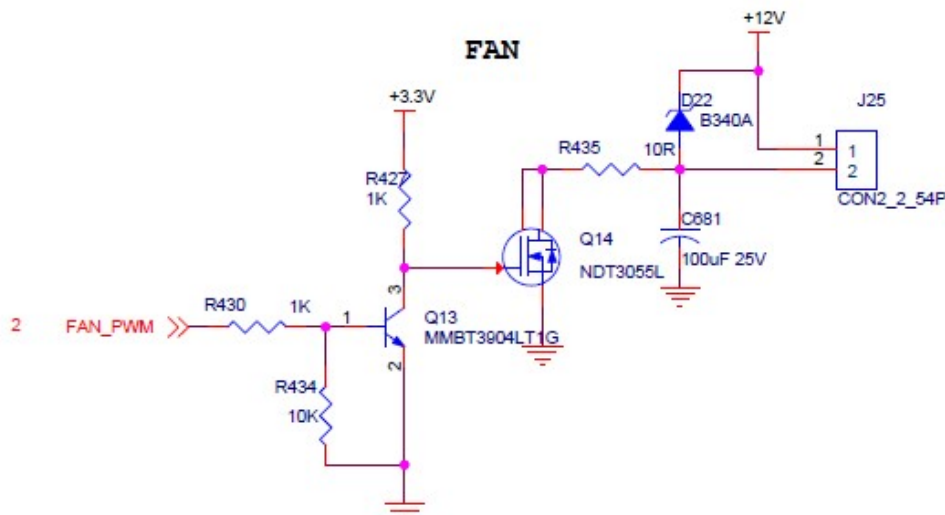

Figure 3-16-1: Fan design schematic

The fan has been fixed on the development board with screws before leaving the factory. The power supply of the fan is connected to the socket of the J25. The red one is positive and the black one is negative.
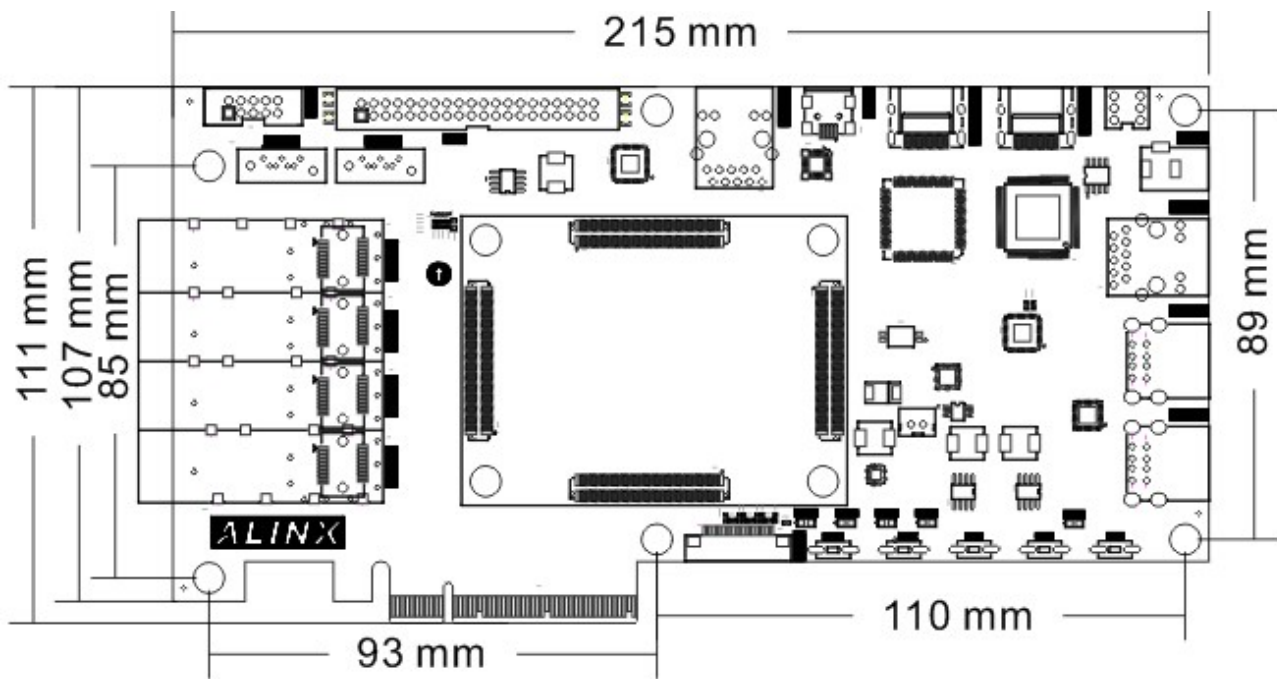
3.17 Size Dimension

Figure 3-17-1: Top View