

**ZYNQ7000 FPGA  
Development Board  
AX7Z100B  
User Manual**



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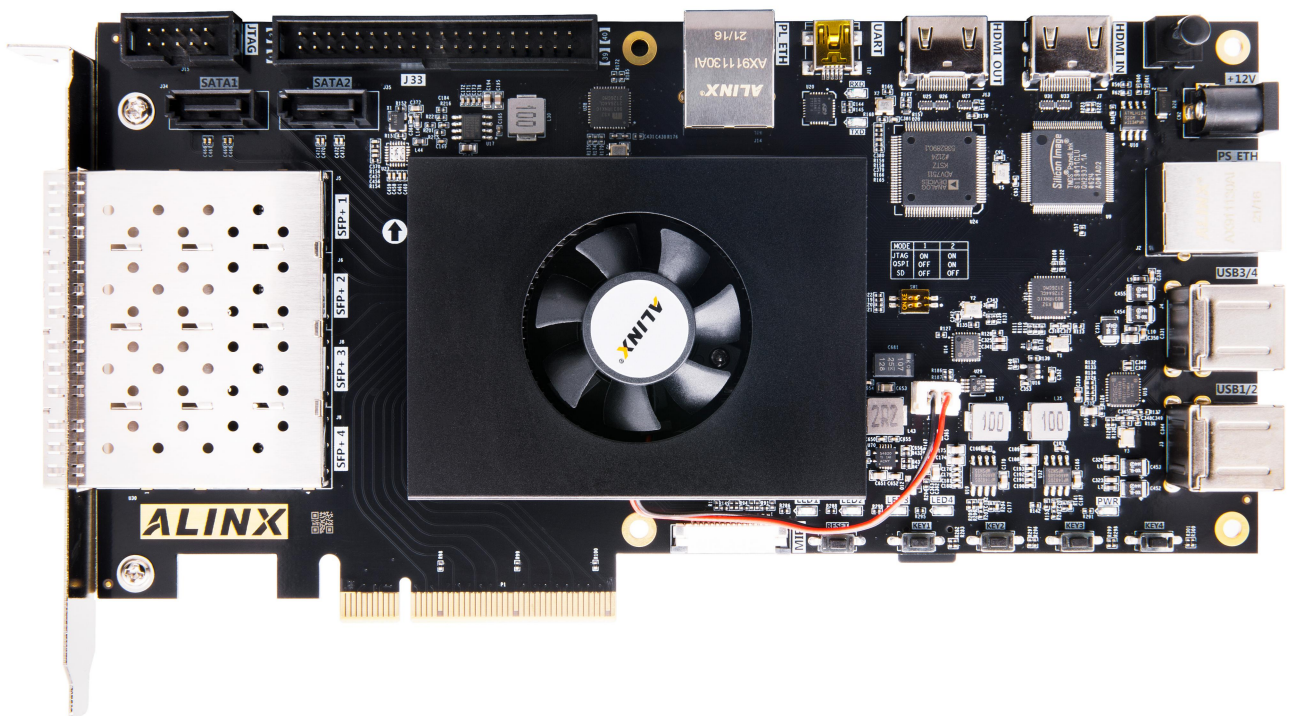
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This ZYNQ7000 FPGA development platform adopts the core board + carrier board mode, which is convenient for users to use the core board for secondary development. The core board uses XILINX's Zynq7000 SOC chip XC7Z100 solution, uses ARM+FPGA SOC technology to integrate dual-core ARM Cortex-A9 and FPGA programmable logic on a single chip. In addition, the core board contains 4 pieces of 2GB high-speed DDR3 SDRAM chips, 1 piece of 8GB eMMC memory chip and 2 pieces of 256Mb QSPI FLASH chips.

In the design of carrier board, we have extended a wealth of interfaces for users, such as a PCIe x8 slot, 4 fiber interfaces, 2 Gigabit Ethernet interfaces, 4 USB2.0 HOST interfaces, 1 HDMI output interface, 1 HDMI input interface, 1 UART serial interface, 1 SD card interface, 1 40-pin expansion interface and so on. It is a "professional" ZYNQ development platform and can meet users' requirements for high-speed data exchange, data storage, video transmission processing and industrial control. It provides possibility for high-speed data transmission and exchange, pre-verification and post-application of data processing. This product is very suitable for students, engineers and other groups engaged in ZYNQ development.

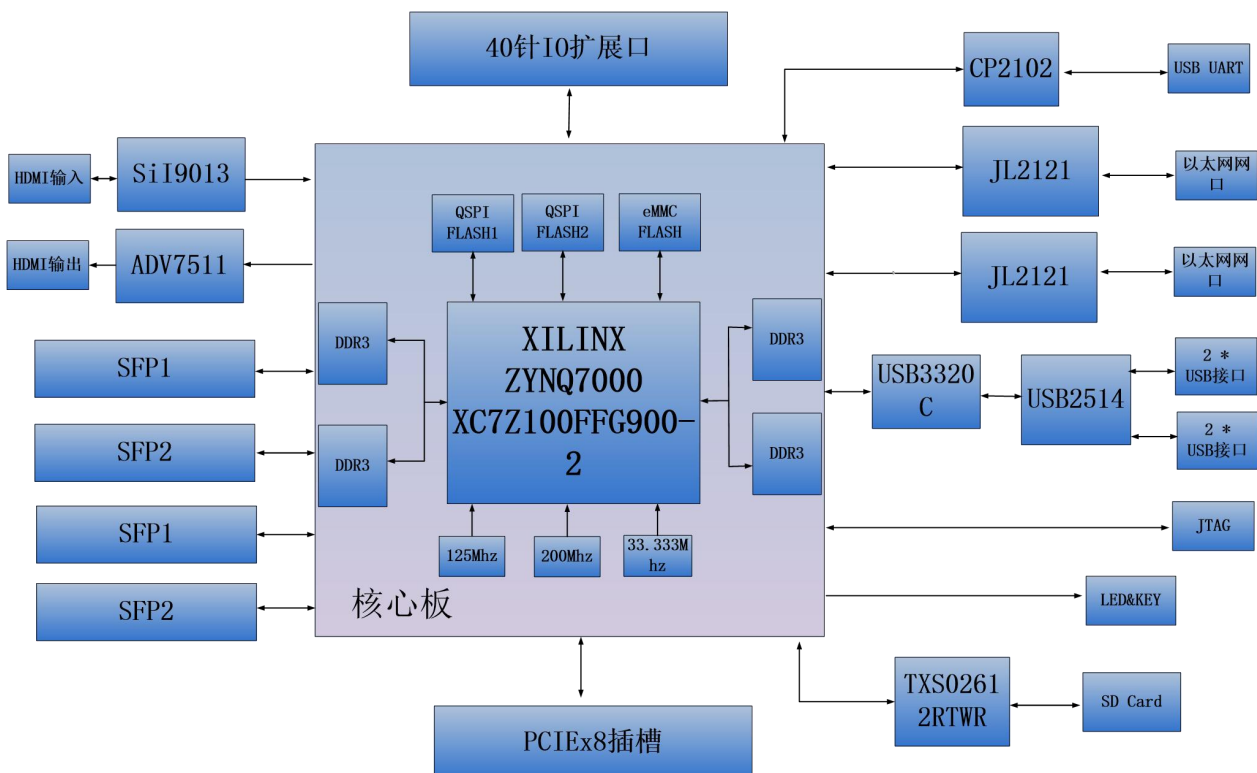


# 1. Development Board Introduction

The entire structure of the AX7Z100B FPGA development board is inherited from our consistent core board + carrier board model. High-speed board-to-board connectors are used between the core board and the carrier board.

The core board is mainly composed of ZYNQ7100 + 4 DDR3 + eMMC + QSPI FLASH. The ZYNQ7100 uses the Xilinx Zynq7000 series of chips, model XC7Z100-2FFG900. The ZYNQ7100 chip can be divided into Processor System (PS) and Programmable Logic (PL). Each side of PS and PL sides mounts two DDR3s, each DDR3 has a capacity of up to 512 Mbytes, so that ARM system and the FPGA system can independently process and store data. The PS-side 8GB eMMC FLASH memory chip and 512Mb QSPI FLASH are used to statically store ZYNQ's operating system, file system and user data.

The AX7Z100B carrier board expands rich peripheral interfaces for core board, including 1 PCIe8 interface, 4 SFP interfaces, 2 Gigabit Ethernet interfaces (one for PS and one for PL), 4 USB2.0 HOST interfaces, 1 HDMI output interface, 1 HDMI input interface, and 1 UART serial interface, 1 SD card interface, 1 40-pin expansion interface and some key LEDs. The following is the structure diagram of the whole development system:



Through this diagram, you can see the interfaces and functions that the AX7Z100B FPGA Development Board contains:

- ZYNQ7100 Core Board

The core board consists of XC7Z100+2GB DDR3+8GB eMMC FLASH + 512Mb QSPI FLASH. In addition, three crystal oscillators provide clocks. A single-ended 33.3333MHz crystal oscillator is supplied to the PS system, a differential 200MHz crystal oscillator provides the PL logic with DDR reference clock, and a differential 125MHz crystal provides the GTX transceiver with reference clock.

- PCIe x8 Interface

Supports the PCI Express 2.0 standard and provides standard PCIe x8 high-speed data transmission interface, single-channel communication rates can up to 5GBaud.

- 4 SFP Interfaces

4 high-speed transceivers of ZYNQ's GTX transceiver are connected to the transmission and reception of four optical modules to realize four high-speed optical fiber communication interfaces. Each fiber optic data communication reception and transmission at speeds up to 10 Gb/s.

- Gigabit Ethernet Interface

2 10/100M/1000M Ethernet RJ45 interfaces used for Ethernet data exchange with computers or other network devices. The network interface chip uses the JL2121 industrial-grade GPHY chip from JLSemi company. One Ethernet is connected to the PS end of the ZYNQ chip, and the other one is connected to the PL end of the ZYNQ chip.

- HDMI Video Output

1 HDMI video output interface, using ANALOG DEVICE company's ADV7511 HDMI coding chip, has a highest 1080P@60Hz output, supports 3D output.

- HDMI Video Input

1 HDMI video input interface, using Silion Image company's SIL9011/SIL9013 HDMI decoding chip, has a maximum 1080P@60Hz input, supports different formats of data input.

- USB2.0 HOST Interface

Extend 4 USB HOST interfaces through the USB Hub chip for connecting external USB slave devices, such as mouse, keyboard, USB flash drive and so on. The USB interface uses A flat USB interface (USB Type A).

- USB Uart Interface

1 Uart to USB interface used to communicate with the computer, convenient user debugging. The serial chip uses the USB-UAR chip of Silicon Labs CP2102GM, and the USB interface uses the MINI USB interface.

- Micro SD Card Slot

One Micro SD card slot used to store operating system images and file systems.

- 40-pin Expansion Port

A 40-pin 2.54mm pitch expansion port can be connected to various ALINX modules, such as binocular camera, TFT LCD screen, high-speed AD module, etc. The expansion port contains one 5V power supply, two 3.3V power supplies, three ground power supplies, and 34 I/O ports.

- JTAG Debugging Interface

A 10-pin 2.54mm standard JTAG interface for downloading and debugging FPGA programs. Users can debug and download ZYNQ system through XILINX downloader.

- LED

9 LEDs: 2 on the core board, 7 on the carrier board. On core board: 1 power indicator, 1 DONE configuration indicator. On carrier board: 1 power indicator, 4 user indicators, 2 serial port indicators.

- Key

5 keys: 1 reset key, 4 PL user keys.

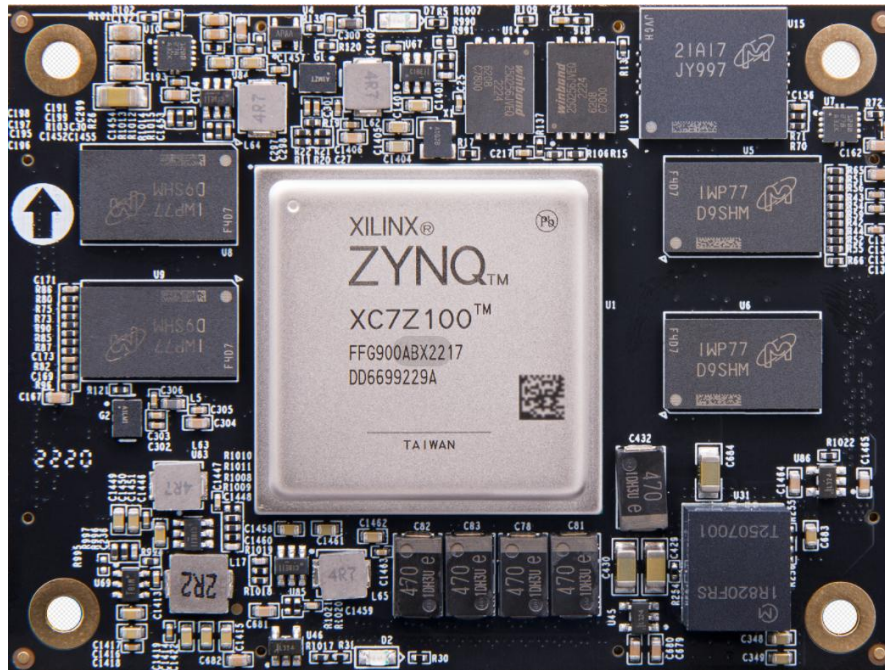
## 2. AC7Z100C Core Board

### 2.1 Introduction

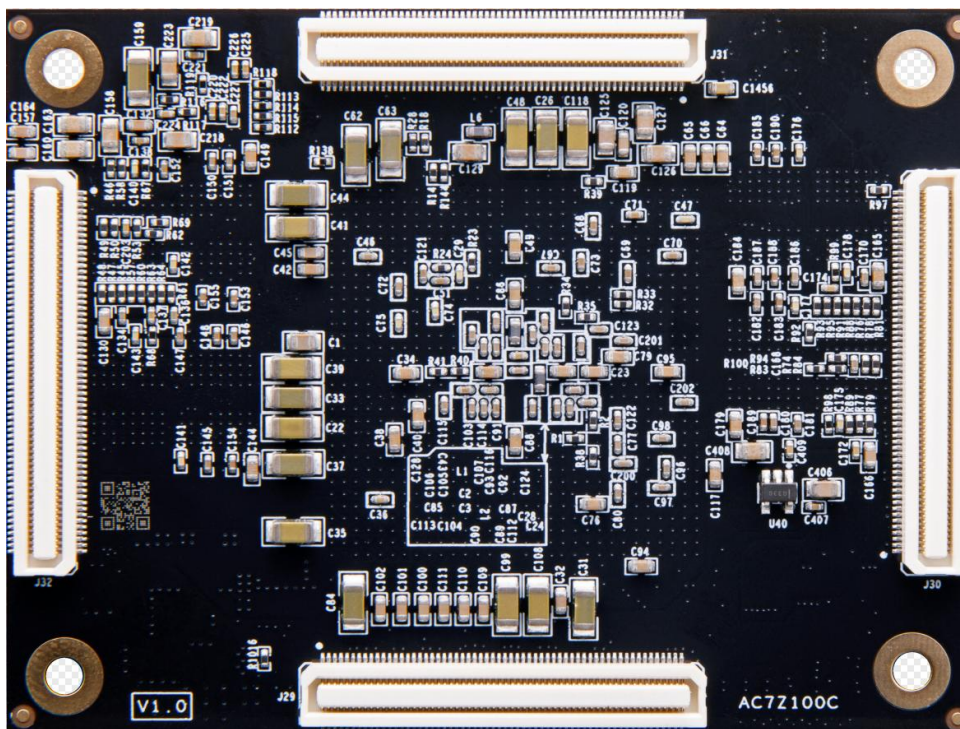
AC7Z100C (core board model, the same below) FPGA core board, ZYNQ chip is based on XC7Z100-2FFG900 of XILINX company ZYNQ7000 series. The ZYNQ chip's PS system integrates two ARM Cortex™-A9 processors, AMBA® interconnection, internal memory, external memory interfaces and peripherals. The FPGA of the ZYNQ chip contains a wealth of programmable logic cells, DSP and internal RAM.

The core board uses four Micron 512MB DDR3 chips MT41J256M16HA-125 for a total capacity of 2GB. Two DDR3s are mounted on the PS and PL sides, respectively, which form a 32-bit bus width. The DDR3 SDRAM on the PS side can run at up to 533MHz (data rate 1066Mbps), and the DDR3 SDRAM on the PL side can run at speeds up to 800MHz (data rate 1600Mbps). In addition, two 256MBit QSPI FLASH and 8GB eMMC FLASH chips are integrated on the core board to boot the storage configuration and system files.

In order to connect with the carrier board, the four board-to-board connectors of the core board extend the USB interface, the Gigabit Ethernet interface, the SD card interface and other remaining IO ports on the PS side; and also extend 16 pairs of high-speed transceiver GTX interfaces of the ZYNQ, and almost all IO ports (144 3.3V IOs and 48 1.8V IOs) on the PL side. The level of IO of BANK10, BANK11 and BANK12 can be modified by replacing the LDO chip on the core board to meet the requirements of different level interfaces of users. For users who need a lot of IOs, this core board will be a good choice. Moreover, as for the IO connection, lines between ZYNQ chip and interfaces are processed with equal length and differential length, and the core board size is only 80\*60 (mm), which is very suitable for secondary development.



AC7Z100C Front View



AC7Z100C Back View

## 2.2 ZYNQ Chip

The FPGA core board AC7Z100C uses Xilinx's Zynq7000 series chip, model XC7Z100-2FFG900. The chip's PS system integrates two ARM Cortex™-A9 processors, AMBA® interconnection, internal memory, external memory interfaces and



peripherals. These peripherals mainly include USB bus interface, Ethernet interface, SD/SDIO interface, I2C bus interface, CAN bus interface, UART interface, GPIO, etc. The PS can operate independently and start up under power-on or reset condition. Figure 2-2-1 shows the Overall Block Diagram of the ZYNQ7000 Chip.

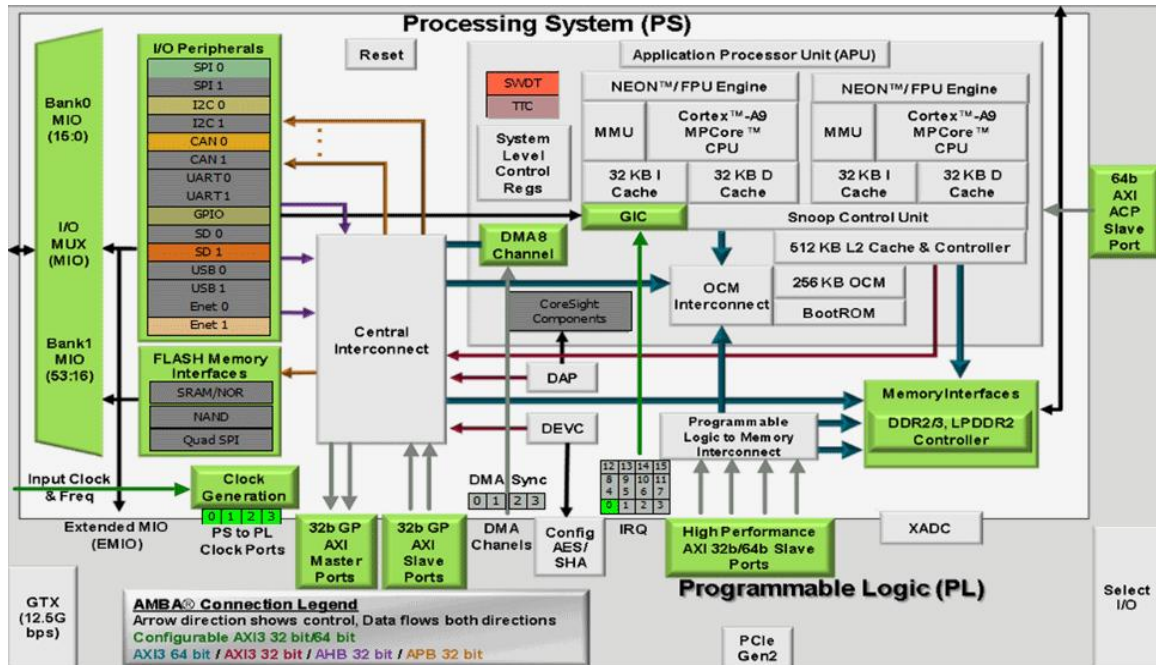


Figure 2-2-1: Overall Block Diagram of the ZYNQ7000 Chip

The main parameters of the PS system are as follows:

- ARM dual-core CortexA9-based application processor, ARM-v7 architecture, up to 800MHz
- 32KB level 1 instruction and data cache per CPU, 512KB level 2 cache shared by 2 CPUs
- On-chip boot ROM and 256KB on-chip RAM
- External storage interface, support 16/32 bit DDR2, DDR3 interface
- Two Gigabit NIC, support: divergence-aggregation DMA, GMII, RGMII, SGMII interface
- Two USB2.0 OTG interfaces, each supporting up to 12 nodes
- Two CAN2.0B bus interfaces
- Two SD cards, SDIO, MMC compatible controllers
- Two SPIs, two UARTs, two I2C interfaces
- 54 multi-function IOs that can be configured as normal IO or peripheral control interfaces
- High bandwidth connection within PS and PS to PL

The main parameters of the PL logic are as follows:

- Logic Cells: 444K;
- LUTs: 277400
- Flip-flops:554,800
- 18x25MACCs: 2020;
- Block RAM: 26.5Mb;
- 16-channel high-speed GTX transceivers, support PCIE Gen2x8;
- Two AD converters for on-chip voltage measurement, temperature sensing and up to 17 external differential input channels, 1MBPS

XC7Z100-2FFG900I chip' s speed grade is -2, industrial grade, package is FGG900, pin pitch is 1.0mm. The specific chip model definition of ZYNQ7000 series is shown in Figure 2-2-2:

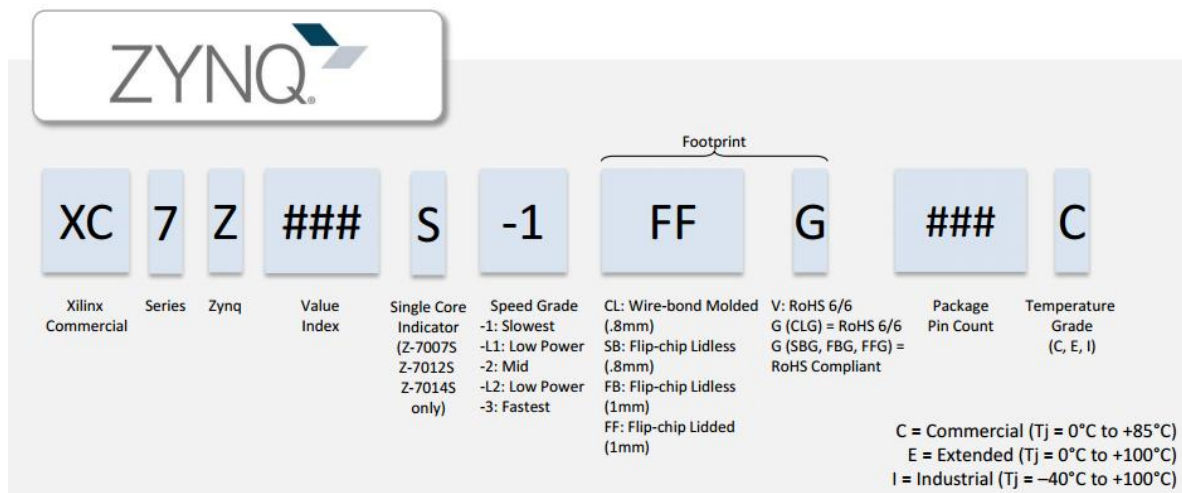


Figure 2-2-2: The Specific Chip Model Definition of ZYNQ7000 Series



Figure 2-2-3: XC7Z100 chip

## 2.3 DDR3 DRAM

The FPGA core board AC7Z100C is equipped with four Micron 512MB DDR3 chips, model MT41J256M16HA-125 (compatible with MT41K256M16HA-125), in which Two DDR3s are mounted on the PS and PL sides respectively. Two DDR3 SDRAMs comprise a 32bit bus width. The DDR3 SDRAM on the PS side can run at a maximum speed of 533MHz (data rate of 1066Mbps), and the two DDR3 memory systems are directly connected to the memory interface of the BANK 502 of the ZYNQ processing system (PS). The two DDR3 memory systems are directly connected to the memory interface of the BANK 502 of the ZYNQ processing system (PS). DDR3 SDRAM on the PL side can run up to 800MHz (data rate of 1600Mbps), and the two DDR3 storage systems are connected to BANK33 and BANK34 interface of the FPGA. The DDR3 SDRAM configuration is shown in Table 2-3-1 below.

Table 2-3-1: DDR3 SDRAM Configuration

Bit Number	Model	Capacity	Manufacturer
U4,U5,U7,U8	MT41J256M16HA-125	256M x 16bit	Micron

The hardware design of DDR3 requires strict consideration of signal integrity. We have fully considered the matching resistor/terminal resistance, line impedance control, and line length control in circuit design and PCB design to ensure high-speed and stable operation of DDR3.

The hardware connection of DDR3 DRAM on the PS side is shown in Figure 2-3-1:

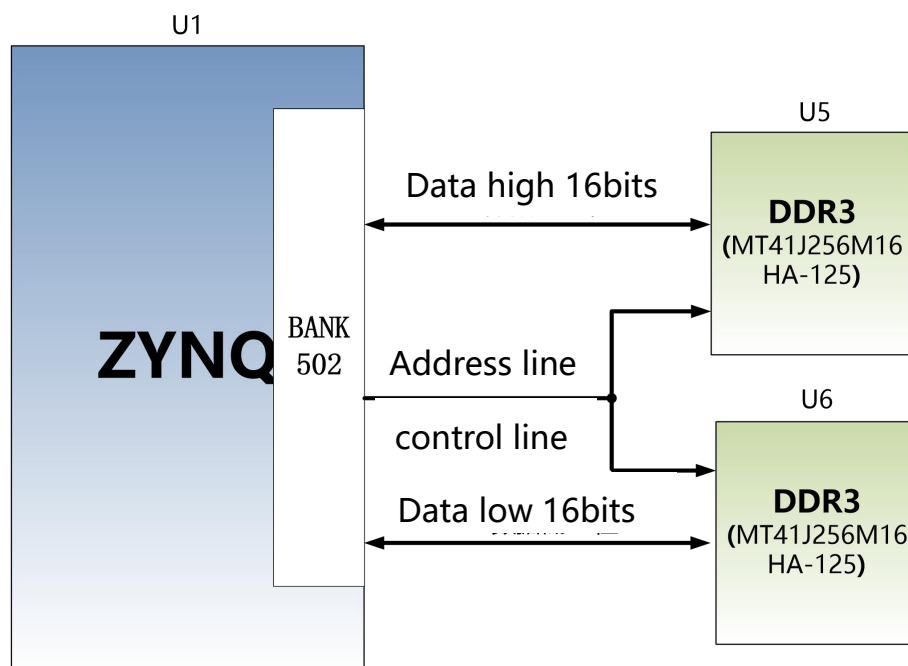


Figure 2-3-1: PS DDR3 DRAM schematic

The hardware connection of DDR3 DRAM on the PL side is shown in Figure 2-3-2:

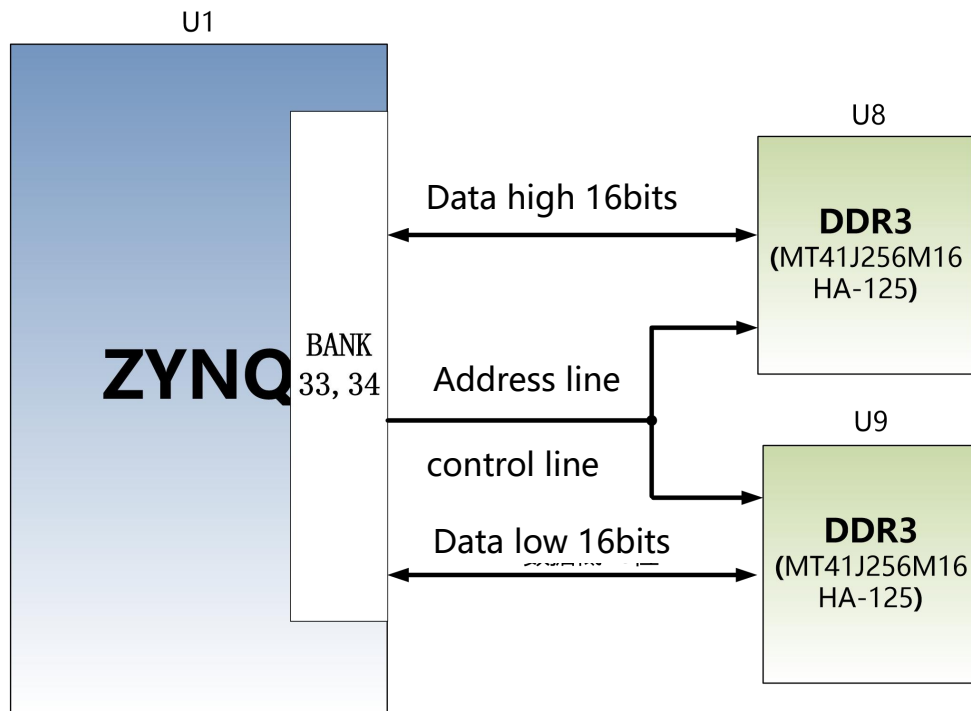


Figure 2-3-2: PL DDR3 DRAM schematic

**PS DDR3 DRAM pin assignment:**

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number
PS_DDR3_DQS0_P	PS_DDR_DQS_P0_502	C26
PS_DDR3_DQS0_N	PS_DDR_DQS_N0_502	B26
PS_DDR3_DQS1_P	PS_DDR_DQS_P1_502	C29
PS_DDR3_DQS1_N	PS_DDR_DQS_N1_502	B29
PS_DDR3_DQS2_P	PS_DDR_DQS_P2_502	G29
PS_DDR3_DQS2_N	PS_DDR_DQS_N2_502	F29
PS_DDR3_DQS3_P	PS_DDR_DQS_P3_502	L28
PS_DDR3_DQS4_N	PS_DDR_DQS_N3_502	L29
PS_DDR3_D0	PS_DDR_DQ0_502	A25
PS_DDR3_D1	PS_DDR_DQ1_502	E25
PS_DDR3_D2	PS_DDR_DQ2_502	B27
PS_DDR3_D3	PS_DDR_DQ3_502	D25
PS_DDR3_D4	PS_DDR_DQ4_502	B25
PS_DDR3_D5	PS_DDR_DQ5_502	E26
PS_DDR3_D6	PS_DDR_DQ6_502	D26

<b>PS_DDR3_D7</b>	<b>PS_DDR_DQ7_502</b>	<b>E27</b>
<b>PS_DDR3_D8</b>	<b>PS_DDR_DQ8_502</b>	<b>A29</b>
<b>PS_DDR3_D9</b>	<b>PS_DDR_DQ9_502</b>	<b>A27</b>
<b>PS_DDR3_D10</b>	<b>PS_DDR_DQ10_502</b>	<b>A30</b>
<b>PS_DDR3_D11</b>	<b>PS_DDR_DQ11_502</b>	<b>A28</b>
<b>PS_DDR3_D12</b>	<b>PS_DDR_DQ12_502</b>	<b>C28</b>
<b>PS_DDR3_D13</b>	<b>PS_DDR_DQ13_502</b>	<b>D30</b>
<b>PS_DDR3_D14</b>	<b>PS_DDR_DQ14_502</b>	<b>D28</b>
<b>PS_DDR3_D15</b>	<b>PS_DDR_DQ15_502</b>	<b>D29</b>
<b>PS_DDR3_D16</b>	<b>PS_DDR_DQ16_502</b>	<b>H27</b>
<b>PS_DDR3_D17</b>	<b>PS_DDR_DQ17_502</b>	<b>G27</b>
<b>PS_DDR3_D18</b>	<b>PS_DDR_DQ18_502</b>	<b>H28</b>
<b>PS_DDR3_D19</b>	<b>PS_DDR_DQ19_502</b>	<b>E28</b>
<b>PS_DDR3_D20</b>	<b>PS_DDR_DQ20_502</b>	<b>E30</b>
<b>PS_DDR3_D21</b>	<b>PS_DDR_DQ21_502</b>	<b>F28</b>
<b>PS_DDR3_D22</b>	<b>PS_DDR_DQ22_502</b>	<b>G30</b>
<b>PS_DDR3_D23</b>	<b>PS_DDR_DQ23_502</b>	<b>F30</b>
<b>PS_DDR3_D24</b>	<b>PS_DDR_DQ24_502</b>	<b>J29</b>
<b>PS_DDR3_D25</b>	<b>PS_DDR_DQ25_502</b>	<b>K27</b>
<b>PS_DDR3_D26</b>	<b>PS_DDR_DQ26_502</b>	<b>J30</b>
<b>PS_DDR3_D27</b>	<b>PS_DDR_DQ27_502</b>	<b>J28</b>
<b>PS_DDR3_D28</b>	<b>PS_DDR_DQ28_502</b>	<b>K30</b>
<b>PS_DDR3_D29</b>	<b>PS_DDR_DQ29_502</b>	<b>M29</b>
<b>PS_DDR3_D30</b>	<b>PS_DDR_DQ30_502</b>	<b>L30</b>
<b>PS_DDR3_D31</b>	<b>PS_DDR_DQ31_502</b>	<b>M30</b>
<b>PS_DDR3_DM0</b>	<b>PS_DDR_DM0_502</b>	<b>C27</b>
<b>PS_DDR3_DM1</b>	<b>PS_DDR_DM1_502</b>	<b>B30</b>
<b>PS_DDR3_DM2</b>	<b>PS_DDR_DM2_502</b>	<b>H29</b>
<b>PS_DDR3_DM3</b>	<b>PS_DDR_DM3_502</b>	<b>K28</b>
<b>PS_DDR3_A0</b>	<b>PS_DDR_A0_502</b>	<b>L25</b>
<b>PS_DDR3_A1</b>	<b>PS_DDR_A1_502</b>	<b>K26</b>
<b>PS_DDR3_A2</b>	<b>PS_DDR_A2_502</b>	<b>L27</b>

PS_DDR3_A3	PS_DDR_A3_502	G25
PS_DDR3_A4	PS_DDR_A4_502	J26
PS_DDR3_A5	PS_DDR_A5_502	G24
PS_DDR3_A6	PS_DDR_A6_502	H26
PS_DDR3_A7	PS_DDR_A7_502	K22
PS_DDR3_A8	PS_DDR_A8_502	F27
PS_DDR3_A9	PS_DDR_A9_502	J23
PS_DDR3_A10	PS_DDR_A10_502	G26
PS_DDR3_A11	PS_DDR_A11_502	H24
PS_DDR3_A12	PS_DDR_A12_502	K23
PS_DDR3_A13	PS_DDR_A13_502	H23
PS_DDR3_A14	PS_DDR_A14_502	J24
PS_DDR3_BA0	PS_DDR_BA0_502	M27
PS_DDR3_BA1	PS_DDR_BA1_502	M26
PS_DDR3_BA2	PS_DDR_BA2_502	M25
PS_DDR3_S0	PS_DDR_CS_B_502	N22
PS_DDR3_RAS	PS_DDR_RAS_B_502	N24
PS_DDR3_CAS	PS_DDR_CAS_B_502	M24
PS_DDR3_WE	PS_DDR_WE_B_502	N23
PS_DDR3_ODT	PS_DDR_ODT_502	L23
PS_DDR3_RESET	PS_DDR_DRST_B_502	F25
PS_DDR3_CLK0_P	PS_DDR_CKP_502	K25
PS_DDR3_CLK0_N	PS_DDR_CKN_502	J25
PS_DDR3_CKE	PS_DDR_CKE_502	M22

**PL DDR3 DRAM pin assignment:**

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number
PL_DDR3_DQS0_P	IO_L3P_T0_DQS_33	K3
PL_DDR3_DQS0_N	IO_L3N_T0_DQS_33	K2
PL_DDR3_DQS1_P	IO_L9P_T1_DQS_33	J1
PL_DDR3_DQS1_N	IO_L9N_T1_DQS_33	H1
PL_DDR3_DQS2_P	IO_L15P_T2_DQS_33	E6

PL_DDR3_DQS2_N	IO_L15N_T2_DQS_33	D5
PL_DDR3_DQS3_P	IO_L21P_T3_DQS_33	A5
PL_DDR3_DQS4_N	IO_L21N_T3_DQS_33	A4
PL_DDR3_D0	IO_L1N_T0_33	J3
PL_DDR3_D1	IO_L4N_T0_33	L2
PL_DDR3_D2	IO_L1P_T0_33	J4
PL_DDR3_D3	IO_L4P_T0_33	L3
PL_DDR3_D4	IO_L2N_T0_33	K1
PL_DDR3_D5	IO_L6P_T0_33	K6
PL_DDR3_D6	IO_L5N_T0_33	J5
PL_DDR3_D7	IO_L5P_T0_33	K5
PL_DDR3_D8	IO_L11P_T1_SRCC_33	H4
PL_DDR3_D9	IO_L10N_T1_33	G1
PL_DDR3_D10	IO_L8P_T1_33	H6
PL_DDR3_D11	IO_L7N_T1_33	F2
PL_DDR3_D12	IO_L10P_T1_33	H2
PL_DDR3_D13	IO_L12N_T1_MRCC_33	G4
PL_DDR3_D14	IO_L8N_T1_33	G6
PL_DDR3_D15	IO_L11N_T1_SRCC_33	H3
PL_DDR3_D16	IO_L18P_T2_33	E1
PL_DDR3_D17	IO_L17P_T2_33	E3
PL_DDR3_D18	IO_L16N_T2_33	D3
PL_DDR3_D19	IO_L14P_T2_SRCC_33	F4
PL_DDR3_D20	IO_L18N_T2_33	D1
PL_DDR3_D21	IO_L13N_T2_MRCC_33	E5
PL_DDR3_D22	IO_L16P_T2_33	D4
PL_DDR3_D23	IO_L17N_T2_33	E2
PL_DDR3_D24	IO_L22P_T3_33	C2
PL_DDR3_D25	IO_L24N_T3_33	A2
PL_DDR3_D26	IO_L20N_T3_33	B4
PL_DDR3_D27	IO_L20P_T3_33	B5
PL_DDR3_D28	IO_L22N_T3_33	C1

PL_DDR3_D29	IO_L24P_T3_33	A3
PL_DDR3_D30	IO_L19P_T3_33	C4
PL_DDR3_D31	IO_L23P_T3_33	B2
PL_DDR3_DM0	IO_L2P_T0_33	L1
PL_DDR3_DM1	IO_L12P_T1_MRCC_33	G5
PL_DDR3_DM2	IO_L14N_T2_SRCC_33	F3
PL_DDR3_DM3	IO_L23N_T3_33	B1
PL_DDR3_A0	IO_L18P_T2_34	H7
PL_DDR3_A1	IO_L21P_T3_DQS_34	L8
PL_DDR3_A2	IO_L7N_T1_34	H11
PL_DDR3_A3	IO_L10N_T1_34	D10
PL_DDR3_A4	IO_L15N_T2_DQS_34	H8
PL_DDR3_A5	IO_L8N_T1_34	D11
PL_DDR3_A6	IO_L19P_T3_34	L7
PL_DDR3_A7	IO_L10P_T1_34	E10
PL_DDR3_A8	IO_L23P_T3_34	L10
PL_DDR3_A9	IO_L9P_T1_DQS_34	H12
PL_DDR3_A10	IO_L18N_T2_34	G7
PL_DDR3_A11	IO_L20N_T3_34	J9
PL_DDR3_A12	IO_L13P_T2_MRCC_34	H9
PL_DDR3_A13	IO_L7P_T1_34	J11
PL_DDR3_A14	IO_L22N_T3_34	K10
PL_DDR3_BA0	IO_L22P_T3_34	K11
PL_DDR3_BA1	IO_L21N_T3_DQS_34	K8
PL_DDR3_BA2	IO_L9N_T1_DQS_34	G11
PL_DDR3_S0	IO_L16P_T2_34	F8
PL_DDR3_RAS	IO_L13N_T2_MRCC_34	G9
PL_DDR3_CAS	IO_L17P_T2_34	E7
PL_DDR3_WE	IO_L16N_T2_34	F7
PL_DDR3_ODT	IO_L20P_T3_34	J10
PL_DDR3_RESET	IO_L8P_T1_34	E11
PL_DDR3_CLK0_P	IO_L12P_T1_MRCC_34	D9



PL_DDR3_CLK0_N	IO_L12N_T1_MRCC_34	D8
PL_DDR3_CKE	IO_L17N_T2_34	D6

## 2.4 QSPI Flash

The FPGA core board AC7Z100C is equipped with two 256MBit Quad-SPI FLASH chips to form an 8-bit bandwidth data bus, the flash model is W25Q256FVEI, which uses the 3.3V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, it can be used as a boot device for the system to store the boot images, mainly including FPGA bit files, ARM application code, and other user data files. The specific models and related parameters of QSPI FLASH are shown in Table 2-4-1.

Bit Number	Model	Capacity	Manufacturer
U13,U14	W25Q256FVEI	256M bit	Winbond

Table 2-4-1: QSPI Flash model and parameter

The QSPI FLASH is connected to the GPIO port of PS BANK500 of the ZYNQ chip. In the system design, the function of GPIO ports need to be configured as QSPI FLASH interfaces. Figure 2-4-1 shows the QSPI Flash in the schematic diagram.

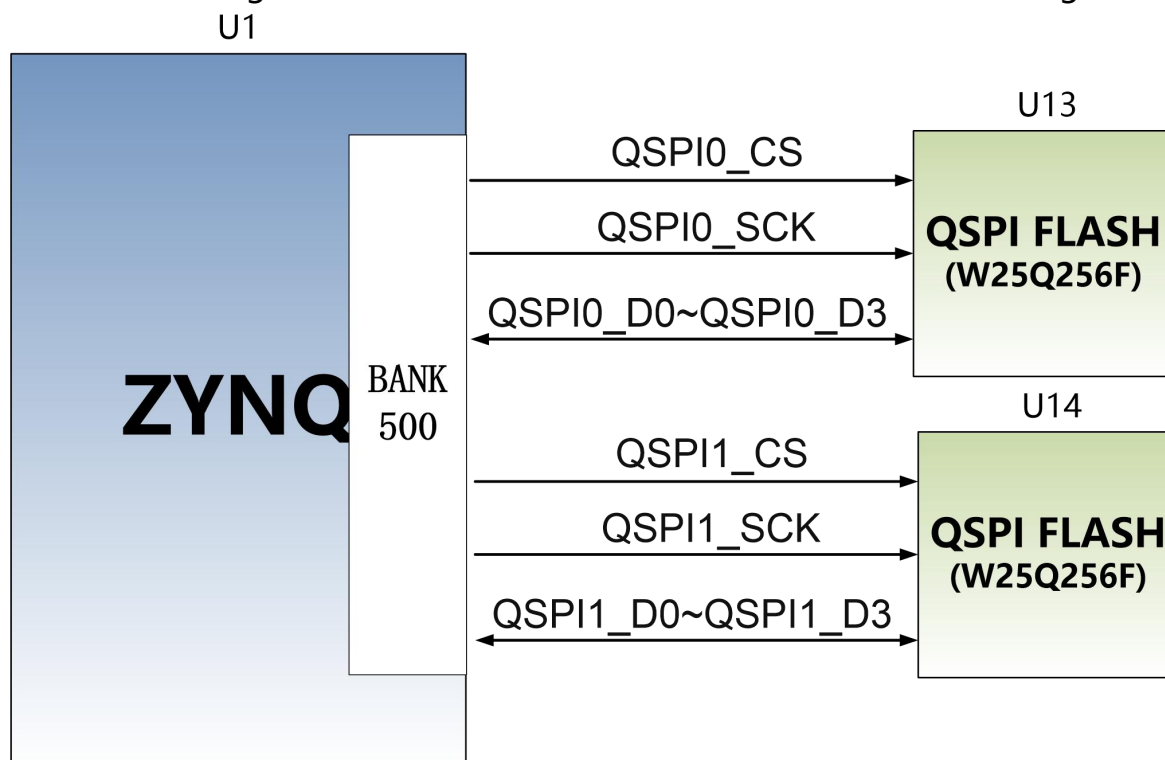


Figure 2-4-1 QSPI Flash connection diagram

**Configuration Chip Pin Assignment:**

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number
QSPIO_SCK	PS_MIO6_500	D24
QSPIO_CS	PS_MIO1_500	D23
QSPIO_D0	PS_MIO2_500	F23
QSPIO_D1	PS_MIO3_500	C23
QSPIO_D2	PS_MIO4_500	E23
QSPIO_D3	PS_MIO5_500	C24
QSPI1_SCK	PS_MIO9_500	A24
QSPI1_CS	PS_MIO0_500	F24
QSPI1_D0	PS_MIO10_500	E22
QSPI1_D1	PS_MIO11_500	A23
QSPI1_D2	PS_MIO12_500	E21
QSPI1_D3	PS_MIO13_500	F22

## 2.5 eMMC Flash

The FPGA core board AC7Z100C is equipped with a large-capacity 8GB eMMC FLASH chip, model THGBMFG6C1LBAIL, which supports the JEDEC e-MMC V5.0 standard HS-MMC interface with level support of 1.8V or 3.3V. The data width of the eMMC FLASH and ZYNQ connections is 4 bits. Due to the large capacity and non-volatile nature of eMMC FLASH, it can be used as a large-capacity storage device for the ZYNQ system, such as ARM applications, system files and other user data files. Table 2-5-1 lists the eMMC FLASH models and related parameters.

Bit Number	Model	Capacity	Manufacturer
U15	THGBMFG6C1LBAIL	8G Byte	TOSHIBA

Table 2-5-1: eMMC Flash model and parameter

eMMC FLASH is connected to the GPIO port of PS BANK501 of the ZYNQ chip. In the system design, the functions of PS GPIO ports need to be configured as the SD interfaces. Figure 2-5-1 shows the eMMC Flash in the schematic.

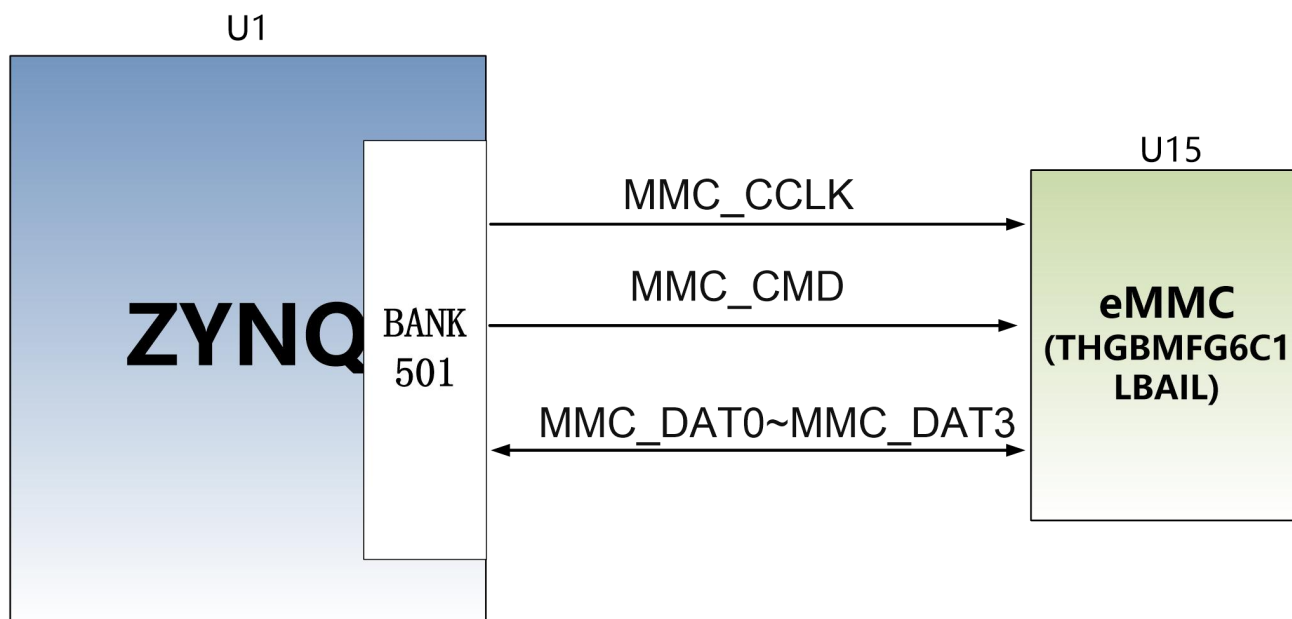


Figure 2-5-1 eMMC Flash connection diagram

**Configuration Chip Pin Assignment:**

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number
MMC_CCLK	PS_MIO48_501	C19
MMC_CMD	PS_MIO47_501	A18
MMC_D0	PS_MIO46_501	F20
MMC_D1	PS_MIO49_501	D18
MMC_D2	PS_MIO50_501	A19
MMC_D3	PS_MIO51_501	F19

**2.6 Clock Configuration**

The core system provides a reference clock for the PS system, the PL logic, and the GTX transceiver respectively, allowing the PS system and PL logic to work independently. The schematic diagram of the clock circuit design is shown in Figure 2.6-1:

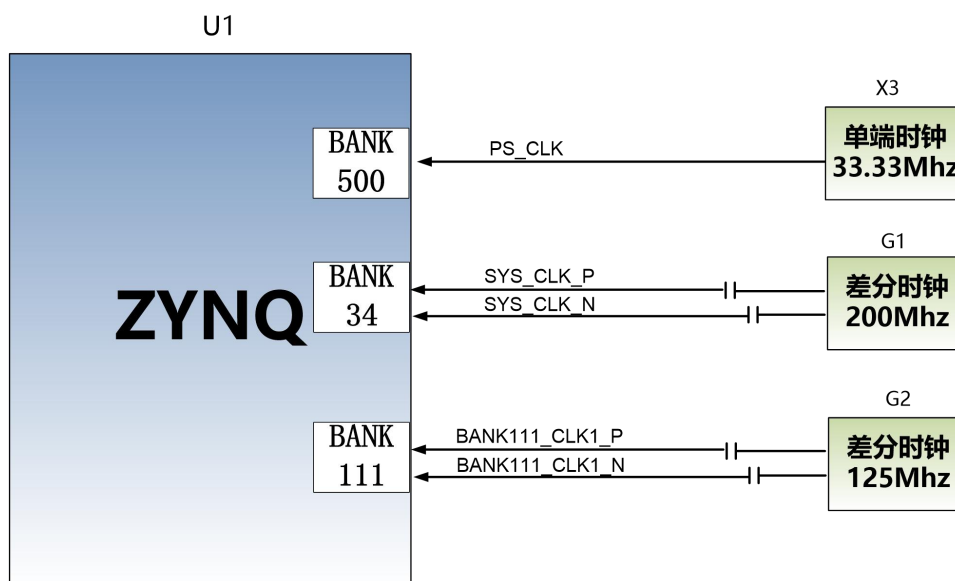


Figure 2-6-1: core board clock source

### PS system clock source

The ZYNQ chip provides a 33.333MHz clock input to the PS via the X4 crystal on the FPGA core board AC7Z100C. The input of the clock is connected to the pin of the PS\_CLK\_500 of the BANK500 of the ZYNQ chip. The schematic diagram is shown in Figure 2.6-2:

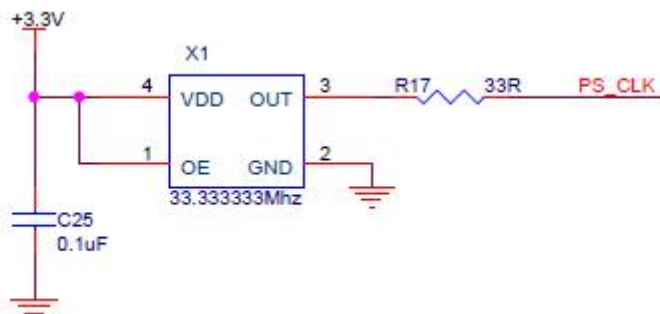


Figure 2-6-2: PS Active crystal oscillator

### PS Clock Pin Assignment:

Signal Name	ZYNQ Pin
PS_CLK	A22

### PL system clock source

The differential 200MHz PL system clock source is provided on the FPGA core board AC7Z100C for the reference clock of the DDR3 controller. The crystal output is connected to the global clock (MRCC) of the FPGA BANK34, which can be used to

drive the DDR3 controller and user logic in the FPGA. The schematic diagram of the clock source is shown in Figure 2-6-3:

**SYSTEM CLOCK**

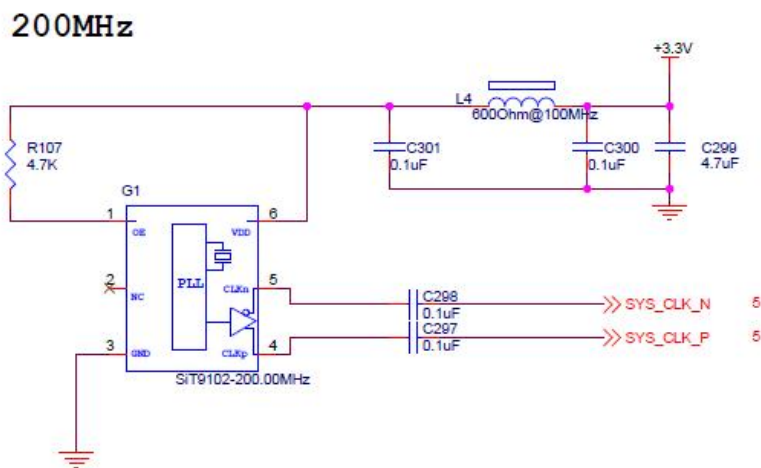


Figure 2-6-3: PL system clock source

**PL Clock Pin Assignment:**

Signal Name	ZYNQ Pin
SYS_CLK_P	F9
SYS_CLK_N	E8

**GTX reference clock**

The FPGA core board AC7Z100C provides a 125Mhz reference clock for the GTX transceiver. The reference clock is connected to the reference clock input REFCLK1P/REFCLK1N of the BANK110. The schematic diagram of the clock source is shown in Figure 2-6-4:

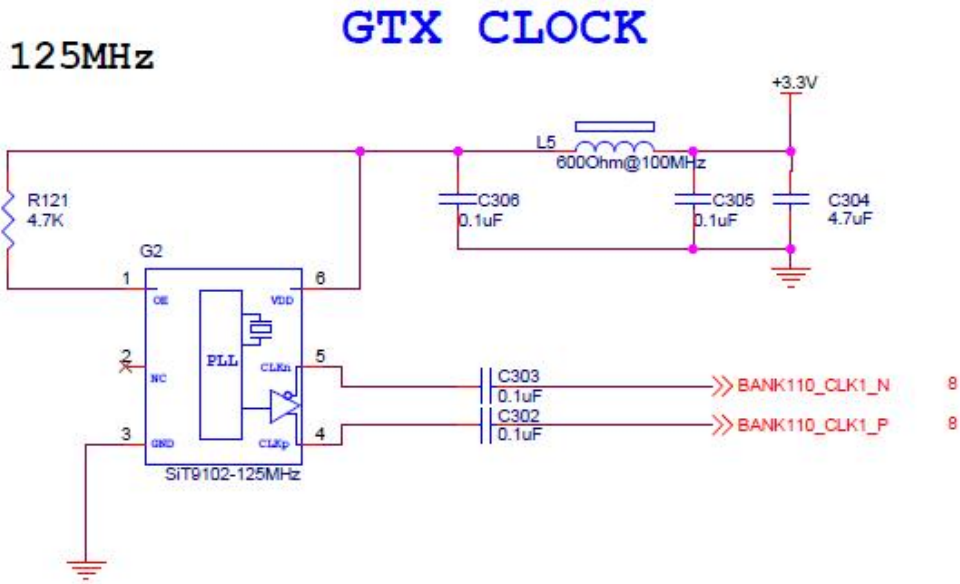


Figure 2-6-4: GTX clock source

Figure 2-6-5 shows the GTX clock source on the board:

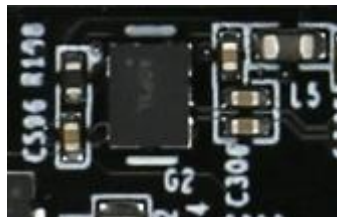


Figure 2-6-5: GTX clock source

**GTX clock source ZYNQ pin assignment:**

Signal Name	ZYNQ Pin
BANK110_CLK1_P	AC8
BANK110_CLK1_N	AC7

**2.7 LED Light**

There are 2 red LED lights on the AC7Z100C FPGA core board, one of which is the power indicator light (PWR), one is the configuration LED light (DONE). When the core board is powered, the power indicator will light up; when the FPGA is configured, the configuration LED will light up. The schematic diagram of the LED light hardware connection is shown in Figure 2.7-1:

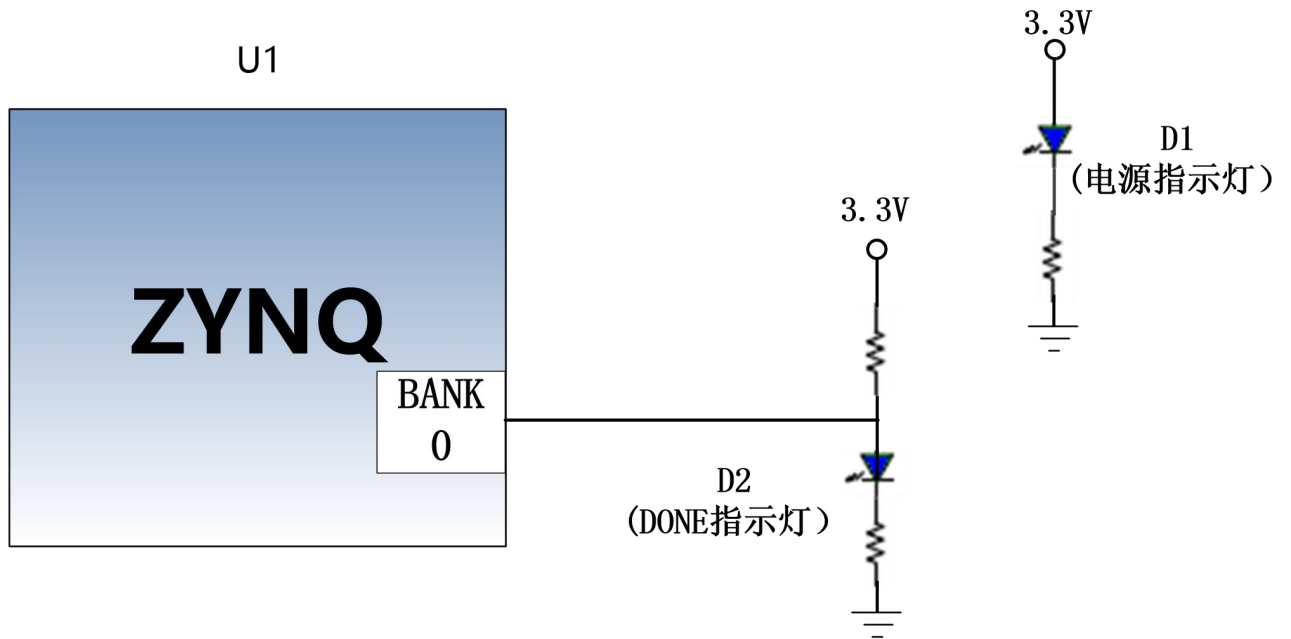


Figure 2-7-1: LED light hardware connection

## 2.8 Reset Key

There is a reset circuit on the AC7Z100C core board. The reset input signal is connected to the reset key on the carrier board. The reset output is connected to the PS reset pin of the ZYNQ chip. Users can use this carrier board key to reset the ZYNQ system. The schematic diagram of the reset connection is shown in Figure 2.8-1:

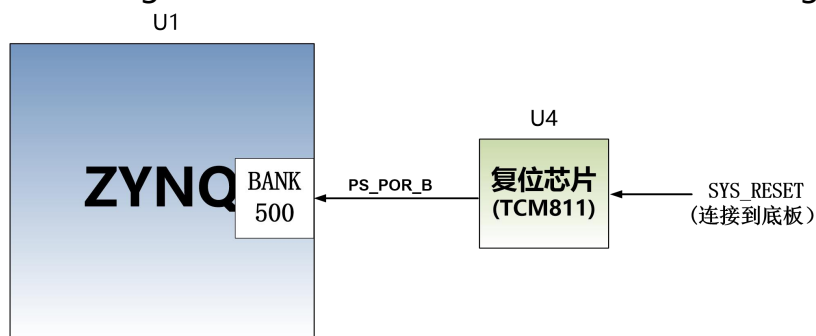


Figure 2-8-1: Reset connection diagram

### Reset key ZYNQ pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
PS_POR_B	PS_POR_B_500	D21	ZYNQ system reset signal

## 2.9 Power Supply

The AC7Z100C FPGA core board is powered by DC5V and is powered by connecting the carrier board. The power supply design diagram on the FPGA board is shown in Figure 2.9-1:

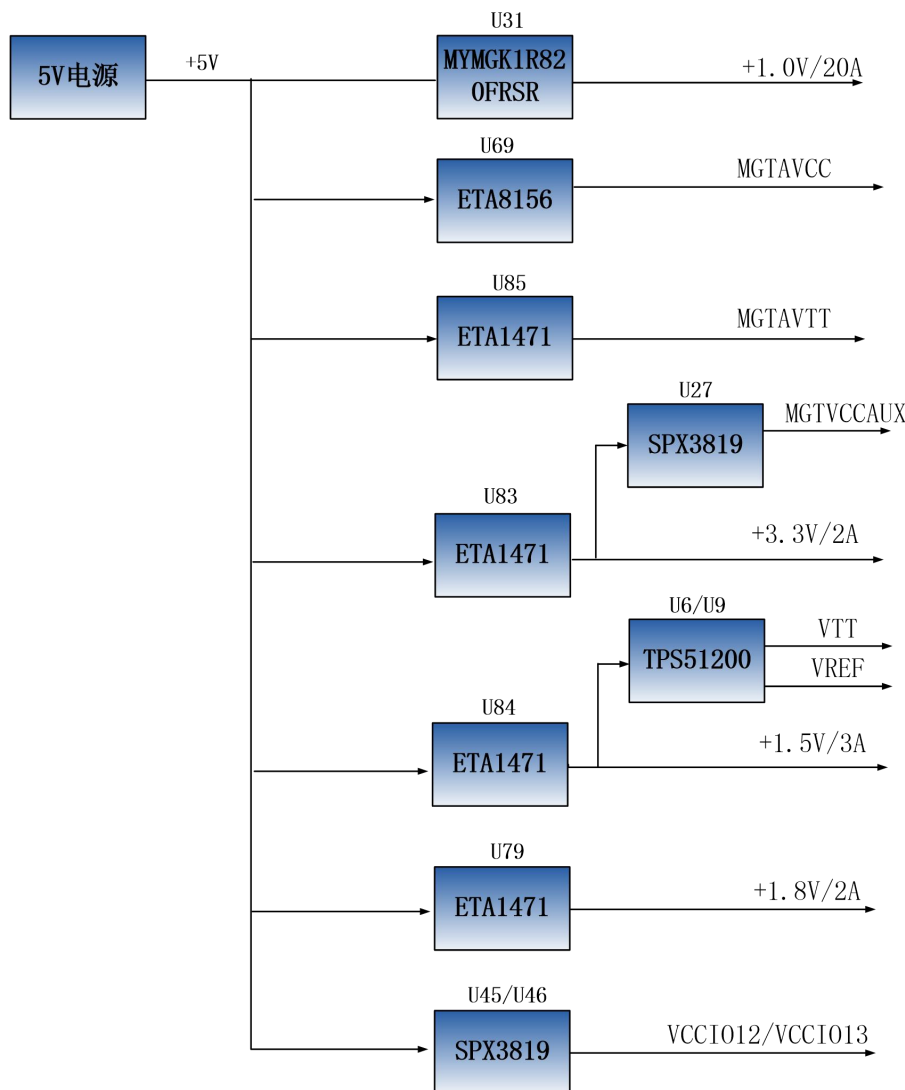


Figure 2-9-1: Power interface in the schematic

+5V generates +1.0V ZYNQ core power through DCDC power chip MYMGK1R820FRSR. +1.0V output current is up to 20A, which is enough to meet the current demand of ZYNQ core voltage. The +5V power supply then uses the DCDC chip ETA1471 to generate four power supplies: MGTAVTT, +1.5V, +3.3V, +1.5V. The power supply MGTAVTT is generated by DCDC chip ETA8156, and +3.3V generates the +1.8V auxiliary power supply of GTX through an LDO chip SPX3819-1-8. The VTT and VREF voltages of the DDR3 of the PS and the PL are generated by TPS51200. In addition, the IO power supply of BANK12 and BANK13 are generated by two-channel



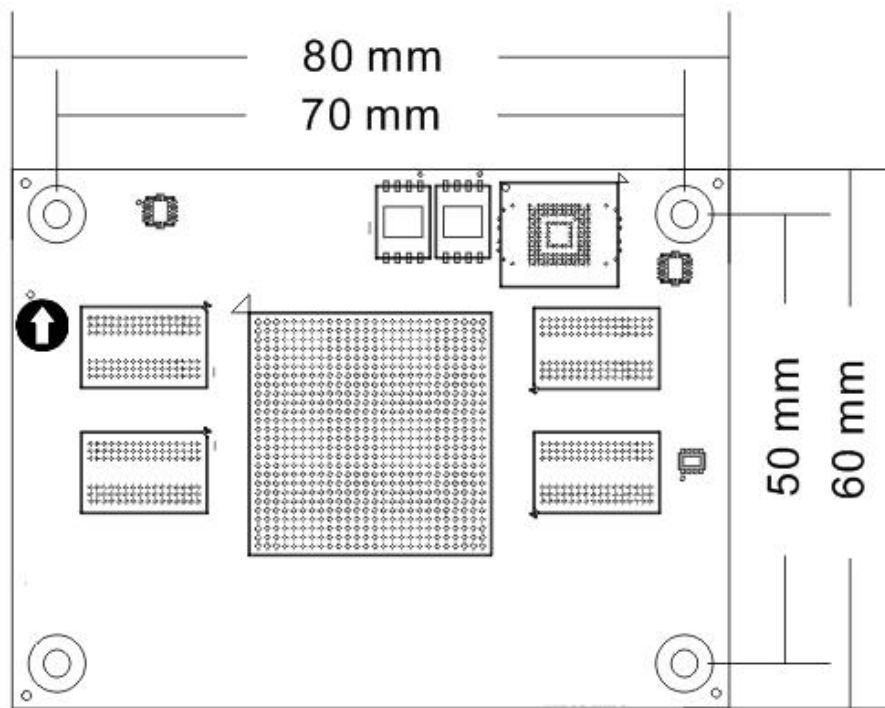
SPX3819M5-3-3. Users can change the IO input and output of these two BANKs to other voltage standards by replacing the LDO chip.

The functions of each power distribution are shown in the following table:

Power Supply	Function
+1.0V	kernel voltage of ZYNQ PS and PL
+1.8V	auxiliary voltage of ZYNQ PS and PL, BANK501, BANK35, eMMC
+3.3V	ZYNQ Bank0,Bank500, QSIP FLASH, Clock crystal oscillator
+1.5V	DDR3, ZYNQ Bank502, Bank33,Bank34
VCCIO12	ZYNQ Bank12
VCCIO13	ZYNQ Bank13
VREF, VTT (+0.75V)	PS DDR3, PL DDR3
MGTAVCC(+1.0V)	ZYNQ Bank111, Bank112
MGTAVTT(+1.2V)	ZYNQ Bank111, Bank112
MGTVCCAUX (+1.8V)	ZYNQ Bank111, Bank112

Because the power supply of the ZYNQ FPGA has the power-on sequence requirements, in the circuit design, we have designed according to the power requirements of the chip. The power-on sequence is +1.0V->+1.8V->(+1.5 V, +3.3V, VCCIO12,VCCIO13) circuit design to ensure the normal operation of the chip.

## 2.10 Size Dimension



Top View

## 2.11 Board to Board Connectors Pin Assignment

The core board is extended to a total of four high-speed expansion ports, using four 120Pin board-to-board connectors (J29~J32) to connecting the core board with the carrier board. Connectors use Panasonic AXK5A2137YG, and corresponded connectors on the carrier board are AXK6A2337YG. J29 connects to IO of BANK10 and BANK11; J30 connects to GTX's transceiver signal; J31 connects JTAG and BANK35's IO (1.8V level standard); J32 connects to PS's MIO, IO of BANK11 and BANK12, and +5V power supply.

J29 pin assignment:

J29 Pin	Signal Name	ZYNQ Pin Number	J29 Pin	Signal Name	ZYNQ Pin Number
1	B11_L4_N	AJ24	2	B11_L1_N	AK25
3	B11_L4_P	AJ23	4	B11_L1_P	AJ25
5	GND	-	6	GND	-
7	B11_L3_P	AJ21	8	B11_L8_N	AG25

9	B11_L3_N	AK21	10	B11_L8_P	AG24
11	GND	-	12	GND	-
13	B11_L2_N	AK23	14	B11_L12_N	AF22
15	B11_L2_P	AK22	16	B11_L12_P	AE22
17	GND	-	18	GND	-
19	B11_L5_N	AH24	20	B11_L16_N	AK18
21	B11_L5_P	AH23	22	B11_L16_P	AK17
23	GND	-	24	GND	-
25	B11_L15_P	AJ20	26	B11_L6_N	AH22
27	B11_L15_N	AK20	28	B11_L6_P	AG22
29	GND	-	30	GND	-
31	B11_L13_N	AH21	32	B11_L17_N	AJ19
33	B11_L13_P	AG21	34	B11_L17_P	AH19
35	GND	-	36	GND	-
37	B11_L14_N	AG20	38	B11_L18_N	AG19
39	B11_L14_P	AF20	40	B11_L18_P	AF19
41	GND	-	42	GND	-
43	B11_L19_P	AB21	44	B11_L20_N	Y21
45	B11_L19_N	AB22	46	B11_L20_P	W21
47	GND	-	48	GND	-
49	B10_L13_P	AG17	50	B10_L17_P	AE18
51	B10_L13_N	AG16	52	B10_L17_N	AE17
53	GND	-	54	GND	-
55	B10_L2_P	AH18	56	B10_L15_P	AF18
57	B10_L2_N	AJ18	58	B10_L15_N	AF17
59	GND	-	60	GND	-
61	B10_L4_P	AJ16	62	B10_L6_P	AH17
63	B10_L4_N	AK16	64	B10_L6_N	AH16
65	GND	-	66	GND	-
67	B10_L16_P	AE16	68	B10_L24_N	AB16
69	B10_L16_N	AE15	70	B10_L24_P	AB17
71	GND	-	72	GND	-

73	B10_L20_P	AA15	74	B10_L5_N	AK15
75	B10_L20_N	AA14	76	B10_L5_P	AJ15
77	GND	-	78	GND	-
79	B10_L18_P	AD16	80	B10_L23_P	AC17
81	B10_L18_N	AD15	82	B10_L23_N	AC16
83	GND	-	84	GND	-
85	B10_L14_N	AG15	86	B10_L12_P	AF14
87	B10_L14_P	AF15	88	B10_L12_N	AG14
89	GND	-	90	GND	-
91	B10_L1_P	AK13	92	B10_L22_P	AB15
93	B10_L1_N	AK12	94	B10_L22_N	AB14
95	GND	-	96	GND	-
97	B10_L8_P	AH14	98	B10_L3_P	AJ14
99	B10_L8_N	AH13	100	B10_L3_N	AJ13
101	GND	-	102	GND	-
103	B10_L10_N	AH12	104	B10_L11_N	AF13
105	B10_L10_P	AG12	106	B10_L11_P	AE13
107	GND	-	108	GND	-
109	B10_L7_N	AF12	110	B10_L9_P	AD14
111	B10_L7_P	AE12	112	B10_L9_N	AD13
113	GND	-	114	GND	-
115	B10_L19_P	AC14	116	B10_L21_N	AC12
117	B10_L19_N	AC13	118	B10_L21_P	AB12
119	GND	-	120	GND	-

**J30 pin assignment:**

J30 Pin	Signal Name	ZYNQ Pin Number	J30 Pin	Signal Name	ZYNQ Pin Number
1	BANK111_TX0_N	AB1	2	BANK111_RX0_N	AC3
3	BANK111_TX0_P	AB2	4	BANK111_RX0_P	AC4
5	GND	-	6	GND	-
7	BANK111_TX1_N	Y1	8	BANK111_RX1_N	AB5

9	BANK111_TX1_P	Y2	10	BANK111_RX1_P	AB6
11	GND	-	12	GND	-
13	BANK111_TX2_N	W3	14	BANK111_RX2_N	Y5
15	BANK111_TX2_P	W4	16	BANK111_RX2_P	Y6
17	GND	-	18	GND	-
19	BANK111_TX3_N	V1	20	BANK111_RX3_N	AA3
21	BANK111_TX3_P	V2	22	BANK111_RX3_P	AA4
23	GND	-	24	GND	-
25	BANK111_CLK0_N	U7	26	BANK111_CLK1_N	W7
27	BANK111_CLK0_P	U8	28	BANK111_CLK1_P	W8
29	GND	-	30	GND	-
31	BANK112_TX0_N	T1	32	BANK112_RX0_N	V5
33	BANK112_TX0_P	T2	34	BANK112_RX0_P	V6
35	GND	-	36	GND	-
37	BANK112_TX1_N	R3	38	BANK112_RX1_N	U3
39	BANK112_TX1_P	R4	40	BANK112_RX1_P	U4
41	GND	-	42	GND	-
43	BANK112_TX2_N	P1	44	BANK112_RX2_N	T5
45	BANK112_TX2_P	P2	46	BANK112_RX2_P	T6
47	GND	-	48	GND	-
49	BANK112_TX3_N	N3	50	BANK112_RX3_N	P5
51	BANK112_TX3_P	N4	52	BANK112_RX3_P	P6
53	GND	-	54	GND	-
55	BANK112_CLK0_N	N7	56	BANK112_CLK1_N	R7
57	BANK112_CLK0_P	N8	58	BANK112_CLK1_P	R8
59	GND	-	60	GND	-
61	BANK109_RX2_N	AG7	62	BANK110_RX0_N	AH5
63	BANK109_RX2_P	AG8	64	BANK110_RX0_P	AH6
65	GND	-	66	GND	-
67	BANK109_RX3_N	AE7	68	BANK110_TX0_N	AH1
69	BANK109_RX3_P	AE8	70	BANK110_TX0_P	AH2
71	GND	-	72	GND	-

73	BANK109_RX1_P	AJ8	74	BANK110_RX1_N	AG3
75	BANK109_RX1_N	AJ7	76	BANK110_RX1_P	AG4
77	GND	-	78	GND	-
79	BANK109_TX1_P	AK6	80	BANK110_TX1_N	AF1
81	BANK109_TX1_N	AK5	82	BANK110_TX1_P	AF2
83	GND	-	84	GND	-
85	BANK109_TX2_P	AJ4	86	BANK110_RX2_N	AF5
87	BANK109_TX2_N	AJ3	88	BANK110_RX2_P	AF6
89	GND	-	90	GND	-
91	BANK109_TX3_P	AK2	92	BANK110_TX2_N	AE3
93	BANK109_TX3_N	AK1	94	BANK110_TX2_P	AE4
95	GND	AA12	96	GND	-
97	BANK109_TX0_N	AK9	98	BANK110_RX3_N	AD5
99	BANK109_TX0_P	AK10	100	BANK110_RX3_P	AD6
101	GND	-	102	GND	-
103	BANK109_RX0_N	AH9	104	BANK110_TX3_N	AD1
105	BANK109_RX0_P	AH10	106	BANK110_TX3_P	AD2
107	GND	-	108	GND	-
109	BANK109_CLK0_N	AD9	110	BANK110_CLK0_N	AA7
111	BANK109_CLK0_P	AD10	112	BANK110_CLK0_P	AA8
113	GND	-	114	GND	-
115			116		
117			118		
119	GND	AA12	120	GND	AA12

**J31 pin assignment:**

J31 Pin	Signal Name	ZYNQ Pin Number	J31 Pin	Signal Name	ZYNQ Pin Number
1	FPGA_TCK	Y12	2	FPGA_TDI	P10
3	FPGA_TMS	V10	4	FPGA_TDO	Y10
5	GND	-	6	GND	-
7	B35_L2_P	J13	8	B35_L8_N	G14

9	B35_L2_N	H13	10	B35_L8_P	G15
11	GND	-	12	GND	-
13	B35_L9_P	G12	14	B35_L3_N	K13
15	B35_L9_N	F12	16	B35_L3_P	L13
17	GND	-	18	GND	-
19	B35_L22_N	B11	20	B35_L5_P	K15
21	B35_L22_P	C11	22	B35_L5_N	J15
23	GND	-	24	GND	-
25	B35_L20_N	B12	26	B35_L10_P	F13
27	B35_L20_P	C12	28	B35_L10_N	E12
29	GND	-	30	GND	AA12
31	B35_L19_N	C13	32	B35_L12_N	F14
33	B35_L19_P	C14	34	B35_L12_P	F15
35	GND	-	36	GND	-
37	B35_L24_N	A12	38	B35_L11_N	D13
39	B35_L24_P	A13	40	B35_L11_P	E13
41	GND	-	42	GND	-
43	B35_L4_N	H14	44	B35_L23_P	B14
45	B35_L4_P	J14	46	B35_L23_N	A14
47	GND	-	48	GND	-
49	B35_L1_N	L14	50	B35_L21_P	B15
51	B35_L1_P	L15	52	B35_L21_N	A15
53	GND	-	54	GND	-
55	B35_L16_N	C16	56	B35_L14_P	D15
57	B35_L16_P	D16	58	B35_L14_N	D14
59	GND	-	60	GND	-
61	B35_L18_N	A17	62	B35_L13_N	E15
63	B35_L18_P	B17	64	B35_L13_P	E16
65	GND	-	66	GND	-
67	B35_L15_N	E17	68	B35_L17_N	B16
69	B35_L15_P	F17	70	B35_L17_P	C17
71	GND	-	72	GND	-

73	B35_L7_N	G16	74	B12_L17_N	AG27
75	B35_L7_P	G17	76	B12_L17_P	AG26
77	GND	-	78	GND	-
79	B35_L6_N	H16	80	B12_L18_N	AF25
81	B35_L6_P	J16	82	B12_L18_P	AE25
83	GND	-	84	GND	-
85	B12_L6_N	AB26	86	B12_L10_N	AE26
87	B12_L6_P	AB25	88	B12_L10_P	AD25
89	GND	-	90	GND	-
91	B12_L11_N	AC27	92	B12_L13_N	AF28
93	B12_L11_P	AB27	94	B12_L13_P	AE28
95	GND	-	96	GND	-
97	B12_L12_N	AD28	98	B12_L16_N	AG30
99	B12_L12_P	AC28	100	B12_L16_P	AF30
101	GND	-	102	GND	-
103	B12_L9_N	AD29	104	B12_L22_N	AK28
105	B12_L9_P	AC29	106	B12_L22_P	AK27
107	GND	-	108	GND	-
109	B12_L14_N	AF27	110	B12_L20_N	AK30
111	B12_L14_P	AE27	112	B12_L20_P	AJ30
113	GND	-	114	GND	-
115	PS_POR_B		116	B12_L23_N	AH27
117	SYS_RESET	-	118	B12_L23_P	AH26
119	GND	-	120	GND	-

**J32 pin assignment:**

J32 Pin	Signal Name	ZYNQ Pin Number	J32 Pin	Signal Name	ZYNQ Pin Number
1	PS_MIO5	C24	2	PS_MIO17	K21
3	PS_MIO4	E23	4	PS_MIO18	K20
5	GND	-	6	GND	-
7	PS_MIO14	B22	8	PS_MIO19	J20



9	PS_MIO15	C22	10	PS_MIO20	M20
11	GND	-	12	GND	-
13	PS_MIO52	D19	14	PS_MIO16	L19
15	PS_MIO53	C18	16	PS_MIO21	J19
17	GND	-	18	GND	-
19	PS_MIO7	B24	20	PS_MIO26	M17
21			22	PS_MIO25	G19
23	GND	-	24	GND	-
25	PS_MIO40	B20	26	PS_MIO24	M19
27	PS_MIO41	J18	28	PS_MIO23	J21
29	GND	-	30	GND	-
31	PS_MIO42	D20	32	PS_MIO27	G20
33	PS_MIO43	E18	34	PS_MIO22	L20
35	GND	-	36	GND	-
37	PS_MIO44	E20	38	PS_MIO30	L18
39	PS_MIO45	H18	40	PS_MIO29	H22
41	GND	-	42	GND	-
43	B12_L2_N	AB30	44	PS_MIO36	H17
45	B12_L2_P	AB29	46	PS_MIO31	H21
47	GND	-	48	GND	-
49	B12_L4_N	AA29	50	PS_MIO32	K17
51	B12_L4_P	Y28	52	PS_MIO33	G22
53	GND	-	54	GND	-
55	B12_L19_P	AH28	56	PS_MIO34	K18
57	B12_L19_N	AH29	58	PS_MIO35	G21
59	GND	-	60	GND	-
61	B12_L3_P	Y26	62	PS_MIO28	L17
63	B12_L3_N	Y27	64	PS_MIO37	B21
65	GND	-	66	GND	-
67	B12_L5_P	AA27	68	PS_MIO38	A20
69	B12_L5_N	AA28	70	PS_MIO39	F18
71	GND	-	72	GND	-

73	B12_L8_N	AE30	74	B12_L21_P	AJ28
75	B12_L8_P	AD30	76	B12_L21_N	AJ29
77	GND	-	78	GND	-
79	B12_L15_N	AG29	80	B12_L7_N	AD26
81	B12_L15_P	AF29	82	B12_L7_P	AC26
83	GND	-	84	GND	-
85	B11_L23_N	AA23	86	B11_L11_P	AD23
87	B11_L23_P	AA22	88	B11_L11_N	AE23
89	GND	-	90	GND	-
91	B11_L21_N	Y23	92	B11_L9_P	AF23
93	B11_L21_P	Y22	94	B11_L9_N	AF24
95	GND	-	96	GND	-
97	B11_L22_N	AB24	98	B11_L10_N	AE21
99	B11_L22_P	AA24	100	B11_L10_P	AD21
101	GND	-	102	GND	-
103	B11_L7_P	AC24	104	B11_L24_P	AC22
105	B11_L7_N	AD24	106	B11_L24_N	AC23
107	+5V	-	108	+5V	-
109	+5V	-	110	+5V	-
111	+5V	-	112	+5V	-
113	+5V	-	114	+5V	-
115	+5V	-	116	+5V	-
117	+5V	-	118	+5V	-
119	+5V	-	120	+5V	-

## 3. Carrier Board

### 3.1 Introduction

Through the previous function introduction, you can understand the function of the carrier board.

- 1 channel PCIe8 interface
- 4-channel SFP interfaces
- 2-channel 10/100M/1000M Ethernet RJ-45 interfaces
- 1-channel HDMI video output interface
- 1-channel HDMI video Input interface
- 4-channel USB HOST interfaces
- 1-channel USB Uart communication interface
- 1-channel SD card interface
- 1-channel 40-pin expansion port
- JTAG debugging interface
- 4 independent keys
- 4 user LED lights

### 3.2 USB to Serial Port

The AX7Z100B FPGA carrier board is equipped with a Uart to USB interface for system debugging. The conversion chip uses the USB-UAR chip of Silicon Labs CP2102GM. The USB interface uses the MINI USB interface, which can be connected to the USB port of the upper PC with a USB cable for separate power supply and serial data communication of the core board.

The schematic diagram of USB Uart circuit design is shown in the following figure:

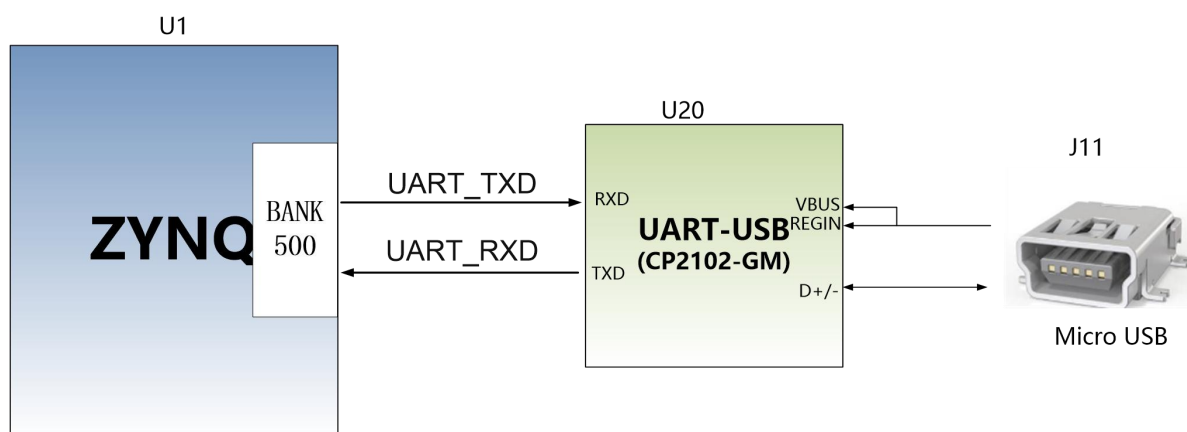


Figure 3-2-1: USB to serial port schematic

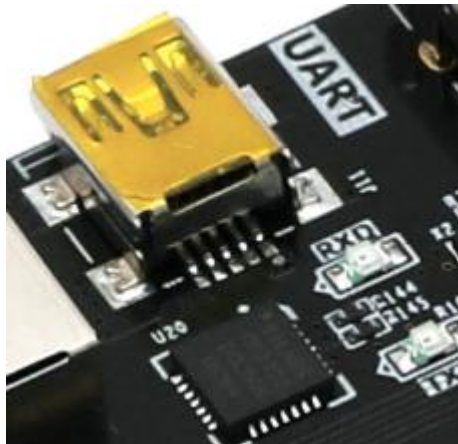


Figure 3-2-2: USB to serial port picture

**USB to serial port ZYNQ pin assignment:**

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
UART_RXD	PS_MIO14_500	B22	Uart data input
UART_TXD	PS_MIO15_500	C22	Uart data output

### 3.3 Gigabit Ethernet Interface

The AX7Z100B FPGA development board has two Gigabit Ethernet interfaces, one of which is connected to PS system, and the other one is connected to the logical IO port of the PL. The Gigabit Ethernet interface connected to the PL side needs to be mounted to the ZYNQ AXI bus system by calling the IP.

Ethernet chip adopts industrial-grade Ethernet GPHY chip (JL2121-N040I) from JLSemi company to provide users with network communication services. The Ethernet PHY chip on PS is connected to the GPIO interface of PS BANK501 of ZYNQ. The Ethernet PHY chip on the PL side is connected to the IO of the BANK35. The JL2121 chip supports 10/100/1000 Mbps network transmission rate and communicates data with the MAC layer of the Zynq7000 system through the RGMII interface. JL2121D supports MDI/MDX self-adaptive, various speed self-adaptive, Master/Slave self-adaptive, and supports MDIO bus for PHY register management.

When the JL2121 is powered on, it detects some specific IO level states to determine its own working mode. Table 3-3-1 describes the default settings of the

GPHY chip after it is powered on.

Configured Pin	Description	Configuration Value
RXD3_ADR0 RXC_ADR1 RXCTL_ADR2	PHY address in MDIO/MDC mode	PHY Address is 001
RXD1_TXDLY	TX clock 2ns delay	Delay
RXD0_RXDLY	RX clock 2ns delay	Delay

Table 3-3-1: PHY chip default settings

When the network is connected to Gigabit Ethernet, the data transmission of ZYNQ and PHY chip JL2121 is communicated through the RGMII bus with a 125Mhz transmission clock, and the data is sampled on the rising edge and falling edge of the clock.

When the network is connected to 100M Ethernet, the data transmission of ZYNQ and PHY chip JL2121 is communicated through RMII bus with a 25Mhz transmission clock. Data is sampled on the rising edge and falling edge of the clock.

Figure 3-3-1 shows the connection diagram of 1-channel Ethernet PHY chip on ZYNQ PS terminal:

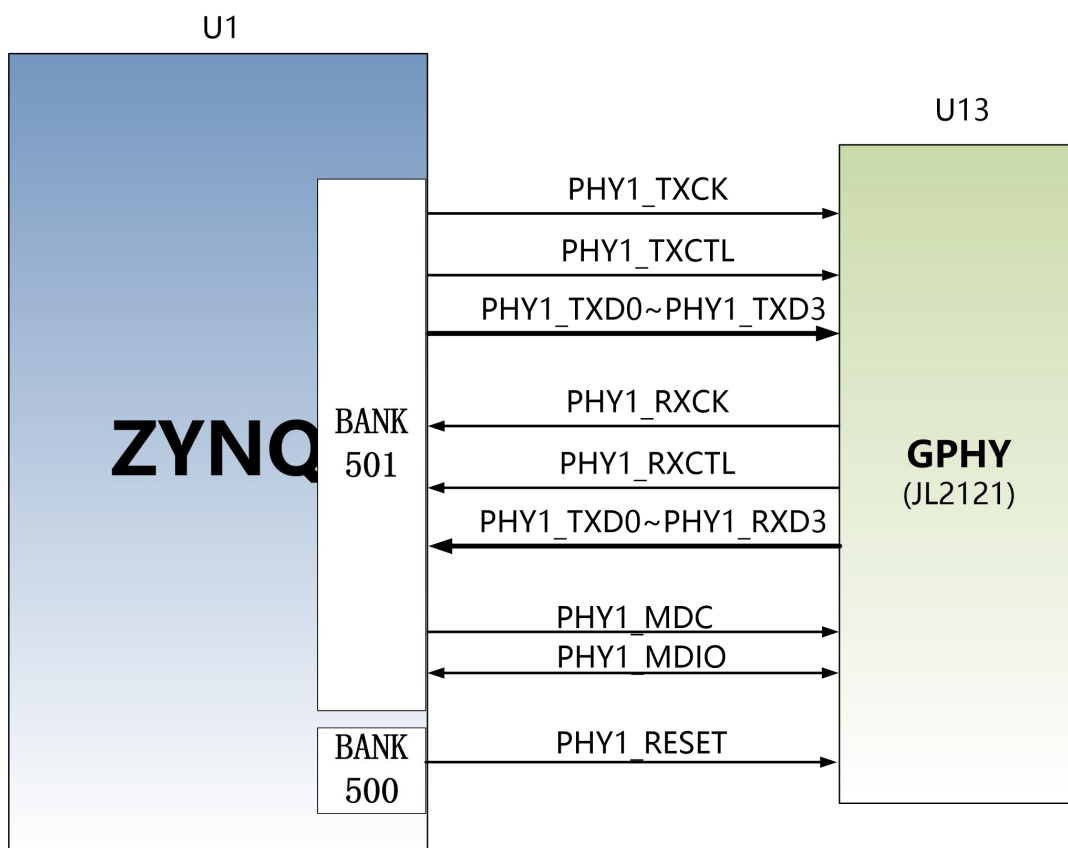


Figure 3-3-1: Connection diagram between ZYNQ PS system and GPHY

Figure 3-3-2 shows the connection diagram of ZYNQ PL-side 1-channel Ethernet PHY chip:

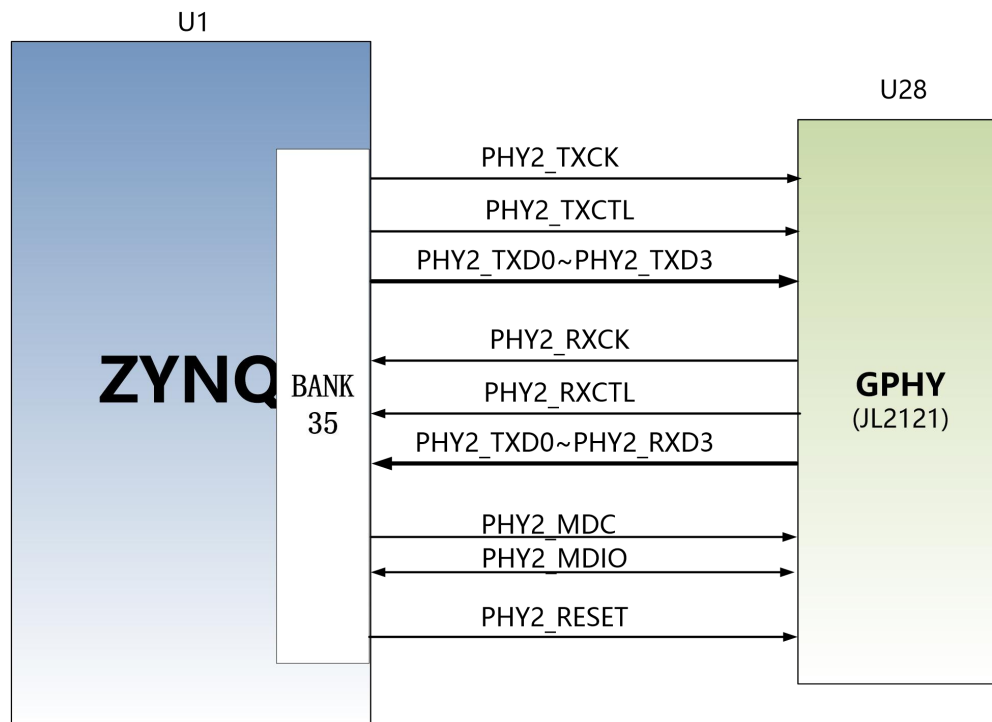


Figure 3-3-2: Connection diagram between ZYNQ PL side and GPHY

**PS side Gigabit Ethernet pin assignment:**

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
PHY1_TXCK	PS_MIO16_501	L19	RGMIITransmit Clock
PHY1_TXD0	PS_MIO17_501	K21	Transmit data bit0
PHY1_TXD1	PS_MIO18_501	K20	Transmit data bit1
PHY1_TXD2	PS_MIO19_501	J20	Transmit data bit2
PHY1_TXD3	PS_MIO20_501	M20	Transmit data bit3
PHY1_TXCTL	PS_MIO21_501	J19	Transmit enable signal
PHY1_RXCK	PS_MIO22_501	L20	RGMIIReceive Clock
PHY1_RXD0	PS_MIO23_501	J21	Receive data Bit0
PHY1_RXD1	PS_MIO24_501	M19	Receive data Bit1
PHY1_RXD2	PS_MIO25_501	G19	Receive data Bit2
PHY1_RXD3	PS_MIO26_501	M17	Receive data Bit3
PHY1_RXCTL	PS_MIO27_501	G20	Receive data valid signal
PHY1_MDC	PS_MIO52_501	D19	MDIO Management

			clock
<b>PHY1_MDIO</b>	PS_MIO53_501	C18	MDIO Management data
<b>PHY1_RESET</b>	PS_MIO7_500	B24	Reset signal

#### PL side Gigabit Ethernet pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
PHY2_TXCK	B35_L5_P	K15	RGMII Transmit Clock
PHY2_TXD0	B35_L8_N	G14	Transmit data bit0
PHY2_TXD1	B35_L8_P	G15	Transmit data bit1
PHY2_TXD2	B35_L3_N	K13	Transmit data bit2
PHY2_TXD3	B35_L3_P	L13	Transmit data bit3
PHY2_TXCTL	B35_L5_N	J15	Transmit enable signal
PHY2_RXCK	B35_L11_P	E13	RGMII Receive Clock
PHY2_RXD0	B35_L12_P	F15	Receive data Bit0
PHY2_RXD1	B35_L12_N	F14	Receive data Bit1
PHY2_RXD2	B35_L10_N	E12	Receive data Bit2
PHY2_RXD3	B35_L10_P	F13	Receive data Bit3
PHY2_RXCTL	B35_L11_N	D13	Receive data valid signal
PHY2_MDC	B35_L23_P	B14	MDIO Management clock
PHY2_MDIO	B35_L23_N	A14	MDIO Management data
PHY2_RESET	B35_L21_P	B15	Reset signal

### 3.4 USB2.0 Host Interface

The AX7Z100B carrier board has four USB2.0 HOST interfaces, and the USB2.0 transceiver uses a 1.8V high-speed USB3320C-EZK chip that supports the ULPI standard interface, and then extends four USB HOST interfaces through a USB HUB chip USB2514. ZYNQ's USB bus interface is connected to the USB3320C-EZK transceiver for high-speed USB2.0 Host mode data communication. The USB data and control signals of the USB3320C are connected to the IO port of PS BANK501 of the ZYNQ chip, and the differential signals of the USB interface (DP/DM) are connected to

the USB2514 chip to extend four USB interfaces. Two 24MHz crystal oscillators provide the clock for the USB3320C and USB2514 chips, respectively.

Four USB interfaces are flat USB interfaces (USB Type A), which is convenient for users to connect different USB Slave peripherals (such as USB mouse and USB keyboard) at the same time, and each USB interface provides +5V power supply.

The connection diagram between the ZYNQ processor and the USB3320C-EZK chip and the USB2514 chip is shown in 3-4-1:

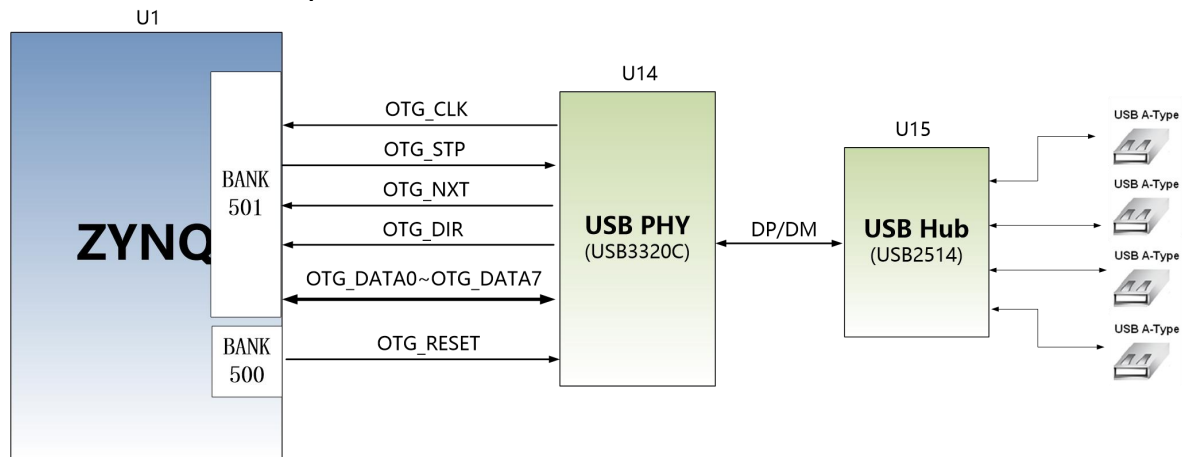


Figure 3-4-1: Connection diagram between Zynq7000 and USB chip

**USB2.0 pin assignment:**

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
OTG_DATA4	PS_MIO28_501	L17	USB data Bit4
OTG_DIR	PS_MIO29_501	H22	USB data direction signal
OTG_STP	PS_MIO30_501	L18	USB stop signal
OTG_NXT	PS_MIO31_501	H21	USB next data signal
OTG_DATA0	PS_MIO32_501	K17	USB data Bit0
OTG_DATA1	PS_MIO33_501	G22	USB data Bit1
OTG_DATA2	PS_MIO34_501	K18	USB data Bit2
OTG_DATA3	PS_MIO35_501	G21	USB data Bit3
OTG_CLK	PS_MIO36_501	H17	USB clock signal
OTG_DATA5	PS_MIO37_501	B21	USB data Bit5
OTG_DATA6	PS_MIO38_501	A20	USB data Bit6
OTG_DATA7	PS_MIO39_501	F18	USB data Bit7



OTG_RESETN	PS_MIO7_500	B24	USB reset signal
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### 3.5 HDMI Output Interface

The HDMI output interface is implemented by using ANALOG DEVICE's ADV7511 HDMI (DVI) coding chip, which supports a maximum 1080P@60Hz output and 3D output.

Among them, the video digital interface, audio digital interface and I2C configuration interface of the ADV7511 are connected to the BANK35 IO of the ZYNQ7000 PL, and the ZYNQ7000 system initializes and controls the ADV7511 through I2C pins. The hardware connection diagram of ADV7511 chip and ZYNQ7000 is shown in Figure 3-5-1 below:

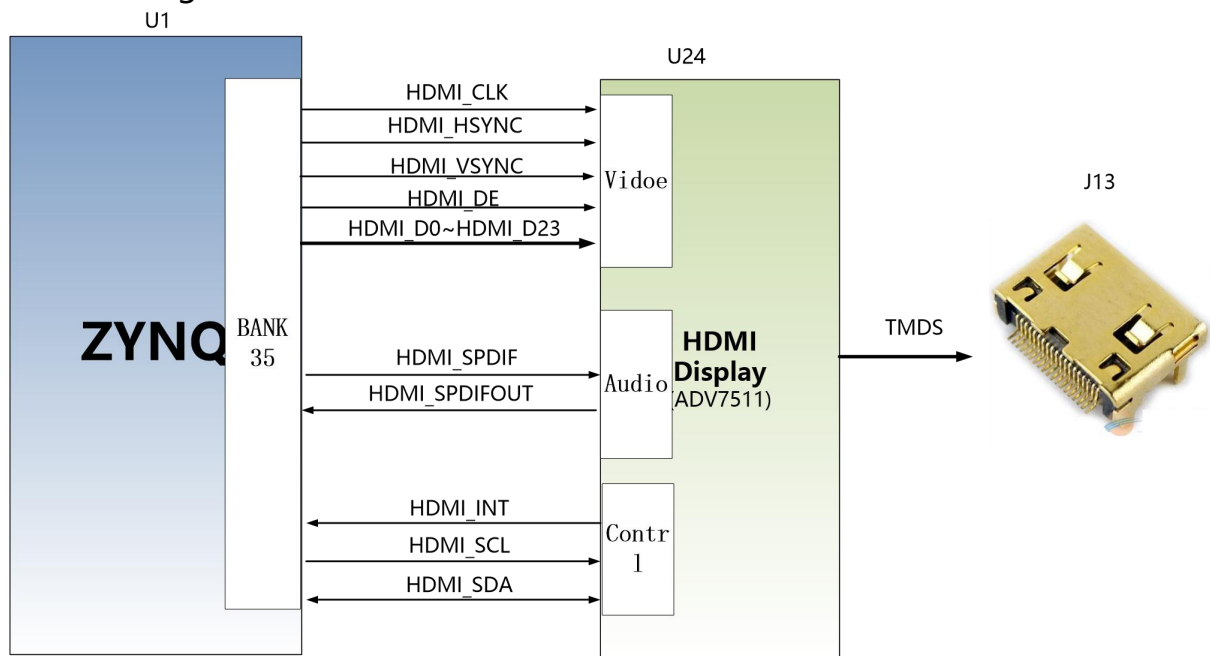


Figure 3-5-1: HDMI output design schematic

#### ZYNQ pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
HDMI_CLK	B35_L4_N	H14	HDMI video signal clock
HDMI_HSYNC	B35_L2_P	J13	HDMI video signal line synchronization
HDMI_VSYNC	B35_L2_N	H13	HDMI video signal column synchronization

HDMI_DE	B35_L9_P	G12	HDMI video signal valid
HDMI_D0	B35_L9_N	F12	HDMI video signal data 0
HDMI_D1	B35_L22_N	B11	HDMI video signal data 1
HDMI_D2	B35_L22_P	C11	HDMI video signal data 2
HDMI_D3	B35_L20_N	B12	HDMI video signal data 3
HDMI_D4	B35_L20_P	C12	HDMI video signal data 4
HDMI_D5	B35_L19_N	C13	HDMI video signal data 5
HDMI_D6	B35_L19_P	C14	HDMI video signal data 6
HDMI_D7	B35_L24_N	A12	HDMI video signal data 7
HDMI_D8	B35_L24_P	A13	HDMI video signal data 8
HDMI_D9	B35_L4_P	J14	HDMI video signal data 9
HDMI_D10	B35_L1_N	L14	HDMI video signal data 10
HDMI_D11	B35_L1_P	L15	HDMI video signal data 11
HDMI_D12	B35_L16_N	C16	HDMI video signal data 12
HDMI_D13	B35_L16_P	D16	HDMI video signal data 13
HDMI_D14	B35_L18_N	A17	HDMI video signal data 14
HDMI_D15	B35_L18_P	B17	HDMI video signal data 15
HDMI_D16	B35_L15_N	E17	HDMI video signal data 16
HDMI_D17	B35_L15_P	F17	HDMI video signal data 17
HDMI_D18	B35_L7_N	G16	HDMI video signal data 18
HDMI_D19	B35_L7_P	G17	HDMI video signal data 19
HDMI_D20	B35_L6_N	H16	HDMI video signal data 20
HDMI_D21	B35_L6_P	J16	HDMI video signal data 21
HDMI_D22	B35_L17_P	C17	HDMI video signal data 22
HDMI_D23	B35_L17_N	B16	HDMI video signal data 23
HDMI_INT	B35_L21_N	A15	HDMI interrupt signal
HDMI_SCL	B35_L13_N	E15	HDMI IIC control clock
HDMI_SDA	B35_L13_P	E16	HDMI IIC control data

### 3.6 HDMI Input Interface

HDMI input interface is implemented by using Sillion Image's SiI9011/ SiI9013 HDMI decoding chip, which supports a maximum 1080P@60Hz input and supports data output in different formats.

Among them, the IIC configuration interface of SiI9011/SiI9013 is also connected to the IO of FPGA BANK13. ZYNQ initializes and controls SiI9013 through I2C bus programming, and the hardware connection of the HDMI input interface is shown in Figure 3-6-1:

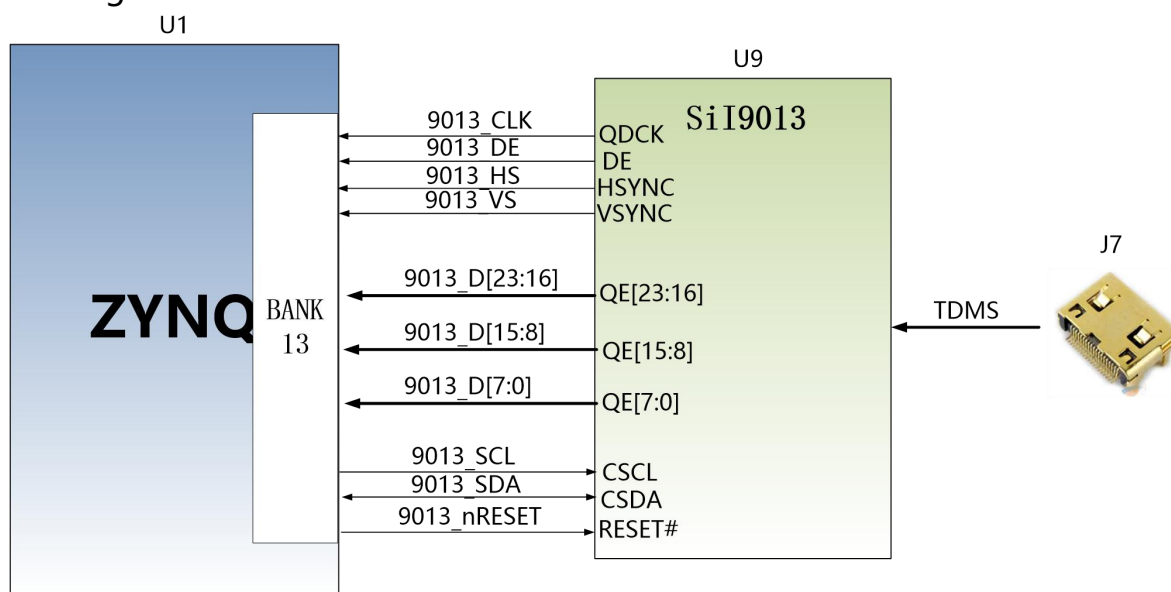


Figure 3-6-1: HDMI input schematic

#### ZYNQ pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
9013_nRESET	B11_L19_P	AB21	9013 reset signal
9013_CLK	B11_L11_P	AD23	9013 video signal clock
9013_HS	B11_L10_N	AE21	9013 video signal line synchronization
9013_VS	B11_L10_P	AD21	9013 video signal column synchronization
9013_DE	B11_L9_N	AF24	9013 video signal valid
9013_D[0]	B11_L9_P	AF23	9013 video signal data 0
9013_D[1]	B11_L11_N	AE23	9013 video signal data 1

9013_D[2]	B11_L7_N	AD24	9013 video signal data 2
9013_D[3]	B11_L7_P	AC24	9013 video signal data 3
9013_D[4]	B11_L22_P	AA24	9013 video signal data 4
9013_D[5]	B11_L22_N	AB24	9013 video signal data 5
9013_D[6]	B11_L21_P	Y22	9013 video signal data 6
9013_D[7]	B11_L21_N	Y23	9013 video signal data 7
9013_D[8]	B11_L23_P	AA22	9013 video signal data 8
9013_D[9]	B11_L23_N	AA23	9013 video signal data 9
9013_D[10]	B11_L4_N	AJ24	9013 video signal data 10
9013_D[11]	B11_L4_P	AJ23	9013 video signal data 11
9013_D[12]	B11_L3_P	AJ21	9013 video signal data 12
9013_D[13]	B11_L3_N	AK21	9013 video signal data 13
9013_D[14]	B11_L2_N	AK23	9013 video signal data 14
9013_D[15]	B11_L2_P	AK22	9013 video signal data 15
9013_D[16]	B11_L5_N	AH24	9013 video signal data 16
9013_D[17]	B11_L5_P	AH23	9013 video signal data 17
9013_D[18]	B11_L15_P	AJ20	9013 video signal data 18
9013_D[19]	B11_L15_N	AK20	9013 video signal data 19
9013_D[20]	B11_L13_N	AH21	9013 video signal data 20
9013_D[21]	B11_L13_P	AG21	9013 video signal data 21
9013_D[22]	B11_L14_N	AG20	9013 video signal data 22
9013_D[23]	B11_L14_P	AF20	9013 video signal data 23
9013_SCL	B11_L24_N	AC23	9013 IIC control clock
9013_SDA	B11_L24_P	AC22	9013 IIC control data

### 3.7 Optical Fiber Interface

The AX7Z100B carrier board has four optical fiber interfaces. Users can purchase SFP optical modules (1.25G, 2.5G, and 10G optical modules in the market) and insert them into the four optical fiber interfaces for optical fiber data communication. Four optical fiber interfaces are respectively connected to the two RX/TX channels of ZYNQ's BANK110 GTX transceiver. The TX and RX signals are connected to the ZYNQ

and optical modules in differential signals via capacitance. Each TX transmission and RX reception data rate can up to 10Gb/s. The reference clock for the BANK110's GTX transceiver is provided by the 125M differential clock on the core board.

The schematic diagram of FPGA and optical fiber design is shown in Figure 3-7-1 below:

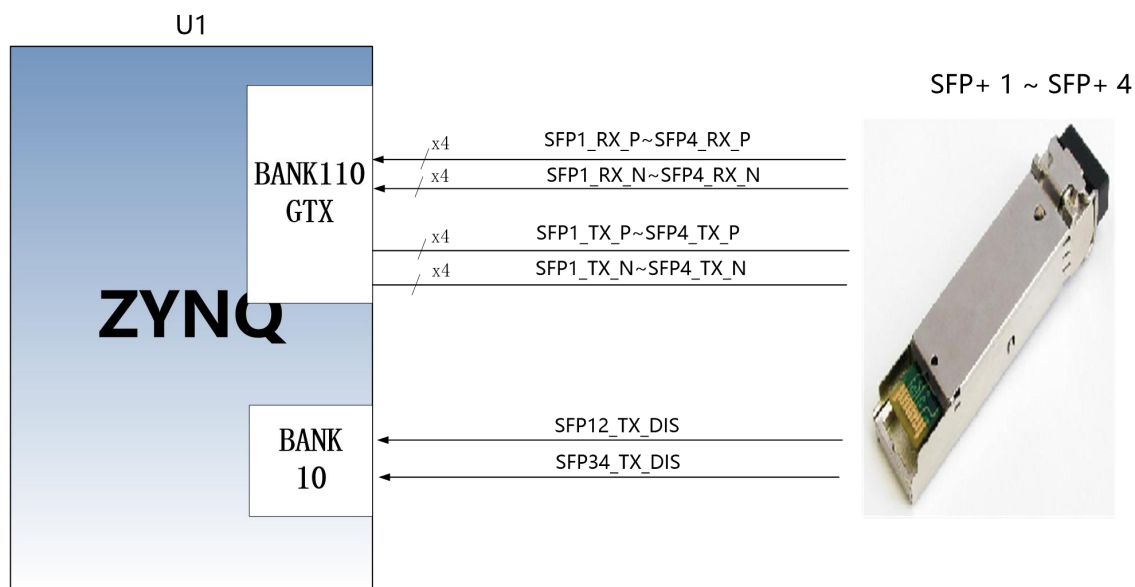


Figure 3-7-1: Optical fiber design diagram

**ZYNQ pin assignments of four optical fiber interfaces:**

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
SFP1_TX_P	BANK110_TX3_P	AD2	Optical module 1 data transmission, Positive
SFP1_TX_N	BANK110_TX3_N	AD1	Optical module 1 data transmission, Negative
SFP1_RX_P	BANK110_RX3_P	AD6	Optical module 1 data reception, Positive
SFP1_RX_N	BANK110_RX3_N	AD5	Optical module 1 data reception, Negative
SFP2_TX_P	BANK110_TX2_P	AE4	Optical module 2 data transmission, Positive
SFP2_TX_N	BANK110_TX2_N	AE3	Optical module 2 data transmission, Negative

SFP2_RX_P	BANK110_RX2_P	AF6	Optical module 2 data reception, Positive
SFP2_RX_N	BANK110_RX2_N	AF5	Optical module 2 data reception, Negative
SFP3_TX_P	BANK110_TX1_P	AF2	Optical module 3 data transmission, Positive
SFP3_TX_N	BANK110_TX1_N	AF1	Optical module 3 data transmission, Negative
SFP3_RX_P	BANK110_RX1_P	AG4	Optical module 3 data reception, Positive
SFP3_RX_N	BANK110_RX1_N	AG3	Optical module 3 data reception, Negative
SFP4_TX_P	BANK110_TX0_P	AH2	Optical module 4 data transmission, Positive
SFP4_TX_N	BANK110_TX0_N	AH1	Optical module 4 data transmission, Negative
SFP4_RX_P	BANK110_RX0_P	AH6	Optical module 4 data reception, Positive
SFP4_RX_N	BANK110_RX0_N	AH5	Optical module 4 data reception, Negative
SFP12_TX_DIS	B10_L17_P	AE18	Optical module 12 optical emission disabled, high validity
SFP34_TX_DIS	B10_L17_N	AE17	Optical module 34 optical emission disabled, high validity

### 3.8 PCIe Slot

AX7Z100B carrier board has a PCIe x8 interface, and 8 pairs of transceivers are connected to the golden finger of PCIe x8, which can realize the data communication of PCIe x8, PCIe x4, PCIe x2 and PCIe x1.

The transceiver signals of PCIe interface are directly connected to GTX transceivers of ZYNQ BANK111 and BANK112, 8-channel TX signals and RX signals are connected to the ZYNQ transceiver in differential signal mode, and the single channel communication rate can be up to 5G bit bandwidth.

The design diagram of the PCIe interface of the development board is shown in Figure 3-8-1, where the TX sending signal is connected in AC coupling mode.

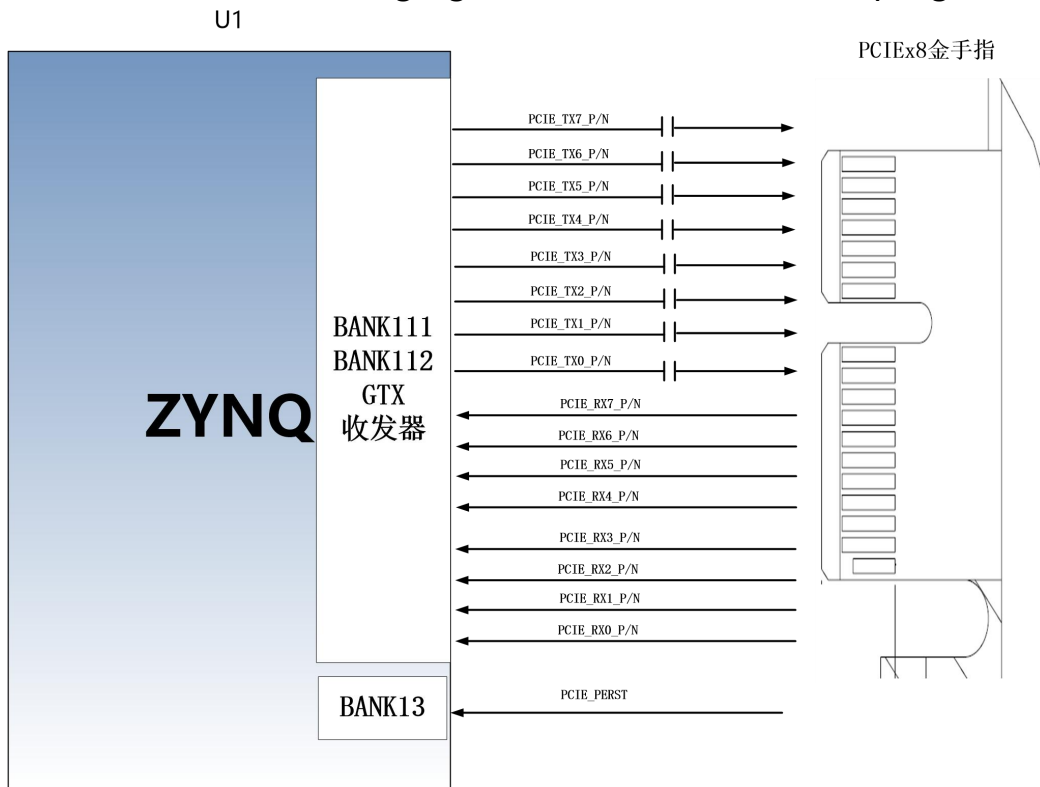


Figure 3-8-1: PCIe slot design diagram

#### PCIe x8 interface ZYNQ pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
PCIE_RX0_P	BANK112_RX3_P	P6	PCIe channel 0 data reception, Positive
PCIE_RX0_N	BANK112_RX3_N	P5	PCIe channel 0 data reception, Negative

PCIE_RX1_P	BANK112_RX2_P	T6	PCIE channel 1 data reception, Positive
PCIE_RX1_N	BANK112_RX2_N	T5	PCIE channel 1 data reception, Negative
PCIE_RX2_P	BANK112_RX1_P	U4	PCIE channel 2 data reception, Positive
PCIE_RX2_N	BANK112_RX1_N	U3	PCIE channel 2 data reception, Negative
PCIE_RX3_P	BANK112_RX0_P	V6	PCIE channel 3 data reception, Positive
PCIE_RX3_N	BANK112_RX0_N	V5	PCIE channel 3 data reception, Negative
PCIE_RX4_P	BANK111_RX3_P	AA4	PCIE channel 4 data reception, Positive
PCIE_RX4_N	BANK111_RX3_N	AA3	PCIE channel 4 data reception, Negative
PCIE_RX5_P	BANK111_RX2_P	Y6	PCIE channel 5 data reception, Positive
PCIE_RX5_N	BANK111_RX2_N	Y5	PCIE channel 5 data reception, Negative
PCIE_RX6_P	BANK111_RX1_P	AB6	PCIE channel 6 data reception, Positive
PCIE_RX6_N	BANK111_RX1_N	AB5	PCIE channel 6 data reception, Negative
PCIE_RX7_P	BANK111_RX0_P	AC4	PCIE channel 7 data reception, Positive
PCIE_RX7_N	BANK111_RX0_N	AC3	PCIE channel 7 data reception, Negative
PCIE_TX0_P	BANK112_TX3_P	N4	PCIE channel 0 data transmission, Positive
PCIE_TX0_N	BANK112_TX3_N	N3	PCIE channel 0 data transmission, Negative
PCIE_TX1_P	BANK112_TX2_P	P2	PCIE channel 1 data



			transmission, Positive
PCIE_TX1_N	BANK112_TX2_N	P1	PCIE channel 1 data transmission, Negative
PCIE_TX2_P	BANK112_TX1_P	R4	PCIE channel 2 data transmission, Positive
PCIE_TX2_N	BANK112_TX1_N	R3	PCIE channel 2 data transmission, Negative
PCIE_TX3_P	BANK112_TX0_P	T2	PCIE channel 3 data transmission, Positive
PCIE_TX3_N	BANK112_TX0_N	T1	PCIE channel 3 data transmission, Negative
PCIE_TX4_P	BANK111_TX3_P	V2	PCIE channel 4 data transmission, Positive
PCIE_TX4_N	BANK111_TX3_N	V1	PCIE channel 4 data transmission, Negative
PCIE_TX5_P	BANK111_TX2_P	W4	PCIE channel 5 data transmission, Positive
PCIE_TX5_N	BANK111_TX2_N	W3	PCIE channel 5 data transmission, Negative
PCIE_TX6_P	BANK111_TX1_P	Y2	PCIE channel 6 data transmission, Positive
PCIE_TX6_N	BANK111_TX1_N	Y1	PCIE channel 6 data transmission, Negative
PCIE_TX7_P	BANK111_TX0_P	AB2	PCIE channel 7 data transmission, Positive
PCIE_TX7_N	BANK111_TX0_N	AB1	PCIE channel 7 data transmission, Negative
PCIE_CLK_P	BANK112_CLK0_P	N8	PCIE channel reference clock, Positive
PCIE_CLK_N	BANK112_CLK0_N	N7	PCIE channel reference clock, Negative
PCIE_PERST	B11_L19_N	AB22	PCIE board reset signal

### 3.9 SD Card Slot

The AX7Z100B carrier board has a Micro-type SD card interface to provide user access to the SD card memory for storing ZYNQ chip BOOT programs, Linux operating system kernel, file system, and other user data files.

The SDIO signal is connected to the IO signal of the PS BANK501 of ZYNQ, because the VCCIO of the BANK is set to 1.8V, but the data level of the SD card is 3.3V, so here, we connect them by using a TXS02612 level converter. The schematic diagram of Zynq7000 PS and SD card connector is shown in Figure 3-9-1.

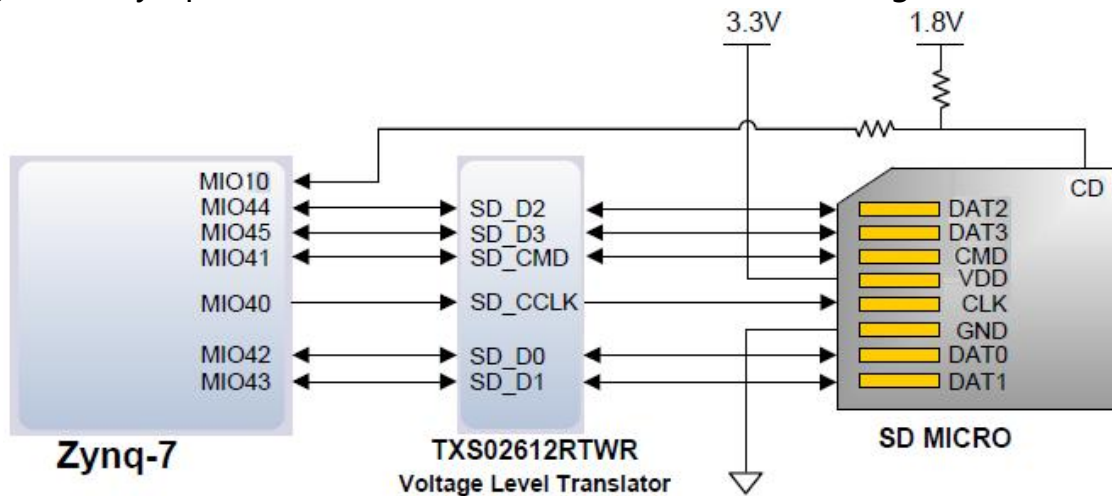


Figure 3-9-1: SD card connection diagram

**SD card slot pin assignment:**

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
SD_CLK	PS_MIO40	B20	SD clock signal
SD_CMD	PS_MIO41	J18	SD command signal
SD_D0	PS_MIO42	D20	SD Data0
SD_D1	PS_MIO43	E18	SD Data1
SD_D2	PS_MIO44	E20	SD Data2
SD_D3	PS_MIO45	H18	SD Data3

### 3.10 40-pin Expansion Port

The carrier board reserves a 40-pin expansion port J33 with 0.1-inch standard pitch, which is used to connect various ALINX modules or the external circuit designed by the user. The expansion port has 40 signals, including 1 5V power supply, 2 3.3V power supplies, 3 ground channels, and 34 IO ports. The IO of the expansion port is connected to the IO of ZYNQ BANK10, which is 3.3V by default. Do not directly connect to an external 5V device to avoid burning the ZYNQ7000 chip. If you want to connect a 5V device, you need to connect a level conversion chip.

The circuit of the expansion port (J33) is shown in Figure 3-10-1:

## FPGA 40 PIN External IO

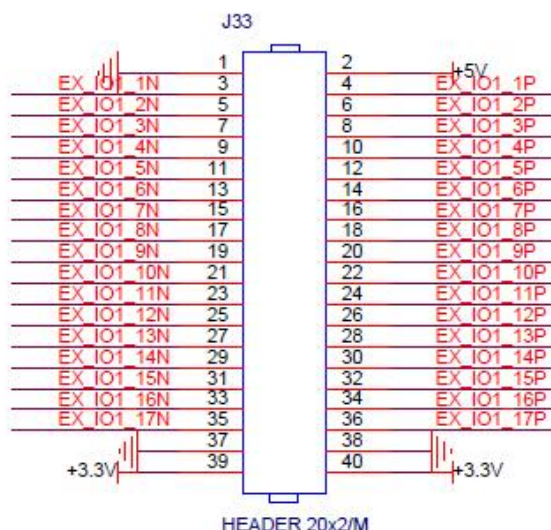


Figure 3-10-1: J33 schematic

#### J33 ZYNQ pin assignment:

J33 Pin	Signal Name	ZYNQ Pin Name	J33 Pin	Signal Name	ZYNQ Pin Number
1	GND	-	2	+5V	-
3	IO1_1N	AC13	4	IO1_1P	AC14
5	IO1_2N	AB12	6	IO1_2P	AC12
7	IO1_3N	AE12	8	IO1_3P	AF12
9	IO1_4N	AD13	10	IO1_4P	AD14

11	IO1_5N	AG12	12	IO1_5P	AH12
13	IO1_6N	AE13	14	IO1_6P	AF13
15	IO1_7N	AH13	16	IO1_7P	AH14
17	IO1_8N	AJ13	18	IO1_8P	AJ14
19	IO1_9N	AK12	20	IO1_9P	AK13
21	IO1_10N	AB14	22	IO1_10P	AB15
23	IO1_11N	AF15	24	IO1_11P	AG15
25	IO1_12N	AG14	26	IO1_12P	AF14
27	IO1_13N	AD15	28	IO1_13P	AD16
29	IO1_14N	AC16	30	IO1_14P	AC17
31	IO1_15N	AA14	32	IO1_15P	AA15
33	IO1_16N	AJ15	34	IO1_16P	AK15
35	IO1_17N	AB17	36	IO1_17P	AB16
37	GND	-	38	GND	-
39	+3.3V	-	40	+3.3V	-

### 3.11 LED Light

The AX7Z100B carrier board has 7 LEDs: 1 power indicator, 2 serial communication indicators, 4 PL control indicators. When the development board is powered on, the power indicator will light up; Four LED lights are connected to the IO of PL, and users can control the on and off through the program. When the IO voltage connected to user LED is low, the user LED will be turned off. When the IO voltage connected to user LED is high, the user LED will be turned on. The diagram of hardware connection of user LED light is shown in Figure 3-11-1:

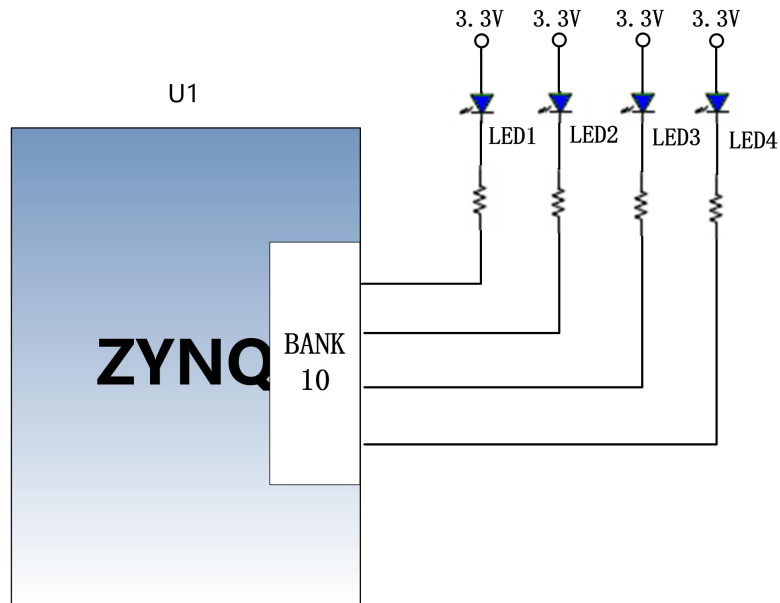


Figure 3-11-1: Hardware connection diagram of user LED light

#### User LED light pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
PL_LED1	B10_L4_P	AJ16	User PL LED1
PL_LED2	B10_L4_N	AK16	User PL LED2
PL_LED3	B10_L16_P	AE16	User PL LED3
PL_LED4	B10_L16_N	AE15	User PL LED4

### 3.12 Reset Key and User Keys

The AX7Z100B has one RESET key and four user keys on the carrier board. The reset signal is connected to the reset chip input of the core board. Users can use this reset key to reset the ZYNQ system, and the other four keys are connected to the IO of PL. All the reset key and user keys are active at low levels. The connection diagram of the reset key and user keys is shown in Figure 3-12-1:

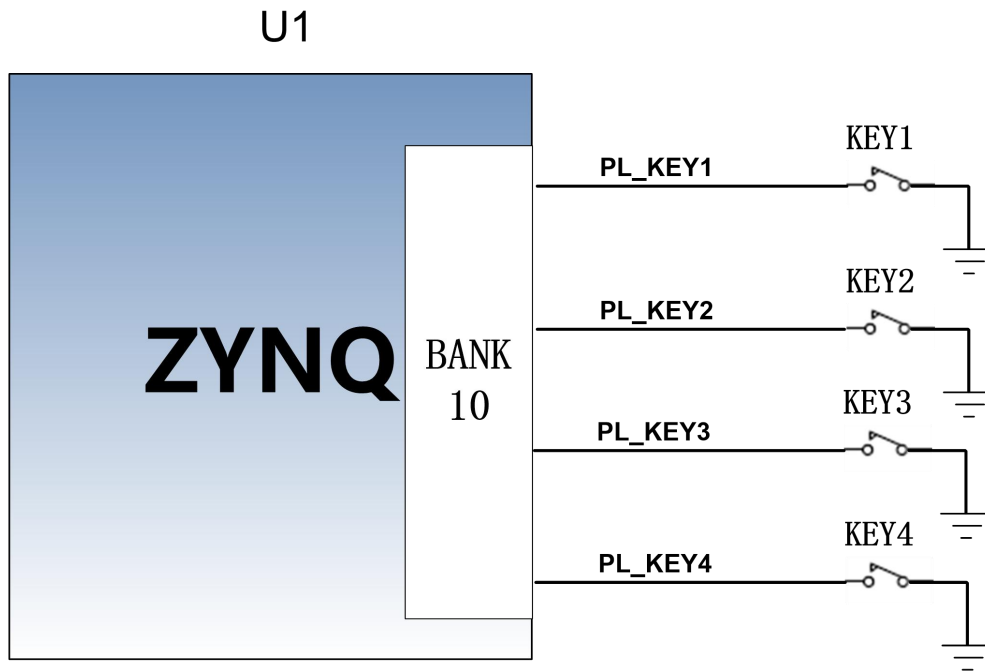


Figure 3-12-1 复位按键连接示意图

Keys ZYNQ pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
PL_KEY1	B10_L15_P	AF18	PL KEY1 input
PL_KEY2	B10_L15_N	AF17	PL KEY2 input
PL_KEY3	B10_L6_P	AH17	PL KEY3 input
PL_KEY4	B10_L6_N	AH16	PL KEY4 input

### 3.13 JTAG Debugging Interface

A JTAG interface is reserved on the AX7Z100B carrier board for downloading ZYNQ programs or curing programs to FLASH. In order to prevent ZYNQ chip damage due to hot plugging, we add a protection diode to the JTAG signal to ensure that the voltage of the signal is within the range accepted by the FPGA to avoid damage to the ZYNQ chip.

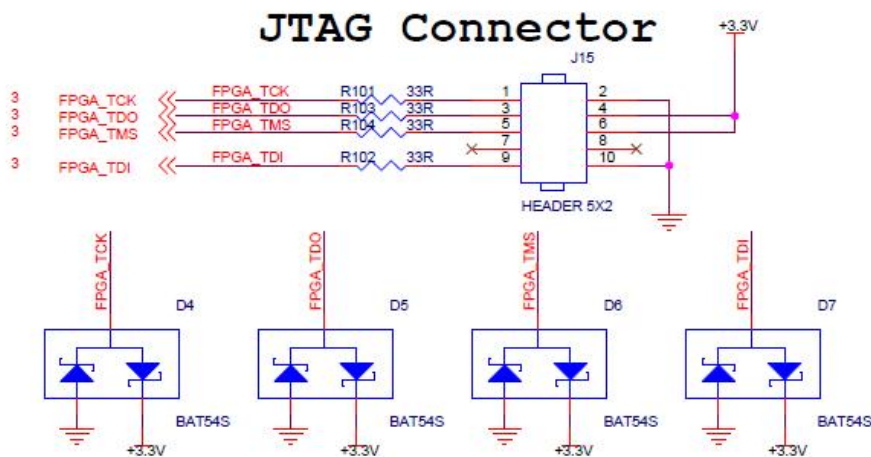


Figure 3-13-1: JTAG interface in schematic

The following is the physical picture of the JTAG interface on the carrier board. Users can connect the PC to the JTAG interface through the USB downloader provided by us to debug the ZYNQ system. Do not hot-plug the JTAG cable when plugging or unplugging the cable.

### 3.14 Dip Switch Configuration

There is a 2-bit dip switch SW1 on the development board to configure the boot mode of the ZYNQ system. The AX7Z100B system development platform supports three boot modes: JTAG debugging mode, QSPI FLASH and SD card boot mode. When powered on, the XC7Z0100 chip detects the level responded to MIO ports (MIO5 and MIO4) to determine the boot mode. Users can select different boot modes through the dip switch SW1 on the core board. Table 3-14-1 lists the boot mode configuration of SW1.

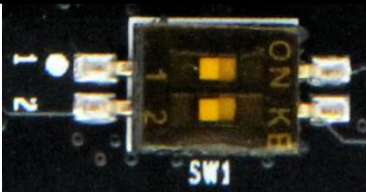
SW1	Dip Position (1, 2)	MIO5, MIO4 Level	Boot Mode
	ON、 ON	0、 0	JTAG
	OFF、 OFF	1、 1	SD card
	OFF、 ON	1、 0	QSPI FLASH

Table 3-14-1: SW1 boot mode configuration

### 3.15 Power Supply

The power input voltage of the development board is DC12V. You can supply power to the development board through the PCIE slot or externally connect a +12V power supply. If the external power supply is used, please use the power supply of the development board. Do not use other power, 1-channel DC/DC power chip ETA8156FT2G and 2-channel DC/DC power chip ETA1471FT2G are converted into +5V, +3.3V and 1.8V power supplies. Because the +5V power supply supplies the core board through the board-to-board connectors, the current output of the DCDC power supply is 6A, and the current output of the other 2 power supplies is 3A.

The power supply design diagram on the board is shown in Figure 3-15-1 below:

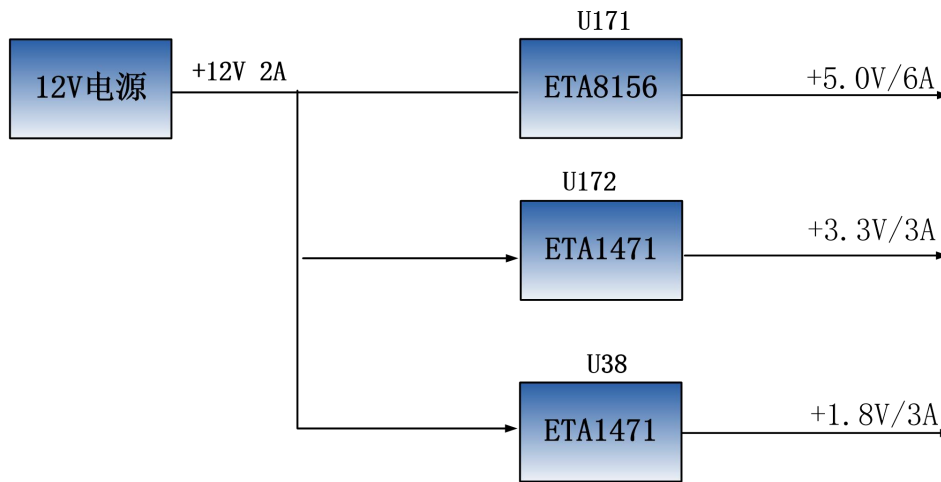


Figure 3-15-1: Power supply interface in schematic

The functions of each power distribution are shown in the following table:

Power Supply	Function
+5.0V	Core board power supply
+1.8V	Ethernet, HDMI, USB
+3.3V	Ethernet, HDMI, USB, SD, Fiber, PCIE



### 3.16 Fan

Because ZYNQ7100 generates a lot of heat when it is working properly, we added a heat sink and fan to the board to prevent the chip from overheating. Fan control is controlled by ZYNQ chip, the control pin is connected to the IO of BANK10, if the IO level output is low, the MOSFET tube will on, the fan will work; if the IO level output is high, the fan will stop working. The fan design diagram on the board is shown in FIG. 3-16-1 below:

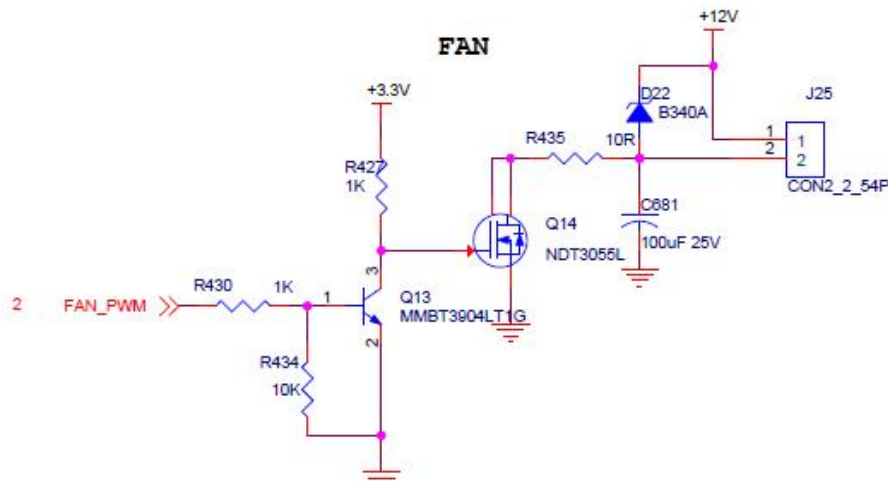


Figure 3-16-1: Fan design schematic

The fan has been fixed on the development board with screws before leaving the factory. The power supply of the fan is connected to the J25 socket. The red one is positive and the black one is negative.

#### Fan control pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
FAN_PWM	IO_L13N_T2_MRCC_10	AG16	Fan control

### 3.17 Size Dimension

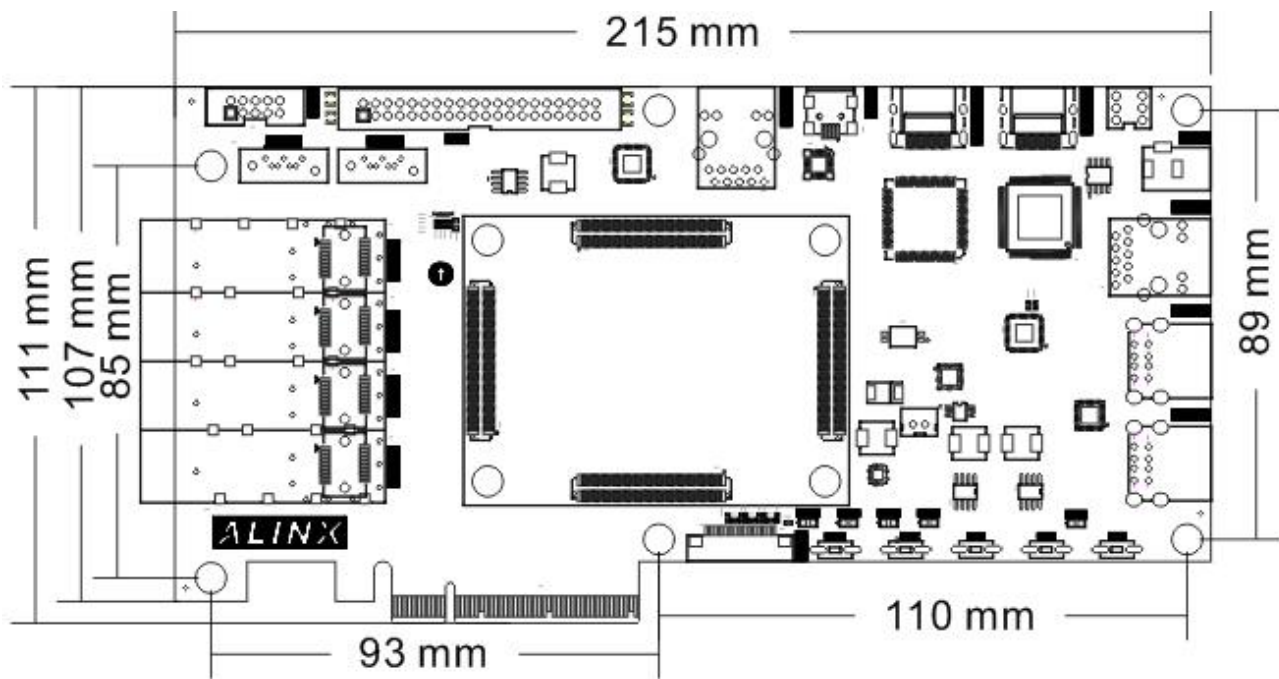


Figure 3-17-1: Top View