KINTEX UltraScale FPGA Development Board AXKU040

User Manual

ALINX

Version Record

Version	Date	Release By	Description
Rev 1.1	2021-09-13	Rachel Zhou	First Release

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Part 1: FPGA Development Board Introduction

The AXKU040 FPGA development board is mainly composed of KINTEX UltraScale+ chip. It meets users' requirements for high-speed data exchange, data storage, Video transmission processing, deep learning, artificial intelligence and industrial control, and it is a "professional" FPGA development platform. For high-speed data transmission and exchange, pre-verification and post-application of data processing is possible. This product is very suitable for students, engineers and other groups engaged in FPGA development.

AXKU040 FPGA development board mounts four 1GB high-speed DDR4 SDRAM chips. FPGA chip configuration uses a 128Mb QSPI FLASH chip.

The AXKU040 FPGA development board expands the rich peripheral interface, including four 10G optical SFP interfaces, three FMC expansion interfaces, one UART serial interface, one SD card interface, one HDMI Output, 2 Gigabit Ethernet Interfaces, SAM and SATA Interfaces etc.

The following figure shows the structure of the entire development system:

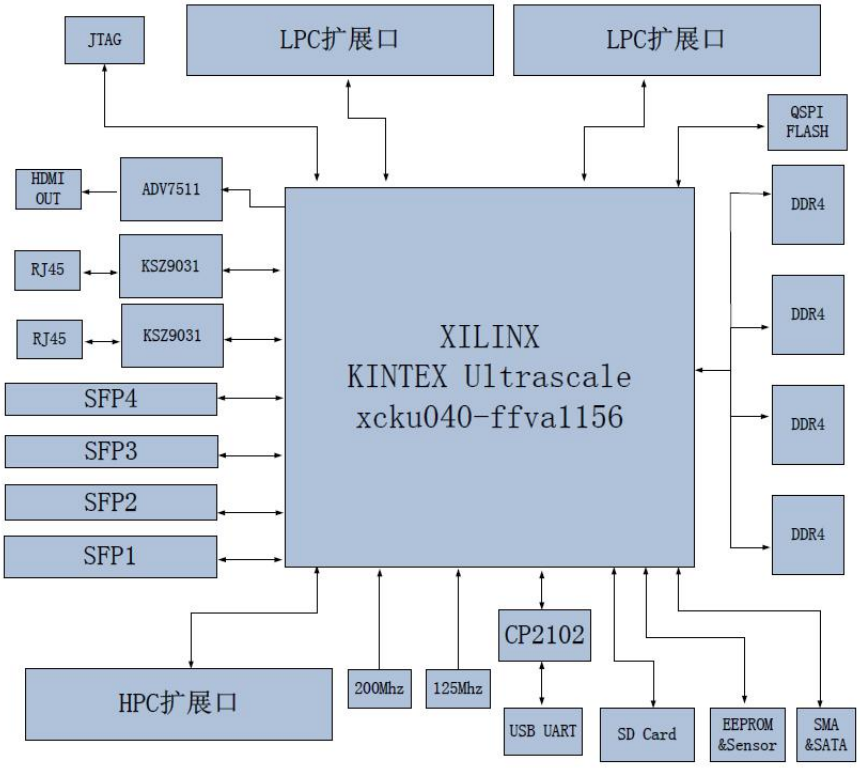

Figure 1-1: The Schematic Diagram of the AXKU040

Through this diagram, you can see the interfaces and functions that the AXKU040 FPGA Development Board contains:

- Xilinx KINTEX-7 UltraScale FPGA chip XCKU040
- DDR4

  With four large-capacity 1GB (4 GB total) high-speed DDR4 SDRAM, used as FPGA data storage, image analysis cache, data processing.
- QSPI FLASH

  A 128Mbit QSPI FLASH memory chip can be used as a storage for FPGA chip configuration files and user data;
- 4 SFP+ interfaces

  The four high-speed transceivers of the GTX transceiver of the FPGA are connected to the transmission and reception of four optical modules to realize four high-speed optical fiber communication interfaces. Each fiber optic data communication receives and transmits at speeds of up to 12.5 Gb/s.
- USB Uart interface

  1-channel Uart to USB interface for communication with the computer for user debugging. The serial port chip adopts the USB-UAR chip of Silicon Labs CP2102GM, and the USB interface adopts the MINI USB interface.
- HDMI Output Interface

  1 HDMI video output interface, using ADV7511 HDMI encoding chip from ANALOG DEVICE, supports up to 1080P@60Hz output and 3D output.
- Gigabit Ethernet Interface

  2-Channel 10/100M/1000M Ethernet RJ45 interface for Ethernet data exchange with computers or other network devices. The network interface chip uses Micrel's KSZ9031 industrial grade GPHY chip.
- FMC Expansion Interface

3 standard FMC expansion port, including 2 LPC FMC expansion ports and 1 HPC FMC expansion port, which can be connected to various FMC modules of XILINX or ALINX (HDMI input and output modules, binocular camera modules, high-speed AD modules, etc.).

- Micro SD slot

  1 Micro SD card holder, used to store operating system image and file system.

- SMA Interface and SATA Interfaces

  6 SMA external interfaces and 2 SATA interfaces, the pins are connected to the transceiver for external high-speed input and output signals.

- Temperature and humidity sensor

  Onboard a temperature and humidity sensor chip LM75 for detecting the temperature and humidity of the environment around the board

- EEPROM

  One EEPROM 24LC04 with I2C interface, which is Used for IIC bus communication and storage of some customer-defined information.

- JTAG Interface

  A 10-pin0.1 spacing standard JTAG ports for FPGA program download and debugging. Users can debug and download FPGAs through XILINX downloader.

- Clock

  A 200Mhz differential crystal onboard provides a stable clock source for the FPGA system.

  A 125Mhz differential crystal onboard provides reference clock for optical fiber.

  A 156.25Mhz differential crystal onboard provides reference clock for transceiver

- LED Light

  6LEDs, 1 power indicator, 1 DONE configuration indicator, 4 user indicators

- Key

  2 user keys, 1 reset key, connect to the normal IO of the FPGA.

Part 2: FPGA Chip

The FPGA development board uses Xilinx's KINTEX UltraScale FPGA chip, model number XCKU040-2FFVA1156I. The speed class is 2 and the temperature class is industrial. This model is a FFVA1156 package with 1156 pins and a 1.0mm pitch. The chip naming rules for Xilinx KINTEX UltraScale FPGA are shown in Figure 2-1 below:

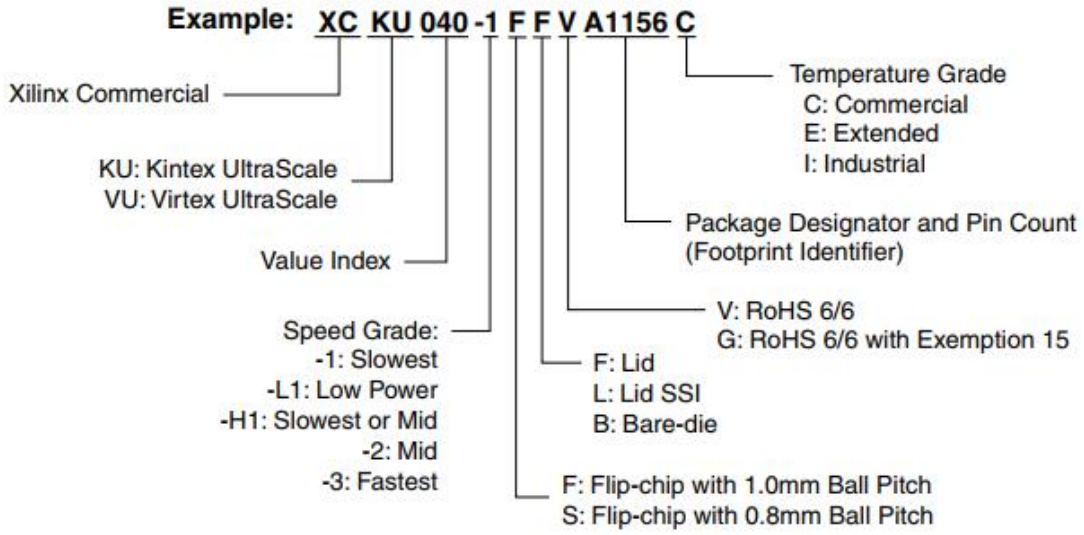

Figure 2-1: The Chip Model Definition of KINTEX UltraScale Series

The main parameters of the FPGA chip XCKU040 are as follows

Name	Specific parameters
Logic Cells	530,250
CLB Look-Up-Tables	242,400
CLB flip-flops	41,600
Block RAM（kb）	21.1
DSP Slices	1,920
PCIe Gen3 x 8	3
XADC	12bit, 1Mbps AD
GTP Transceiver	20, 16.3Gb/s max
Speed Grade	-2
Temperature Grade	Industrial

FPGA power supply system

XCKU040 FPGA power supplies are V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, V_{CCAUX_IO} V_{CCO}, $V_{MGTAVCC}$, $V_{MGTAVTT}$, $V_{MGTVCCAUK}$, $V_{MGTAVTTRCAL}$, V_{CCADC}. V_{CCINT} is the FPGA core power supply pin, which needs to be connected to 0.95V; V_{CCBRAM} is the power supply pin of FPGA Block RAM, connect to 0.95V; V_{CCAUX} and V_{CCAUX_IO} are FPGA auxiliary power supply pin, connect 1.8V; V_{CCO} is the voltage of each BANK of FPGA, including BANK0, BANK44~48, BANK64~68. $V_{MGTAVCC}$ is the power supply voltage of the GTH and GTY transceivers inside the FPGA, connected to 1.0V; $V_{MGTAVTT}$ is the terminal voltage of GTH transmission and reception, connected to 1.2V. $V_{MGTAVTTRCAL}$ is the transceiver resistance calibration voltage, connect to 1.2V. V_{CCADC} is the supply voltage of XADC, connected to 1.8V.

The XCKU040 FPGA system requires the power-on sequence as shown in Figure 2-2.

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT}/V_{CCINT_IO}, V_{CCBRAM}, V_{CCAUX}/V_{CCAUX_IO}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT}/V_{CCINT_IO} and V_{CCBRAM} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCINT_IO} must be connected to V_{CCINT}. If V_{CCAUX}/V_{CCAUX_IO} and V_{CCO} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCAUX} and V_{CCAUX_IO} must be connected together. When the current minimums are met, the device powers on after the V_{CCINT}/V_{CCINT_IO}, V_{CCBRAM}, V_{CCAUX}/V_{CCAUX_IO}, and V_{CCO} supplies have all passed through their power-on reset threshold voltages. The device must not be configured until after V_{CCINT} is applied.

V_{CCADC} and V_{REF} can be powered at any time and have no power-up sequencing recommendations.

The recommended power-on sequence to achieve minimum current draw for the GTH or GTY transceivers is V_{CCINT}, $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT}, $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw. If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

Figure 2-2: Power-On/Off Power Supply Sequencing

Part 3: DDR4 DRAM

The AXKU040 FPGA development board is equipped with four Micron 1GB DDR4 chips, model MT40A512M16LY-062EIT. Four DDR4 SDRAMs form a 64-bit bus width. Because four DDR4 chips are connected to the FPGA, the DDR4 SDRAM can run at speeds up to 1200MHz, and four DDR4 memory systems are directly connected to the BANK44, BANK45, and BANK46 interfaces of the FPGA. The specific configuration of DDR4 SDRAM is shown in Table 3-1.

Bit Number	Chip Model	Capacity	Factory
U45,U47,U48,U49	MT40A512M16LY-062EIT	512M x 16bit	Micron

Table 3-1: DDR4 SDRAM Configuration

The hardware design of DDR4 requires strict consideration of signal integrity. We have fully considered the matching resistor/terminal resistance, trace impedance control, and trace length control in circuit design and PCB design to ensure high-speed and stable operation of DDR3.

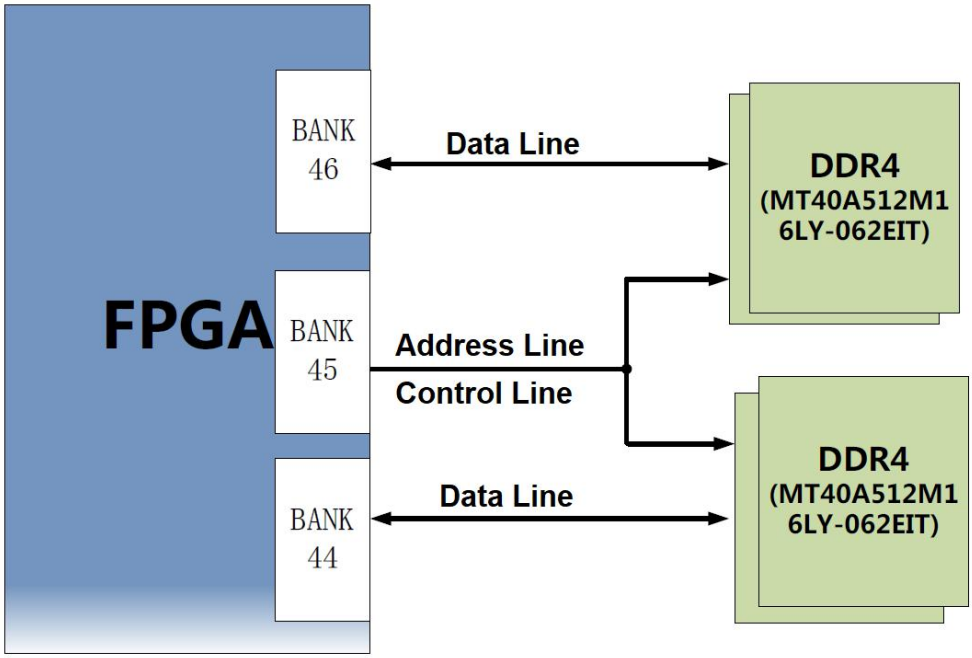

Figure 3-1: The DDR4 DRAM Schematic

4 DDR4 DRAM pin assignments:

Signal Name	FPGA Pin Name	FPGA Pin
PL_DDR4_DQ0	IO_L3N_T0L_N5_AD15N_44	AE20
PL_DDR4_DQ1	IO_L2N_T0L_N3_44	AG20
PL_DDR4_DQ2	IO_L2P_T0L_N2_44	AF20
PL_DDR4_DQ3	IO_L5P_T0U_N8_AD14P_44	AE22
PL_DDR4_DQ4	IO_L3P_T0L_N4_AD15P_44	AD20
PL_DDR4_DQ5	IO_L6N_T0U_N11_AD6N_44	AG22
PL_DDR4_DQ6	IO_L6P_T0U_N10_AD6P_44	AF22
PL_DDR4_DQ7	IO_L5N_T0U_N9_AD14N_44	AE23
PL_DDR4_DQ8	IO_L8N_T1L_N3_AD5N_44	AF24
PL_DDR4_DQ9	IO_L11P_T1U_N8_GC_44	AJ23
PL_DDR4_DQ10	IO_L8P_T1L_N2_AD5P_44	AF23
PL_DDR4_DQ11	IO_L12N_T1U_N11_GC_44	AH23
PL_DDR4_DQ12	IO_L9N_T1L_N5_AD12N_44	AG25
PL_DDR4_DQ13	IO_L11N_T1U_N9_GC_44	AJ24
PL_DDR4_DQ14	IO_L9P_T1L_N4_AD12P_44	AG24
PL_DDR4_DQ15	IO_L12P_T1U_N10_GC_44	AH22
PL_DDR4_DQ16	IO_L14P_T2L_N2_GC_44	AK22
PL_DDR4_DQ17	IO_L17P_T2U_N8_AD10P_44	AL22
PL_DDR4_DQ18	IO_L15N_T2L_N5_AD11N_44	AM20
PL_DDR4_DQ19	IO_L17N_T2U_N9_AD10N_44	AL23
PL_DDR4_DQ20	IO_L14N_T2L_N3_GC_44	AK23
PL_DDR4_DQ21	IO_L18N_T2U_N11_AD2N_44	AL25
PL_DDR4_DQ22	IO_L15P_T2L_N4_AD11P_44	AL20
PL_DDR4_DQ23	IO_L18P_T2U_N10_AD2P_44	AL24
PL_DDR4_DQ24	IO_L20P_T3L_N2_AD1P_44	AM22
PL_DDR4_DQ25	IO_L23P_T3U_N8_44	AP24
PL_DDR4_DQ26	IO_L20N_T3L_N3_AD1N_44	AN22
PL_DDR4_DQ27	IO_L21N_T3L_N5_AD8N_44	AN24
PL_DDR4_DQ28	IO_L24P_T3U_N10_44	AN23
PL_DDR4_DQ29	IO_L23N_T3U_N9_44	AP25
PL_DDR4_DQ30	IO_L24N_T3U_N11_44	AP23
PL_DDR4_DQ31	IO_L21P_T3L_N4_AD8P_44	AM24
PL_DDR4_DQ32	IO_L2P_T0L_N2_46	AM26
PL_DDR4_DQ33	IO_L6P_T0U_N10_AD6P_46	AJ28

PL_DDR4_DQ34	IO_L2N_T0L_N3_46	AM27
PL_DDR4_DQ35	IO_L6N_T0U_N11_AD6N_46	AK28
PL_DDR4_DQ36	IO_L5P_T0U_N8_AD14P_46	AH27
PL_DDR4_DQ37	IO_L5N_T0U_N9_AD14N_46	AH28
PL_DDR4_DQ38	IO_L3P_T0L_N4_AD15P_46	AK26
PL_DDR4_DQ39	IO_L3N_T0L_N5_AD15N_46	AK27
PL_DDR4_DQ40	IO_L9N_T1L_N5_AD12N_46	AN28
PL_DDR4_DQ41	IO_L12N_T1U_N11_GC_46	AM30
PL_DDR4_DQ42	IO_L8P_T1L_N2_AD5P_46	AP28
PL_DDR4_DQ43	IO_L11N_T1U_N9_GC_46	AM29
PL_DDR4_DQ44	IO_L9P_T1L_N4_AD12P_46	AN27
PL_DDR4_DQ45	IO_L12P_T1U_N10_GC_46	AL30
PL_DDR4_DQ46	IO_L11P_T1U_N8_GC_46	AL29
PL_DDR4_DQ47	IO_L8N_T1L_N3_AD5N_46	AP29
PL_DDR4_DQ48	IO_L14P_T2L_N2_GC_46	AK31
PL_DDR4_DQ49	IO_L18P_T2U_N10_AD2P_46	AH34
PL_DDR4_DQ50	IO_L14N_T2L_N3_GC_46	AK32
PL_DDR4_DQ51	IO_L15N_T2L_N5_AD11N_46	AJ31
PL_DDR4_DQ52	IO_L15P_T2L_N4_AD11P_46	AJ30
PL_DDR4_DQ53	IO_L17P_T2U_N8_AD10P_46	AH31
PL_DDR4_DQ54	IO_L18N_T2U_N11_AD2N_46	AJ34
PL_DDR4_DQ55	IO_L17N_T2U_N9_AD10N_46	AH32
PL_DDR4_DQ56	IO_L21P_T3L_N4_AD8P_46	AN31
PL_DDR4_DQ57	IO_L24P_T3U_N10_46	AL34
PL_DDR4_DQ58	IO_L23N_T3U_N9_46	AN32
PL_DDR4_DQ59	IO_L20P_T3L_N2_AD1P_46	AN33
PL_DDR4_DQ60	IO_L23P_T3U_N8_46	AM32
PL_DDR4_DQ61	IO_L24N_T3U_N11_46	AM34
PL_DDR4_DQ62	IO_L21N_T3L_N5_AD8N_46	AP31
PL_DDR4_DQ63	IO_L20N_T3L_N3_AD1N_46	AP33
PL_DDR4_DM0	IO_L1P_T0L_N0_DBC_44	AD21
PL_DDR4_DM1	IO_L7P_T1L_N0_QBC_AD13P_44	AE25
PL_DDR4_DM2	IO_L13P_T2L_N0_GC_QBC_44	AJ21
PL_DDR4_DM3	IO_L19P_T3L_N0_DBC_AD9P_44	AM21
PL_DDR4_DM4	IO_L1P_T0L_N0_DBC_46	AH26
PL_DDR4_DM5	IO_L7P_T1L_N0_QBC_AD13P_46	AN26

PL_DDR4_DM6	IO_L13P_T2L_N0_GC_QBC_46	AJ29
PL_DDR4_DM7	IO_L19P_T3L_N0_DBC_AD9P_46	AL32
PL_DDR4_DQS0_P	IO_L4P_T0U_N6_DBC_AD7P_44	AG21
PL_DDR4_DQS0_N	IO_L4N_T0U_N7_DBC_AD7N_44	AH21
PL_DDR4_DQS1_P	IO_L10P_T1U_N6_QBC_AD4P_44	AH24
PL_DDR4_DQS1_N	IO_L10N_T1U_N7_QBC_AD4N_44	AJ25
PL_DDR4_DQS2_P	IO_L16P_T2U_N6_QBC_AD3P_44	AJ20
PL_DDR4_DQS2_N	IO_L16N_T2U_N7_QBC_AD3N_44	AK20
PL_DDR4_DQS3_P	IO_L22P_T3U_N6_DBC_AD0P_44	AP20
PL_DDR4_DQS3_N	IO_L22N_T3U_N7_DBC_AD0N_44	AP21
PL_DDR4_DQS4_P	IO_L4P_T0U_N6_DBC_AD7P_46	AL27
PL_DDR4_DQS4_N	IO_L4N_T0U_N7_DBC_AD7N_46	AL28
PL_DDR4_DQS5_P	IO_L10P_T1U_N6_QBC_AD4P_46	AN29
PL_DDR4_DQS5_N	IO_L10N_T1U_N7_QBC_AD4N_46	AP30
PL_DDR4_DQS6_P	IO_L16P_T2U_N6_QBC_AD3P_46	AH33
PL_DDR4_DQS6_N	IO_L16N_T2U_N7_QBC_AD3N_46	AJ33
PL_DDR4_DQS7_P	IO_L22P_T3U_N6_DBC_AD0P_46	AN34
PL_DDR4_DQS7_N	IO_L22N_T3U_N7_DBC_AD0N_46	AP34
PL_DDR4_A0	IO_L18N_T2U_N11_AD2N_45	AG14
PL_DDR4_A1	IO_L23N_T3U_N9_45	AF17
PL_DDR4_A2	IO_L20P_T3L_N2_AD1P_45	AF15
PL_DDR4_A3	IO_L16N_T2U_N7_QBC_AD3N_45	AJ14
PL_DDR4_A4	IO_L19N_T3L_N1_DBC_AD9N_45	AD18
PL_DDR4_A5	IO_L15P_T2L_N4_AD11P_45	AG17
PL_DDR4_A6	IO_L23P_T3U_N8_45	AE17
PL_DDR4_A7	IO_L11N_T1U_N9_GC_45	AK18
PL_DDR4_A8	IO_L24P_T3U_N10_45	AD16
PL_DDR4_A9	IO_L13P_T2L_N0_GC_QBC_45	AH18
PL_DDR4_A10	IO_L19P_T3L_N0_DBC_AD9P_45	AD19
PL_DDR4_A11	IO_L24N_T3U_N11_45	AD15
PL_DDR4_A12	IO_L14P_T2L_N2_GC_45	AH16
PL_DDR4_A13	IO_L10N_T1U_N7_QBC_AD4N_45	AL17
PL_DDR4_BA0	IO_L18P_T2U_N10_AD2P_45	AG15
PL_DDR4_BA1	IO_L10P_T1U_N6_QBC_AD4P_45	AL18
PL_DDR4_BG0	IO_L16P_T2U_N6_QBC_AD3P_45	AJ15
PL_DDR4_WE_B	IO_L9N_T1L_N5_AD12N_45	AL15

PL_DDR4_RAS_B	IO_L8N_T1L_N3_AD5N_45	AM19
PL_DDR4_CAS_B	IO_L8P_T1L_N2_AD5P_45	AL19
PL_DDR4_CKE	IO_L14N_T2L_N3_GC_45	AJ16
PL_DDR4_ACT_B	IO_L21N_T3L_N5_AD8N_45	AF18
PL_DDR4_CLK_N	IO_L22N_T3U_N7_DBC_AD0N_45	AE15
PL_DDR4_CLK_P	IO_L22P_T3U_N6_DBC_AD0P_45	AE16
PL_DDR4_CS_B	IO_L21P_T3L_N4_AD8P_45	AE18
PL_DDR4_OTD	IO_L17P_T2U_N8_AD10P_45	AG19
PL_DDR4_PAR	IO_L20N_T3L_N3_AD1N_45	AF14
PL_DDR4_RST	IO_L15N_T2L_N5_AD11N_45	AG16

Part 4: QSPI Flash

The AXKU040 FPGA development board is equipped with one 128MBit Quad-SPI FLASH, and the model is N25Q128A, which uses the 3.3V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, it can store FPGA configuration Bin files and other user data files in use. The specific models and related parameters of QSPI FLASH are shown in Table 4-1.

Position	Model	Capacity	Factory
U14	N25Q128A	128M Bit	Numonyx

Table 4-1: QSPI FLASH Specification

QSPI FLASH is connected to the dedicated pins of BANK0 of the FPGA chip. The clock pin is connected to CCLK0 of BANK0, and other data signals are connected to D00~D03 and FCS pins. Figure 4-2 shows the hardware connection of QSPI Flash and FPGA Chip.

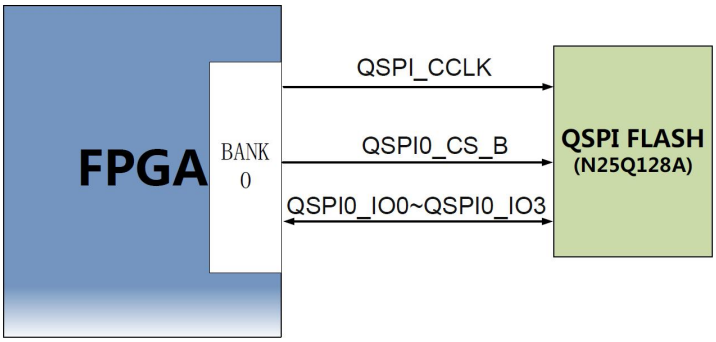

Figure 4-2: QSPI Flash Schematic

QSPI Flash pin assignments:

Signal Name	FPGA Pin Name	FPGA Pin Number
QSPI_CCLK	CCLK_0	AA9
QSPI0_CS_B	RDWR_FCS_B_0	U7
QSPI0_IO0	D00_MOSI_0	AC7
QSPI0_IO1	D01_DIN_0	AB7
QSPI0_IO2	D02_0	AA7
QSPI0_IO3	D03_0	Y7

Part 5: Clock configuration

Part 5.1: 200Mhz differential clock source

A differential 200MHz clock source is provided on the FPGA development board to provide the system clock to the FPGA. The crystal differential output is connected to the FPGA BANK45, which can be used to drive the DDR controller operating clock and other user logic in the FPGA. The schematic diagram of the clock source is shown in Figure 5-1.

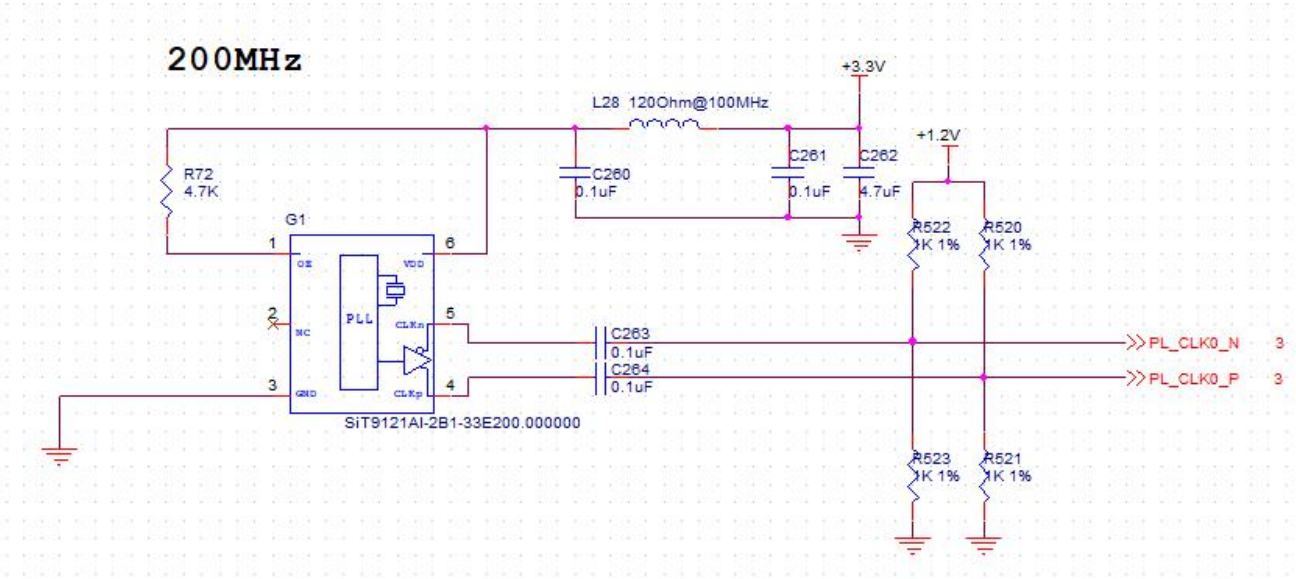

Figure 5-1: 200Mhz System Clock Source Schematic

System Clock pin assignments:

Signal Name	FPGA Pin
SYS_CLK0_P	AK17
SYS_CLK0_N	AK16

Part 5.2: 125Mhz differential clock source

A differential 125MHz clock source is provided on the FPGA development board to provide the clock for transceiver GTH. The crystal differential output is connected to the FPGA BANK224, which can be used for the clock required by 4 optical fibers. The schematic diagram of the clock source is shown in Figure

5-2.

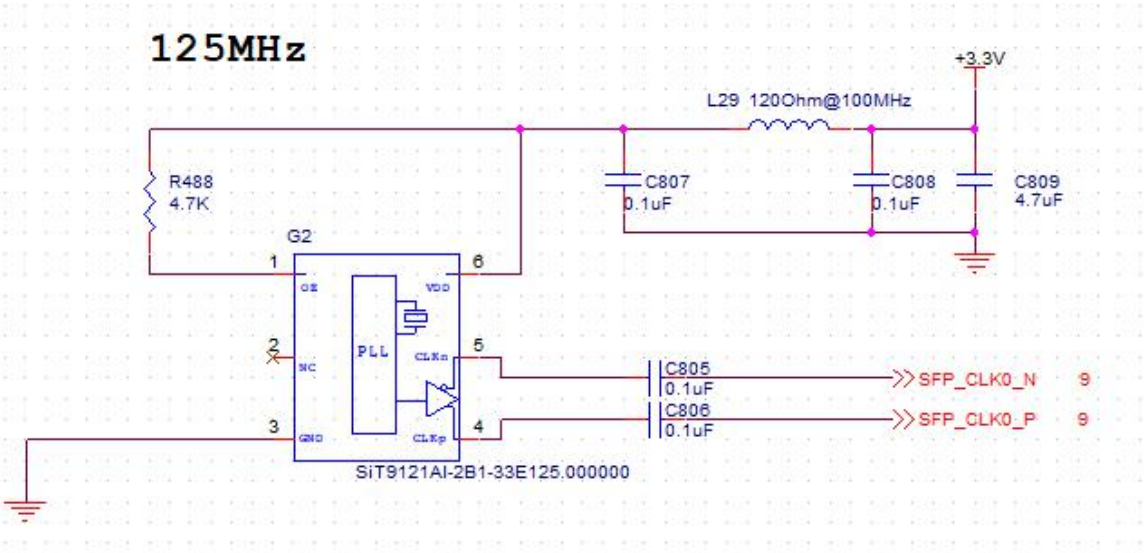

Figure 5-2: 125Mhz System Clock Source Schematic

System Clock pin assignments:

Signal Name	FPGA Pin
SFP_CLK0_P	AF6
SFP_CLK0_N	AF5

Part 5.3: 156.25Mhz differential clock source

A differential 156.25MHz clock source is provided on the FPGA development board to provide the clock to the FPGA Transceiver GTH. The crystal differential output is connected to the FPGA BANK228. The schematic diagram of the clock source is shown in Figure 5-3.

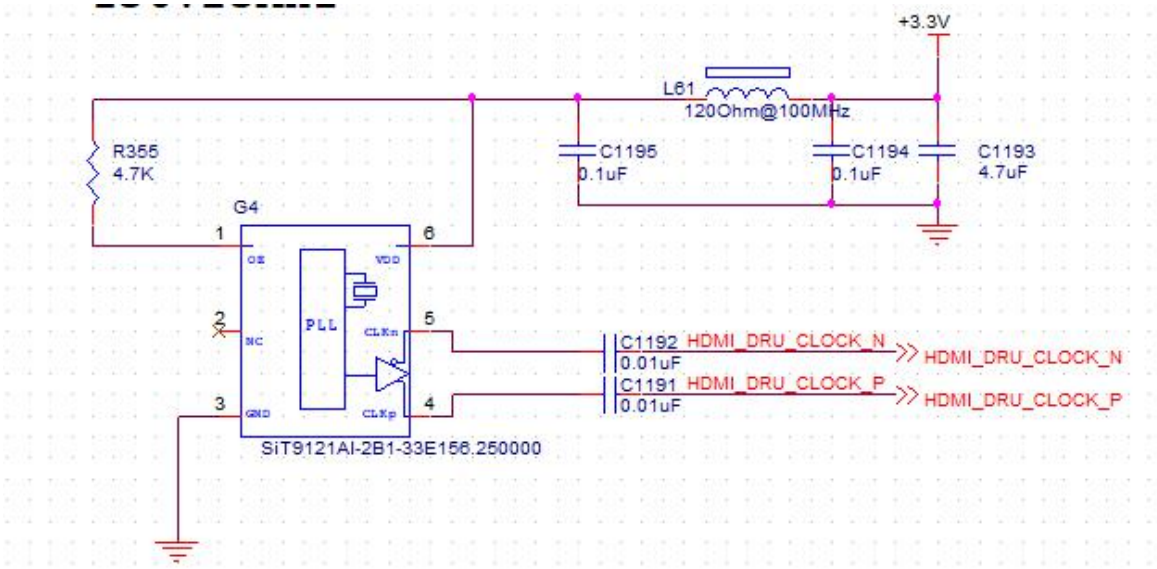

Figure 5-1: 156.25Mhz System Clock Source Schematic

System Clock pin assignments:

Signal Name	FPGA Pin
HDMI_DRU_CLOCK_P	H6
HDMI_DRU_CLOCK_N	H5

Part 6: USB to Serial Port

The AXKU040 FPGA development board is equipped with a Uart to USB interface for serial communication and debugging of the development board. The conversion chip uses the USB-UAR chip of Silicon Labs CP2102GM. The CP2102 serial chip and the FPGA are connected by a level-shifting chip to adapt to different FPGA BANK voltages. The USB interface uses the MINI USB interface, which can be connected to the USB port of the upper PC for serial data communication on the FPGA development board with a USB cable. The schematic diagram of the USB Uart circuit design is shown below:

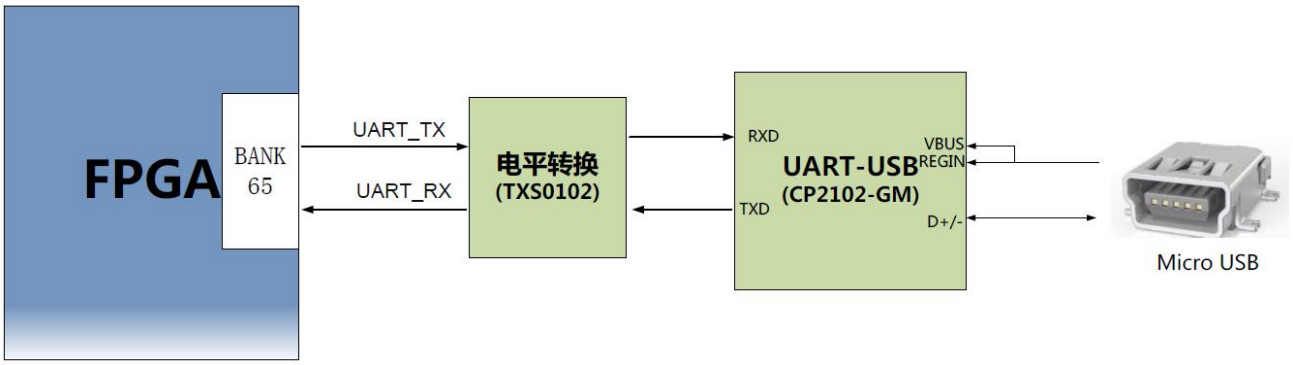

Figure 6-1: USB to serial port schematic

USB to serial port pin assignment:

Signal Name	FPGA Pin Name	FPGA Pin Number	Description
UART_RX	IO_T2U_N12_CSI_ADV_B_65	N27	Uart Data Input
UART_TX	IO_T3U_N12_PERSTN0_65	K22	Uart Data Output

Part 7: SFP+ Optical fiber interface

The AXKU040 FPGA development board has a four SFP interface. The Users can buy SFP optical modules (1.25G, 2.5G, 10G optical modules on the market) and insert them into these 4 optical fiber interfaces for optical fiber data communication. The 4 optical fiber interfaces are respectively connected with 4 RX/TX of FPGA BANK24 GTH transceiver. Both the TX signal and the RX signal are connected to the FPGA and the optical module through a DC blocking capacitor in a differential signal mode, and the data rate of each TX transmission and RX reception is as high as 12.5Gb/s. The reference clock of the GXH transceiver of BANK224 is provided by a differential crystal oscillator 125M.

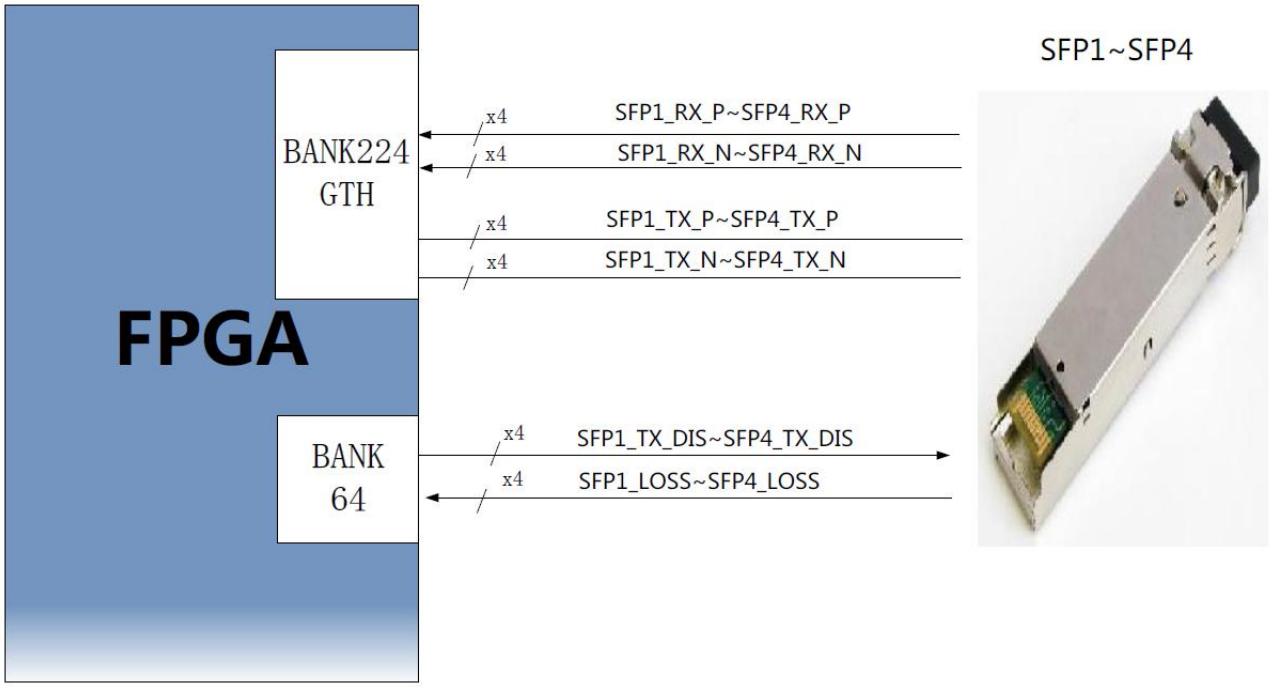

Figure 7-1: SFP Fiber Design Diagram

The 1st fiber interface FPGA pin assignment is as follows:

Signal Name	FPGA PIN	Description
SFP1_TX_P	AN4	SFP1 Data Transmission (Positive)
SFP1_TX_N	AN3	SFP1 Data Transmission (Negative)

SFP1_RX_P	AP2	SFP1 Data Receiver (Positive)
SFP1_RX_P	AP1	SFP1 Data Receiver (Negative)
SFP1_TX_DIS	AM10	SFP1 Optical Transfer Disable, active high
SFP1_LOSS	AK11	SFP1 Optical LOSS,High level means no light signal is received

The 2nd fiber interface FPGA pin assignment is as follows:

Signal Name	FPGA PIN	Description
SFP2_TX_P	AM6	SFP2 Data Transmission (Positive)
SFP2_TX_N	AM5	SFP2 Data Transmission (Negative)
SFP2_RX_P	AM2	SFP2 Data Receiver (Positive)
SFP2_RX_N	AM1	SFP2 Data Receiver (Negative)
SFP2_TX_DIS	AL10	SFP2Optical Transfer Disable, active high
SFP2_LOSS	AJ11	SFP2 Optical LOSS,High level means no light signal is received

The 3rd fiber interface FPGA pin assignment is as follows:

Signal Name	FPGA PIN	Description
SFP3_TX_P	AL4	SFP3 Data Transmission (Positive)
SFP3_TX_N	AL3	SFP3 Data Transmission (Negative)
SFP3_RX_P	AK2	SFP3 Data Receiver (Positive)
SFP3_RX_N	AK1	SFP3 Data Receiver (Negative)
SFP3_TX_DIS	AP9	SFP3 Optical Transfer Disable, active high
SFP3_LOSS	AJ10	SFP3 Optical LOSS,High level means no light signal is received

The 4th fiber interface FPGA pin assignment is as follows:

Signal Name	FPGA PIN	Description
SFP4_TX_P	AK6	SFP4 Data Transmission (Positive)
SFP4_TX_N	AK5	SFP4 Data Transmission (Negative)
SFP4_RX_P	AJ4	SFP4 Data Receiver (Positive)
SFP4_RX_P	AJ3	SFP4 Data Receiver (Negative)
SFP4_TX_DIS	AN9	SFP4 Optical Transfer Disable, active high
SFP4_LOSS	AM9	SFP4 Optical LOSS,High level means no light signal is received

Part 8: HDMI Video Output Interface

The HDMI output interface uses the ADV7511 HDMI (DVI) encoding chip from ANALOG DEVICE, which supports up to 1080P@60Hz output and 3D output.

The video digital interface, audio digital interface and I2C configuration interface of ADV7511 are connected to the IO of BANK47 and BANK48.

The hardware connection diagram of ADV7511 chip and XCKU040 is shown in Figure 8-1:

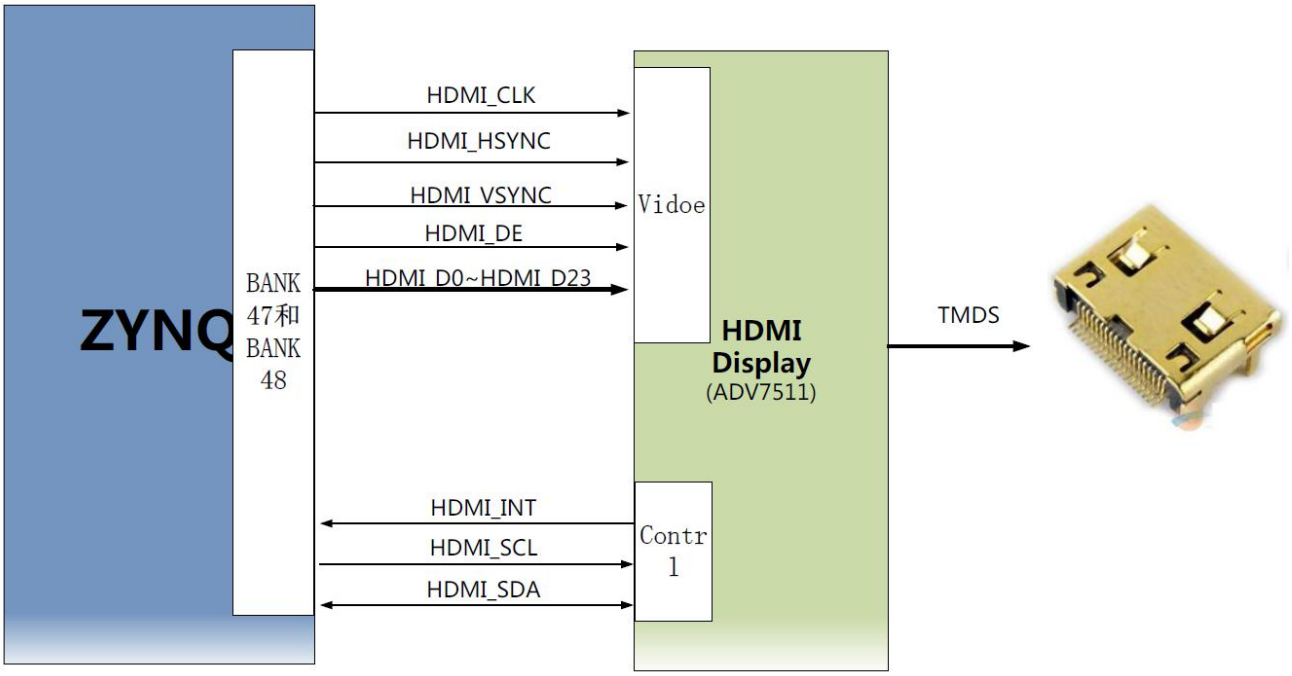

Figure 8-1: HDMI Output Interface Schematic

ADV7511 pin assignment:

Signal Name	Pin Name	Pin Number	Description
HDMI_CLK	IO_L21P_T3L_N4_AD8P_48	V33	HDMI Video Signal Clock
HDMI_HSYNC	IO_L21N_T3L_N5_AD8N_47	Y28	HDMI Video Signal Line Synchronization
HDMI_VSYNC	IO_T1U_N12_48	AE31	HDMI Video Signal Column Synchronization
HDMI_DE	IO_T2U_N12_48	AA33	HDMI Video Signal Enable

HDMI_D0	IO_L20N_T3L_N3_AD1N_48	Y30	HDMI Video Signal Data 0
HDMI_D1	IO_L19N_T3L_N1_DBC_AD9N_48	Y33	HDMI Video Signal Data 1
HDMI_D2	IO_L22N_T3U_N7_DBC_AD0N_48	Y32	HDMI Video Signal Data 2
HDMI_D3	IO_L19P_T3L_N0_DBC_AD9P_48	W33	HDMI Video Signal Data 3
HDMI_D4	IO_L21N_T3L_N5_AD8N_48	W34	HDMI Video Signal Data 4
HDMI_D5	IO_L24N_T3U_N11_48	W31	HDMI Video Signal Data 5
HDMI_D6	IO_L22P_T3U_N6_DBC_AD0P_48	Y31	HDMI Video Signal Data 6
HDMI_D7	IO_L23N_T3U_N9_48	V34	HDMI Video Signal Data 7
HDMI_D8	IO_T3U_N12_48	V32	HDMI Video Signal Data 8
HDMI_D9	IO_L23P_T3U_N8_48	U34	HDMI Video Signal Data 9
HDMI_D10	IO_L24P_T3U_N10_48	V31	HDMI Video Signal Data 10
HDMI_D11	IO_L20P_T3L_N2_AD1P_48	W30	HDMI Video Signal Data 11
HDMI_D12	IO_L23N_T3U_N9_47	W29	HDMI Video Signal Data 12
HDMI_D13	IO_L23P_T3U_N8_47	V29	HDMI Video Signal Data 13
HDMI_D14	IO_L21P_T3L_N4_AD8P_47	W28	HDMI Video Signal Data 14
HDMI_D15	IO_L19N_T3L_N1_DBC_AD9N_47	V28	HDMI Video Signal Data 15
HDMI_D16	IO_L19P_T3L_N0_DBC_AD9P_47	V27	HDMI Video Signal Data 16
HDMI_D17	IO_L24N_T3U_N11_47	W26	HDMI Video Signal Data 17
HDMI_D18	IO_L24P_T3U_N10_47	V26	HDMI Video Signal Data 18
HDMI_D19	IO_L22N_T3U_N7_DBC_AD0N_47	U27	HDMI Video Signal Data 19
HDMI_D20	IO_L22P_T3U_N6_DBC_AD0P_47	U26	HDMI Video Signal Data 20
HDMI_D21	IO_L20N_T3L_N3_AD1N_47	U25	HDMI Video Signal Data 21
HDMI_D22	IO_L20P_T3L_N2_AD1P_47	U24	HDMI Video Signal Data 22
HDMI_D23	IO_T1U_N12_47	Y22	HDMI Video Signal Data 23
HDMI_SCL	IO_L21N_T3L_N5_AD8N_D07_65	R22	HDMI IIC Control Clock
HDMI _SDA	IO_L21P_T3L_N4_AD8P_D06_65	R21	HDMI IIC Control Data

Part 9: Gigabit Ethernet Interface

There are 2 Gigabit Ethernet ports on the AXKU040 FPGA Development board. The GPHY chip uses Micrel's KSZ9031RNX Ethernet PHY chip to provide users with network communication services. The KSZ9031RNX chip supports 10/100/1000 Mbps network transmission rate, and communicates with the MAC layer of the system through the RGMII interface. KSZ9031RNX supports MDI/MDX adaptation, various speed adaptation, Master/Slave adaptation, and supports MDIO bus for PHY register management.

When the KSZ9031RNX is powered on, it will detect the level status of some specific IOs to determine its own operating mode. Table 3-5-1 describes the default settings after the GPHY chip is powered on.

Configuration Pin	Instructions	Configuration value
PHYAD[2:0]	MDIO/MDC Mode PHY Address	PHY Address 011
CLK125_EN	Enable 125Mhz clock output selection	Enable
LED_MODE	LED light mode configuration	Single LED light mode
MODE0~MODE3	Link adaptation and full duplex configuration	10/100/1000 adaptive, compatible with full-duplex, half-duplex

Table 9-1: PHY chip default configuration value

When the network is connected to Gigabit Ethernet, the data transmission of FPGA chip and PHY chip KSZ9031RNX is communicated through the RGMII bus, the transmission clock is 125Mhz, and the data is sampled on the rising edge and falling samples of the clock.

When the network is connected to 100M Ethernet, the data transmission of FPGA chip and PHY chip KSZ9031RNX is communicated through RMII bus, and the transmission clock is 25Mhz. Data is sampled on the rising edge and falling samples of the clock.

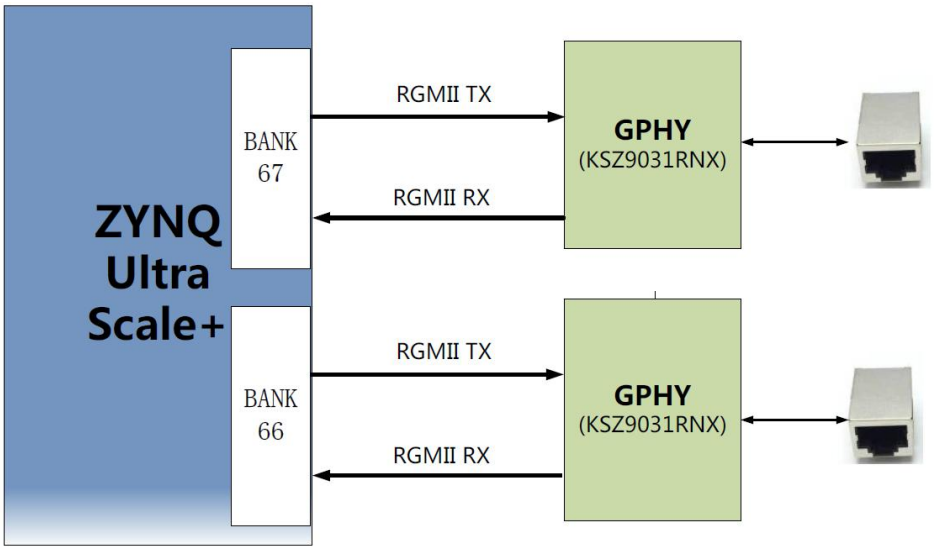

Figure 9-1: FPGA Chip and GPHY connection diagram

The 1st Gigabit Ethernet interface pin assignments are as follows:

Signal Name	Pin Name	Pin Number	Description
PHY1_GTXC	IO_L4N_T0U_N7_DBC_AD7N_66	A10	Ethernet 1 Transmit Clock
PHY1_TXD0	IO_L14N_T2L_N3_GC_66	G12	Ethernet 1 Transmit Data bit0
PHY1_TXD1	IO_L2P_T0L_N2_66	B9	Ethernet 1 Transmit Data bit1
PHY1_TXD2	IO_L2N_T0L_N3_66	A9	Ethernet 1 Transmit Data bit2
PHY1_TXD3	IO_L4P_T0U_N6_DBC_AD7P_66	B10	Ethernet 1 Transmit Data bit3
PHY1_TXEN	IO_L21N_T3L_N5_AD8N_66	B11	Ethernet 1 Transmit Enable Signal
PHY1_RXC	IO_L14P_T2L_N2_GC_66	H12	Ethernet 1 Receive Clock
PHY1_RXD0	IO_L23P_T3U_N8_66	A13	Ethernet 1 Receive Data Bit0
PHY1_RXD1	IO_L20N_T3L_N3_AD1N_66	B12	Ethernet 1 Receive Data Bit1
PHY1_RXD2	IO_L23N_T3U_N9_66	A12	Ethernet 1 Receive Data Bit2
PHY1_RXD3	IO_L21P_T3L_N4_AD8P_66	C11	Ethernet 1 Receive Data Bit3
PHY1_RXDV	IO_L20P_T3L_N2_AD1P_66	C12	Ethernet 1 Receive Data Enable Signal
PHY1_MDC	IO_T2U_N12_66	F12	Ethernet 1 MDIO Management Clock
PHY1_MDIO	IO_T3U_N12_66	E12	Ethernet 1 MDIO Management Data
PHY1_RESET	IO_T1U_N12_66	L9	Ethernet Chip Reset

The 2nd Gigabit Ethernet interface pin assignments are as follows:

Signal Name	Pin Name	Pin Number	Description
PHY2_GTXC	IO_L10P_T1U_N6_QBC_AD4P_67	B24	Ethernet 2 Transmit Clock
PHY2_TXD0	IO_L17P_T2U_N8_AD10P_67	B20	Ethernet 2 Transmit Data bit0
PHY2_TXD1	IO_L17N_T2U_N9_AD10N_67	A20	Ethernet 2 Transmit Data bit1
PHY2_TXD2	IO_L15P_T2L_N4_AD11P_67	B21	Ethernet 2 Transmit Data bit2
PHY2_TXD3	IO_L15N_T2L_N5_AD11N_67	B22	Ethernet 2 Transmit Data bit3
PHY2_TXEN	IO_L10N_T1U_N7_QBC_AD4N_67	A24	Ethernet 2 Transmit Enable Signal
PHY2_RXC	IO_L13P_T2L_N0_GC_QBC_67	D23	Ethernet 2 Receive Clock
PHY2_RXD0	IO_L4P_T0U_N6_DBC_AD7P_67	B29	Ethernet 2 Receive Data Bit0
PHY2_RXD1	IO_L6N_T0U_N11_AD6N_67	A28	Ethernet 2 Receive Data Bit1
PHY2_RXD2	IO_L6P_T0U_N10_AD6P_67	A27	Ethernet 2 Receive Data Bit2
PHY2_RXD3	IO_L13N_T2L_N1_GC_QBC_67	C23	Ethernet 2 Receive Data Bit3
PHY2_RXDV	IO_L4N_T0U_N7_DBC_AD7N_67	A29	Ethernet 2 Receive Data Enable Signal
PHY2_MDC	IO_T1U_N12_67	A23	Ethernet 2 MDIO Management Clock
PHY2_MDIO	IO_T2U_N12_67	A22	Ethernet 2 MDIO Management Data
PHY2_RESET	IO_T3U_N12_67	H22	Ethernet Chip Reset

Part 10: FMC Expansion Port

The AXKU040 FPGA development board comes with two standard FMC LPC expansion ports and one standard FMC HPC expansion ports that can be connected to various FMC modules of XILINX or ALINX (HDMI input and output modules, binocular camera modules, high-speed AD modules, etc.). The FMC expansion port contains 33 pairs of differential IO signals and one I2C bus signal.

The LPC FMC1 expansion port has 33 pairs of differential signals, which are respectively connected to the IO of BANK47 and BANK48 of the FPGA chip. The IO level of BANK47 and BANK48 is 1.8V and cannot be modified. The 1 pair speed GTH transceiver signal is connected to BNAK226.

The LPC FMC2 expansion port has 33 pairs of differential signals, which are respectively connected to the IO of the BANK64 and BANK65 of the FPGA chip. The level standard is determined by the voltage VADJ of the BANK, and the default is +1.8V. The voltage of VADJ can be configured by the program to change the output voltage of the PMIC chip LP873220. The 1 pair speed GTH transceiver signal is connected to BNAK226.

The FMC HPC expansion port contains 57 pairs of differential IO signals, which are connected to FPGA chips BANK66, BANK67, BANK68, and the voltage standard is 1.8V. 8 high-speed GTH transceiver signals are connected to the IO of the FPGA chip BANK227 and BANK228.

The schematic diagrams of FPGA and FMC LPC connectors are shown in Figures 10-1 and 10-2:

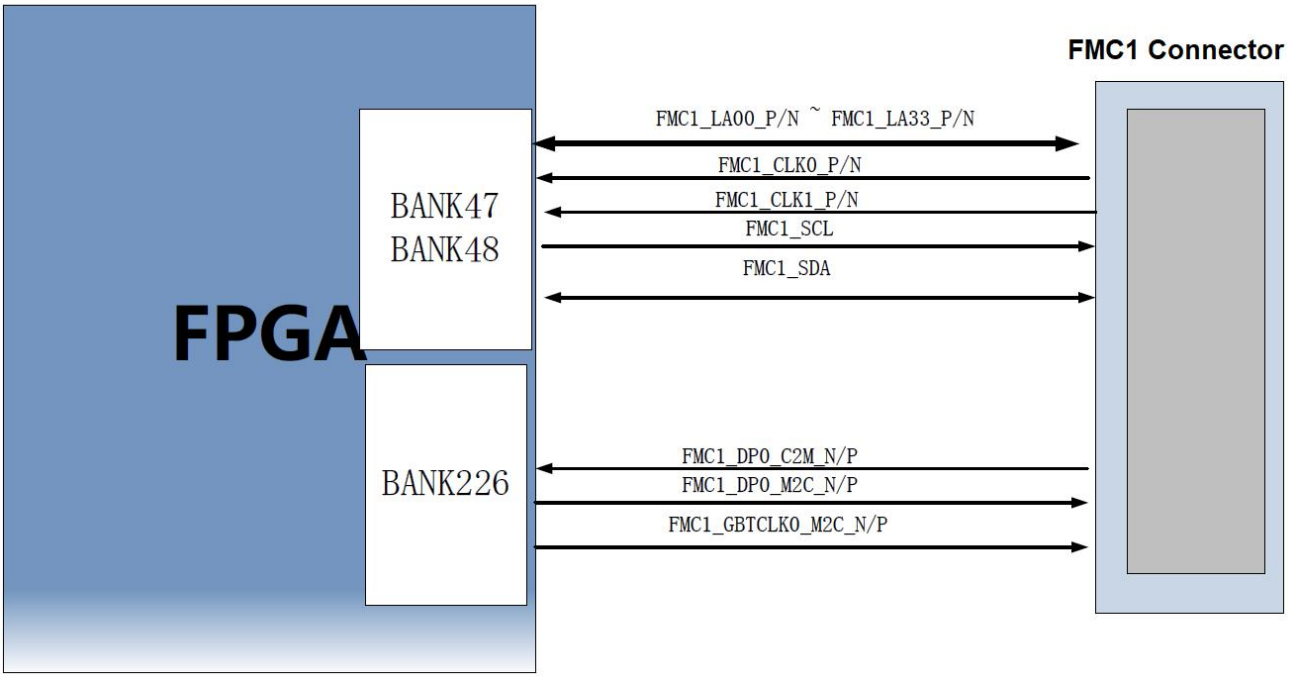

Figure 10-1：LPC FMC1 Connector Diagram

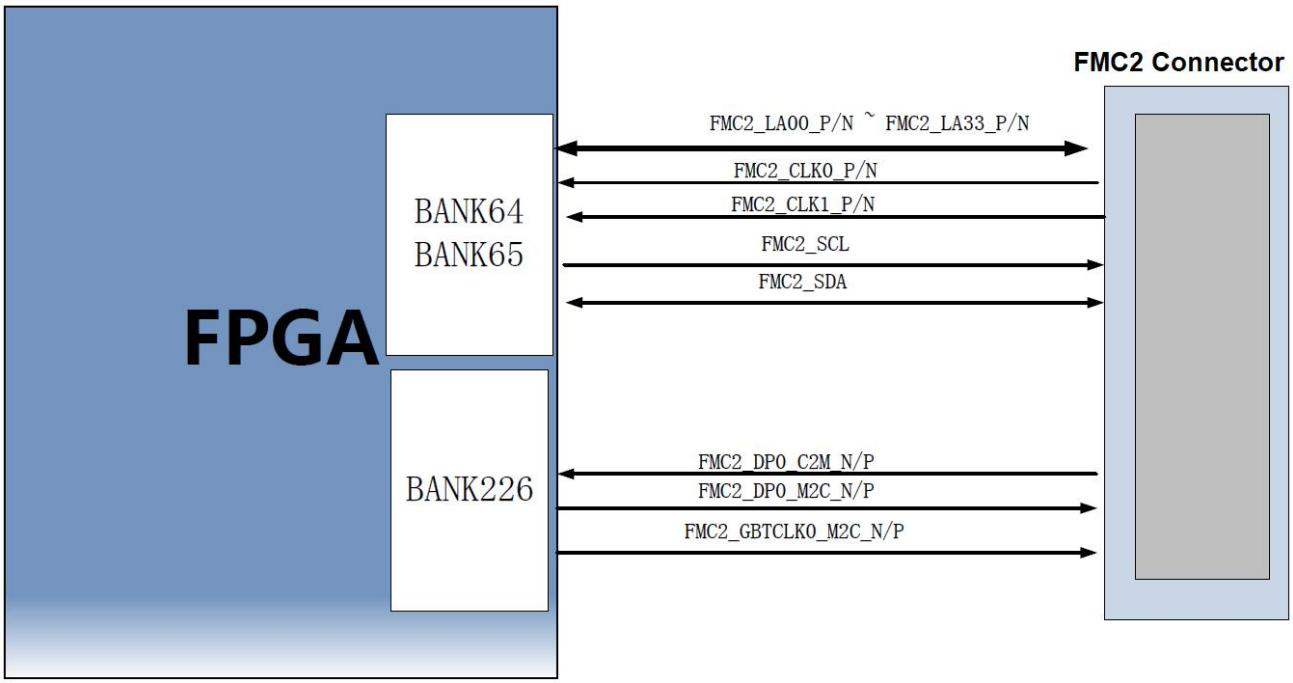

Figure 10-2：LPC FMC2 Connector Diagram

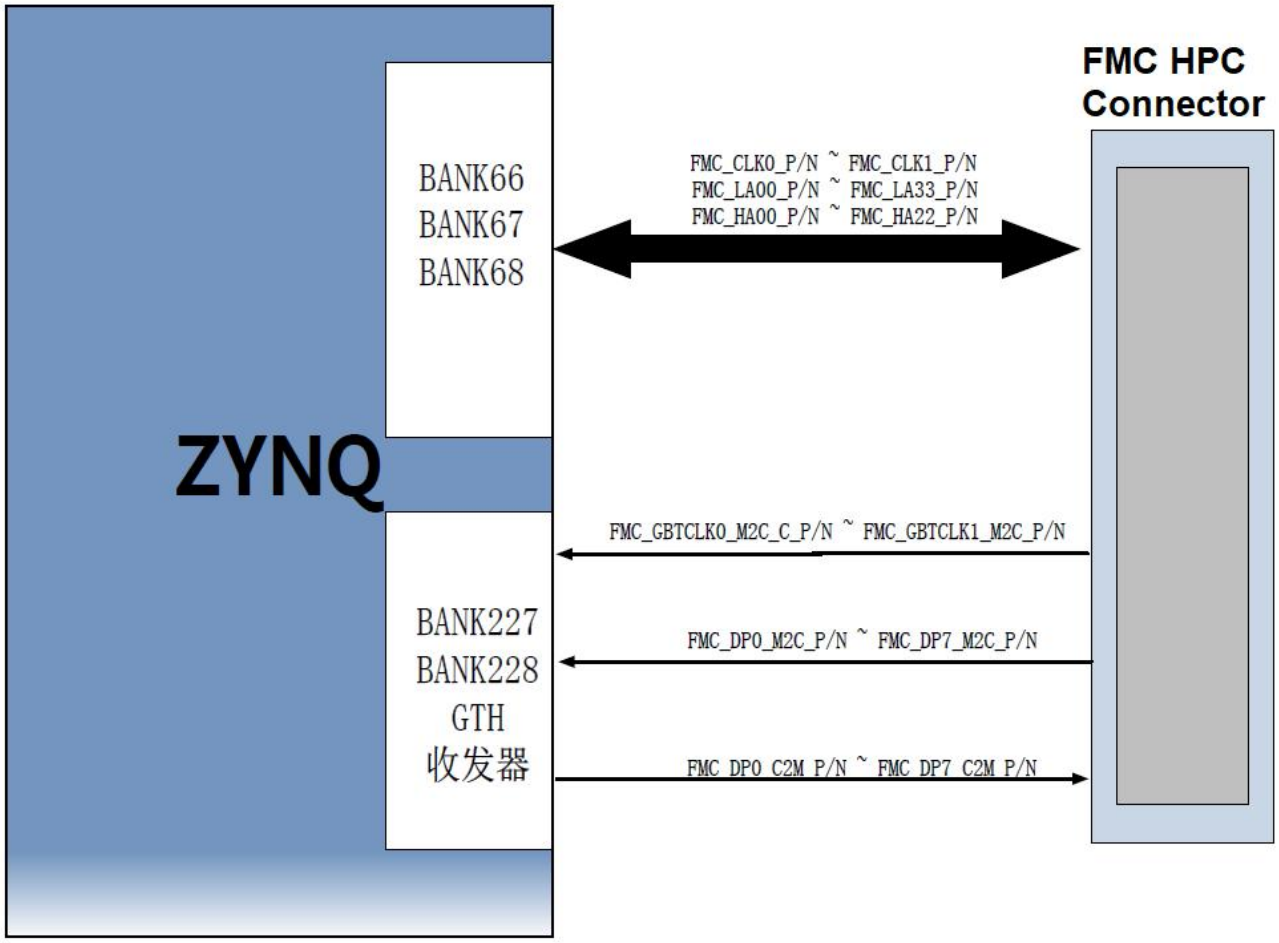

Figure 10-3：LPC FMC3 Connector Diagram

The 1st FMC LPC Connectors Pin Assignment

Signal Name	FPGA Pin Number	FPGA Pin Name	Description
FMC1_LPC_CLK0_P	IO_L11P_T1U_N8_GC_47	Y23	FMC Reference 1st Reference Clock P
FMC1_LPC_CLK0_N	IO_L11N_T1U_N9_GC_47	AA23	FMC Reference 1st Reference Clock N
FMC1_LPC_CLK1_P	IO_L11P_T1U_N8_GC_48	AD30	FMC Reference 2nd Reference Clock P
FMC1_LPC_CLK1_N	IO_L11N_T1U_N9_GC_48	AD31	FMC Reference 2nd Reference Clock N
FMC1_LPC_LA00_CC_P	IO_L12P_T1U_N10_GC_47	AA24	FMC Reference 0th Data (Clock) P
FMC1_LPC_LA00_CC_N	IO_L12N_T1U_N11_GC_47	AA25	FMC Reference 0th Data

			(Clock) N
FMC1_LPC_LA01_CC_P	IO_L13P_T2L_N0_GC_QBC_47	W23	FMC Reference 1st Data (Clock) P
FMC1_LPC_LA01_CC_N	IO_L13N_T2L_N1_GC_QBC_47	W24	FMC Reference 1st Data (Clock) N
FMC1_LPC_LA02_P	IO_L10P_T1U_N6_QBC_AD4P_47	AB21	FMC Reference 2nd Data P
FMC1_LPC_LA02_N	IO_L10N_T1U_N7_QBC_AD4N_47	AC21	FMC Reference 2nd Data N
FMC1_LPC_LA03_P	IO_L8P_T1L_N2_AD5P_47	AC22	FMC Reference 3rd Data P
FMC1_LPC_LA03_N	IO_L8N_T1L_N3_AD5N_47	AC23	FMC Reference 3rd Data N
FMC1_LPC_LA04_P	IO_L7P_T1L_N0_QBC_AD13P_47	AA22	FMC Reference 4th Data P
FMC1_LPC_LA04_N	IO_L7N_T1L_N1_QBC_AD13N_47	AB22	FMC Reference 4th Data N
FMC1_LPC_LA05_P	IO_L2P_T0L_N2_47	AD25	FMC Reference 5th Data P
FMC1_LPC_LA05_N	IO_L2N_T0L_N3_47	AD26	FMC Reference 5th Data N
FMC1_LPC_LA06_P	IO_L3P_T0L_N4_AD15P_47	AB24	FMC Reference 6th Data P
FMC1_LPC_LA06_N	IO_L3N_T0L_N5_AD15N_47	AC24	FMC Reference 6th Data N
FMC1_LPC_LA07_P	IO_L6P_T0U_N10_AD6P_47	AB25	FMC Reference 7th Data P
FMC1_LPC_LA07_N	IO_L6N_T0U_N11_AD6N_47	AB26	FMC Reference 7th Data N
FMC1_LPC_LA08_P	IO_L4P_T0U_N6_DBC_AD7P_47	AC26	FMC Reference 8th Data P
FMC1_LPC_LA08_N	IO_L4N_T0U_N7_DBC_AD7N_47	AC27	FMC Reference 8th Data N
FMC1_LPC_LA09_P	IO_L1P_T0L_N0_DBC_47	Y26	FMC Reference 9th Data P
FMC1_LPC_LA09_N	IO_L1N_T0L_N1_DBC_47	Y27	FMC Reference 9th Data N

FMC1_LPC_LA10_P	IO_L5P_T0U_N8_AD14P_47	AA27	FMC Reference 10th Data P
FMC1_LPC_LA10_N	IO_L5N_T0U_N9_AD14N_47	AB27	FMC Reference 10th Data N
FMC1_LPC_LA11_P	IO_L18P_T2U_N10_AD2P_47	V21	FMC Reference 11th Data P
FMC1_LPC_LA11_N	IO_L18N_T2U_N11_AD2N_47	W21	FMC Reference 11th Data N
FMC1_LPC_LA12_P	IO_L9P_T1L_N4_AD12P_47	AA20	FMC Reference 12th Data P
FMC1_LPC_LA12_N	IO_L9N_T1L_N5_AD12N_47	AB20	FMC Reference 12th Data N
FMC1_LPC_LA13_P	IO_L14P_T2L_N2_GC_47	W25	FMC Reference 13th Data P
FMC1_LPC_LA13_N	IO_L14N_T2L_N3_GC_47	Y25	FMC Reference 13th Data N
FMC1_LPC_LA14_P	IO_L16P_T2U_N6_QBC_AD3P_47	V22	FMC Reference 14th Data P
FMC1_LPC_LA14_N	IO_L16N_T2U_N7_QBC_AD3N_47	V23	FMC Reference 14th Data N
FMC1_LPC_LA15_P	IO_L17P_T2U_N8_AD10P_47	T22	FMC Reference 15th Data P
FMC1_LPC_LA15_N	IO_L17N_T2U_N9_AD10N_47	T23	FMC Reference 15th Data N
FMC1_LPC_LA16_P	IO_L15P_T2L_N4_AD11P_47	U21	FMC Reference 16th Data P
FMC1_LPC_LA16_N	IO_L15N_T2L_N5_AD11N_47	U22	FMC Reference 16th Data N
FMC1_LPC_LA17_CC_P	IO_L12P_T1U_N10_GC_48	AC31	FMC Reference 17th Data (Clock) P
FMC1_LPC_LA17_CC_N	IO_L12N_T1U_N11_GC_48	AC32	FMC Reference 17th Data (Clock) N
FMC1_LPC_LA18_CC_P	IO_L13P_T2L_N0_GC_QBC_48	AA32	FMC Reference 18th Data (Clock) P
FMC1_LPC_LA18_CC_N	IO_L13N_T2L_N1_GC_QBC_48	AB32	FMC Reference 18th Data (Clock) N
FMC1_LPC_LA19_P	IO_L7P_T1L_N0_QBC_AD13P_48	AG31	FMC Reference 19th

			Data P
FMC1_LPC_LA19_N	IO_L7N_T1L_N1_QBC_AD13N_48	AG32	FMC Reference 19th Data N
FMC1_LPC_LA20_P	IO_L6P_T0U_N10_AD6P_48	AF30	FMC Reference 20th Data P
FMC1_LPC_LA20_N	IO_L6N_T0U_N11_AD6N_48	AG30	FMC Reference 20th Data N
FMC1_LPC_LA21_P	IO_L10P_T1U_N6_QBC_AD4P_48	AE33	FMC Reference 21st Data P
FMC1_LPC_LA21_N	IO_L10N_T1U_N7_QBC_AD4N_48	AF34	FMC Reference 21st Data N
FMC1_LPC_LA22_P	IO_L8P_T1L_N2_AD5P_48	AF33	FMC Reference 22nd Data P
FMC1_LPC_LA22_N	IO_L8N_T1L_N3_AD5N_48	AG34	FMC Reference 22nd Data N
FMC1_LPC_LA23_P	IO_L4P_T0U_N6_DBC_AD7P_48	AF29	FMC Reference 23rd Data P
FMC1_LPC_LA23_N	IO_L4N_T0U_N7_DBC_AD7N_48	AG29	FMC Reference 23rd Data N
FMC1_LPC_LA24_P	IO_L15P_T2L_N4_AD11P_48	AC34	FMC Reference 24th Data P
FMC1_LPC_LA24_N	IO_L15N_T2L_N5_AD11N_48	AD34	FMC Reference 24th Data N
FMC1_LPC_LA25_P	IO_L9P_T1L_N4_AD12P_48	AE32	FMC Reference 25th Data P
FMC1_LPC_LA25_N	IO_L9N_T1L_N5_AD12N_48	AF32	FMC Reference 25th Data N
FMC1_LPC_LA26_P	IO_L16P_T2U_N6_QBC_AD3P_48	AA29	FMC Reference 26th Data P
FMC1_LPC_LA26_N	IO_L16N_T2U_N7_QBC_AD3N_48	AB29	FMC Reference 26th Data N
FMC1_LPC_LA27_P	IO_L14P_T2L_N2_GC_48	AB30	FMC Reference 27th Data P
FMC1_LPC_LA27_N	IO_L14N_T2L_N3_GC_48	AB31	FMC Reference 27th Data N
FMC1_LPC_LA28_P	IO_L17P_T2U_N8_AD10P_48	AA34	FMC Reference 28th Data P

FMC1_LPC_LA28_N	IO_L17N_T2U_N9_AD10N_48	AB34	FMC Reference 28th Data N
FMC1_LPC_LA29_P	IO_L18P_T2U_N10_AD2P_48	AC33	FMC Reference 29th Data P
FMC1_LPC_LA29_N	IO_L18N_T2U_N11_AD2N_48	AD33	FMC Reference 29th Data N
FMC1_LPC_LA30_P	IO_L2P_T0L_N2_48	AE28	FMC Reference 30th Data P
FMC1_LPC_LA30_N	IO_L2N_T0L_N3_48	AF28	FMC Reference 30th Data N
FMC1_LPC_LA31_P	IO_L5P_T0U_N8_AD14P_48	AD29	FMC Reference 31st Data P
FMC1_LPC_LA31_N	IO_L5N_T0U_N9_AD14N_48	AE30	FMC Reference 31st Data N
FMC1_LPC_LA32_P	IO_L1P_T0L_N0_DBC_48	AE27	FMC Reference 32nd Data P
FMC1_LPC_LA32_N	IO_L1N_T0L_N1_DBC_48	AF27	FMC Reference 32nd Data N
FMC1_LPC_LA33_P	IO_L3P_T0L_N4_AD15P_48	AC28	FMC Reference 33rd Data P
FMC1_LPC_LA33_N	IO_L3N_T0L_N5_AD15N_48	AD28	FMC Reference 33rd Data N
FMC1_LPC_SCL	IO_T2U_N12_47	Y21	FMC I2C Bus Clock
FMC1_LPC_SDA	IO_T3U_N12_47	U29	FMC I2C Bus Data

The 2nd FMC LPC Connectors Pin Assignment

Signal Name	FPGA Pin Number	FPGA Pin Name	Description
FMC2_LPC_CLK0_P	IO_L11P_T1U_N8_GC_64	AG12	FMC Reference 1st Reference Clock P
FMC2_LPC_CLK0_N	IO_L11N_T1U_N9_GC_64	AH12	FMC Reference 1st Reference Clock N
FMC2_LPC_CLK1_P	IO_L13P_T2L_N0_GC_ QBC_A06_D22_65	P26	FMC Reference 2nd Reference Clock P
FMC2_LPC_CLK1_N	IO_L13N_T2L_N1_GC_ QBC_A07_D23_65	N26	FMC Reference 2nd Reference Clock N

FMC2_LPC_LA00_CC_P	IO_L12P_T1U_N10_GC_64	AG11	FMC Reference 0th Data (Clock) P
FMC2_LPC_LA00_CC_N	IO_L12N_T1U_N11_GC_64	AH11	FMC Reference 0th Data (Clock) N
FMC2_LPC_LA01_CC_P	IO_L13P_T2L_N0_GC_QBC_64	AF10	FMC Reference 1st Data (Clock) P
FMC2_LPC_LA01_CC_N	IO_L13N_T2L_N1_GC_QBC_64	AG10	FMC Reference 1st Data (Clock) N
FMC2_LPC_LA02_P	IO_L2P_T0L_N2_64	AN13	FMC Reference 2nd Data P
FMC2_LPC_LA02_N	IO_L2N_T0L_N3_64	AP13	FMC Reference 2nd Data N
FMC2_LPC_LA03_P	IO_L6P_T0U_N10_AD6P_64	AK13	FMC Reference 3rd Data P
FMC2_LPC_LA03_N	IO_L6N_T0U_N11_AD6N_64	AL13	FMC Reference 3rd Data N
FMC2_LPC_LA04_P	IO_L10P_T1U_N6_QBC_AD4P_64	AD11	FMC Reference 4th Data P
FMC2_LPC_LA04_N	IO_L10N_T1U_N7_QBC_AD4N_64	AE11	FMC Reference 4th Data N
FMC2_LPC_LA05_P	IO_L4P_T0U_N6_DBC_AD7P_64	AM12	FMC Reference 5th Data P
FMC2_LPC_LA05_N	IO_L4N_T0U_N7_DBC_AD7N_64	AN12	FMC Reference 5th Data N
FMC2_LPC_LA06_P	IO_L8P_T1L_N2_AD5P_64	AH13	FMC Reference 6th Data P
FMC2_LPC_LA06_N	IO_L8N_T1L_N3_AD5N_64	AJ13	FMC Reference 6th Data N
FMC2_LPC_LA07_P	IO_L14P_T2L_N2_GC_64	AF9	FMC Reference 7th Data P
FMC2_LPC_LA07_N	IO_L14N_T2L_N3_GC_64	AG9	FMC Reference 7th Data N
FMC2_LPC_LA08_P	IO_L16P_T2U_N6_QBC_AD3P_64	AD10	FMC Reference 8th Data P
FMC2_LPC_LA08_N	IO_L16N_T2U_N7_QBC_AD3N_64	AE10	FMC Reference 8th Data N
FMC2_LPC_LA09_P	IO_L9P_T1L_N4_AD12P_64	AE12	FMC Reference 9th Data

			P
FMC2_LPC_LA09_N	IO_L9N_T1L_N5_AD12N_64	AF12	FMC Reference 9th Data N
FMC2_LPC_LA10_P	IO_L5P_T0U_N8_AD14P_64	AK12	FMC Reference 10th Data P
FMC2_LPC_LA10_N	IO_L5N_T0U_N9_AD14N_64	AL12	FMC Reference 10th Data N
FMC2_LPC_LA11_P	IO_L17P_T2U_N8_AD10P_64	AD9	FMC Reference 11th Data P
FMC2_LPC_LA11_N	IO_L17N_T2U_N9_AD10N_64	AD8	FMC Reference 11th Data N
FMC2_LPC_LA12_P	IO_L7P_T1L_N0_QBC_AD13P_64	AE13	FMC Reference 12th Data P
FMC2_LPC_LA12_N	IO_L7N_T1L_N1_QBC_AD13N_64	AF13	FMC Reference 12th Data N
FMC2_LPC_LA13_P	IO_L1P_T0L_N0_DBC_64	AP11	FMC Reference 13th Data P
FMC2_LPC_LA13_N	IO_L1N_T0L_N1_DBC_64	AP10	FMC Reference 13th Data N
FMC2_LPC_LA14_P	IO_L18P_T2U_N10_AD2P_64	AH9	FMC Reference 14th Data P
FMC2_LPC_LA14_N	IO_L18N_T2U_N11_AD2N_64	AH8	FMC Reference 14th Data N
FMC2_LPC_LA15_P	IO_L15P_T2L_N4_AD11P_64	AE8	FMC Reference 15th Data P
FMC2_LPC_LA15_N	IO_L15N_T2L_N5_AD11N_64	AF8	FMC Reference 15th Data N
FMC2_LPC_LA16_P	IO_L3P_T0L_N4_AD15P_64	AM11	FMC Reference 16th Data P
FMC2_LPC_LA16_N	IO_L3N_T0L_N5_AD15N_64	AN11	FMC Reference 16th Data N
FMC2_LPC_LA17_CC_P	IO_L12P_T1U_N10_GC_A08_D24_65	N24	FMC Reference 17th Data (Clock) P
FMC2_LPC_LA17_CC_N	IO_L12N_T1U_N11_GC_A09_D25_65	M24	FMC Reference 17th Data (Clock) N
FMC2_LPC_LA18_CC_P	IO_L11P_T1U_N8_GC_A10_D26_65	M25	FMC Reference 18th Data (Clock) P

FMC2_LPC_LA18_CC_N	IO_L11N_T1U_N9_GC_A11_D27_65	M26	FMC Reference 18th Data (Clock) N
FMC2_LPC_LA19_P	IO_L15P_T2L_N4_AD11P_A02_D18_65	T27	FMC Reference 19th Data P
FMC2_LPC_LA19_N	IO_L15N_T2L_N5_AD11N_A03_D19_65	R27	FMC Reference 19th Data N
FMC2_LPC_LA20_P	IO_L16P_T2U_N6_QBC_AD3P_A00_D16_65	T24	FMC Reference 20th Data P
FMC2_LPC_LA20_N	IO_L16N_T2U_N7_QBC_AD3N_A01_D17_65	T25	FMC Reference 20th Data N
FMC2_LPC_LA21_P	IO_L18P_T2U_N10_AD2P_D12_65	R23	FMC Reference 21st Data P
FMC2_LPC_LA21_N	IO_L18N_T2U_N11_AD2N_D13_65	P23	FMC Reference 21st Data N
FMC2_LPC_LA22_P	IO_L17P_T2U_N8_AD10P_D14_65	R25	FMC Reference 22nd Data P
FMC2_LPC_LA22_N	IO_L17N_T2U_N9_AD10N_D15_65	R26	FMC Reference 22nd Data N
FMC2_LPC_LA23_P	IO_L19P_T3L_N0_DBC_AD9P_D10_65	N22	FMC Reference 23rd Data P
FMC2_LPC_LA23_N	IO_L19N_T3L_N1_DBC_AD9N_D11_65	M22	FMC Reference 23rd Data N
FMC2_LPC_LA24_P	IO_L9P_T1L_N4_AD12P_A14_D30_65	L25	FMC Reference 24th Data P
FMC2_LPC_LA24_N	IO_L9N_T1L_N5_AD12N_A15_D31_65	K25	FMC Reference 24th Data N
FMC2_LPC_LA25_P	IO_L7P_T1L_N0_QBC_AD13P_A18_65	M27	FMC Reference 25th Data P
FMC2_LPC_LA25_N	IO_L7N_T1L_N1_QBC_AD13N_A19_65	L27	FMC Reference 25th Data N
FMC2_LPC_LA26_P	IO_L8P_T1L_N2_AD5P_A16_65	L23	FMC Reference 26th Data P
FMC2_LPC_LA26_N	IO_L8N_T1L_N3_AD5N_A17_65	L24	FMC Reference 26th Data N
FMC2_LPC_LA27_P	IO_L10P_T1U_N6_QBC_A12_D28_65	L22	FMC Reference 27th Data P
FMC2_LPC_LA27_N	IO_L10N_T1U_N7_QBCA13_D29_6	K23	FMC Reference 27th Data

	5		N
FMC2_LPC_LA28_P	IO_L5P_T0U_N8_AD14P_A22_65	J26	FMC Reference 28th Data P
FMC2_LPC_LA28_N	IO_L5N_T0U_N9_AD14N_A23_65	H26	FMC Reference 28th Data N
FMC2_LPC_LA29_P	IO_L3P_T0L_N4_AD15P_A26_65	K26	FMC Reference 29th Data P
FMC2_LPC_LA29_N	IO_L3N_T0L_N5_AD15N_A27_65	K27	FMC Reference 29th Data N
FMC2_LPC_LA30_P	IO_L2P_T0L_N2_FOE_B_65	G25	FMC Reference 30th Data P
FMC2_LPC_LA30_N	IO_L2N_T0L_N3_FWE_FCS2_B_65	G26	FMC Reference 30th Data N
FMC2_LPC_LA31_P	IO_L1P_T0L_N0_DBC_RS0_65	H27	FMC Reference 31st Data P
FMC2_LPC_LA31_N	IO_L1N_T0L_N1_DBC_RS1_65	G27	FMC Reference 31st Data N
FMC2_LPC_LA32_P	IO_L6P_T0U_N10_AD6P_A20_65	J23	FMC Reference 32nd Data P
FMC2_LPC_LA32_N	IO_L6N_T0U_N11_AD6N_A21_65	H24	FMC Reference 32nd Data N
FMC2_LPC_LA33_P	IO_L4P_T0U_N6_DBC_AD7P_A24_65	J24	FMC Reference 33rd Data P
FMC2_LPC_LA33_N	IO_L4N_T0U_N7_DBC_AD7N_A25_65	J25	FMC Reference 33rd Data N
FMC2_LPC_SCL	IO_T0U_N12_A28_65	H23	FMC I2C Bus Clock
FMC2_LPC_SDA	IO_T1U_N12_PERSTN1_65	N23	FMC I2C Bus Data
FMC2_DP0_C2M_P	MGTHTXP1_226	W4	Transceiver Data Output P
FMC2_DP0_C2M_N	MGTHTXN1_226	W3	Transceiver Data Output N
FMC2_DP0_M2C_P	MGTHRXP1_226	V2	Transceiver Data Input P
FMC2_DP0_M2C_N	MGTHRXN1_226	V1	Transceiver Data Input N
FMC2_GBTCLK0_M2C_P	MGTREFCLK1P_226	T6	Transceiver Reference Clock P
FMC2_GBTCLK0_M2C_N	MGTREFCLK1N_226	T5	Transceiver Reference Clock N

The 3rd FMC HPC Connectors Pin Assignment

Signal Name	FPGA Pin Number	FPGA Pin Name	Description
FMC_HPC_CLK0_M2C_P	IO_L11P_T1U_N8_GC_67	E25	FMC Reference 1st Reference Clock P
FMC_HPC_CLK0_M2C_N	IO_L11N_T1U_N9_GC_67	D25	FMC Reference 1st Reference Clock N
FMC_HPC_CLK1_M2C_P	IO_L12P_T1U_N10_GC_66	G10	FMC Reference 2nd Reference Clock P
FMC_HPC_CLK1_M2C_N	IO_L12N_T1U_N11_GC_66	F10	FMC Reference 2nd Reference Clock N
FMC_HPC_LA00_CC_P	IO_L12P_T1U_N10_GC_67	D24	FMC LA Reference 0th Data (Clock) P
FMC_HPC_LA00_CC_N	IO_L12N_T1U_N11_GC_67	C24	FMC LA Reference 0th Data (Clock) N
FMC_HPC_LA01_CC_N	IO_L14P_T2L_N2_GC_67	E22	FMC LA Reference 1st Data (Clock) P
FMC_HPC_LA01_CC_P	IO_L14N_T2L_N3_GC_67	E23	FMC LA Reference 1st Data (Clock) N
FMC_HPC_LA02_P	IO_L3P_T0L_N4_AD15P_67	E28	FMC LA Reference 2nd Data P
FMC_HPC_LA02_N	IO_L3N_T0L_N5_AD15N_67	D29	FMC LA Reference 2nd Data N
FMC_HPC_LA03_P	IO_L5P_T0U_N8_AD14P_67	D28	FMC LA Reference 3rd Data P
FMC_HPC_LA03_N	IO_L5N_T0U_N9_AD14N_67	C28	FMC LA Reference 3rd Data N
FMC_HPC_LA04_P	IO_L2P_T0L_N2_67	C27	FMC LA Reference 4th Data P
FMC_HPC_LA04_N	IO_L2N_T0L_N3_67	B27	FMC LA Reference 4th Data N
FMC_HPC_LA05_P	IO_L8P_T1L_N2_AD5P_67	B25	FMC LA Reference 5th Data P
FMC_HPC_LA05_N	IO_L8N_T1L_N3_AD5N_67	A25	FMC LA Reference 5th Data N
FMC_HPC_LA06_P	IO_L9P_T1L_N4_AD12P_67	C26	FMC LA Reference 6th Data P

FMC_HPC_LA06_N	IO_L9N_T1L_N5_AD12N_67	B26	FMC LA Reference 6th Data N
FMC_HPC_LA07_P	IO_L1P_T0L_N0_DBC_67	F27	FMC LA Reference 7th Data P
FMC_HPC_LA07_N	IO_L1N_T0L_N1_DBC_67	E27	FMC LA Reference 7th Data N
FMC_HPC_LA08_P	IO_L7P_T1L_N0_QBC_AD13P_67	E26	FMC LA Reference 8th Data P
FMC_HPC_LA08_N	IO_L7N_T1L_N1_QBC_AD13N_67	D26	FMC LA Reference 8th Data N
FMC_HPC_LA09_P	IO_L19P_T3L_N0_DBC_AD9P_67	G24	FMC LA Reference 9th Data P
FMC_HPC_LA09_N	IO_L19N_T3L_N1_DBC_AD9N_67	F25	FMC LA Reference 9th Data N
FMC_HPC_LA10_P	IO_L21P_T3L_N4_AD8P_67	F23	FMC LA Reference 10th Data P
FMC_HPC_LA10_N	IO_L21N_T3L_N5_AD8N_67	F24	FMC LA Reference 10th Data N
FMC_HPC_LA11_P	IO_L18P_T2U_N10_AD2P_67	D20	FMC LA Reference 11th Data P
FMC_HPC_LA11_N	IO_L18N_T2U_N11_AD2N_67	D21	FMC LA Reference 11th Data N
FMC_HPC_LA12_P	IO_L16P_T2U_N6_QBC_AD3P_67	C21	FMC LA Reference 12th Data P
FMC_HPC_LA12_N	IO_L16N_T2U_N7_QBC_AD3N_67	C22	FMC LA Reference 12th Data N
FMC_HPC_LA13_P	IO_L20P_T3L_N2_AD1P_67	E20	FMC LA Reference 13th Data P
FMC_HPC_LA13_N	IO_L20N_T3L_N3_AD1N_67	E21	FMC LA Reference 13th Data N
FMC_HPC_LA14_P	IO_L23P_T3U_N8_67	G22	FMC LA Reference 14th Data P
FMC_HPC_LA14_N	IO_L23N_T3U_N9_67	F22	FMC LA Reference 14th Data N
FMC_HPC_LA15_P	IO_L24P_T3U_N10_67	H21	FMC LA Reference 15th Data P
FMC_HPC_LA15_N	IO_L24N_T3U_N11_67	G21	FMC LA Reference 15th

			Data N
FMC_HPC_LA16_P	IO_L22P_T3U_N6_DBC_AD0P_67	G20	FMC LA Reference 16th Data P
FMC_HPC_LA16_N	IO_L22N_T3U_N7_DBC_AD0N_67	F20	FMC LA Reference 16th Data N
FMC_HPC_LA17_CC_P	IO_L11P_T1U_N8_GC_66	G9	FMC LA Reference 17th Data (Clock) P
FMC_HPC_LA17_CC_N	IO_L11N_T1U_N9_GC_66	F9	FMC LA Reference 17th Data (Clock) N
FMC_HPC_LA18_CC_P	IO_L13P_T2L_N0_GC_QBC_66	H11	FMC LA Reference 18th Data (Clock) P
FMC_HPC_LA18_CC_N	IO_L13N_T2L_N1_GC_QBC_66	G11	FMC LA Reference 18th Data (Clock) N
FMC_HPC_LA19_P	IO_L22P_T3U_N6_DBC_AD0P_66	F13	FMC LA Reference 19th Data P
FMC_HPC_LA19_N	IO_L22N_T3U_N7_DBC_AD0N_66	E13	FMC LA Reference 19th Data N
FMC_HPC_LA20_P	IO_L24P_T3U_N10_66	D13	FMC LA Reference 20th Data P
FMC_HPC_LA20_N	IO_L24N_T3U_N11_66	C13	FMC LA Reference 20th Data N
FMC_HPC_LA21_P	IO_L5P_T0U_N8_AD14P_66	D9	FMC LA Reference 21st Data P
FMC_HPC_LA21_N	IO_L5N_T0U_N9_AD14N_66	C9	FMC LA Reference 21st Data N
FMC_HPC_LA22_P	IO_L6P_T0U_N10_AD6P_66	E10	FMC LA Reference 22nd Data P
FMC_HPC_LA22_N	IO_L6N_T0U_N11_AD6N_66	D10	FMC LA Reference 22nd Data N
FMC_HPC_LA23_P	IO_L19P_T3L_N0_DBC_AD9P_66	E11	FMC LA Reference 23rd Data P
FMC_HPC_LA23_N	IO_L19N_T3L_N1_DBC_AD9N_66	D11	FMC LA Reference 23rd Data N
FMC_HPC_LA24_P	IO_L15P_T2L_N4_AD11P_66	K11	FMC LA Reference 24th Data P
FMC_HPC_LA24_N	IO_L15N_T2L_N5_AD11N_66	J11	FMC LA Reference 24th Data N

FMC_HPC_LA25_P	IO_L1P_T0L_N0_DBC_66	F8	FMC LA Reference 25th Data P
FMC_HPC_LA25_N	IO_L1N_T0L_N1_DBC_66	E8	FMC LA Reference 25th Data N
FMC_HPC_LA26_P	IO_L18P_T2U_N10_AD2P_66	J13	FMC LA Reference 26th Data P
FMC_HPC_LA26_N	IO_L18N_T2U_N11_AD2N_66	H13	FMC LA Reference 26th Data N
FMC_HPC_LA27_P	IO_L3P_T0L_N4_AD15P_66	D8	FMC LA Reference 27th Data P
FMC_HPC_LA27_N	IO_L3N_T0L_N5_AD15N_66	C8	FMC LA Reference 27th Data N
FMC_HPC_LA28_P	IO_L9P_T1L_N4_AD12P_66	J8	FMC LA Reference 28th Data P
FMC_HPC_LA28_N	IO_L9N_T1L_N5_AD12N_66	H8	FMC LA Reference 28th Data N
FMC_HPC_LA29_P	IO_L8P_T1L_N2_AD5P_66	J9	FMC LA Reference 29th Data P
FMC_HPC_LA29_N	IO_L8N_T1L_N3_AD5N_66	H9	FMC LA Reference 29th Data N
FMC_HPC_LA30_P	IO_L7P_T1L_N0_QBC_AD13P_66	L8	FMC LA Reference 30th Data P
FMC_HPC_LA30_N	IO_L7N_T1L_N1_QBC_AD13N_66	K8	FMC LA Reference 30th Data N
FMC_HPC_LA31_P	IO_L10P_T1U_N6_QBC_AD4P_66	K10	FMC LA Reference 31st Data P
FMC_HPC_LA31_N	IO_L10N_T1U_N7_QBC_AD4N_66	J10	FMC LA Reference 31st Data N
FMC_HPC_LA32_P	IO_L16P_T2U_N6_QBC_AD3P_66	L13	FMC LA Reference 32nd Data P
FMC_HPC_LA32_N	IO_L16N_T2U_N7_QBC_AD3N_66	K13	FMC LA Reference 32nd Data N
FMC_HPC_LA33_P	IO_L17P_T2U_N8_AD10P_66	L12	FMC LA Reference 33rd Data P
FMC_HPC_LA33_N	IO_L17N_T2U_N9_AD10N_66	K12	FMC LA Reference 33rd Data N
FMC_HA00_CC_P	IO_L12P_T1U_N10_GC_68	E18	FMC HA Reference 0th

			Data (Clock) P
FMC_HA00_CC_N	IO_L12N_T1U_N11_GC_68	E17	FMC HA Reference 0th Data (Clock) N
FMC_HA01_CC_P	IO_L11P_T1U_N8_GC_68	E16	FMC HA Reference 1st Data (Clock) P
FMC_HA01_CC_N	IO_L11N_T1U_N9_GC_68	D16	FMC HA Reference 1st Data (Clock) N
FMC_HA02_P	IO_L18P_T2U_N10_AD2P_68	H19	FMC HA Reference 2nd Data P
FMC_HA02_N	IO_L18N_T2U_N11_AD2N_68	H18	FMC HA Reference 2nd Data N
FMC_HA03_P	IO_L24P_T3U_N10_68	L19	FMC HA Reference 3rd Data P
FMC_HA03_N	IO_L24N_T3U_N11_68	L18	FMC HA Reference 3rd Data N
FMC_HA04_P	IO_L16P_T2U_N6_QBC_AD3P_68	G19	FMC HA Reference 4th Data P
FMC_HA04_N	IO_L16N_T2U_N7_QBC_AD3N_68	F19	FMC HA Reference 4th Data N
FMC_HA05_P	IO_L10P_T1U_N6_QBC_AD4P_68	D19	FMC HA Reference 5th Data P
FMC_HA05_N	IO_L10N_T1U_N7_QBC_AD4N_68	D18	FMC HA Reference 5th Data N
FMC_HA06_P	IO_L23P_T3U_N8_68	K16	FMC HA Reference 6th Data P
FMC_HA06_N	IO_L23N_T3U_N9_68	J16	FMC HA Reference 6th Data N
FMC_HA07_P	IO_L14P_T2L_N2_GC_68	F18	FMC HA Reference 7th Data P
FMC_HA07_N	IO_L14N_T2L_N3_GC_68	F17	FMC HA Reference 7th Data N
FMC_HA08_P	IO_L20P_T3L_N2_AD1P_68	K18	FMC HA Reference 8th Data P
FMC_HA08_N	IO_L20N_T3L_N3_AD1N_68	K17	FMC HA Reference 8th Data N
FMC_HA09_P	IO_L22P_T3U_N6_DBC_AD0P_68	J19	FMC HA Reference 9th Data P

FMC_HA09_N	IO_L22N_T3U_N7_DBC_AD0N_68	J18	FMC HA Reference 9th Data N
FMC_HA10_P	IO_L9P_T1L_N4_AD12P_68	F15	FMC HA Reference 10th Data P
FMC_HA10_N	IO_L9N_T1L_N5_AD12N_68	F14	FMC HA Reference 10th Data N
FMC_HA11_P	IO_L21P_T3L_N4_AD8P_68	L15	FMC HA Reference 11th Data P
FMC_HA11_N	IO_L21N_T3L_N5_AD8N_68	K15	FMC HA Reference 11th Data N
FMC_HA12_P	IO_L19P_T3L_N0_DBC_AD9P_68	J15	FMC HA Reference 12th Data P
FMC_HA12_N	IO_L19N_T3L_N1_DBC_AD9N_68	J14	FMC HA Reference 12th Data N
FMC_HA13_P	IO_L1P_T0L_N0_DBC_68	B14	FMC HA Reference 13th Data P
FMC_HA13_N	IO_L1N_T0L_N1_DBC_68	A14	FMC HA Reference 13th Data N
FMC_HA14_P	IO_L3P_T0L_N4_AD15P_68	B15	FMC HA Reference 14th Data P
FMC_HA14_N	IO_L3N_T0L_N5_AD15N_68	A15	FMC HA Reference 14th Data N
FMC_HA15_P	IO_L4P_T0U_N6_DBC_AD7P_68	C19	FMC HA Reference 15th Data P
FMC_HA15_N	IO_L4N_T0U_N7_DBC_AD7N_68	B19	FMC HA Reference 15th Data N
FMC_HA16_P	IO_L2P_T0L_N2_68	A19	FMC HA Reference 16th Data P
FMC_HA16_N	IO_L2N_T0L_N3_68	A18	FMC HA Reference 16th Data N
FMC_HA17_CC_P	IO_L13P_T2L_N0_GC_QBC_68	G17	FMC HA Reference 17th Data (Clock) P
FMC_HA17_CC_N	IO_L13N_T2L_N1_GC_QBC_68	G16	FMC HA Reference 17th Data (Clock) N
FMC_HA18_P	IO_L17P_T2U_N8_AD10P_68	H17	FMC HA Reference 18th Data P
FMC_HA18_N	IO_L17N_T2U_N9_AD10N_68	H16	FMC HA Reference 18th

			Data N
FMC_HA19_P	IO_L5P_T0U_N8_AD14P_68	B17	FMC HA Reference 19th Data P
FMC_HA19_N	IO_L5N_T0U_N9_AD14N_68	B16	FMC HA Reference 19th Data N
FMC_HA20_P	IO_L6P_T0U_N10_AD6P_68	C18	FMC HA Reference 20th Data P
FMC_HA20_N	IO_L6N_T0U_N11_AD6N_68	C17	FMC HA Reference 20th Data N
FMC_HA21_P	IO_L8P_T1L_N2_AD5P_68	E15	FMC HA Reference 21st Data P
FMC_HA21_N	IO_L8N_T1L_N3_AD5N_68	D15	FMC HA Reference 21st Data N
FMC_HA22_P	IO_L7P_T1L_N0_QBC_AD13P_68	D14	FMC HA Reference 22nd Data P
FMC_HA22_N	IO_L7N_T1L_N1_QBC_AD13N_68	C14	FMC HA Reference 22nd Data N
FMC_HA23_P	IO_L15P_T2L_N4_AD11P_68	G15	FMC HA Reference 23rd Data P
FMC_HA23_N	IO_L15N_T2L_N5_AD11N_68	G14	FMC HA Reference 23rd Data N
FMC_HPC_SCL	IO_T1U_N12_68	C16	FMC I2C Bus Clock
FMC_HPC_SDA	IO_T2U_N12_68	H14	FMC I2C Bus Data
FMC_GBTCLK0_M2C_P	MGTREFCLK0P_228	K6	Transceiver Reference Clock 0 Input P
FMC_GBTCLK0_M2C_N	MGTREFCLK0N_228	K5	Transceiver Reference Clock 0 Input N
FMC_GBTCLK1_M2C_P	MGTREFCLK0P_227	P6	Transceiver Reference Clock 1 Input P
FMC_GBTCLK1_M2C_N	MGTREFCLK0N_227	P5	Transceiver Reference Clock 1 Input N
FMC_DP0_M2C_P	MGTHRXP3_228	A4	Transceiver Data 0 Input P
FMC_DP0_M2C_N	MGTHRXN3_228	A3	Transceiver Data 0 Input N
FMC_DP1_M2C_P	MGTHRXP2_228	B2	Transceiver Data 1 Input P
FMC_DP1_M2C_N	MGTHRXN2_228	B1	Transceiver Data 1 Input N
FMC_DP2_M2C_P	MGTHRXP1_228	D2	Transceiver Data 2 Input P
FMC_DP2_M2C_N	MGTHRXN1_228	D1	Transceiver Data 2 Input N

FMC_DP3_M2C_P	MGTHRXP0_228	E4	Transceiver Data 3 Input P
FMC_DP3_M2C_N	MGTHRXN0_228	E3	Transceiver Data 3 Input N
FMC_DP4_M2C_P	MGTHRXP3_227	F2	Transceiver Data 4 Input P
FMC_DP4_M2C_N	MGTHRXN3_227	F1	Transceiver Data 4 Input N
FMC_DP5_M2C_P	MGTHRXP2_227	H2	Transceiver Data 5 Input P
FMC_DP5_M2C_N	MGTHRXN2_227	H1	Transceiver Data 5 Input N
FMC_DP6_M2C_P	MGTHRXP1_227	K2	Transceiver Data 6 Input P
FMC_DP6_M2C_N	MGTHRXN1_227	K1	Transceiver Data 6 Input N
FMC_DP7_M2C_P	MGTHRXP0_227	M2	Transceiver Data 7 Input P
FMC_DP7_M2C_N	MGTHRXN0_227	M1	Transceiver Data 7 Input N
FMC_DP0_C2M_P	MGTHTXP3_228	B6	Transceiver Data 0 Output P
FMC_DP0_C2M_N	MGTHTXN3_228	B5	Transceiver Data 0 Output N
FMC_DP1_C2M_P	MGTHTXP2_228	C4	Transceiver Data 1 Output P
FMC_DP1_C2M_N	MGTHTXN2_228	C3	Transceiver Data 1 Output N
FMC_DP2_C2M_P	MGTHTXP1_228	D6	Transceiver Data 2 Output P
FMC_DP2_C2M_N	MGTHTXN1_228	D5	Transceiver Data 2 Output N
FMC_DP3_C2M_P	MGTHTXP0_228	F6	Transceiver Data 3 Output P
FMC_DP3_C2M_N	MGTHTXN0_228	F5	Transceiver Data 3 Output N
FMC_DP4_C2M_P	MGTHTXP3_227	G4	Transceiver Data 4 Output P
FMC_DP4_C2M_N	MGTHTXN3_227	G3	Transceiver Data 4 Output N
FMC_DP5_C2M_P	MGTHTXP2_227	J4	Transceiver Data 5 Output P
FMC_DP5_C2M_N	MGTHTXN2_227	J3	Transceiver Data 5 Output N
FMC_DP6_C2M_P	MGTHTXP1_227	L4	Transceiver Data 6 Output P
FMC_DP6_C2M_N	MGTHTXN1_227	L3	Transceiver Data 6 Output

			N
FMC_DP7_C2M_P	MGTHTXP0_227	N4	Transceiver Data 7 Output P
FMC_DP7_C2M_N	MGTHTXN0_227	N3	Transceiver Data 7 Output N

Part 11: SD Card Slot

The SD card (Secure Digital Memory Card) is a memory card based on the semiconductor flash memory process. It was completed in 1999 by the Japanese Panasonic-led concept, and the participants Toshiba and SanDisk of the United States conducted substantial research and development. In 2000, these companies launched the SD Association (Secure Digital Association), which has a strong lineup and attracted a large number of vendors. These include IBM, Microsoft, Motorola, NEC, Samsung, and others. Driven by these leading manufacturers, SD cards have become the most widely used memory card in consumer digital devices.

The AXKU040 FPGA development board includes a Micro SD card interface to provide users with access to SD card memory for storing pictures, music or other user data files.

The IO signal is connected to the IO signal of the FPGA BANK64, because the VCCIO of the BANK is FMC2_VADJ, the default is +1.8V. However, the SD card has a data level of 3.3 and needs to be connected via the TXS02612 level shifter. The schematic diagram of the FPGA and SD card connector is shown in Figure 11-1.

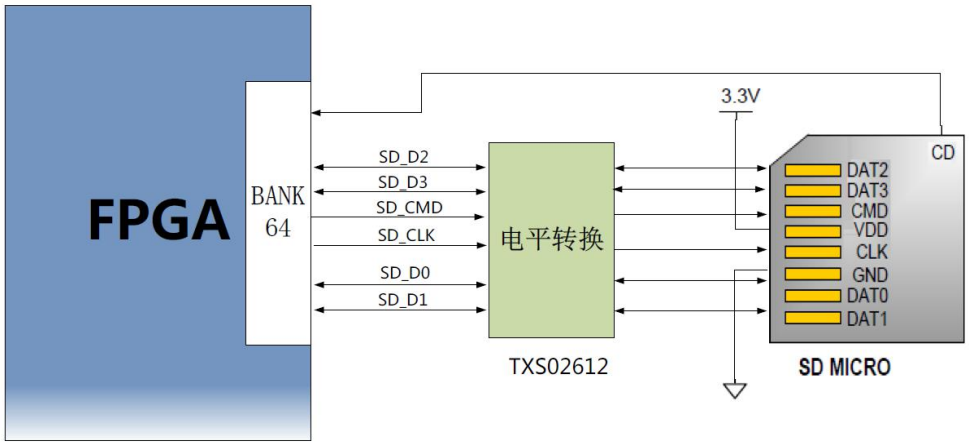

Figure 11-1: SD Card Slot Schematic

SD Card Slot pin assignment:

Signal Name	FPGA Pin	FPGA Pin Number	Description
SD_CLK	IO_L22P_T3U_N6_DBC_AD0P_64	AN8	SD Clock Signal
SD_CMD	IO_L21N_T3L_N5_AD8N_64	AL9	SD Command Signal
SD_D0	IO_L24N_T3U_N11_64	AL8	SDData0
SD_D1	IO_L22N_T3U_N7_DBC_AD0N_64	AP8	SDData1
SD_D2	IO_L23P_T3U_N8_64	AJ9	SDData2
SD_D3	IO_L21P_T3L_N4_AD8P_64	AK10	SDData3
SD_CD	IO_L23N_T3U_N9_64	AJ8	SD card insertion signal

Part 12: SMA and SATA Interface

The AXKU040 FPGA development board is designed with 6 SMA interfaces, which are connected to the BANK225 high-speed transceiver , including a pair of TX, a pair of RX, and a pair of clock signals. Provide customers with high-speed external interfaces. In addition, two SATA ports are reserved on the FPGA board for connecting solid state drives.

The schematic diagram of FPGA and SMA interface connection is shown in Figure 12-1.

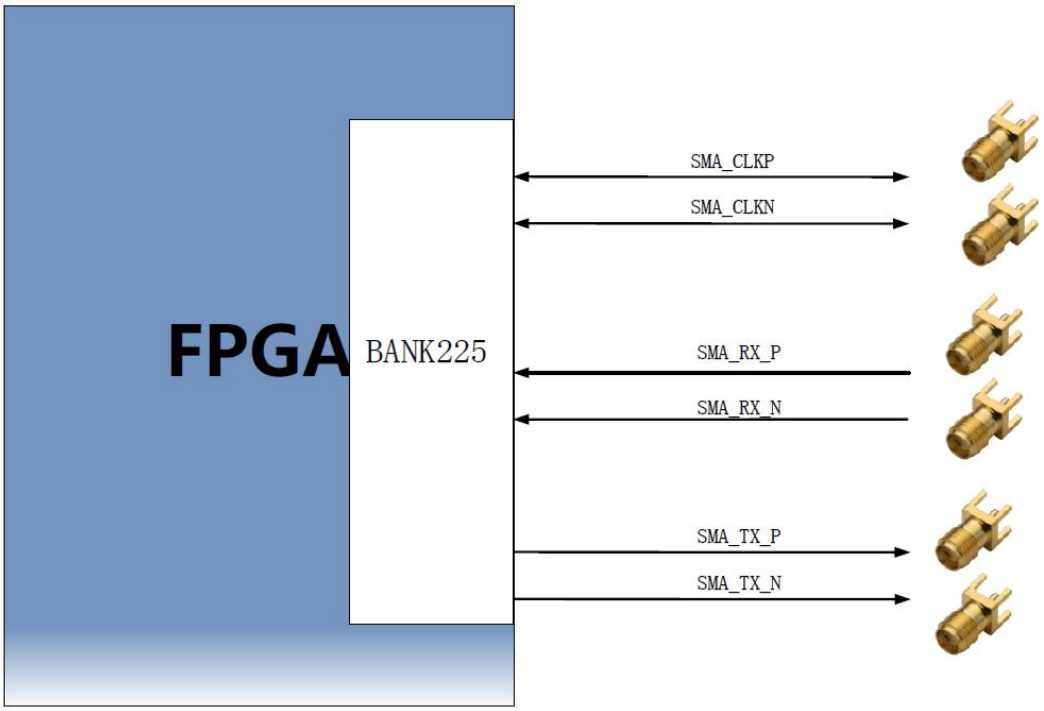

Figure 12-1: SMA Connection Schematic

SMA Interface pin assignment:

Signal Name	FPGA Pin	FPGA Pin Number	Description
SMA_CLKP	MGTREFCLK1P_225	Y6	Transceiver Clock Signal
SMA_CLKN	MGTREFCLK1N_225	Y5	Transceiver Clock Signal
SMA_TX_P	MGTHTXP3_225	AC4	Transceiver Signal Output
SMA_TX_N	MGTHTXN3_225	AC3	Transceiver Signal Output
SMA_RX_P	MGTHRXP3_225	AB2	Transceiver Signal Input

SMA_RX_N	MGTHRXN3_225	AB1	Transceiver Signal Input

The schematic diagram of FPGA and SATA interface connection is shown in Figure 12-2.

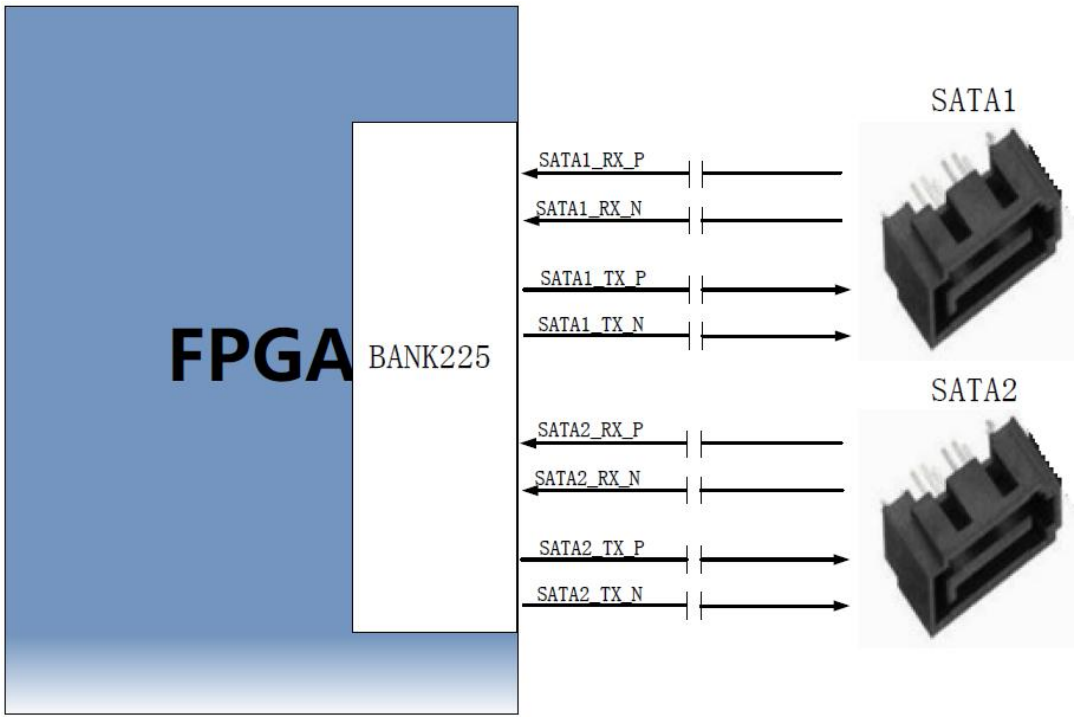

Figure 12-2: SATA Connection Schematic

SATA Interface pin assignment:

Signal Name	FPGA Pin	FPGA Pin Number	Description
SATA1_ TX_P	MGTHTXP0_225	AH6	SATA1 Data Transmission P
SATA1_ TX_N	MGTHTXN0_225	AH5	SATA1 Data Transmission N
SATA1_ RX_P	MGTHRXP0_225	AH2	SATA1 Data Receive P
SATA1_ RX_N	MGTHRXN0_225	AH1	SATA1 Data Receive N
SATA2_ TX_P	MGTHTXP1_225	AG4	SATA2 Data Transmission P
SATA2_ TX_N	MGTHTXN1_225	AG3	SATA2 Data Transmission N
SATA2_ RX_P	MGTHRXP1_225	AF2	SATA2 Data Receive P
SATA2_ RX_N	MGTHRXN1_225	AF1	SATA2 Data Receive N

Part 13: Temperature Sensor

A high-precision, low-power, digital temperature sensor chip is mounted on the AXKU040 FPGA development board, and the model is LM75 of ON Semiconductor. The temperature accuracy of the LM75 chip is 0.5 degrees. The sensor and FPGA are directly connected to the I2C digital interface. The FPGA reads the temperature near the current FPGA development board through the I2C interface. Figure 13-1 below shows the design of the LM75 sensor chip.

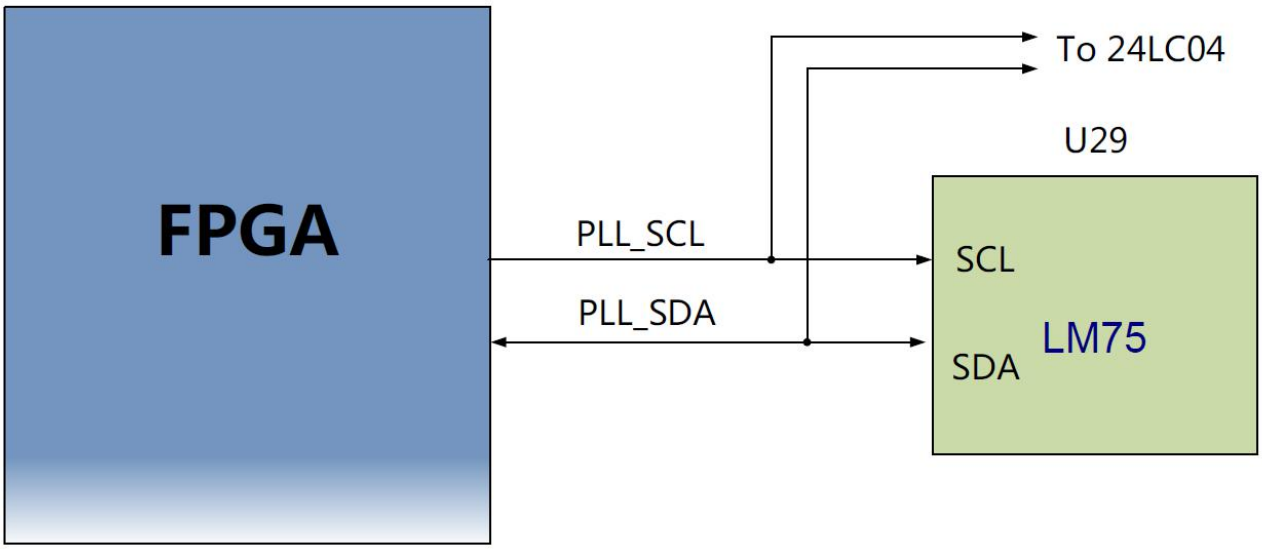

Figure 13-1: LM75 Sensor Schematic

LM75 Sensor Pin Assignment

Pin Name	FPGA Pin
I2C_SCL_3V3	P24
I2C_SDA_3V3	P25

Part 14: JTAG Interface

A JTAG interface is reserved JTAG interface one the AXKU040 FPGA development board for downloading FPGA programs or firmware to FLASH. In order to prevent damage to the FPGA chip caused by hot plugging, a protection diode is added to the JTAG signal to ensure that the voltage of the signal is within the range accepted by the FPGA to avoid damage of the FPGA chip.

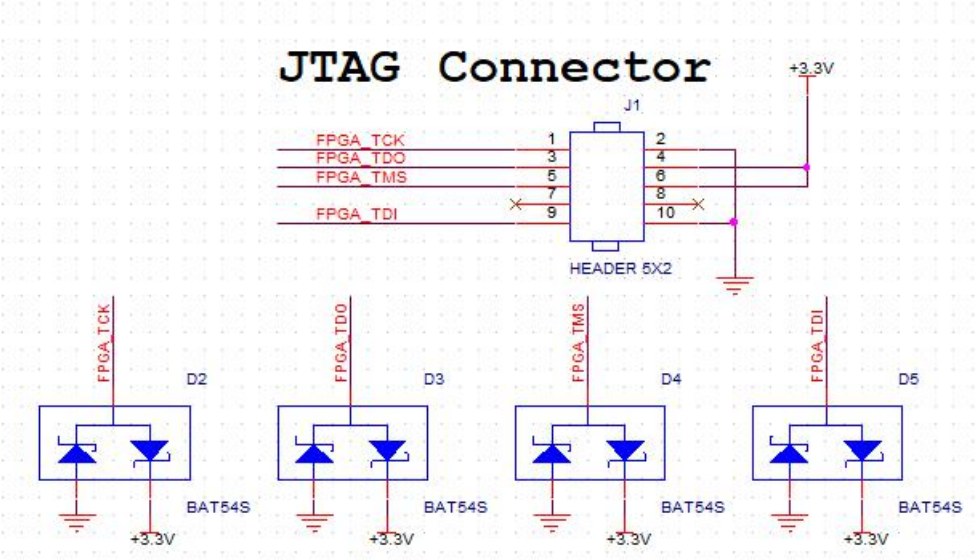

Figure 14-1: JTAG Interface Schematic

JTAG Pin Assignment

Signal Name	FPGA Pin	FPGA Pin Number	Description
FPGA_TDI	TDI_0	V9	JTAG Data Input Pin
FPGA_TMS	TMS_0	W9	JTAG Control Pin
FPGA_TDO	TDO_0	U9	JTAG Data Output Pin
FPGA_TCK	TCK_0	AC9	JTAG Clock Pin

Part 15: LED Light

There are Six red LEDs on the AXKU040 FPGA development board, one of which is the power indicator (PWR), one is DONE indicator,four are users LED lights. When the AXKU040 FPGA board is powered on, the power indicator will light up; when the AXKU040 FPGA is configured, the configuration LED will light up; 4 user LEDs are connected to the IO of the FPGA BANK65, the user can control the lighting and extinction through the program. When the IO voltage connected to the user LED is configured low level, the user LED lights up. When the connected IO voltage is configured as high level, the user LED will be extinguished. Because the level of BANK65 is 1.8V, here we have added a three-stage tube to drive the LED to light up. DONE light to judge whether FPGA startup is normal

The LEDs hardware connection is shown in Figure 15-1.

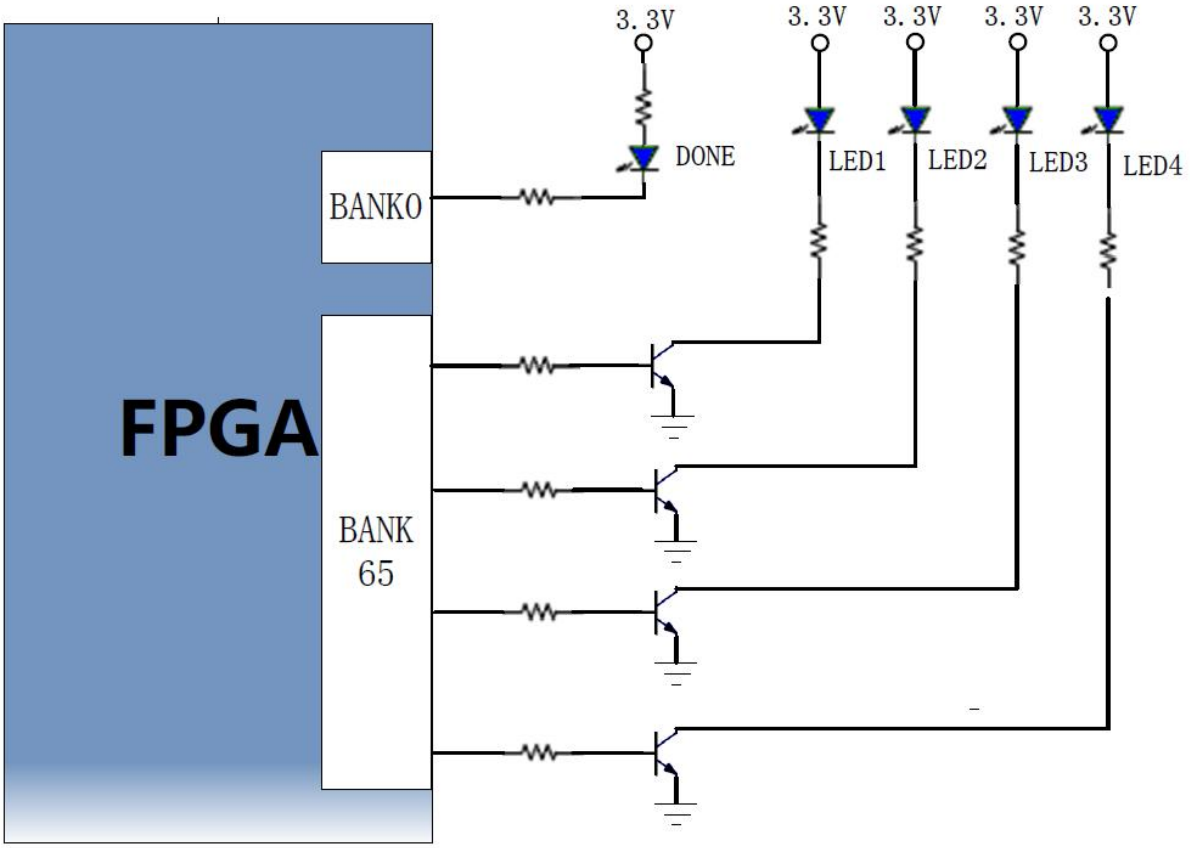

Figure 15-1: The LED lights hardware connection diagram

Pin assignment of user LED lights

Signal Name	FPGA Pin	FPGA Pin Number	Description
LED1	IO_L22N_T3U_N7_DBC_AD0N_D05_65	L20	User LED1
LED2	IO_L22P_T3U_N6_DBC_AD0P_D04_65	M20	User LED2
LED3	IO_L23N_T3U_N9_I2C_SDA_65	M21	User LED3
LED3	IO_L23P_T3U_N8_I2C_SCLK_65	N21	User LED4
FPGA_DONE	DONE_0	N7	FPGA Configuration Indicator

Part 16: Keys

The AXKU040 FPGA development board contains two user Keys and 1 reset key. Two user keys are connected to the IO of FPGA BANK65.The user key is active at low level to realize some functions of the board for customers; The reset key is connected to FPGA BANK64 for system reset.

The circuit of user key part is shown in Figure 16-1.

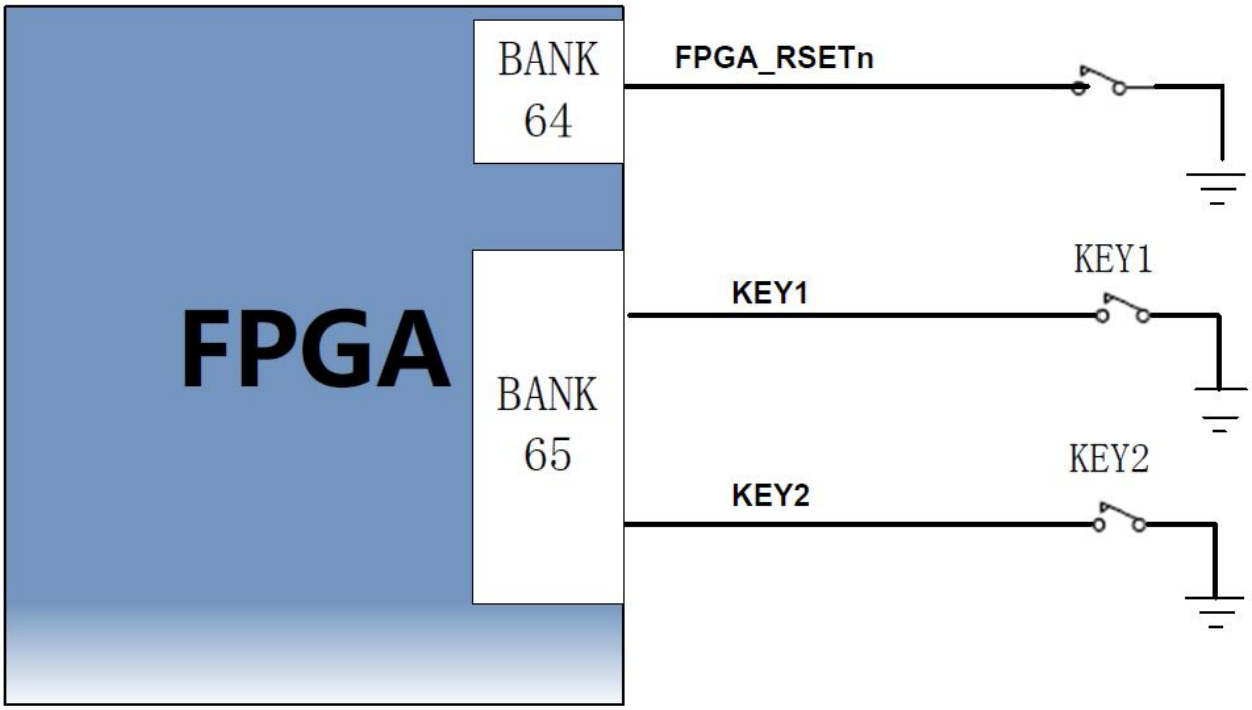

Figure 16-1: Keys Schematic

Keys Pin Assignment

Signal Name	FPGA Pin	FPGA Pin Number	Description
KEY1	IO_L13N_T2L_N1_GC_QBC_44	K21	User Key Input
KEY2	IO_L24P_T3U_N10_EMCCLK_65	K20	User Key Input
FPGA_RSETn	IO_L24P_T3U_N10_64	AK8	System Reset

Part 17: Power Supply

The power input voltage of the AXKU040 FPGA development board is DC12V, and the external +12V power supply supplies power to the FPGA development board.

The Power supply design diagram shown in Figure 18-1.

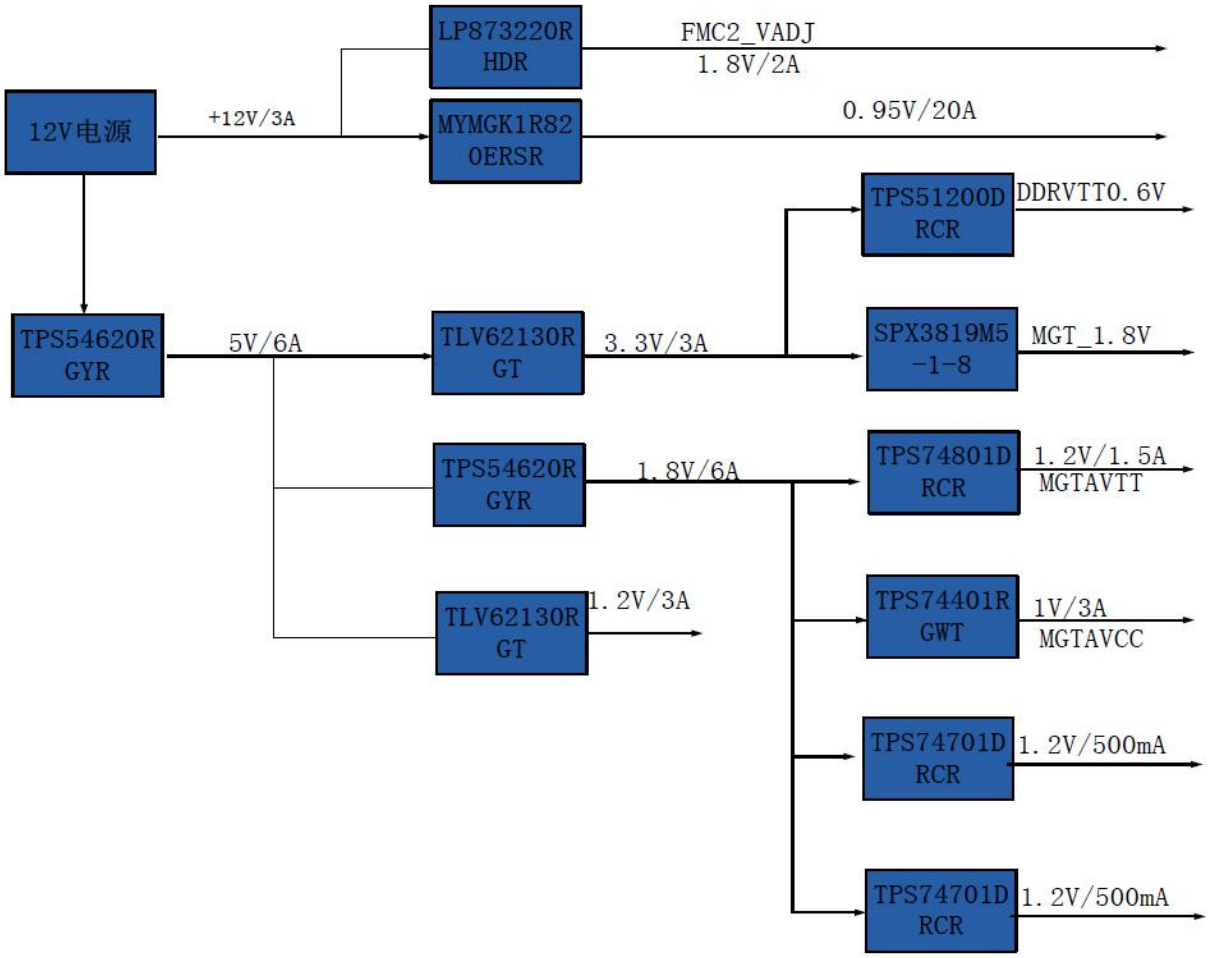

Figure 17-1: Power Supply Design Diagram

The functions of each power distribution are shown in the following table:

Power Supply	Function
+0.95V	FPGA core voltage
+3.3V	FMC Chip IO Voltage, FMC, SFP, LED, SD Card, Level Conversion Chip
+1.8V	HDMI Chip, Level Conversion Chip, Power Supply Voltage
+1.2 V/ 1.5A	DDR4, FPGA Chip, Voltage in the FMC

+1.2 V/ 500mA	Auxiliary Voltage, Gigabit Chip
MGTAVCC(+1.0V)	FPGA Chip Voltage
MGTAVTT(+1.2V)	FPGA Chip Voltage
DDRVTT（0.6V）	DDR4 pull-up voltage
FMC2_VADJ（1.8V）	FPGA chip voltage, Level shift voltage, Voltage on FMC
MGT_1.8V (+1.2V)	FPGA GTH auxiliary voltage

Part 18: Fan

Because AXKU040 FPGA development board generates a lot of heat when it works normally, we add a heat sink and fan to the chip on the board to prevent the chip from overheating. The control of the fan is controlled by the FPGA Chip. The control pin is connected to the IO of the BANK65. If the IO level output is high, the MOSFET is turned on and the fan is working. The fan design on the board is shown in Figure 18-1.

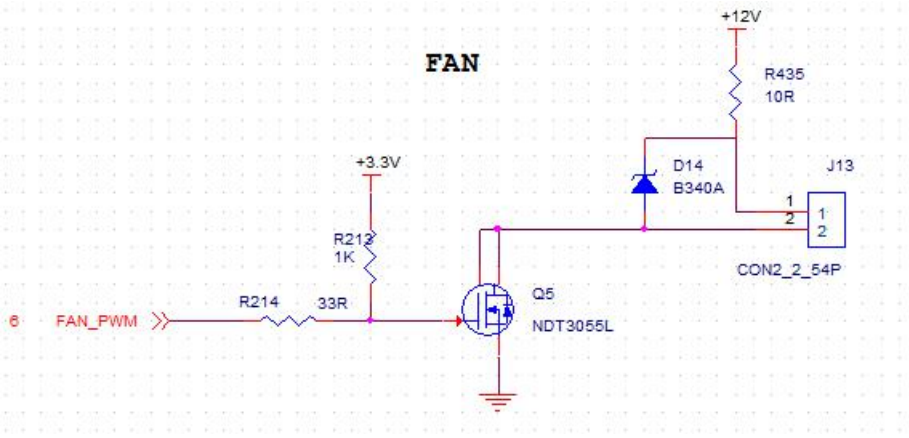

Figure 18-1：Fan design in the schematic

Fan Control Pin Assignment

Signal Name	FPGA Pin	FPGA Pin Number	Description
FAN_PWM	IO_L20P_T3L_N2_AD1P_D08_65	P20	User Key Input

Part 19: Form Factory

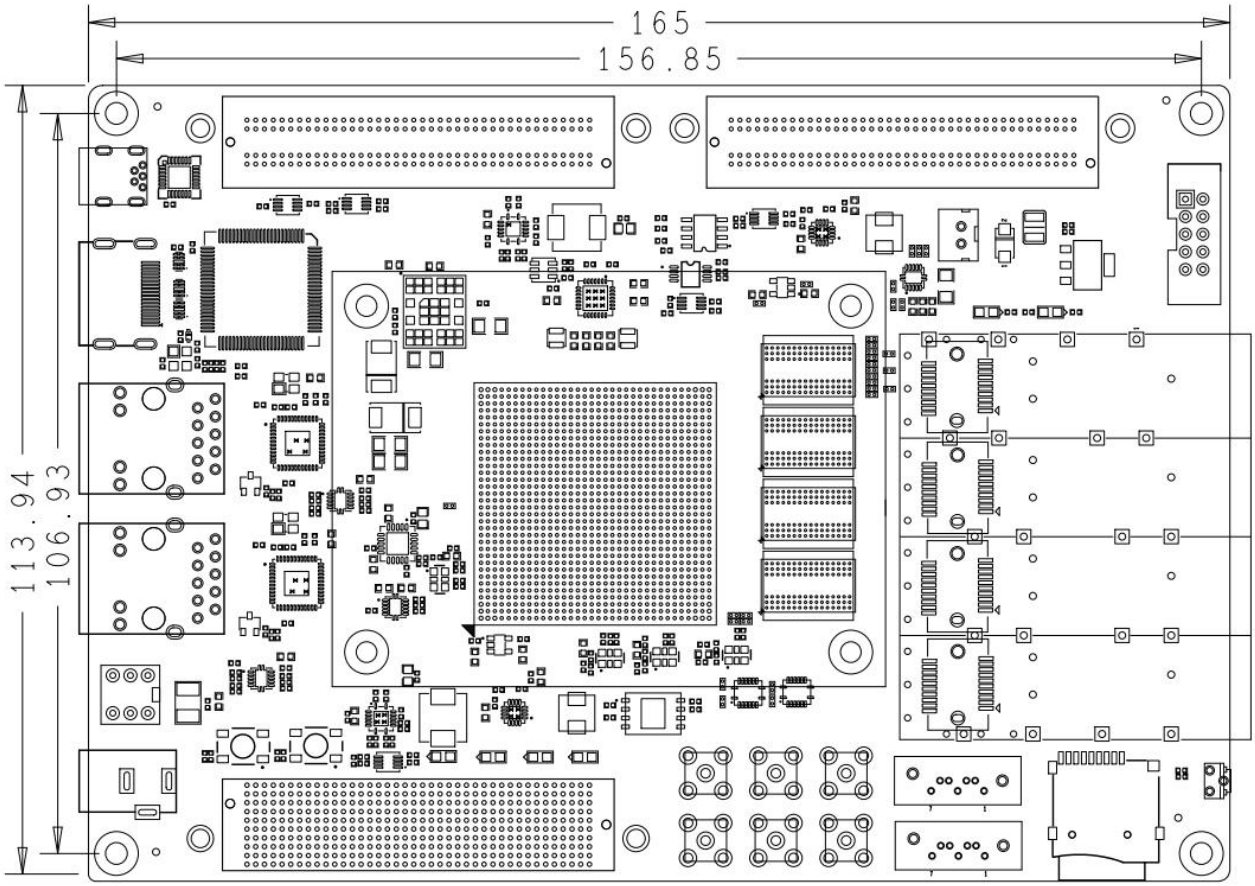

Figure 19-1: Form Factor (Top View)