KINTEX UltraScale development Board

User Manual

AXKU041

ALINX

Version Record

Version	Date
REV1.0	2020-2-1

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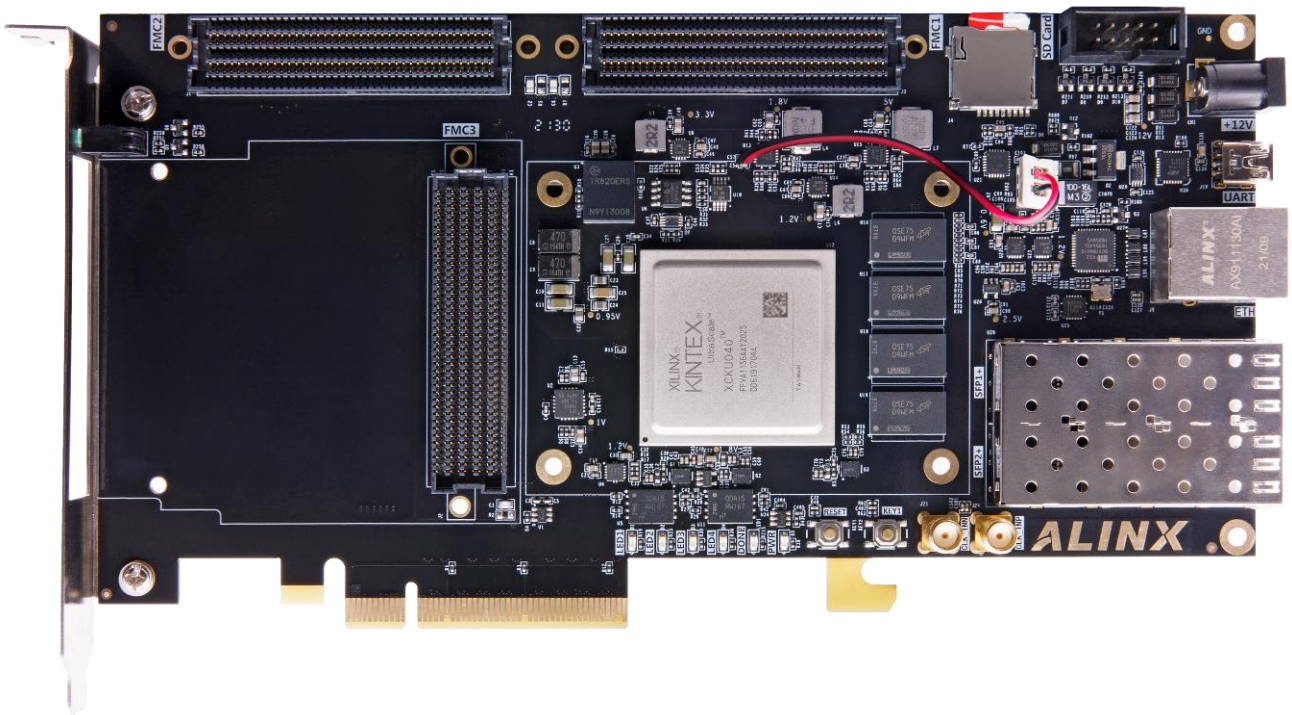
Part 1 FPGA Development Board Introduction

AXKU041 is a development board based on XILINX development platform KINTEX UltraSacale architecture provided by Xinye Electronic Technology (Shanghai) Co., LTD. It can meet users' requirements of various high-speed data exchange, data storage, video transmission processing and industrial control. It is a "professional-grade" FPGA development platform. It is possible for high speed data transmission and exchange, early validation and late application of data processing. I believe that such a product is very suitable for students and engineers engaged in FPGA development. To give you a quick overview of this development platform, we have written this user manual.

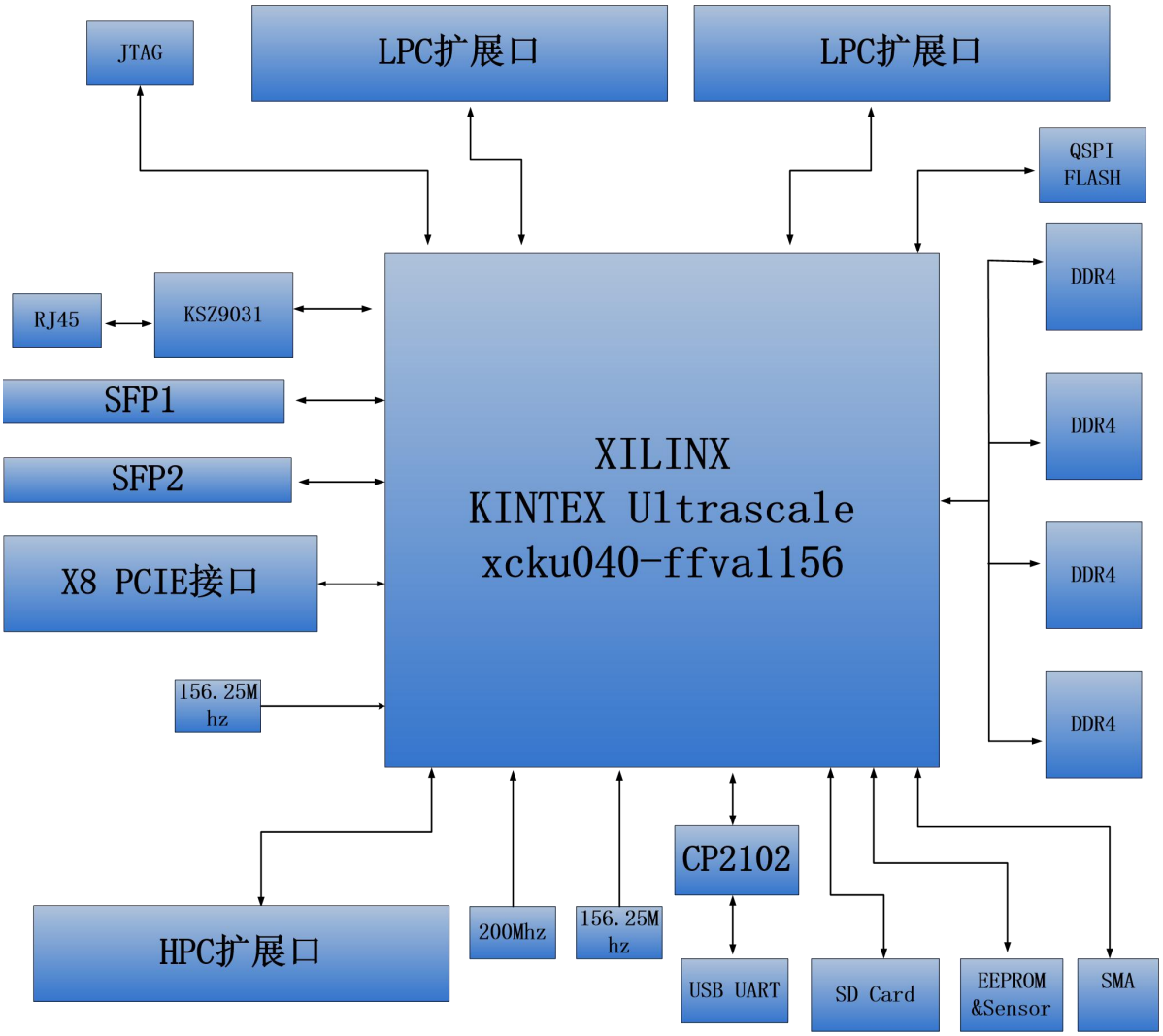


The AXKU041 development board is mounted with four 1GB high-speed DDR4 SDRAM chips, and the FPGA chip configuration uses two 256Mb QSPI NOR FLASH chips.

In terms of peripheral circuit, we have extended a variety of interfaces for users: 2 10G SFP+ optical fiber interfaces, 3 FMC expansion interfaces, 1 UART serial

interface, 1 SD card interface, 1 road network interface, SMA and so on.

The diagram below is the schematic diagram of the whole development system:



Through this diagram, we can see the interfaces and functions that our development platform can contain

- **Xilinx KINTEX UltraSacale chip XCKU040**
- **DDR4**

It comes with four high-speed DDR4 SDRAM with a large capacity of 1 gigabyte (4GB). Can be used as FPGA data storage, image analysis cache, data processing.

- **QSPI FLASH**

Two 256Mbit QSPI NOR FLASH memory chips, which can be used to store FPGA chip configuration files and user data;

- **2 SFP+Fiber Interface**

The two-channel high-speed transceiver of THE GTH transceiver of FPGA is connected to the transmitting and receiving of two optical modules to realize the two-channel high-speed optical communication interface. Each channel of optical fiber data communication receives and sends up to 16.3Gb/s

- **USB Uart interface**

1 Uart to USB interface, used for communication with computer, convenient user debugging. Serial port chip adopts USB-UAR chip of Silicon Labs CP2102GM, USB interface adopts MINI USB interface.

- **Ethernet interface**

One 10/100m /1000M Ethernet RJ45 port, used for Ethernet data exchange with computers or other network devices. The network interface chip adopts Micrel KSZ9031 industrial grade GPHY chip.

- **FMC Interface**

Three standard FMC expansions, including two LPC expansions and one HPC expansions. XILINX or our black gold can be connected to various FMC modules (HDMI input/output module, binocular camera module, high-speed AD module and so on.

- **Micro SD**

1 Micro SD card holder, used for FPGA to read and write SD card data and storage

- **SMA**

2 channels SMA external interface, pin connection common clock signal, used for external input and output signals.

- **Temperature and humidity sensor EEPROM**

The onboard TEMPERATURE and humidity sensor chip LM75 is used to detect the ambient temperature and humidity of the board.

An ONBOARD EEPROM is used to communicate with IIC bus and store some customized information.

- **JTAG**

A 10-pin 2.54mm standard JTAG port is used for downloading and debugging of FPGA programs. Users can debug and download FPGA through XILINX downloader.

- **CLK**

A 200Mhz differential crystal oscillator provides a stable clock source for FPGA

system;

A 156.25mhz differential crystal oscillator is onboard to provide a reference clock for the optical fiber.

Onboard is a 156.25mhz differential crystal oscillator that gives the transceiver a reference clock.

- **LED Light**

6 leds, 1 power indicator; 1 DONE configuration indicator; 4 user indicators and a pair of panel indicators.

- **Button**

2 user buttons, 1 reset button, and 1 normal IO connected to FPGA

Part 2 FPGA Chip

The development board uses Xilinx's KINTEX UltraSacale chip, model XCKU040-2FFVA1156I. The speed grade is 2 and the temperature grade is industrial grade. This model is FFVA1156 package, 1156 pins, pin spacing 1.0mm. Figure 2-1 shows the chip naming rules of Xilinx KINTEX UltraSacale:

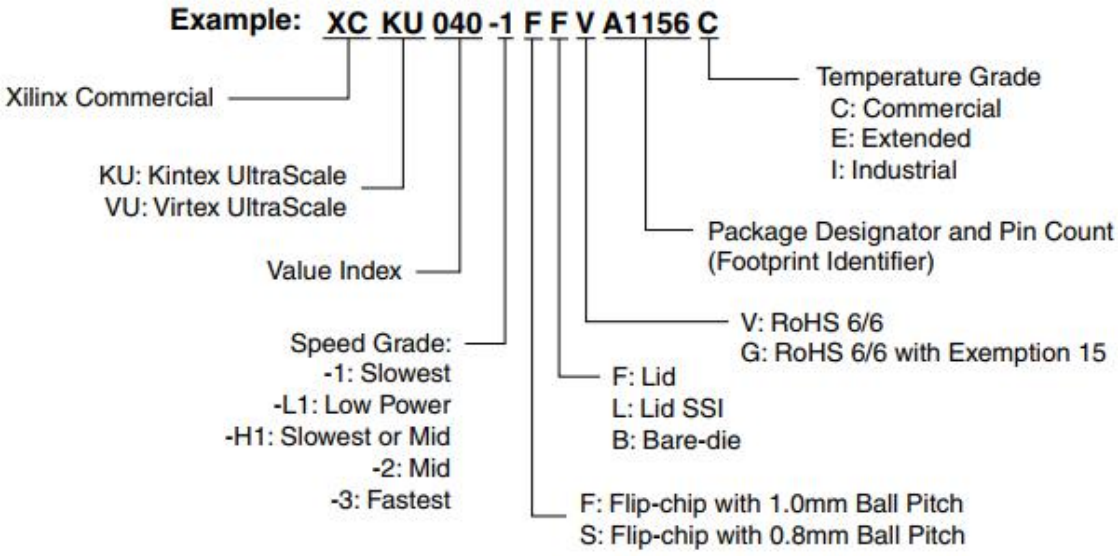


Figure 2-1 KINTEX UltraSacale FPGA

The main parameters of XCKU040 are as follows:

Name	Specific parameters
Logic Cells	530,250
CLB LUTs	242,400
CLB flip-flops	484,800
Block RAM (Mb)	21.1
DSP Slices	1,920
PCIe Gen3 x8	3
GTH Transceiver	20个，16.3Gb/s max
Speed Grade	-2
Temperature Grade	Industrial

Part 3 FPGA power supply system

XCKU040 FPGA power supply has VCCINT, VCCBRAM, VCCAUX, VCCAUX_IO VCCO, VMGTAVCC,VMGTAVTT, VMGTVCCAUX, VMGTAVTTRCAL, VCCADC。**VCCINT** is the FPGA core power supply pin, which needs to be connected to 0.95V; **VCCBRAM** is the power supply pin of FPGA Block RAM, connect to 0.95V; **VCCAUX&VCCAUX_IO** is FPGA auxiliary power supply pin, connect 1.8V; **VCCO** is the voltage of each BANK of FPGA, including BANK0,BANK44~48, BANK64~68. **$V_{MGTAVcc}$** For the supply voltage of GTH and GTY transceiver in FPGA, connect1.0V; **$V_{MGTAVTT}$** Is the terminal voltage of GTH sending and receiving, connected to 1.2V. **$V_{MGTAVTTRCAL}$** Calibrate voltage for transceiver resistor, connected to 1.2V; **V_{CCADC}** Supply voltage for XADC, 1.8V。

Figure 2-2 shows the sequence for powering on the XCKU040 FPGA system

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT}/V_{CCINT_IO}, V_{CCBRAM}, V_{CCAUX}/V_{CCAUX_IO}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT}/V_{CCINT_IO} and V_{CCBRAM} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCINT_IO} must be connected to V_{CCINT}. If V_{CCAUX}/V_{CCAUX_IO} and V_{CCO} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCAUX} and V_{CCAUX_IO} must be connected together. When the current minimums are met, the device powers on after the V_{CCINT}/V_{CCINT_IO}, V_{CCBRAM}, V_{CCAUX}/V_{CCAUX_IO}, and V_{CCO} supplies have all passed through their power-on reset threshold voltages. The device must not be configured until after V_{CCINT} is applied.

V_{CCADC} and V_{REF} can be powered at any time and have no power-up sequencing recommendations.

The recommended power-on sequence to achieve minimum current draw for the GTH or GTY transceivers is V_{CCINT}, $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT}, $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw. If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

Figure 2-2

Part4 DDR4 DRAM

The AXKU040 development board is equipped with four Micron 1GB DDR4 chips, model mt40A512M16LY-062EIT. Four DDR4 SDRAM chips form a 64-bit bus width. Because the four DDR4 chips are connected to the FPGA, DDR4 SDRAM has a maximum operating clock of 1200Mhz, and the four DDR4 storage systems are directly connected to the BANK44, BANK45, and BANK46 interfaces of the FPGA. The following table describes the configuration of DDR4 SDRAM 3-1.

Table 3-1 DDR4 SDRAM configuration

Bit Number	Chip Model	Capacity	Factory
U45,U47,U48,U49	MT40A512M16LY-062EIT	512M x 16bit	Micron

DDR4 hardware design requires strict consideration of signal integrity, we have fully considered the circuit design and PCB design of the matching resistance/terminal resistance, wiring impedance control, line length control, to ensure the high-speed and stable operation of DDR4

Figure 3-1 shows the hardware connections of FPGA and DDR4 DRAM:

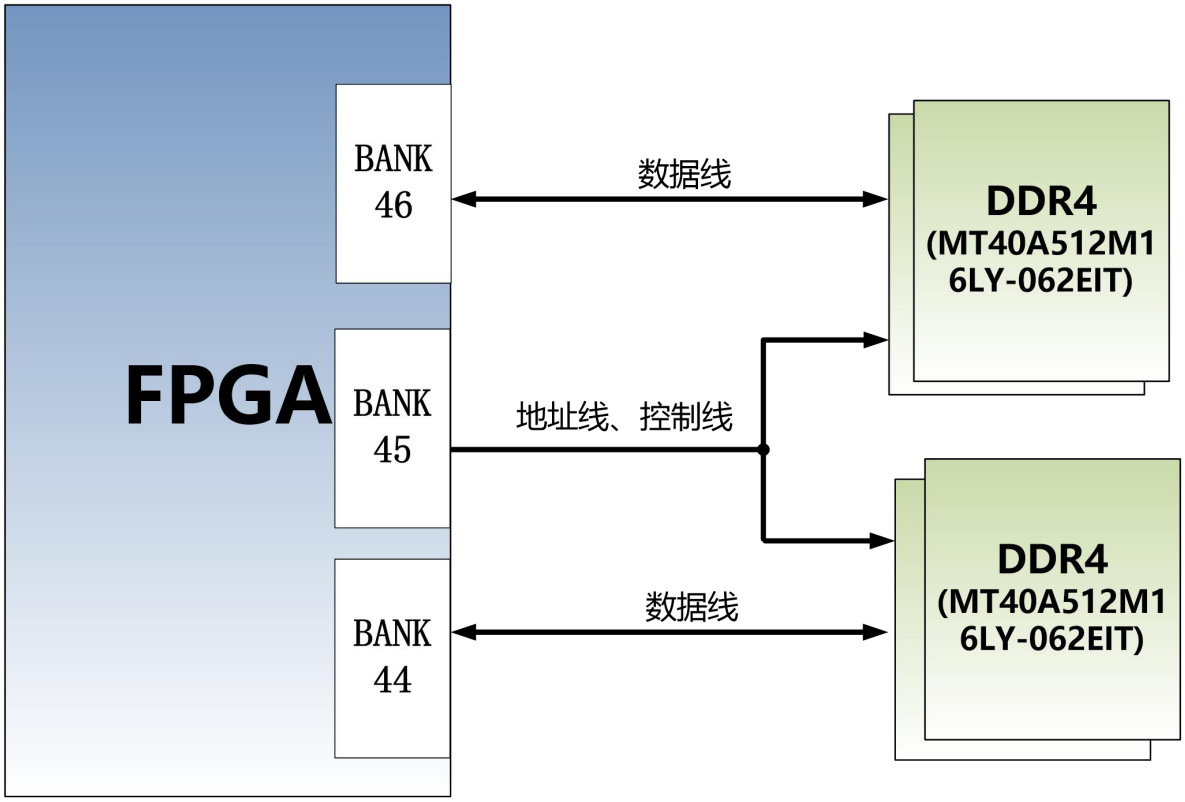


Figure 3-1 DDR4 DRAM

4 DDR4 DRAM pins allocated:

Signal Name	FPGA Pin Name	FPGA Pin
PL_DDR4_DQ0	IO_L3N_T0L_N5_AD15N_44	AE20
PL_DDR4_DQ1	IO_L2N_T0L_N3_44	AG20
PL_DDR4_DQ2	IO_L2P_T0L_N2_44	AF20
PL_DDR4_DQ3	IO_L5P_T0U_N8_AD14P_44	AE22
PL_DDR4_DQ4	IO_L3P_T0L_N4_AD15P_44	AD20
PL_DDR4_DQ5	IO_L6N_T0U_N11_AD6N_44	AG22
PL_DDR4_DQ6	IO_L6P_T0U_N10_AD6P_44	AF22
PL_DDR4_DQ7	IO_L5N_T0U_N9_AD14N_44	AE23
PL_DDR4_DQ8	IO_L8N_T1L_N3_AD5N_44	AF24
PL_DDR4_DQ9	IO_L11P_T1U_N8_GC_44	AJ23
PL_DDR4_DQ10	IO_L8P_T1L_N2_AD5P_44	AF23
PL_DDR4_DQ11	IO_L12N_T1U_N11_GC_44	AH23
PL_DDR4_DQ12	IO_L9N_T1L_N5_AD12N_44	AG25
PL_DDR4_DQ13	IO_L11N_T1U_N9_GC_44	AJ24
PL_DDR4_DQ14	IO_L9P_T1L_N4_AD12P_44	AG24
PL_DDR4_DQ15	IO_L12P_T1U_N10_GC_44	AH22

PL_DDR4_DQ16	IO_L14P_T2L_N2_GC_44	AK22
PL_DDR4_DQ17	IO_L17P_T2U_N8_AD10P_44	AL22
PL_DDR4_DQ18	IO_L15N_T2L_N5_AD11N_44	AM20
PL_DDR4_DQ19	IO_L17N_T2U_N9_AD10N_44	AL23
PL_DDR4_DQ20	IO_L14N_T2L_N3_GC_44	AK23
PL_DDR4_DQ21	IO_L18N_T2U_N11_AD2N_44	AL25
PL_DDR4_DQ22	IO_L15P_T2L_N4_AD11P_44	AL20
PL_DDR4_DQ23	IO_L18P_T2U_N10_AD2P_44	AL24
PL_DDR4_DQ24	IO_L20P_T3L_N2_AD1P_44	AM22
PL_DDR4_DQ25	IO_L23P_T3U_N8_44	AP24
PL_DDR4_DQ26	IO_L20N_T3L_N3_AD1N_44	AN22
PL_DDR4_DQ27	IO_L21N_T3L_N5_AD8N_44	AN24
PL_DDR4_DQ28	IO_L24P_T3U_N10_44	AN23
PL_DDR4_DQ29	IO_L23N_T3U_N9_44	AP25
PL_DDR4_DQ30	IO_L24N_T3U_N11_44	AP23
PL_DDR4_DQ31	IO_L21P_T3L_N4_AD8P_44	AM24
PL_DDR4_DQ32	IO_L2P_T0L_N2_46	AM26
PL_DDR4_DQ33	IO_L6P_T0U_N10_AD6P_46	AJ28
PL_DDR4_DQ34	IO_L2N_T0L_N3_46	AM27
PL_DDR4_DQ35	IO_L6N_T0U_N11_AD6N_46	AK28
PL_DDR4_DQ36	IO_L5P_T0U_N8_AD14P_46	AH27
PL_DDR4_DQ37	IO_L5N_T0U_N9_AD14N_46	AH28
PL_DDR4_DQ38	IO_L3P_T0L_N4_AD15P_46	AK26
PL_DDR4_DQ39	IO_L3N_T0L_N5_AD15N_46	AK27
PL_DDR4_DQ40	IO_L9N_T1L_N5_AD12N_46	AN28
PL_DDR4_DQ41	IO_L12N_T1U_N11_GC_46	AM30
PL_DDR4_DQ42	IO_L8P_T1L_N2_AD5P_46	AP28
PL_DDR4_DQ43	IO_L11N_T1U_N9_GC_46	AM29
PL_DDR4_DQ44	IO_L9P_T1L_N4_AD12P_46	AN27
PL_DDR4_DQ45	IO_L12P_T1U_N10_GC_46	AL30
PL_DDR4_DQ46	IO_L11P_T1U_N8_GC_46	AL29
PL_DDR4_DQ47	IO_L8N_T1L_N3_AD5N_46	AP29
PL_DDR4_DQ48	IO_L14P_T2L_N2_GC_46	AK31
PL_DDR4_DQ49	IO_L18P_T2U_N10_AD2P_46	AH34
PL_DDR4_DQ50	IO_L14N_T2L_N3_GC_46	AK32

PL_DDR4_DQ51	IO_L15N_T2L_N5_AD11N_46	AJ31
PL_DDR4_DQ52	IO_L15P_T2L_N4_AD11P_46	AJ30
PL_DDR4_DQ53	IO_L17P_T2U_N8_AD10P_46	AH31
PL_DDR4_DQ54	IO_L18N_T2U_N11_AD2N_46	AJ34
PL_DDR4_DQ55	IO_L17N_T2U_N9_AD10N_46	AH32
PL_DDR4_DQ56	IO_L21P_T3L_N4_AD8P_46	AN31
PL_DDR4_DQ57	IO_L24P_T3U_N10_46	AL34
PL_DDR4_DQ58	IO_L23N_T3U_N9_46	AN32
PL_DDR4_DQ59	IO_L20P_T3L_N2_AD1P_46	AN33
PL_DDR4_DQ60	IO_L23P_T3U_N8_46	AM32
PL_DDR4_DQ61	IO_L24N_T3U_N11_46	AM34
PL_DDR4_DQ62	IO_L21N_T3L_N5_AD8N_46	AP31
PL_DDR4_DQ63	IO_L20N_T3L_N3_AD1N_46	AP33
PL_DDR4_DM0	IO_L1P_T0L_N0_DBC_44	AD21
PL_DDR4_DM1	IO_L7P_T1L_N0_QBC_AD13P_44	AE25
PL_DDR4_DM2	IO_L13P_T2L_N0_GC_QBC_44	AJ21
PL_DDR4_DM3	IO_L19P_T3L_N0_DBC_AD9P_44	AM21
PL_DDR4_DM4	IO_L1P_T0L_N0_DBC_46	AH26
PL_DDR4_DM5	IO_L7P_T1L_N0_QBC_AD13P_46	AN26
PL_DDR4_DM6	IO_L13P_T2L_N0_GC_QBC_46	AJ29
PL_DDR4_DM7	IO_L19P_T3L_N0_DBC_AD9P_46	AL32
PL_DDR4_DQS0_P	IO_L4P_T0U_N6_DBC_AD7P_44	AG21
PL_DDR4_DQS0_N	IO_L4N_T0U_N7_DBC_AD7N_44	AH21
PL_DDR4_DQS1_P	IO_L10P_T1U_N6_QBC_AD4P_44	AH24
PL_DDR4_DQS1_N	IO_L10N_T1U_N7_QBC_AD4N_44	AJ25
PL_DDR4_DQS2_P	IO_L16P_T2U_N6_QBC_AD3P_44	AJ20
PL_DDR4_DQS2_N	IO_L16N_T2U_N7_QBC_AD3N_44	AK20
PL_DDR4_DQS3_P	IO_L22P_T3U_N6_DBC_AD0P_44	AP20
PL_DDR4_DQS3_N	IO_L22N_T3U_N7_DBC_AD0N_44	AP21
PL_DDR4_DQS4_P	IO_L4P_T0U_N6_DBC_AD7P_46	AL27
PL_DDR4_DQS4_N	IO_L4N_T0U_N7_DBC_AD7N_46	AL28
PL_DDR4_DQS5_P	IO_L10P_T1U_N6_QBC_AD4P_46	AN29
PL_DDR4_DQS5_N	IO_L10N_T1U_N7_QBC_AD4N_46	AP30
PL_DDR4_DQS6_P	IO_L16P_T2U_N6_QBC_AD3P_46	AH33
PL_DDR4_DQS6_N	IO_L16N_T2U_N7_QBC_AD3N_46	AJ33

PL_DDR4_DQS7_P	IO_L22P_T3U_N6_DBC_AD0P_46	AN34
PL_DDR4_DQS7_N	IO_L22N_T3U_N7_DBC_AD0N_46	AP34
PL_DDR4_A0	IO_L18N_T2U_N11_AD2N_45	AG14
PL_DDR4_A1	IO_L23N_T3U_N9_45	AF17
PL_DDR4_A2	IO_L20P_T3L_N2_AD1P_45	AF15
PL_DDR4_A3	IO_L16N_T2U_N7_QBC_AD3N_45	AJ14
PL_DDR4_A4	IO_L19N_T3L_N1_DBC_AD9N_45	AD18
PL_DDR4_A5	IO_L15P_T2L_N4_AD11P_45	AG17
PL_DDR4_A6	IO_L23P_T3U_N8_45	AE17
PL_DDR4_A7	IO_L11N_T1U_N9_GC_45	AK18
PL_DDR4_A8	IO_L24P_T3U_N10_45	AD16
PL_DDR4_A9	IO_L13P_T2L_N0_GC_QBC_45	AH18
PL_DDR4_A10	IO_L19P_T3L_N0_DBC_AD9P_45	AD19
PL_DDR4_A11	IO_L24N_T3U_N11_45	AD15
PL_DDR4_A12	IO_L14P_T2L_N2_GC_45	AH16
PL_DDR4_A13	IO_L10N_T1U_N7_QBC_AD4N_45	AL17
PL_DDR4_BA0	IO_L18P_T2U_N10_AD2P_45	AG15
PL_DDR4_BA1	IO_L10P_T1U_N6_QBC_AD4P_45	AL18
PL_DDR4_BG0	IO_L16P_T2U_N6_QBC_AD3P_45	AJ15
PL_DDR4_WE_B	IO_L9N_T1L_N5_AD12N_45	AL15
PL_DDR4_RAS_B	IO_L8N_T1L_N3_AD5N_45	AM19
PL_DDR4_CAS_B	IO_L8P_T1L_N2_AD5P_45	AL19
PL_DDR4_CKE	IO_L14N_T2L_N3_GC_45	AJ16
PL_DDR4_ACT_B	IO_L21N_T3L_N5_AD8N_45	AF18
PL_DDR4_CLK_N	IO_L22N_T3U_N7_DBC_AD0N_45	AE15
PL_DDR4_CLK_P	IO_L22P_T3U_N6_DBC_AD0P_45	AE16
PL_DDR4_CS_B	IO_L21P_T3L_N4_AD8P_45	AE18
PL_DDR4_OTD	IO_L17P_T2U_N8_AD10P_45	AG19
PL_DDR4_PAR	IO_L20N_T3L_N3_AD1N_45	AF14
PL_DDR4_RST	IO_L15N_T2L_N5_AD11N_45	AG16

Prat 5 QSPI Flash

The development board is equipped with two 256MBit quad-SPI FLASH chips, model mt25QU256ABa1EW9-0SIT, which uses the 1.8V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, it can store FPGA configuration Bin files and other user data files in use. Table 4-1 lists the QSPI FLASH models and related parameters.

Position	Model	Capacity	Factory
U5	MT25QU256ABA1EW9-0SIT	256Mbit	Micron
U11	MT25QU256ABA1EW9-0SIT	256Mbit	Micron

Table 4-1 QSPI Flash models and parameters

QSPI FLASH is connected to the pins of BANK0 and BANK65 of FPGA chip, wherein the clock pin is connected to the CCLK0 of BANK0. Figure 4-2 shows the connection diagram of QSPI FLASH and FPGA chip.

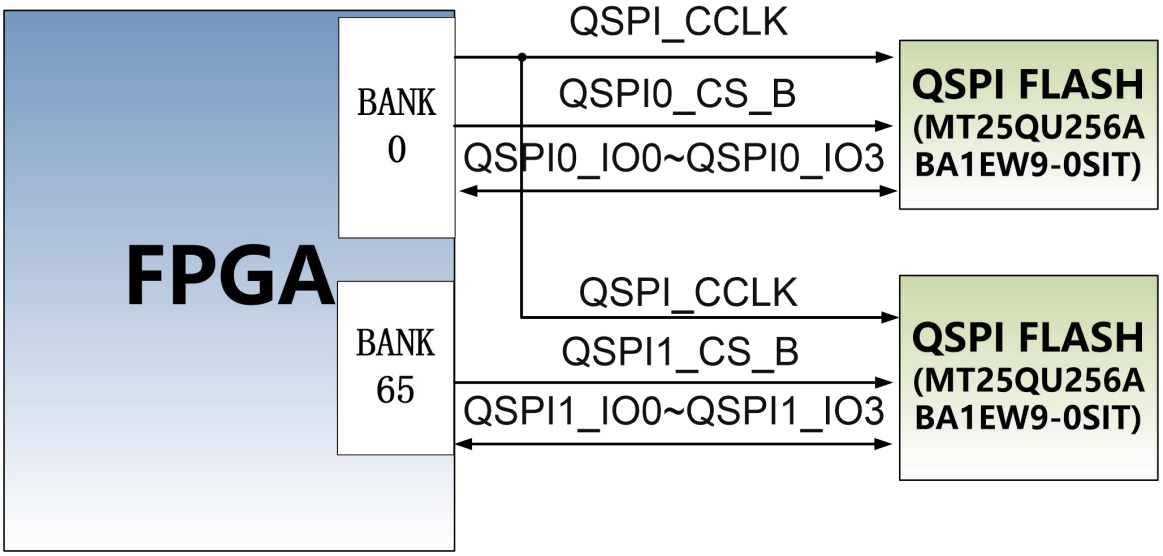


Figure 4-2 QSPI Flash

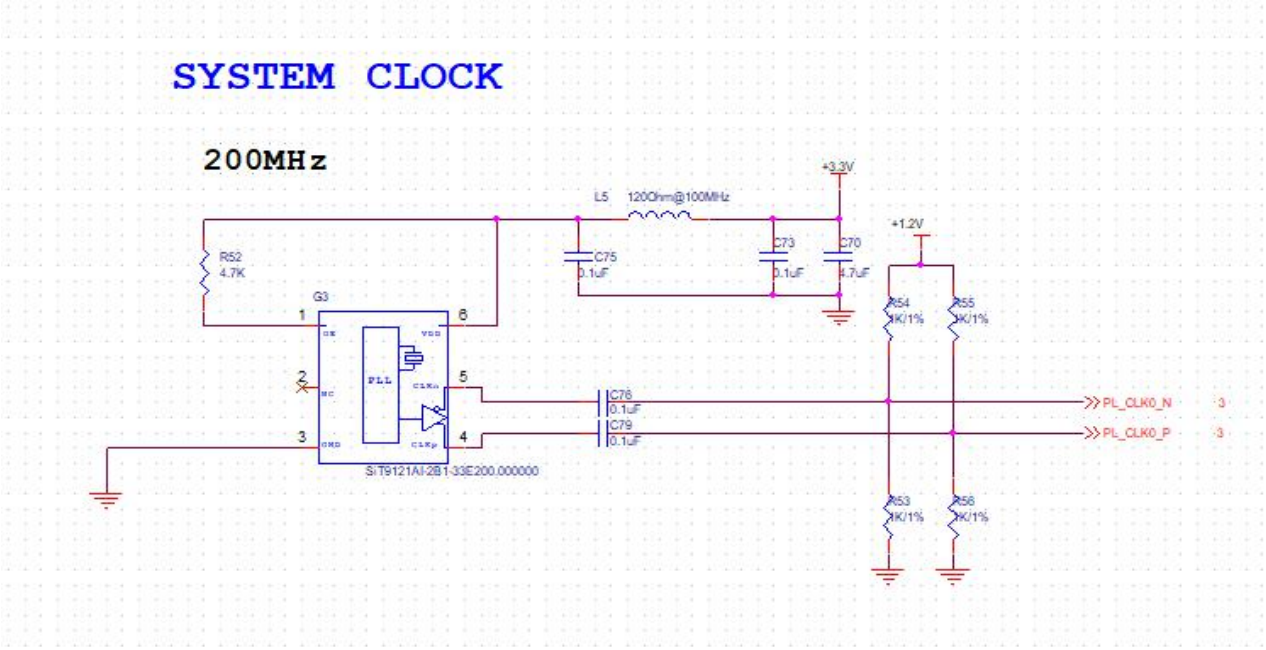
Signal Name	FPGA Pin Name	FPGA Pin Number
QSPI_CCLK	CCLK_0	AA9
QSPI0_CS_B	RDWR_FCS_B_0	U7

QSPI0_IO0	D00_MOSI_0	AC7
QSPI0_IO1	D01_DIN_0	AB7
QSPI0_IO2	D02_0	AA7
QSPI0_IO3	D03_0	Y7

Signal Name	FPGA Pin Name	FPGA Pin Number
QSPI1_CS_B	IO_L2N_T0L_N3_FWE_FCS2_B_65	G26
QSPI1_IO0	IO_L22P_T3U_N6_DBC_AD0P_D04_65	M20
QSPI1_IO1	IO_L22N_T3U_N7_DBC_AD0N_D05_65	L20
QSPI1_IO2	IO_L21P_T3L_N4_AD8P_D06_65	R21
QSPI1_IO3	IO_L21N_T3L_N5_AD8N_D07_65	R22

Part6 Clock configuration

A differential 200MHz clock source is provided on the FPGA development board to provide the system clock to the FPGA。The crystal oscillator differential output is connected to FPGA BANK45, which can be used to drive the DDR controller working clock in FPGA and other user logic circuits



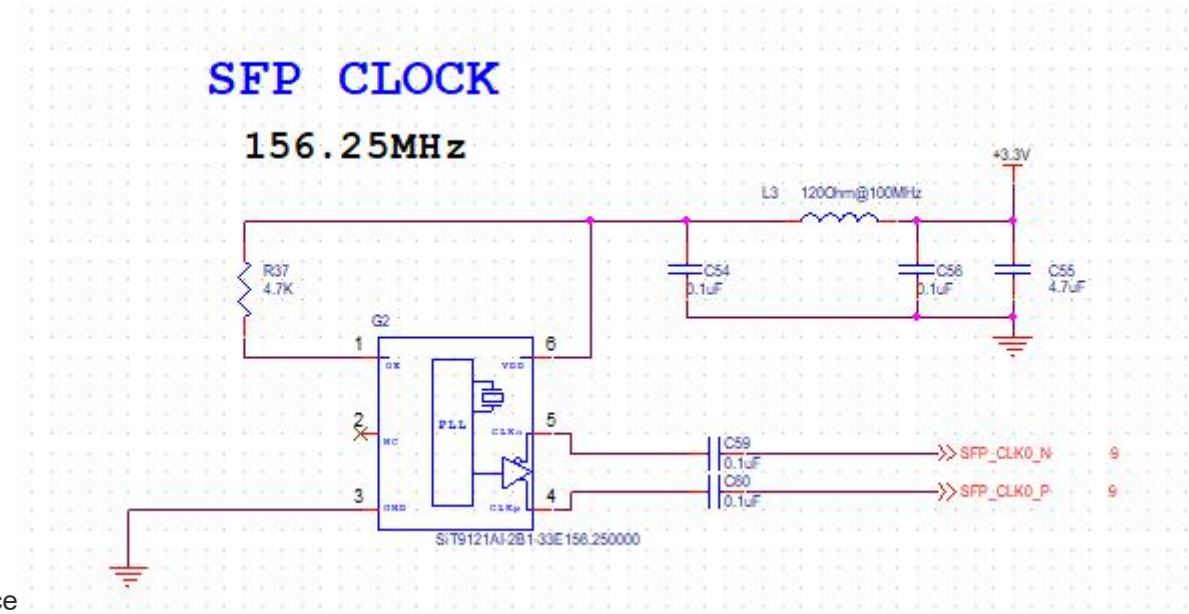
Figuer 5-1

System Clock pin assignments:

Signal Name	FPGA Pin
PL_CLK0_P	AK17
PL_CLK0_N	AK16

156.25mhz differential clock source

A differential 156.25mhz clock source is provided on the board to provide the clock for the transceiver GTH. The crystal oscillator differential output is connected to FPGA BANK226, this clock is used for the clock required for 2 channels of optical fiber. Figure 5-2 shows the working principle of the clock



source

Figure 5-2

Clock pin assignments:

Signal Name	FPGA Pin
SFP_CLK0_P	V6
SFP_CLK0_N	V5

156.25Mhz Differential clock source

A differential 156.25mhz clock source is provided on the board to provide the clock for the transceiver GTH. Crystal oscillator differential output connected to FPGA BANK228. Figure 5-3 shows the working principle of the clock source

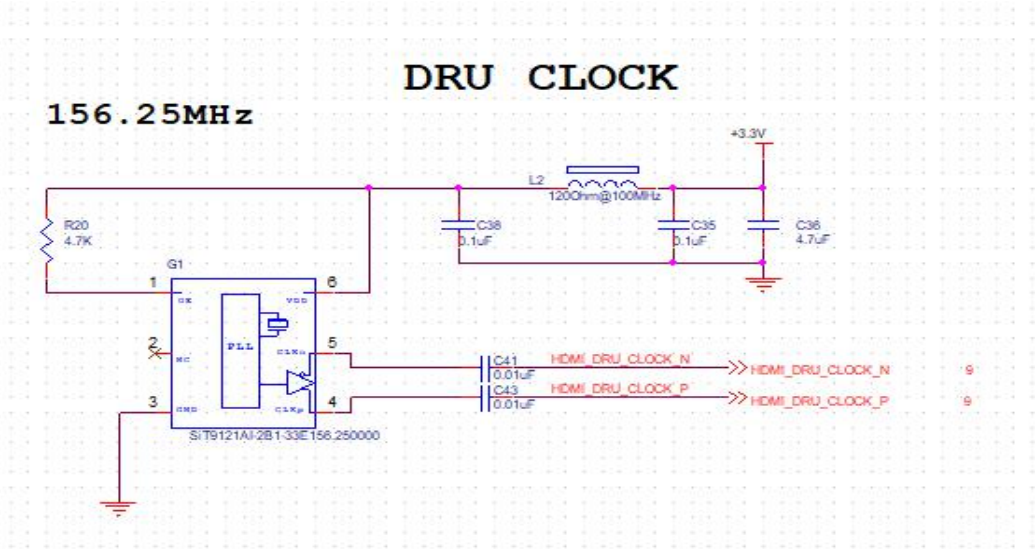


Figure 5-3

Clock pin assignments:

Signal Name	FPGA Pin
HDMI_DRU_CLOCK_P	H6
HDMI_DRU_CLOCK_N	H5

Part 7 USB to Serial Port

AXKU040 development board is equipped with a Uart to USB interface for development board serial communication and debugging. The conversion chip is usB-UAR chip of Silicon Labs CP2102GM, and a level conversion chip is used to connect CP2102 serial port chip and FPGA to adapt to different FPGA BANK voltages. USB interface with MINI USB interface, you can use a USB cable to connect it to the USB port of the PC for serial port data communication of the development board. The schematic diagram of USB Uart circuit design is shown in Figure 6-1 below:

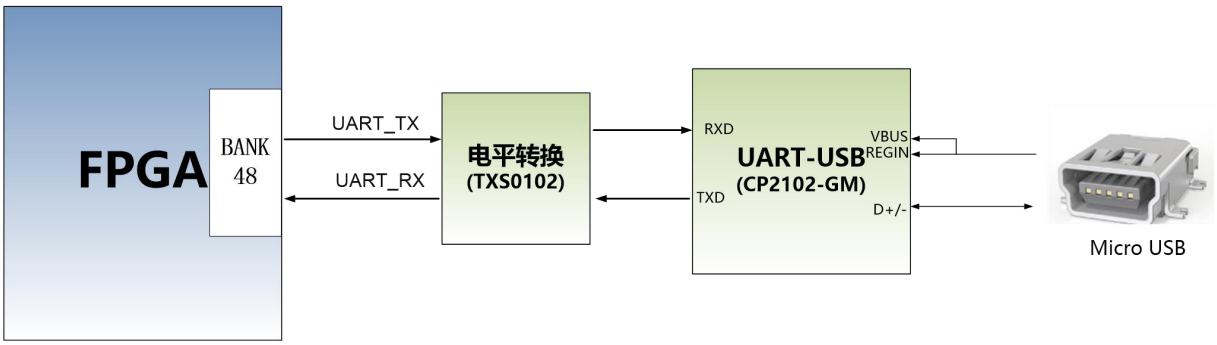


图 6-1 USB to serial port schematic

USB to serial port pin assignment:

Signal Name	FPGA Name	FPGA pin	Description
UART_RXD	IO_L7N_T1L_N1_QBC_AD13N_48	AG32	Uart Data input
UART_TXD	IO_L7P_T1L_N0_QBC_AD13P_48	AG31	Uart Data output

Part 8 SFP+Fiber Interface

The AXKU040 development board has four SFP optical ports. Users can purchase SFP optical modules (1.25G, 2.5g and 10G optical modules on the market) to plug into these four optical ports for optical data communication. Four optical fiber interfaces are respectively connected with four RX/TX channels of BANK24 GTH transceiver of FPGA. Both TX and RX signals are connected to FPGA and optical module through straight capacitor in differential signal mode. The data rate of each CHANNEL TX sending and RX receiving is up to 12.5GB /s. The reference clock for the BANK224's GXH transceiver is provided by the differential crystal oscillator 125M.

Figure 7-1 shows the design of FPGA and SFP optical fibers:

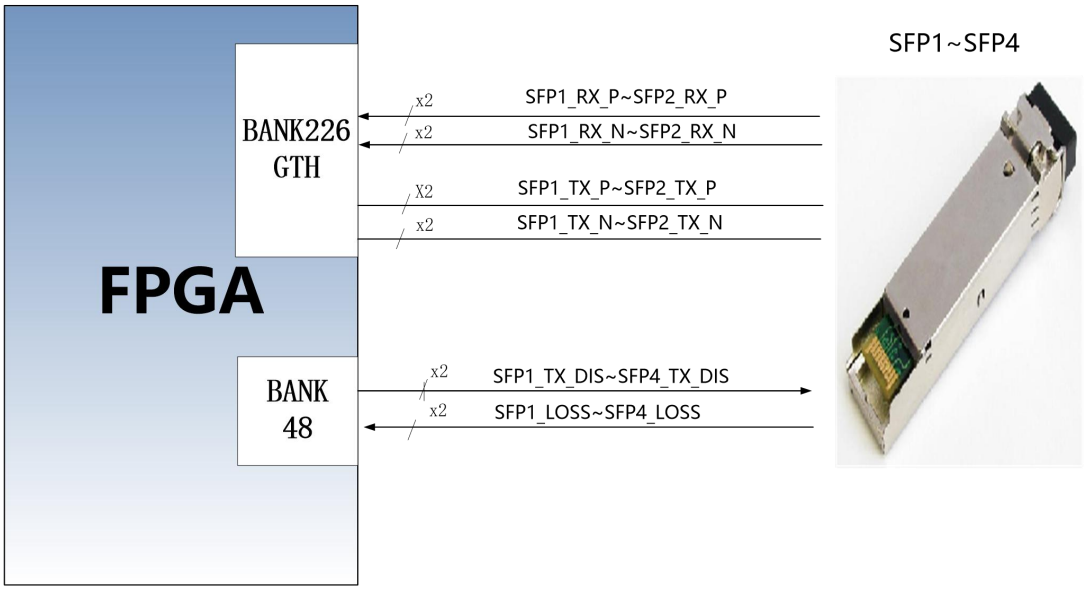


Figure 7-1

The 1st fiber interface FPGA pin assignment is as follows:

Signal Name	FPGA pin	Description
SFP1_TX_P	AA4	SFP1 Data Transfer Positive
SFP1_TX_N	AA3	SFP1 Data Transfer Negative
SFP1_RX_P	Y2	SFP1 Data Receiver Positive
SFP1_RX_N	Y1	SFP1 Data Receiver Negative
SFP1_TX_DIS	AC22	SFP1 Optical Transfer Disable,

		active high
SFP1_LOSS	AF28	SFP1 Optical LOSS,High level means no light signal is received

The 2nd fiber interface FPGA pin assignment is as follows:

Signal Name	FPGA PIN	Description
SFP2_TX_P	R4	SFP2 Data Transfer Positive
SFP2_TX_N	R3	SFP2 Data Transfer Negative
SFP2_RX_P	P2	SFP2 Data Receiver Positive
SFP2_RX_N	P1	SFP2 Data Receiver Negative
SFP2_TX_DIS	AC21	SFP2Optical Transfer Disable, active high
SFP2_LOSS	AE28	SFP2 Optical LOSS,High level means no light signal is received

Part 9 Ethernet interface

AXKU041 has one gigabit Ethernet interface, and the GPHY chip uses Micrel's KSZ9031RNX Ethernet chip to provide network communication services. KSZ9031RNX chip supports 10/100/1000 Mbps network transmission rate, through RGMII interface with the MAC layer of the system for data communication. KSZ9031RNX supports MDI/MDX adaptive, various speed adaptive, Master/Slave adaptive, support MDIO bus PHY register management.

When KSZ9031RNX is powered on, it detects the level status of some specific IO to determine its working mode. Table 3-5-1 describes the default Settings of the GPHY chip after it is powered on

Signal Name	Description
PHYAD[2:0]	MDIO/MDC PHY address of mode
CLK125_EN	Enable 125Mhz clock output selection
LED_MODE	LED light mode configuration
MODE0~MODE3	Link auto-adaptation and full-duplex configuration

When the network is connected to gigabit Ethernet, the PHY chip KSZ9031RNX's data transfer is communicated over the RGMII bus with a transmission clock of 125Mhz, and the data is sampled on the rising edge and falling edge of the clock.

When the network is connected to 100m Ethernet, the PHY chip KSZ9031RNX's data transfer communicates over the RMII bus with a transmission clock of 25Mhz. Data is sampled on the rising and falling edges of the clock.

Figure 8-1 shows the Ethernet PHY chip connection:

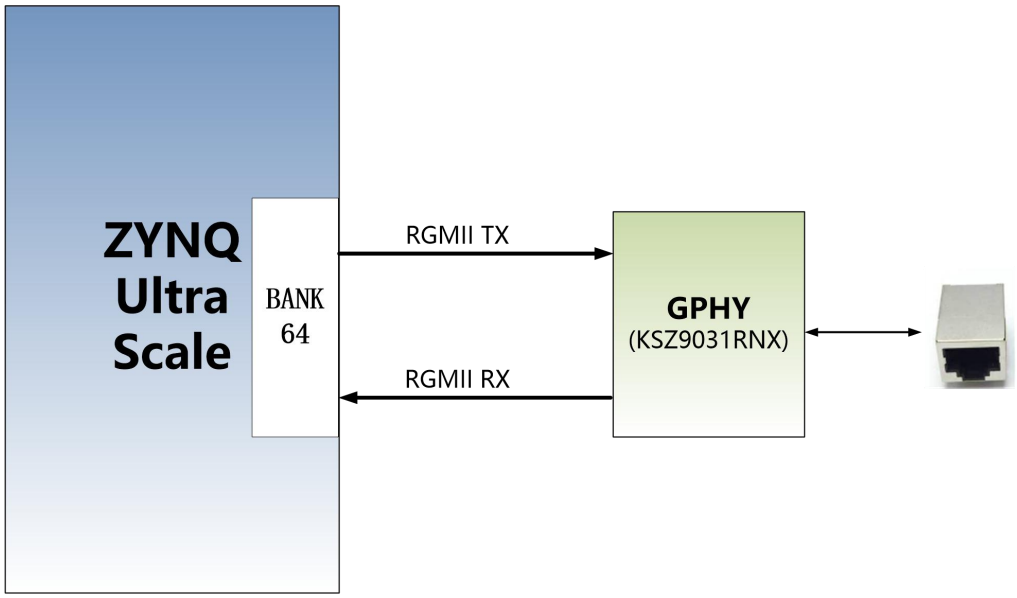


Figure 8-1

Ethernet FPGA pins are assigned as follows:

Signal Name	PIN Name	FPGA PIN
PHY_GTXC	IO_L22P_T3U_N6_DBC_AD0P_64	AN8
PHY_TXD0	IO_L22N_T3U_N7_DBC_AD0N_64	AP8
PHY_TXD1	IO_L24N_T3U_N11_64	AL8
PHY_TXD2	IO_L20N_T3L_N3_AD1N_64	AP9
PHY_TXD3	IO_L21N_T3L_N5_AD8N_64	AL9
PHY_TXEN	IO_L20P_T3L_N2_AD1P_64	AN9
PHY_RXC	IO_L14P_T2L_N2_GC_64	AF9
PHY_RXD0	IO_L23N_T3U_N9_64	AJ8
PHY_RXD1	IO_L23P_T3U_N8_64	AJ9
PHY_RXD2	IO_L24P_T3U_N10_64	AK8
PHY_RXD3	IO_L21P_T3L_N4_AD8P_64	AK10
PHY_RXDV	IO_L14N_T2L_N3_GC_64	AG9
PHY_MDC	IO_T1U_N12_64	AJ11
PHY_MDIO	IO_T2U_N12_64	AJ10
PHY_RESET	IO_T0U_N12_64	AK11

Part 10 PCIE X8 Interface

AXKU041 is equipped with a pci 3.0x8 interface. Eight pairs of transceivers are connected to the gold finger of PCIEx8 to achieve data communication between PCIEx8, pci ex4, PCIex2 and PCIex1.

The transceiver signal of PCIe interface is directly connected with GTH transceiver of FPGA BANK224 and BANK225. Eight TX signals and RX signals are connected to the transceiver of FPGA in differential signal mode, and the single-channel communication rate can be up to 8Gbps bandwidth.

Figure 9-1 shows the design of PCIe interfaces on the development board, where TX signals are connected in AC coupling mode.

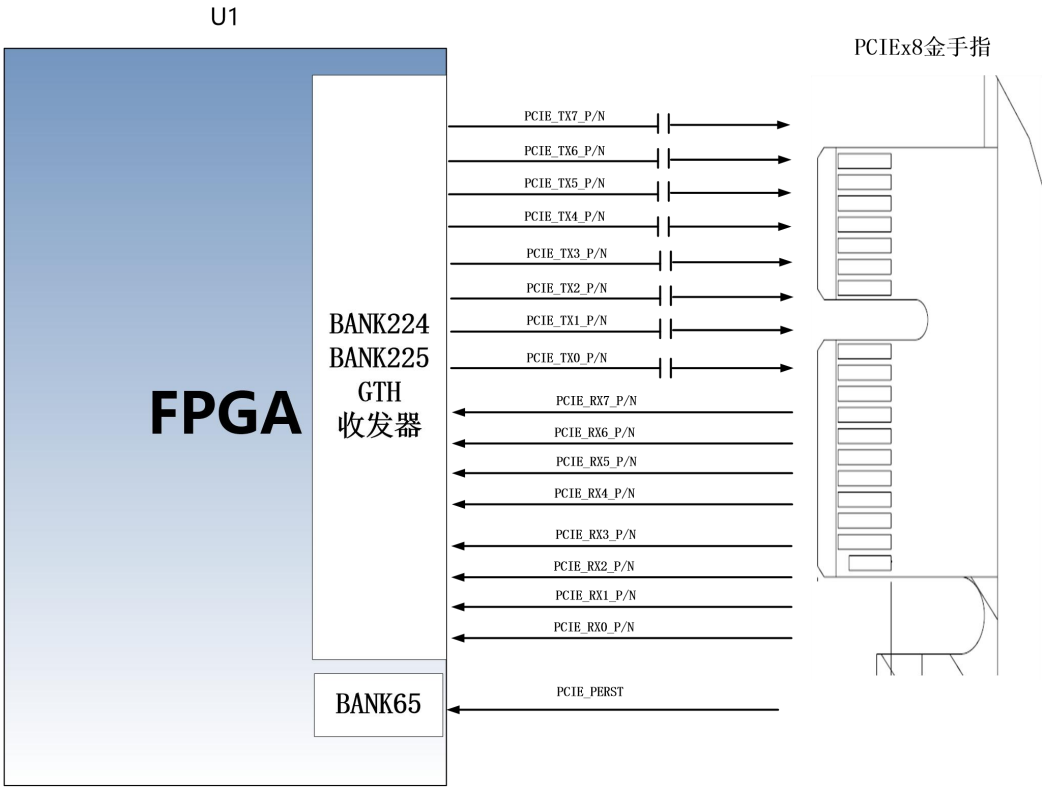


Figure 9-1

The PCIe X8 FPGA pins are assigned as follows:

Signal Name	FPGA Name	FPGA PIN
PCIE_RX0_N	MGTHRXN3_225	AB1
PCIE_RX0_P	MGTHRXP3_225	AB2
PCIE_RX1_N	MGTHRXN2_225	AD1

PCIE_RX1_P	MGTHRXP2_225	AD2
PCIE_RX2_N	MGTHRXN1_225	AF1
PCIE_RX2_P	MGTHRXP1_225	AF2
PCIE_RX3_N	MGTHRXN0_225	AH1
PCIE_RX3_P	MGTHRXP0_225	AH2
PCIE_RX4_N	MGTHRXN3_224	AJ3
PCIE_RX4_P	MGTHRXP3_224	AJ4
PCIE_RX5_N	MGTHRXN2_224	AK1
PCIE_RX5_P	MGTHRXP2_224	AK2
PCIE_RX6_N	MGTHRXN1_224	AM1
PCIE_RX6_P	MGTHRXP1_224	AM2
PCIE_RX7_N	MGTHRXN0_224	AP1
PCIE_RX7_P	MGTHRXP0_224	AP2
PCIE_TX0_N	MGTHTXN3_225	AC3
PCIE_TX0_P	MGTHTXP3_225	AC4
PCIE_TX1_N	MGTHTXN2_225	AE3
PCIE_TX1_P	MGTHTXP2_225	AE4
PCIE_TX2_N	MGTHTXN1_225	AG3
PCIE_TX2_P	MGTHTXP1_225	AG4
PCIE_TX3_N	MGTHTXN0_225	AH5
PCIE_TX3_P	MGTHTXP0_225	AH6
PCIE_TX4_N	MGTHTXN3_224	AK5
PCIE_TX4_P	MGTHTXP3_224	AK6
PCIE_TX5_N	MGTHTXN2_224	AL3
PCIE_TX5_P	MGTHTXP2_224	AL4
PCIE_TX6_N	MGTHTXN1_224	AM5
PCIE_TX6_P	MGTHTXP1_224	AM6
PCIE_TX7_N	MGTHTXN0_224	AN3
PCIE_TX7_P	MGTHTXP0_224	AN4
PCIE_CLK_N	MGTREFCLK0N_225	AB5
PCIE_CLK_P	MGTREFCLK0P_225	AB6
PCIE_PERST	IO_T3U_N12_PERSTN0_65	K22

Part 11 FMC connector

AXKU041 development board has 2-channel standard FMC LPC expansion port and 1-channel standard FMC HPC expansion port, which can be connected to XILINX or our various FMC modules (HDMI input-output module, bineye camera module, high-speed AD module).

The LPC FMC1 expansion port has 33 pairs of differential signals, which are respectively connected to THE IO of BANK47 and BANK48 of FPGA chip. The IO level of BANK47 and BANK48 is 1.8V and cannot be modified.

The LPC FMC2 expansion port has 33 pairs of differential signals, which are respectively connected to THE IO of BANK64 and BANK65 of FPGA chip. The IO level is 1.8V and cannot be modified. 1 Pair speed GTH transceiver signal is connected to BNAK226.

The FMC HPC expansion port contains 57 pairs of differential IO signals, which are connected to FPGA chips BANK66, BANK67 and BANK68 respectively. The voltage standard bit is 1.8V. The 8-channel high-speed GTH transceiver signal is connected to THE IO of BANK227 and BANK228 FPGA chip.

Figure 10-1 and 10-2 show the schematic diagram of the FPGA and FMC LPC connectors:

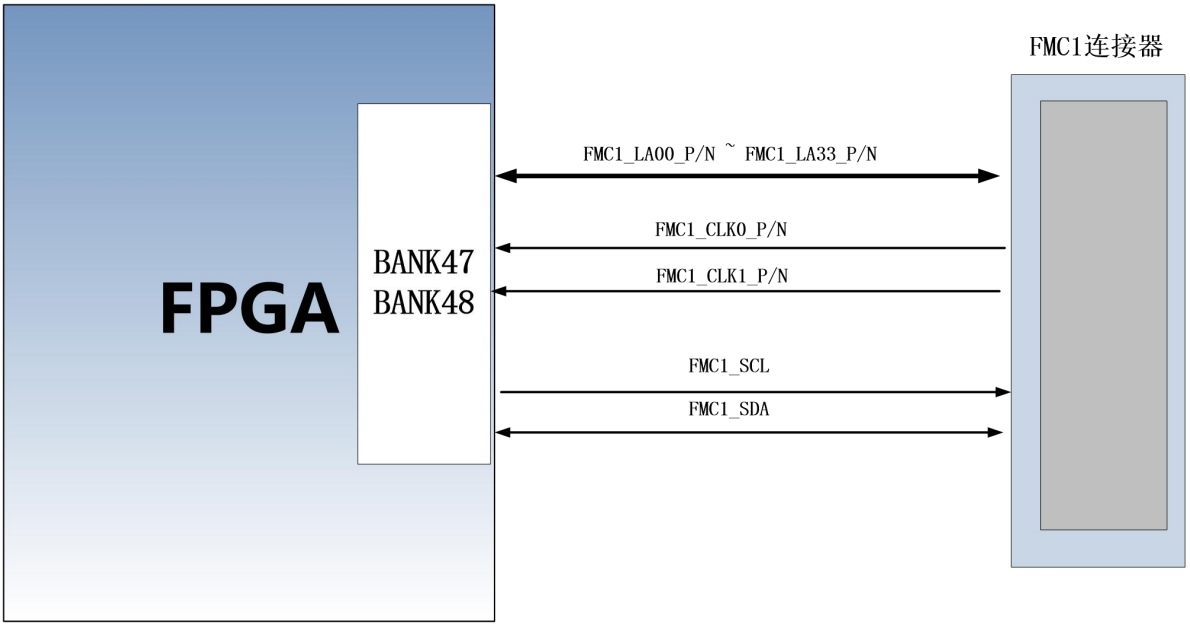


Figure 10-1

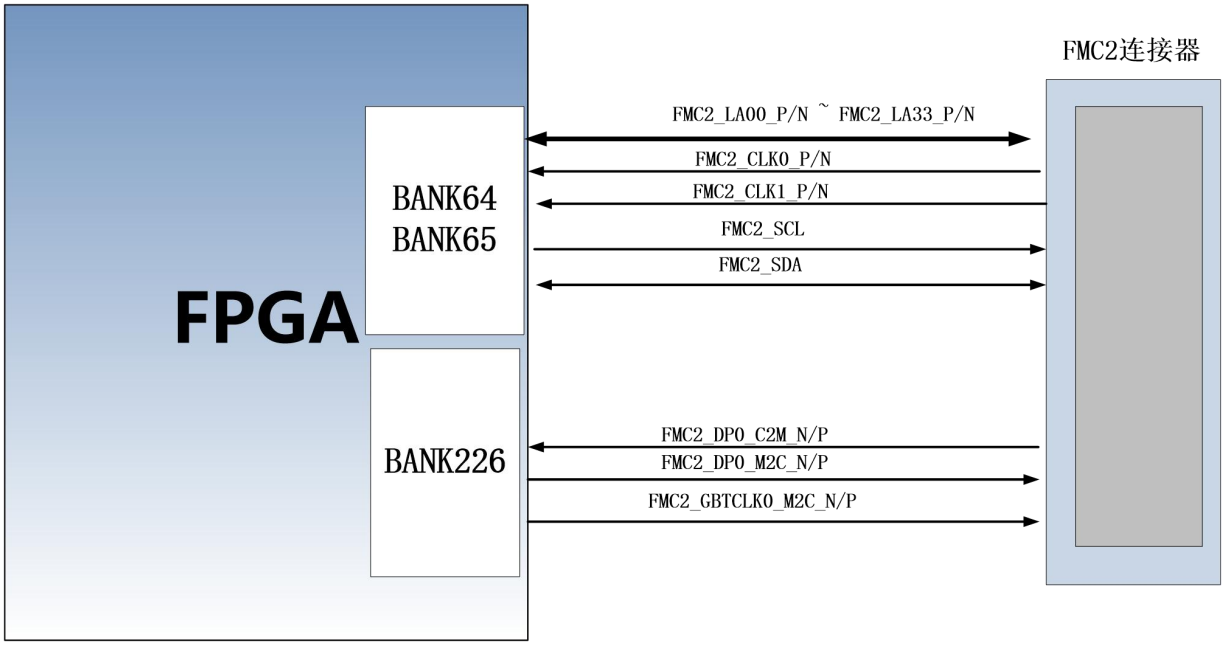


Figure 10-2

Figure 9-3 shows the schematic diagram of the HPC connector of FPGA and FMC3:

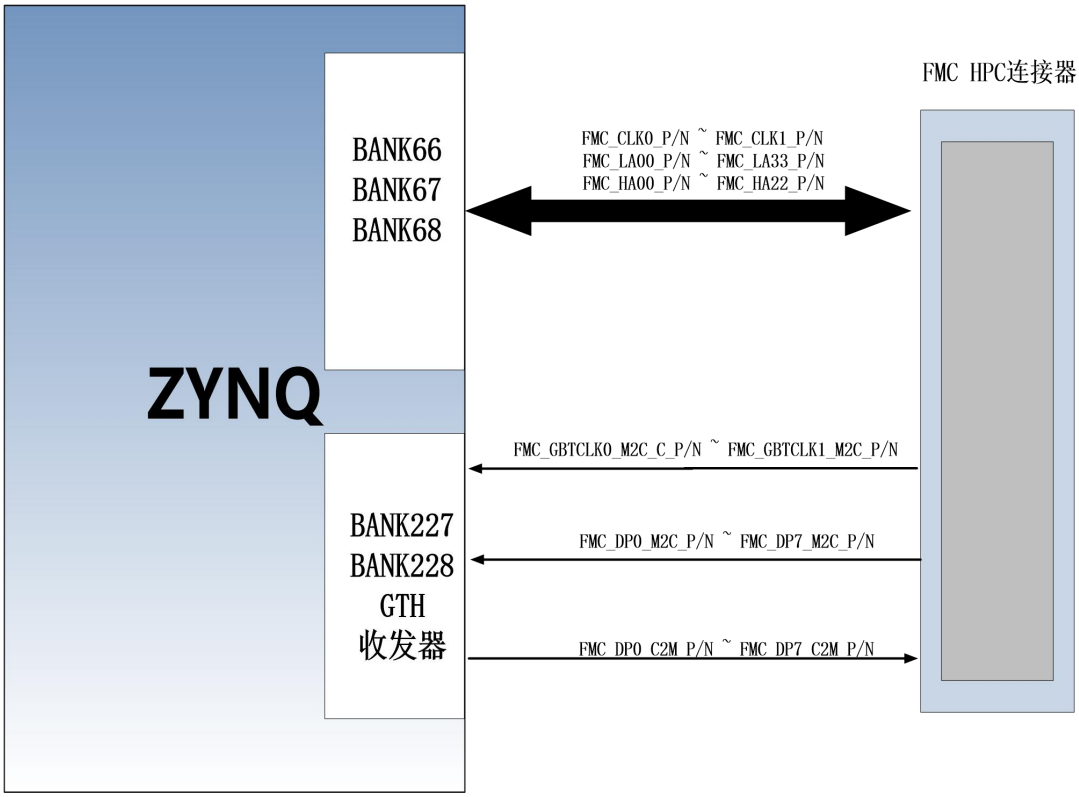


Figure 10-3 HPC FMC3

FMC 1st LPC Connectors Pin Assignment:

Signal Name	FPGA Name	FPGA PIN	Description
FMC1_LPC_CLK0_P	IO_L13P_T2L_N0_GC_QBC_47	W23	FMC reference 1st reference clock P
FMC1_LPC_CLK0_N	IO_L13N_T2L_N1_GC_QBC_47	W24	FMC reference 1st reference clock N
FMC1_LPC_CLK1_P	IO_L11P_T1U_N8_GC_48	AD30	FMC reference 2nd reference clock P
FMC1_LPC_CLK1_N	IO_L11N_T1U_N9_GC_48	AD31	FMC reference 2nd reference clock N
FMC1_LPC_LA00_CC_P	IO_L11P_T1U_N8_GC_47	Y23	FMC reference 0th channel data (clock) P
FMC1_LPC_LA00_CC_N	IO_L11N_T1U_N9_GC_47	AA23	FMC reference 0th channel data (clock) N
FMC1_LPC_LA01_CC_P	IO_L12P_T1U_N10_GC_47	AA24	FMC reference 1st channel data (clock) P
FMC1_LPC_LA01_CC_N	IO_L12N_T1U_N11_GC_47	AA25	FMC reference 1st channel data (clock) N
FMC1_LPC_LA02_P	IO_L2P_T0L_N2_47	AD25	FMC reference 2nd channel data P
FMC1_LPC_LA02_N	IO_L2N_T0L_N3_47	AD26	FMC reference 2nd channel data N
FMC1_LPC_LA03_P	IO_L4P_T0U_N6_DBC_AD7P_47	AC26	FMC reference 3rd channel data P
FMC1_LPC_LA03_N	IO_L4N_T0U_N7_DBC_AD7N_47	AC27	FMC reference 3rd channel data N
FMC1_LPC_LA04_P	IO_L6P_T0U_N10_AD6P_47	AB25	FMC reference 4th channel data P
FMC1_LPC_LA04_N	IO_L6N_T0U_N11_AD6N_47	AB26	FMC reference 4th channel data N
FMC1_LPC_LA05_P	IO_L21P_T3L_N4_AD8P_47	W28	FMC reference 5th

			channeldata P
FMC1_LPC_LA05_N	IO_L21N_T3L_N5_AD8N_47	Y28	**FMC reference 5th channel data N**
FMC1_LPC_LA06_P	IO_L19P_T3L_N0_DBC_AD9P_47	V27	**FMC reference 6th channel data P**
FMC1_LPC_LA06_N	IO_L19N_T3L_N1_DBC_AD9N_47	V28	**FMC reference 6th channel data N**
FMC1_LPC_LA07_P	IO_L9P_T1L_N4_AD12P_47	AA20	**FMC reference 7th channel data P**
FMC1_LPC_LA07_N	IO_L9N_T1L_N5_AD12N_47	AB20	**FMC reference 7th channel data N**
FMC1_LPC_LA08_P	IO_L7P_T1L_N0_QBC_AD13P_47	AA22	**FMC reference 8th channel data P**
FMC1_LPC_LA08_N	IO_L7N_T1L_N1_QBC_AD13N_47	AB22	**FMC reference 8th channel data N**
FMC1_LPC_LA09_P	IO_L14P_T2L_N2_GC_47	W25	**FMC reference 9th channel data P**
FMC1_LPC_LA09_N	IO_L14N_T2L_N3_GC_47	Y25	**FMC reference 9th channel data N**
FMC1_LPC_LA10_P	IO_L5P_T0U_N8_AD14P_47	AA27	**FMC reference 10th channel data P**
FMC1_LPC_LA10_N	IO_L5N_T0U_N9_AD14N_47	AB27	**FMC reference 10th channel data N**
FMC1_LPC_LA11_P	IO_L23P_T3U_N8_47	V29	**FMC reference 11th channel data p**
FMC1_LPC_LA11_N	IO_L23N_T3U_N9_47	W29	**FMC reference 11th channel data N**
FMC1_LPC_LA12_P	IO_L15P_T2L_N4_AD11P_47	U21	**FMC reference 12th channel data P**
FMC1_LPC_LA12_N	IO_L15N_T2L_N5_AD11N_47	U22	**FMC reference 12th channel data N**
FMC1_LPC_LA13_P	IO_L24P_T3U_N10_47	V26	**FMC reference 13th channel data P**

FMC1_LPC_LA13_N	IO_L24N_T3U_N11_47	W26	**FMC reference 13th channel data N**
FMC1_LPC_LA14_P	IO_L1P_T0L_N0_DBC_47	Y26	**FMC reference 14th channel data P**
FMC1_LPC_LA14_N	IO_L1N_T0L_N1_DBC_47	Y27	**FMC reference 14th channel data N**
FMC1_LPC_LA15_P	IO_L22P_T3U_N6_DBC_AD0P_47	U26	**FMC reference 15th channel data P**
FMC1_LPC_LA15_N	IO_L22N_T3U_N7_DBC_AD0N_47	U27	**FMC reference 15th channel data N**
FMC1_LPC_LA16_P	IO_L20P_T3L_N2_AD1P_47	U24	**FMC reference 16th channel data P**
FMC1_LPC_LA16_N	IO_L20N_T3L_N3_AD1N_47	U25	**FMC reference 16th channel data N**
FMC1_LPC_LA17_CC_P	IO_L12P_T1U_N10_GC_48	AC31	**FMC reference 17th channel data P**
FMC1_LPC_LA17_CC_N	IO_L12N_T1U_N11_GC_48	AC32	**FMC reference 17th channel data N**
FMC1_LPC_LA18_CC_P	IO_L13P_T2L_N0_GC_QBC_48	AA32	**FMC reference 18th channel data P**
FMC1_LPC_LA18_CC_N	IO_L13N_T2L_N1_GC_QBC_48	AB32	**FMC reference 18th channel data N**
FMC1_LPC_LA19_P	IO_L8P_T1L_N2_AD5P_48	AF33	**FMC reference 19th channel data P**
FMC1_LPC_LA19_N	IO_L8N_T1L_N3_AD5N_48	AG34	**FMC reference 19th channel data N**
FMC1_LPC_LA20_P	IO_L10P_T1U_N6_QBC_AD4P_48	AE33	**FMC reference 20th channel data P**
FMC1_LPC_LA20_N	IO_L10N_T1U_N7_QBC_AD4N_48	AF34	**FMC reference 20th channel data N**
FMC1_LPC_LA21_P	IO_L9P_T1L_N4_AD12P_48	AE32	**FMC reference 21st channel data P**
FMC1_LPC_LA21_N	IO_L9N_T1L_N5_AD12N_48	AF32	**FMC reference 21st**

			channel data N
FMC1_LPC_LA22_P	IO_L15P_T2L_N4_AD11P_48	AC34	**FMC reference 22nd channel data P**
FMC1_LPC_LA22_N	IO_L15N_T2L_N5_AD11N_48	AD34	**FMC reference 22nd channel data N**
FMC1_LPC_LA23_P	IO_L17P_T2U_N8_AD10P_48	AA34	**FMC reference 23rd channel data P**
FMC1_LPC_LA23_N	IO_L17N_T2U_N9_AD10N_48	AB34	**FMC reference 23rdchannel data N**
FMC1_LPC_LA24_P	IO_L19P_T3L_N0_DBC_AD9P_48	W33	**FMC reference 24th channel data P**
FMC1_LPC_LA24_N	IO_L19N_T3L_N1_DBC_AD9N_48	Y33	**FMC reference 24th channel data N**
FMC1_LPC_LA25_P	IO_L22P_T3U_N6_DBC_AD0P_48	Y31	**FMC reference 25th channel data P**
FMC1_LPC_LA25_N	IO_L22N_T3U_N7_DBC_AD0N_48	Y32	**FMC reference 25th channel data N**
FMC1_LPC_LA26_P	IO_L14P_T2L_N2_GC_48	AB30	**FMC reference 26th channel data P**
FMC1_LPC_LA26_N	IO_L14N_T2L_N3_GC_48	AB31	**FMC reference 26th channel data N**
FMC1_LPC_LA27_P	IO_L16P_T2U_N6_QBC_AD3P_48	AA29	**FMC reference 27th channel data P**
FMC1_LPC_LA27_N	IO_L16N_T2U_N7_QBC_AD3N_48	AB29	**FMC reference 27th channel data N**
FMC1_LPC_LA28_P	IO_L23P_T3U_N8_48	U34	**FMC reference 28th channel data P**
FMC1_LPC_LA28_N	IO_L23N_T3U_N9_48	V34	**FMC reference 28th channel data N**
FMC1_LPC_LA29_P	IO_L21P_T3L_N4_AD8P_48	V33	**FMC reference 29th channel data P**
FMC1_LPC_LA29_N	IO_L21N_T3L_N5_AD8N_48	W34	**FMC reference 29th channel data N**

FMC1_LPC_LA30_P	IO_L20P_T3L_N2_AD1P_48	W30	**FMC reference 30th channel data P**
FMC1_LPC_LA30_N	IO_L20N_T3L_N3_AD1N_48	Y30	**FMC reference 30th channel data N**
FMC1_LPC_LA31_P	IO_L24P_T3U_N10_48	V31	**FMC reference 31st channel data P**
FMC1_LPC_LA31_N	IO_L24N_T3U_N11_48	W31	**FMC reference 31st channel data N**
FMC1_LPC_LA32_P	IO_L5P_T0U_N8_AD14P_48	AD29	**FMC reference 32nd channel data P**
FMC1_LPC_LA32_N	IO_L5N_T0U_N9_AD14N_48	AE30	**FMC reference 32nd channel data N**
FMC1_LPC_LA33_P	IO_L18P_T2U_N10_AD2P_48	AC33	**FMC reference 33rd channel data P**
FMC1_LPC_LA33_N	IO_L18N_T2U_N11_AD2N_48	AD33	**FMC reference 33rd channel data N**
FMC1_LPC_SCL	IO_L17N_T2U_N9_AD10N_47	T23	FMC I2C Bus Clock
FMC1_LPC_SDA	IO_L17P_T2U_N8_AD10P_47	T22	FMC I2C Bus Data

FMC 2nd LPC Connectors Pin Assignment:

Signal Name	PIN Name	FPGA PIN	Description
FMC2_LPC_CLK0_P	IO_L12P_T1U_N10_GC_64	AG11	**FMC reference 1streference clock P**
FMC2_LPC_CLK0_N	IO_L12N_T1U_N11_GC_64	AH11	**FMC reference 1streference clock N**
FMC2_LPC_CLK1_P	IO_L14P_T2L_N2_GC_A04_D20_65	P24	**FMC reference 2nd reference clock P**
FMC2_LPC_CLK1_N	IO_L14N_T2L_N3_GC_A05_D21_65	P25	**FMC reference 2nd reference clock N**
FMC2_LPC_LA00_CC_P	IO_L11P_T1U_N8_GC_64	AG12	**FMC reference 0th channel data clock P**
FMC2_LPC_LA00_CC_N	IO_L11N_T1U_N9_GC_64	AH12	**FMC reference 0th**

			channel data (clock) N
FMC2_LPC_LA01_CC_P	IO_L13P_T2L_N0_GC_QBC_64	AF10	FMC reference 1st channel data (clock) P
FMC2_LPC_LA01_CC_N	IO_L13N_T2L_N1_GC_QBC_64	AG10	FMC reference 1st channel data (clock) N
FMC2_LPC_LA02_P	IO_L2P_T0L_N2_64	AN13	FMC reference 2nd channel data P
FMC2_LPC_LA02_N	IO_L2N_T0L_N3_64	AP13	FMC reference 2nd channel data N
FMC2_LPC_LA03_P	IO_L4P_T0U_N6_DBC_AD7P_64	AM12	FMC reference 3rd channel data P
FMC2_LPC_LA03_N	IO_L4N_T0U_N7_DBC_AD7N_64	AN12	FMC reference 3rd channel data N
FMC2_LPC_LA04_P	IO_L6P_T0U_N10_AD6P_64	AK13	FMC reference 4th channel data P
FMC2_LPC_LA04_N	IO_L6N_T0U_N11_AD6N_64	AL13	FMC reference 4th channel data N
FMC2_LPC_LA05_P	IO_L19P_T3L_N0_DBC_AD9P_64	AL10	FMC reference 5th channeldata P
FMC2_LPC_LA05_N	IO_L19N_T3L_N1_DBC_AD9N_64	AM10	FMC reference 5th channel data N
FMC2_LPC_LA06_P	IO_L1P_T0L_N0_DBC_64	AP11	FMC reference 6th channel data P
FMC2_LPC_LA06_N	IO_L1N_T0L_N1_DBC_64	AP10	FMC reference 6th channel data N
FMC2_LPC_LA07_P	IO_L5P_T0U_N8_AD14P_64	AK12	FMC reference 7th channel data P
FMC2_LPC_LA07_N	IO_L5N_T0U_N9_AD14N_64	AL12	FMC reference 7th channel data N
FMC2_LPC_LA08_P	IO_L3P_T0L_N4_AD15P_64	AM11	FMC reference 8th channel data P
FMC2_LPC_LA08_N	IO_L3N_T0L_N5_AD15N_64	AN11	FMC reference 8th channel data N

FMC2_LPC_LA09_P	IO_L18P_T2U_N10_AD2P_64	AH9	**FMC reference 9th channel data P**
FMC2_LPC_LA09_N	IO_L18N_T2U_N11_AD2N_64	AH8	**FMC reference 9th channel data N**
FMC2_LPC_LA10_P	IO_L15P_T2L_N4_AD11P_64	AE8	**FMC reference 10th channel data P**
FMC2_LPC_LA10_N	IO_L15N_T2L_N5_AD11N_64	AF8	**FMC reference 10th channel data N**
FMC2_LPC_LA11_P	IO_L9P_T1L_N4_AD12P_64	AE12	**FMC reference 11th channel data p**
FMC2_LPC_LA11_N	IO_L9N_T1L_N5_AD12N_64	AF12	**FMC reference 11th channel data N**
FMC2_LPC_LA12_P	IO_L8P_T1L_N2_AD5P_64	AH13	**FMC reference 12th channel data P**
FMC2_LPC_LA12_N	IO_L8N_T1L_N3_AD5N_64	AJ13	**FMC reference 12th channel data N**
FMC2_LPC_LA13_P	IO_L16P_T2U_N6_QBC_AD3P_64	AD10	**FMC reference 13th channel data P**
FMC2_LPC_LA13_N	IO_L16N_T2U_N7_QBC_AD3N_64	AE10	**FMC reference 13th channel data N**
FMC2_LPC_LA14_P	IO_L17P_T2U_N8_AD10P_64	AD9	**FMC reference 14th channel data P**
FMC2_LPC_LA14_N	IO_L17N_T2U_N9_AD10N_64	AD8	**FMC reference 14th channel data N**
FMC2_LPC_LA15_P	IO_L10P_T1U_N6_QBC_AD4P_64	AD11	**FMC reference 15th channel data P**
FMC2_LPC_LA15_N	IO_L10N_T1U_N7_QBC_AD4N_64	AE11	**FMC reference 15th channel data N**
FMC2_LPC_LA16_P	IO_L7P_T1L_N0_QBC_AD13P_64	AE13	**FMC reference 16th channel data P**
FMC2_LPC_LA16_N	IO_L7N_T1L_N1_QBC_AD13N_64	AF13	**FMC reference 16th channel data N**
FMC2_LPC_LA17_CC_P	IO_L12P_T1U_N10_GC_A08_D24_6	N24	**FMC reference 17th**

	5		**channel data P**
FMC2_LPC_LA17_CC_N	IO_L12N_T1U_N11_GC_A09_D25_65	M24	**FMC reference 17th channel data N**
FMC2_LPC_LA18_CC_P	IO_L11P_T1U_N8_GC_A10_D26_65	M25	**FMC reference 18th channel data P**
FMC2_LPC_LA18_CC_N	IO_L11N_T1U_N9_GC_A11_D27_65	M26	**FMC reference 18th channel data N**
FMC2_LPC_LA19_P	IO_L16P_T2U_N6_QBC_AD3P_A00_D16_65	T24	**FMC reference 19th channel data P**
FMC2_LPC_LA19_N	IO_L16N_T2U_N7_QBC_AD3N_A01_D17_65	T25	**FMC reference 19th channel data N**
FMC2_LPC_LA20_P	IO_L15P_T2L_N4_AD11P_A02_D18_65	T27	**FMC reference 20th channel data P**
FMC2_LPC_LA20_N	IO_L15N_T2L_N5_AD11N_A03_D19_65	R27	**FMC reference 20th channel data N**
FMC2_LPC_LA21_P	IO_L17P_T2U_N8_AD10P_D14_65	R25	**FMC reference 21st channel data P**
FMC2_LPC_LA21_N	IO_L17N_T2U_N9_AD10N_D15_65	R26	**FMC reference 21st channel data N**
FMC2_LPC_LA22_P	IO_L13P_T2L_N0_GC_QBC_A06_D22_65	P26	**FMC reference 22nd channel data P**
FMC2_LPC_LA22_N	IO_L13N_T2L_N1_GC_QBC_A07_D23_65	N26	**FMC reference 22nd channel data N**
FMC2_LPC_LA23_P	IO_L5P_T0U_N8_AD14P_A22_65	J26	**FMC reference 23rd channel data P**
FMC2_LPC_LA23_N	IO_L5N_T0U_N9_AD14N_A23_65	H26	**FMC reference 23rdchannel data N**
FMC2_LPC_LA24_P	IO_L8P_T1L_N2_AD5P_A16_65	L23	**FMC reference 24th channel data P**
FMC2_LPC_LA24_N	IO_L8N_T1L_N3_AD5N_A17_65	L24	**FMC reference 24th channel data N**
FMC2_LPC_LA25_P	IO_L7P_T1L_N0_QBC_AD13P_A18_65	M27	**FMC reference 25th channel data P**

FMC2_LPC_LA25_N	IO_L7N_T1L_N1_QBC_AD13N_A19_65	L27	**FMC reference 25th channel data N**
FMC2_LPC_LA26_P	IO_L4P_T0U_N6_DBC_AD7P_A24_65	J24	**FMC reference 26th channel data P**
FMC2_LPC_LA26_N	IO_L4N_T0U_N7_DBC_AD7N_A25_65	J25	**FMC reference 26th channel data N**
FMC2_LPC_LA27_P	IO_L1P_T0L_N0_DBC_RS0_65	H27	**FMC reference 27th channel data P**
FMC2_LPC_LA27_N	IO_L1N_T0L_N1_DBC_RS1_65	G27	**FMC reference 27th channel data N**
FMC2_LPC_LA28_P	IO_L18P_T2U_N10_AD2P_D12_65	R23	**FMC reference 28th channel data P**
FMC2_LPC_LA28_N	IO_L18N_T2U_N11_AD2N_D13_65	P23	**FMC reference 28th channel data N**
FMC2_LPC_LA29_P	IO_L10P_T1U_N6_QBC_AD4P_A12_D28_65	L22	**FMC reference 29th channel data P**
FMC2_LPC_LA29_N	IO_L10N_T1U_N7_QBC_AD4N_A13_D29_65	K23	**FMC reference 29th channel data N**
FMC2_LPC_LA30_P	IO_L9P_T1L_N4_AD12P_A14_D30_65	L25	**FMC reference 30th channel data P**
FMC2_LPC_LA30_N	IO_L9N_T1L_N5_AD12N_A15_D31_65	K25	**FMC reference 30th channel data N**
FMC2_LPC_LA31_P	IO_L19P_T3L_N0_DBC_AD9P_D10_65	N22	**FMC reference 31st channel data P**
FMC2_LPC_LA31_N	IO_L19N_T3L_N1_DBC_AD9N_D11_65	M22	**FMC reference 31st channel data N**
FMC2_LPC_LA32_P	IO_L6P_T0U_N10_AD6P_A20_65	J23	**FMC reference 32nd channel data P**
FMC2_LPC_LA32_N	IO_L6N_T0U_N11_AD6N_A21_65	H24	**FMC reference 32nd channel data N**
FMC2_LPC_LA33_P	IO_L3P_T0L_N4_AD15P_A26_65	K26	**FMC reference 33rd channel data P**
FMC2_LPC_LA33_N	IO_L3N_T0L_N5_AD15N_A27_65	K27	**FMC reference 33rd**

			channel data N
FMC2_LPC_SCL	IO_L23P_T3U_N8_I2C_SCLK_65	N21	FMC I2C Bus Clock
FMC2_LPC_SDA	IO_L23N_T3U_N9_I2C_SDA_65	M21	FMC I2C Bus Data
FMC2_DP0_C2M_P	MGTHTXP2_226	U4	Transceiver data output P
FMC2_DP0_C2M_N	MGTHTXN2_226	U3	Transceiver data output N
FMC2_DP0_M2C_P	MGTHRXP2_226	T2	Transceiver data input P
FMC2_DP0_M2C_N	MGTHRXN2_226	T1	Transceiver data input N
FMC2_GBTCLK0_M2C_P	MGTREFCLK1P_226	T6	Transceiver reference clock P
FMC2_GBTCLK0_M2C_N	MGTREFCLK1N_226	T5	Transceiver reference clock N

FMC 3rd HPC Connectors Pin Assignment:

Signal Name	PIN Name	FPGA PIN	Description
FMC_HPC_CLK0_M2C_P	IO_L12N_T1U_N11_GC_67	C24	**FMC reference 1st reference clock P**
FMC_HPC_CLK0_M2C_N	IO_L11N_T1U_N9_GC_67	D25	**FMC reference 1st reference clock N**
FMC_HPC_CLK1_M2C_P	IO_L12P_T1U_N10_GC_66	G10	**FMC reference 2nd reference clock P**
FMC_HPC_CLK1_M2C_N	IO_L12N_T1U_N11_GC_66	F10	**FMC reference 2nd reference clock N**
FMC_HPC_LA00_CC_P	IO_L12P_T1U_N10_GC_67	D24	**FMC reference 0th channel data clock P**
FMC_HPC_LA00_CC_N	IO_L12N_T1U_N11_GC_67	C24	**FMC reference 0th channel data (clock) N**
FMC_HPC_LA01_CC_N	IO_L14N_T2L_N3_GC_67	E23	**FMC reference 1st channel data (clock) P**
FMC_HPC_LA01_CC_P	IO_L14P_T2L_N2_GC_67	E22	**FMC reference 1st channel data (clock) N**
FMC_HPC_LA02_P	IO_L1P_T0L_N0_DBC_67	F27	**FMC reference 2nd channel data P**
FMC_HPC_LA02_N	IO_L1N_T0L_N1_DBC_67	E27	**FMC reference 2nd channel**

			data N
FMC_HPC_LA03_P	IO_L3P_T0L_N4_AD15P_67	E28	**FMC reference 3rd channel data P**
FMC_HPC_LA03_N	IO_L3N_T0L_N5_AD15N_67	D29	**FMC reference 3rd channel data N**
FMC_HPC_LA04_P	IO_L5P_T0U_N8_AD14P_67	D28	**FMC reference 4th channel data P**
FMC_HPC_LA04_N	IO_L5N_T0U_N9_AD14N_67	C28	**FMC reference 4th channel data N**
FMC_HPC_LA05_P	IO_L2P_T0L_N2_67	C27	**FMC reference 5th channeldata P**
FMC_HPC_LA05_N	IO_L2N_T0L_N3_67	B27	**FMC reference 5th channel data N**
FMC_HPC_LA06_P	IO_L4P_T0U_N6_DBC_AD7P_67	B29	**FMC reference 6th channel data P**
FMC_HPC_LA06_N	IO_L4N_T0U_N7_DBC_AD7N_67	A29	**FMC reference 6th channel data N**
FMC_HPC_LA07_P	IO_L9P_T1L_N4_AD12P_67	C26	**FMC reference 7th channel data P**
FMC_HPC_LA07_N	IO_L9N_T1L_N5_AD12N_67	B26	**FMC reference 7th channel data N**
FMC_HPC_LA08_P	IO_L6P_T0U_N10_AD6P_67	A27	**FMC reference 8th channel data P**
FMC_HPC_LA08_N	IO_L6N_T0U_N11_AD6N_67	A28	**FMC reference 8th channel data N**
FMC_HPC_LA09_P	IO_L8P_T1L_N2_AD5P_67	B25	**FMC reference 9th channel data P**
FMC_HPC_LA09_N	IO_L8N_T1L_N3_AD5N_67	A25	**FMC reference 9th channel data N**
FMC_HPC_LA10_P	IO_L7P_T1L_N0_QBC_AD13P_67	E26	**FMC reference 10th channel data P**
FMC_HPC_LA10_N	IO_L7N_T1L_N1_QBC_AD13N_67	D26	**FMC reference 10th channel data N**

FMC_HPC_LA11_P	IO_L13P_T2L_N0_GC_QBC_67	D23	**FMC reference 11th channel data p**
FMC_HPC_LA11_N	IO_L13N_T2L_N1_GC_QBC_67	C23	**FMC reference 11th channel data N**
FMC_HPC_LA12_P	IO_L10P_T1U_N6_QBC_AD4P_67	B24	**FMC reference 12th channel data P**
FMC_HPC_LA12_N	IO_L10N_T1U_N7_QBC_AD4N_67	A24	**FMC reference 12th channel data N**
FMC_HPC_LA13_P	IO_L15P_T2L_N4_AD11P_67	B21	**FMC reference 13th channel data P**
FMC_HPC_LA13_N	IO_L15N_T2L_N5_AD11N_67	B22	**FMC reference 13th channel data N**
FMC_HPC_LA14_P	IO_L16P_T2U_N6_QBC_AD3P_67	C21	**FMC reference 14th channel data P**
FMC_HPC_LA14_N	IO_L16N_T2U_N7_QBC_AD3N_67	C22	**FMC reference 14th channel data N**
FMC_HPC_LA15_P	IO_L20P_T3L_N2_AD1P_67	E20	**FMC reference 15th channel data P**
FMC_HPC_LA15_N	IO_L20N_T3L_N3_AD1N_67	E21	**FMC reference 15th channel data N**
FMC_HPC_LA16_P	IO_L17P_T2U_N8_AD10P_67	B20	**FMC reference 16th channel data P**
FMC_HPC_LA16_N	IO_L17N_T2U_N9_AD10N_67	A20	**FMC reference 16th channel data N**
FMC_HPC_LA17_CC_P	IO_L13P_T2L_N0_GC_QBC_66	H11	**FMC reference 17th channel data P**
FMC_HPC_LA17_CC_N	IO_L13N_T2L_N1_GC_QBC_66	G11	**FMC reference 17th channel data N**
FMC_HPC_LA18_CC_P	IO_L11P_T1U_N8_GC_66	G9	**FMC reference 18th channel data P**
FMC_HPC_LA18_CC_N	IO_L11N_T1U_N9_GC_66	F9	**FMC reference 18th channel data N**
FMC_HPC_LA19_P	IO_L24P_T3U_N10_66	D13	**FMC reference 19th**

			channel data P
FMC_HPC_LA19_N	IO_L24N_T3U_N11_66	C13	**FMC reference 19th channel data N**
FMC_HPC_LA20_P	IO_L22P_T3U_N6_DBC_AD0P_66	F13	**FMC reference 20th channel data P**
FMC_HPC_LA20_N	IO_L22N_T3U_N7_DBC_AD0N_66	E13	**FMC reference 20th channel data N**
FMC_HPC_LA21_P	IO_L20P_T3L_N2_AD1P_66	C12	**FMC reference 21st channel data P**
FMC_HPC_LA21_N	IO_L20N_T3L_N3_AD1N_66	B12	**FMC reference 21st channel data N**
FMC_HPC_LA22_P	IO_L21P_T3L_N4_AD8P_66	C11	**FMC reference 22nd channel data P**
FMC_HPC_LA22_N	IO_L21N_T3L_N5_AD8N_66	B11	**FMC reference 22nd channel data N**
FMC_HPC_LA23_P	IO_L23P_T3U_N8_66	A13	**FMC reference 23rd channel data P**
FMC_HPC_LA23_N	IO_L23N_T3U_N9_66	A12	**FMC reference 23rdchannel data N**
FMC_HPC_LA24_P	IO_L3P_T0L_N4_AD15P_66	D8	**FMC reference 24th channel data P**
FMC_HPC_LA24_N	IO_L3N_T0L_N5_AD15N_66	C8	**FMC reference 24th channel data N**
FMC_HPC_LA25_P	IO_L5P_T0U_N8_AD14P_66	D9	**FMC reference 25th channel data P**
FMC_HPC_LA25_N	IO_L5N_T0U_N9_AD14N_66	C9	**FMC reference 25th channel data N**
FMC_HPC_LA26_P	IO_L2P_T0L_N2_66	B9	**FMC reference 26th channel data P**
FMC_HPC_LA26_N	IO_L2N_T0L_N3_66	A9	**FMC reference 26th channel data N**
FMC_HPC_LA27_P	IO_L4P_T0U_N6_DBC_AD7P_66	B10	**FMC reference 27th channel data P**

FMC_HPC_LA27_N	IO_L4N_T0U_N7_DBC_AD7N_66	A10	**FMC reference 27th channel data N**
FMC_HPC_LA28_P	IO_L1P_T0L_N0_DBC_66	F8	**FMC reference 28th channel data P**
FMC_HPC_LA28_N	IO_L1N_T0L_N1_DBC_66	E8	**FMC reference 28th channel data N**
FMC_HPC_LA29_P	IO_L6P_T0U_N10_AD6P_66	E10	**FMC reference 29th channel data P**
FMC_HPC_LA29_N	IO_L6N_T0U_N11_AD6N_66	D10	**FMC reference 29th channel data N**
FMC_HPC_LA30_P	IO_L9P_T1L_N4_AD12P_66	J8	**FMC reference 30th channel data P**
FMC_HPC_LA30_N	IO_L9N_T1L_N5_AD12N_66	H8	**FMC reference 30th channel data N**
FMC_HPC_LA31_P	IO_L8P_T1L_N2_AD5P_66	J9	**FMC reference 31st channel data P**
FMC_HPC_LA31_N	IO_L8N_T1L_N3_AD5N_66	H9	**FMC reference 31st channel data N**
FMC_HPC_LA32_P	IO_L7P_T1L_N0_QBC_AD13P_66	L8	**FMC reference 32nd channel data P**
FMC_HPC_LA32_N	IO_L7N_T1L_N1_QBC_AD13N_66	K8	**FMC reference 32nd channel data N**
FMC_HPC_LA33_P	IO_L10P_T1U_N6_QBC_AD4P_66	K10	**FMC reference 33rd channel data P**
FMC_HPC_LA33_N	IO_L10N_T1U_N7_QBC_AD4N_66	J10	**FMC reference 33rd channel data N**
FMC_HPC_HA00_CC_P	IO_L12P_T1U_N10_GC_68	E18	**FMC HA Route 0 data P**
FMC_HPC_HA00_CC_N	IO_L12N_T1U_N11_GC_68	E17	**FMC HA Route 0 data N**
FMC_HPC_HA01_CC_P	IO_L13P_T2L_N0_GC_QBC_68	G17	**FMC HA Route 1 data P**
FMC_HPC_HA01_CC_N	IO_L13N_T2L_N1_GC_QBC_68	G16	**FMC HA Route 1 data N**
FMC_HPC_HA02_P	IO_L10P_T1U_N6_QBC_AD4P_68	D19	**FMC HA Route 2 data P**
FMC_HPC_HA02_N	IO_L10N_T1U_N7_QBC_AD4N_68	D18	**FMC HA Route 2 data N**

FMC_HPC_HA03_P	IO_L14P_T2L_N2_GC_68	F18	**FMC HA Route 3 data P**
FMC_HPC_HA03_N	IO_L14N_T2L_N3_GC_68	F17	**FMC HA Route 3 data N**
FMC_HPC_HA04_P	IO_L22P_T3U_N6_DBC_AD0P_68	J19	**FMC HA Route 4 data P**
FMC_HPC_HA04_N	IO_L22N_T3U_N7_DBC_AD0N_68	J18	**FMC HA Route 4 data N**
FMC_HPC_HA05_P	IO_L24P_T3U_N10_68	L19	**FMC HA Route 5 data P**
FMC_HPC_HA05_N	IO_L24N_T3U_N11_68	L18	**FMC HA Route 5 data N**
FMC_HPC_HA06_P	IO_L2P_T0L_N2_68	A19	**FMC HA Route 6 data P**
FMC_HPC_HA06_N	IO_L2N_T0L_N3_68	A18	**FMC HA Route 6 data N**
FMC_HPC_HA07_P	IO_L4P_T0U_N6_DBC_AD7P_68	C19	**FMC HA Route 7 data P**
FMC_HPC_HA07_N	IO_L4N_T0U_N7_DBC_AD7N_68	B19	**FMC HA Route 7 data N**
FMC_HPC_HA08_P	IO_L18P_T2U_N10_AD2P_68	H19	**FMC HA Route 8 data P**
FMC_HPC_HA08_N	IO_L18N_T2U_N11_AD2N_68	H18	**FMC HA Route 8 data N**
FMC_HPC_HA09_P	IO_L16P_T2U_N6_QBC_AD3P_68	G19	**FMC HA Route 9 data P**
FMC_HPC_HA09_N	IO_L16N_T2U_N7_QBC_AD3N_68	F19	**FMC HA Route 9 data N**
FMC_HPC_HA10_P	IO_L6P_T0U_N10_AD6P_68	C18	**FMC HA Route 10 data P**
FMC_HPC_HA10_N	IO_L6N_T0U_N11_AD6N_68	C17	**FMC HA Route 10 data N**
FMC_HPC_HA11_P	IO_L20P_T3L_N2_AD1P_68	K18	**FMC HA Route 11 data P**
FMC_HPC_HA11_N	IO_L20N_T3L_N3_AD1N_68	K17	**FMC HA Route 11 data N**
FMC_HPC_HA12_P	IO_L17P_T2U_N8_AD10P_68	H17	**FMC HA Route 12 data P**
FMC_HPC_HA12_N	IO_L17N_T2U_N9_AD10N_68	H16	**FMC HA Route 12 data N**
FMC_HPC_HA13_P	IO_L23P_T3U_N8_68	K16	**FMC HA Route 13 data P**
FMC_HPC_HA13_N	IO_L23P_T3U_N8_68	J16	**FMC HA Route 13 data N**
FMC_HPC_HA14_P	IO_L8P_T1L_N2_AD5P_68	E15	**FMC HA Route 14 data P**
FMC_HPC_HA14_N	IO_L8N_T1L_N3_AD5N_68	D15	**FMC HA Route 14 data N**
FMC_HPC_HA15_P	IO_L5P_T0U_N8_AD14P_68	B17	**FMC HA Route 15 data P**
FMC_HPC_HA15_N	IO_L5N_T0U_N9_AD14N_68	B16	**FMC HA Route 15 data N**
FMC_HPC_HA16_P	IO_L21P_T3L_N4_AD8P_68	L15	**FMC HA Route 16 data P**
FMC_HPC_HA16_N	IO_L21N_T3L_N5_AD8N_68	K15	**FMC HA Route 16 data N**
FMC_HPC_HA17_CC_P	IO_L11P_T1U_N8_GC_68	E16	**FMC HA Route 17 data P**
FMC_HPC_HA17_CC_N	IO_L11N_T1U_N9_GC_68	D16	**FMC HA Route 17 data N**
FMC_HPC_HA18_P	IO_L9P_T1L_N4_AD12P_68	F15	**FMC HA Route 18 data P**
FMC_HPC_HA18_N	IO_L9N_T1L_N5_AD12N_68	F14	**FMC HA Route 18 data N**

FMC_HPC_HA19_P	IO_L19P_T3L_N0_DBC_AD9P_68	J15	**FMC HA Route 19 data P**
FMC_HPC_HA19_N	IO_L19N_T3L_N1_DBC_AD9N_68	J14	**FMC HA Route 19 data N**
FMC_HPC_HA20_P	IO_L15P_T2L_N4_AD11P_68	G15	**FMC HA Route 20 data P**
FMC_HPC_HA20_N	IO_L15N_T2L_N5_AD11N_68	G14	**FMC HA Route 20 data N**
FMC_HPC_HA21_P	IO_L3P_T0L_N4_AD15P_68	B15	**FMC HA Route 21 data P**
FMC_HPC_HA21_N	IO_L3N_T0L_N5_AD15N_68	A15	**FMC HA Route 21 data N**
FMC_HPC_HA22_P	IO_L1P_T0L_N0_DBC_68	B14	**FMC HA Route 22 data P**
FMC_HPC_HA22_N	IO_L1N_T0L_N1_DBC_68	A14	**FMC HA Route 22 data N**
FMC_HPC_HA23_P	IO_L7P_T1L_N0_QBC_AD13P_68	D14	**FMC HA Route 23 data P**
FMC_HPC_HA23_N	IO_L7N_T1L_N1_QBC_AD13N_68	C14	**FMC HA Route 23 data N**
FMC_HPC_SCL	IO_L15N_T2L_N5_AD11N_66	J11	FMC I2C Bus Clock
FMC_HPC_SDA	IO_L15P_T2L_N4_AD11P_66	K11	FMC I2C Bus Data
FMC_GBTCLK0_M2C_P	MGTREFCLK0P_228	K6	**Transceiver reference clock 0 input P**
FMC_GBTCLK0_M2C_N	MGTREFCLK0N_228	K5	**Transceiver reference clock 0 input N**
FMC_GBTCLK1_M2C_P	MGTREFCLK0P_227	P6	**Transceiver reference clock 1 input P**
FMC_GBTCLK1_M2C_N	MGTREFCLK0N_227	P5	**Transceiver reference clock 1 input P**
FMC_DP0_M2C_P	MGTHRXP3_228	A4	**Transceiver data 0 input P**
FMC_DP0_M2C_N	MGTHRXN3_228	A3	**Transceiver data 0 input N**
FMC_DP1_M2C_P	MGTHRXP0_228	E4	**Transceiver data 1 input P**
FMC_DP1_M2C_N	MGTHRXN0_228	E3	**Transceiver data 1 input N**
FMC_DP2_M2C_P	MGTHRXP1_228	D2	**Transceiver data 2 input P**
FMC_DP2_M2C_N	MGTHRXN1_228	D1	**Transceiver data 2 input N**
FMC_DP3_M2C_P	MGTHRXP2_228	B2	**Transceiver data 3 input P**
FMC_DP3_M2C_N	MGTHRXN2_228	B1	**Transceiver data 3 input N**
FMC_DP4_M2C_P	MGTHRXP2_227	H2	**Transceiver data 4 input P**
FMC_DP4_M2C_N	MGTHRXN2_227	H1	**Transceiver data 4 input N**
FMC_DP5_M2C_P	MGTHRXP1_227	K2	**Transceiver data 5 input P**
FMC_DP5_M2C_N	MGTHRXN1_227	K1	**Transceiver data 5 input N**

FMC_DP6_M2C_P	MGTHRXP0_227	M2	**Transceiver data 6 input P**
FMC_DP6_M2C_N	MGTHRXN0_227	M1	**Transceiver data 6 input N**
FMC_DP7_M2C_P	MGTHRXP3_227	F2	**Transceiver data 7 input P**
FMC_DP7_M2C_N	MGTHRXN3_227	F1	**Transceiver data 7 input N**
FMC_DP0_C2M_P	MGTHTXP3_228	B6	**Transceiver data 0 output P**
FMC_DP0_C2M_N	MGTHTXN3_228	B5	**Transceiver data 0 output N**
FMC_DP1_C2M_P	MGTHTXP0_228	F6	**Transceiver data 1 output P**
FMC_DP1_C2M_N	MGTHTXN0_228	F5	**Transceiver data 1 output N**
FMC_DP2_C2M_P	MGTHTXP1_228	D6	**Transceiver data 2 output P**
FMC_DP2_C2M_N	MGTHTXN1_228	D5	**Transceiver data 2 output N**
FMC_DP3_C2M_P	MGTHTXP2_228	C4	**Transceiver data 3 output P**
FMC_DP3_C2M_N	MGTHTXN2_228	C3	**Transceiver data 3 output N**
FMC_DP4_C2M_P	MGTHTXP2_227	J4	**Transceiver data 4 output P**
FMC_DP4_C2M_N	MGTHTXN2_227	J3	**Transceiver data 4 output N**
FMC_DP5_C2M_P	MGTHTXP1_227	L4	**Transceiver data 5 output P**
FMC_DP5_C2M_N	MGTHTXN1_227	L3	**Transceiver data 5 output N**
FMC_DP6_C2M_P	MGTHTXP0_227	N4	**Transceiver data 6 output P**
FMC_DP6_C2M_N	MGTHTXN0_227	N3	**Transceiver data 6 output N**
FMC_DP7_C2M_P	MGTHTXP3_227	G4	**Transceiver data 7 output P**
FMC_DP7_C2M_N	MGTHTXN3_227	G3	**Transceiver data 7 output N**

Part 11 SD Card Slot

The AXKU041 development board includes a Micro SD card interface to provide users with access to SD card memory for storing pictures, music or other user data files.

The signal is connected to THE IO signal of BANK48 of FPGA, whose level is 1.8V by default. But the SD card data level is 3.3V, we here through TXS02612 level converter to connect. Figure 11-1 shows the schematic diagram of the FPGA and SD card connector.

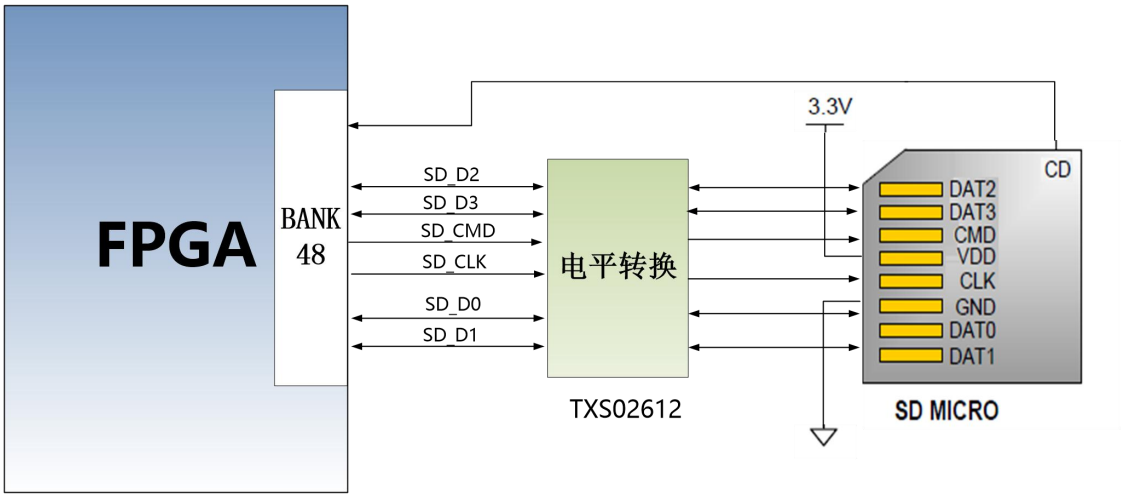


Figure 11-1

SD Slot pin allocation

Signal Name	PIN Name	FPGA PIN	Discription
SD_CLK	IO_L4N_T0U_N7_DBC_AD7N_48	AG29	SD clock signal
SD_CMD	IO_L4P_T0U_N6_DBC_AD7P_48	AF29	SD command signal
SD_D0	IO_L6P_T0U_N10_AD6P_48	AF30	SD Data0
SD_D1	IO_L6N_T0U_N11_AD6N_48	AG30	SD Data1
SD_D2	IO_L3N_T0L_N5_AD15N_48	AD28	SD Data2
SD_D3	IO_L1P_T0L_N0_DBC_48	AE27	SD Data3
SD_CD	IO_L3P_T0L_N4_AD15P_48	AC28	SD card insertion signal

Part 12 SMA、SATA Interface

The AXKU041 development board provides two SMA interfaces, differential signals connected to the BANK66 common clock IO port, providing customers with external clock interface or according to the common IO port, interface level is 1.8V.

Figure 12-1 shows the interface connection between FPGA and SMA.

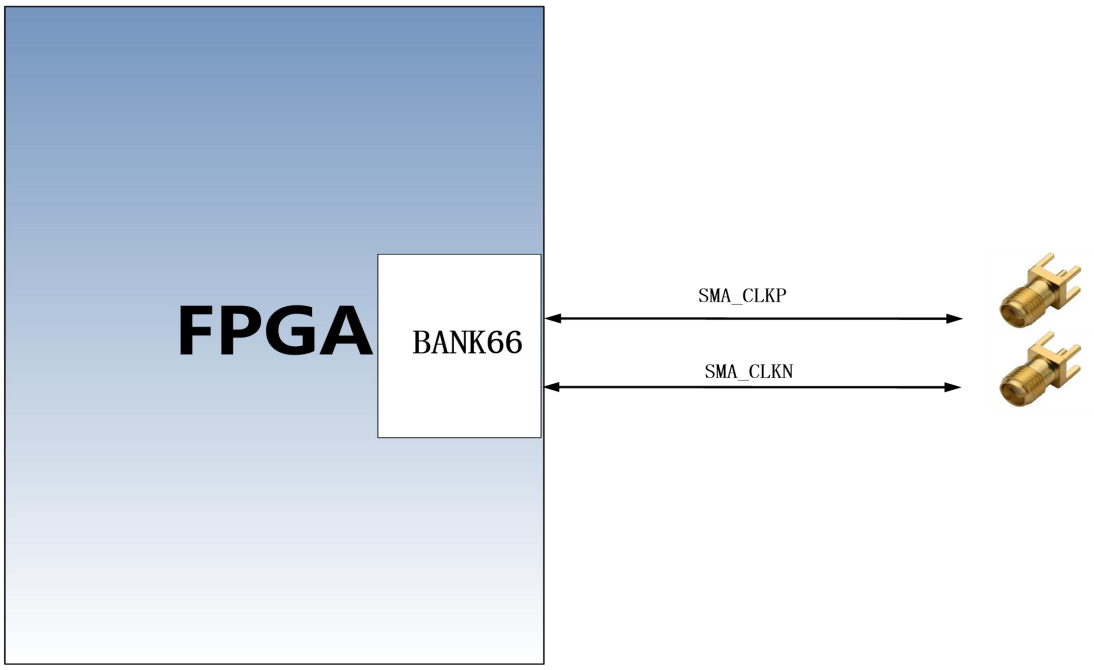


Figure 12-1

SMA interface pin assignment

Signal Name	PIN Name	FPGA PIN	Description
SMA_CLKIN_P	IO_L14P_T2L_N2_GC_66	H12	Transceiver clock signal P
SMA_CLKIN_N	IO_L14N_T2L_N3_GC_66	G12	Transceiver clock signal N

Part 13 temperature sensor

The AXKU040 development board is equipped with a high-precision, low-power, digital temperature sensor chip named ON Semiconductor'S LM75A. The temperature accuracy of LM75A chip is 0.5 degrees. The sensor and FPGA are directly I2C digital interfaces. FPGA reads the temperature near the current development board through the I2C interface.

Figure 13-1 shows the LM75 sensor chip design;

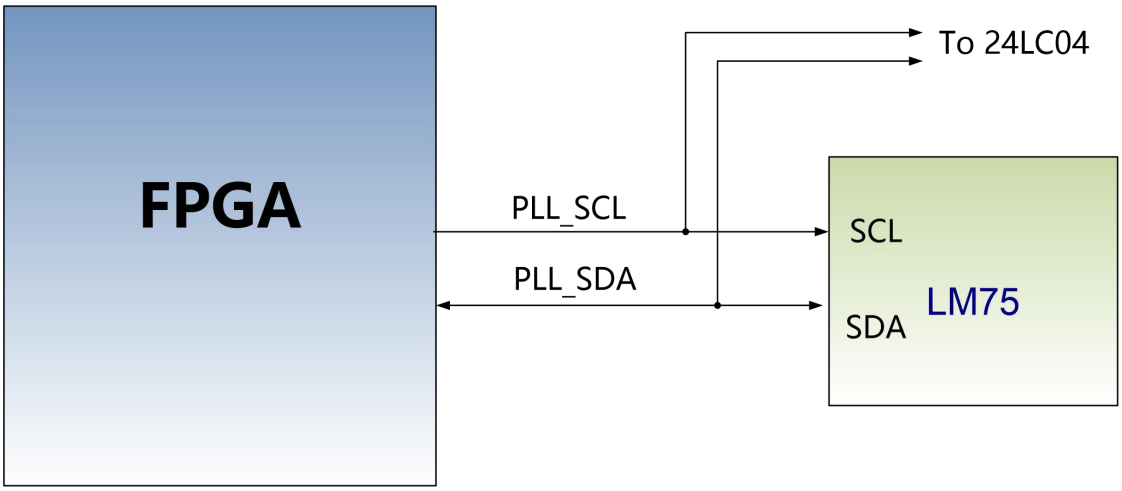


Figure 13-1

LM75 Sensor pin assignment:

Signal Name	FPGA PIN
I2C_SCL	P20
I2C_SDA	P21

Part 14 JTAG

A JTAG interface is reserved on the AXKU041 development board for downloading FPGA programs or solidified programs to FLASH. In order to damage FPGA chip caused by charged plug and remove, we added protection diode to JTAG signal to ensure that the signal voltage is within the range accepted by FPGA and avoid FPGA damage.

Figure 14-1 shows the schematic diagram of JTAG

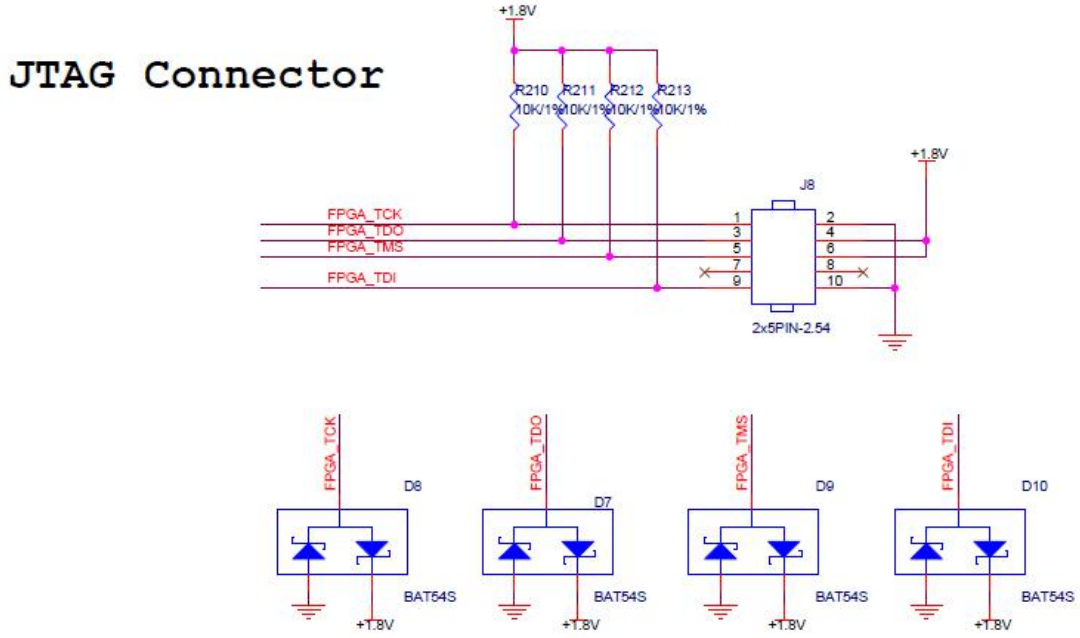


Figure 14-1

JTAG:

Signal Name	PIN Name	FPGA PIN	Description
FPGA_TDI	TDI_0	V9	Input Data PIN
FPGA_TMS	TMS_0	W9	Control PIN
FPGA_TDO	TDO_0	U9	Output Data PIN
FPGA_TCK	TCK_0	AC9	CLK PIN

Part 15 LED

AXKU041 development board has 6 LED, including 1 power indicator; 1 DONE light, 4 FPGA control lights, and 1 double panel indicator light holder. When the development board is powered on, the power indicator light will light up; When FPGA configures the program, the configuration LED light will light up. Four user LED lights are connected to IO of FPGA BANK65 and BANK47. The user can control on and off by program. When IO voltage connected to user LED lights is low, user LED lights will be off; when IO voltage connected to user LED lights is high, user LED lights will be on. Since the level of BANK65 and BANK47 is 1.8V, we added three tubes here to drive LED on and off. DONE lamp to judge whether FPGA starts normally. Panel indicator connected to BANK67, level is 1.8v.

Figure 15-1 shows the hardware connection of an LED lamp:

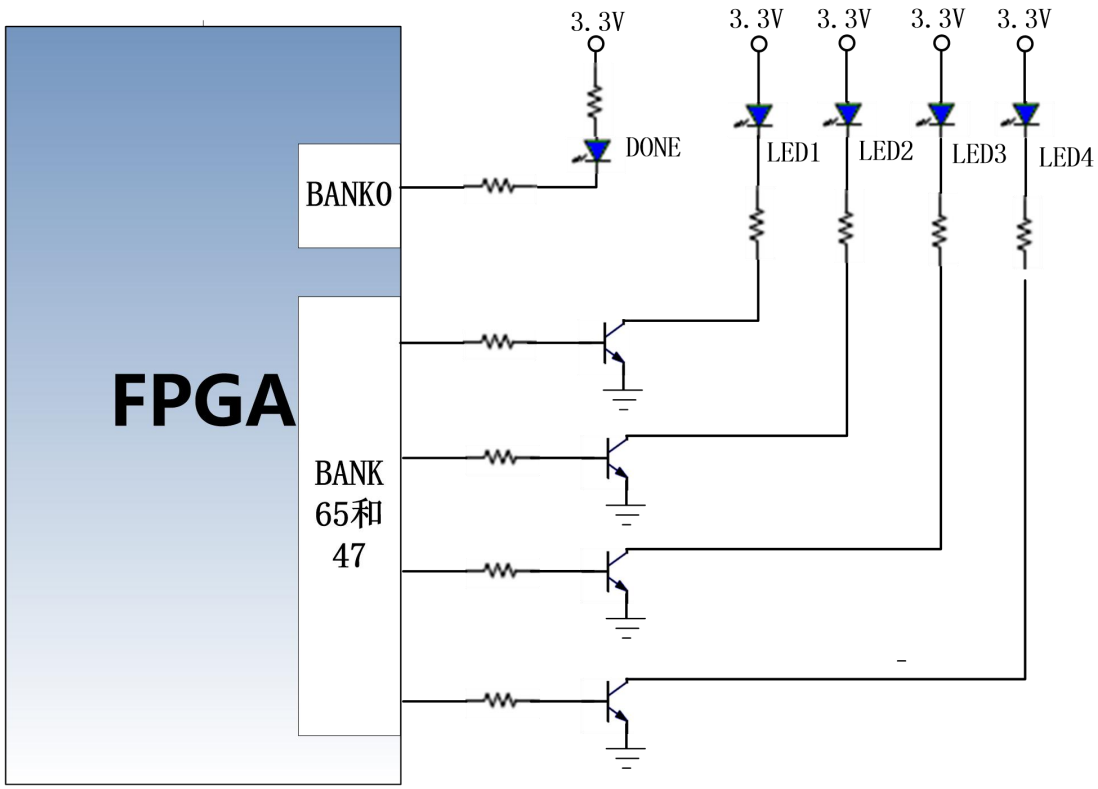


Figure 15-1

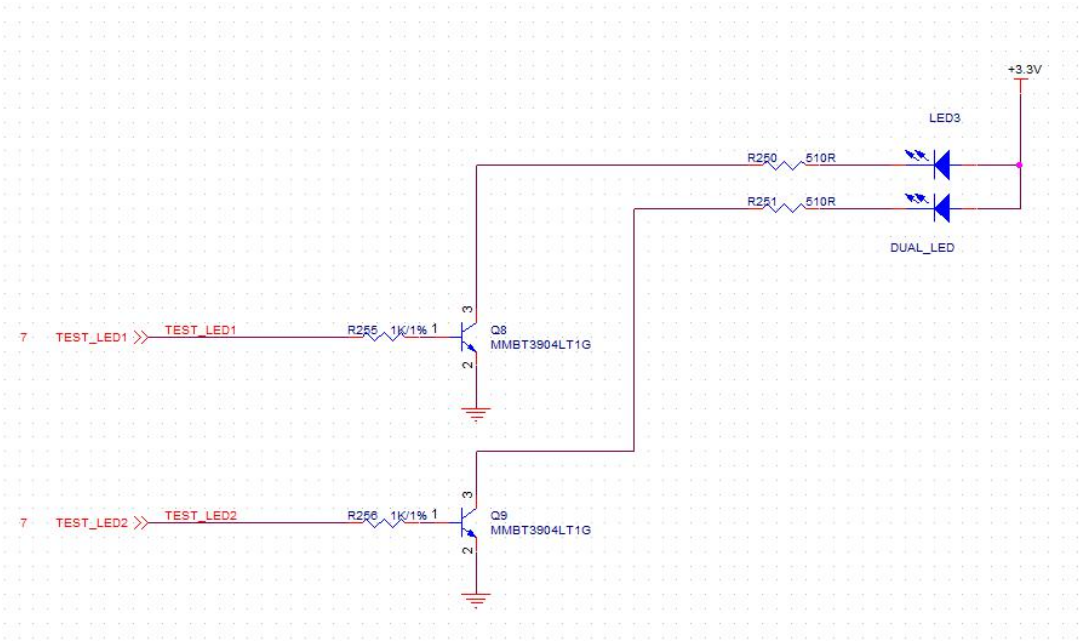


Figure 15-2

Signal Name	PIN Name	FPGA PIN
LED1	IO_T1U_N12_PERSTN1_65	N23
LED2	IO_L16N_T2U_N7_QBC_AD3N_47	V23
LED3	IO_L16P_T2U_N6_QBC_AD3P_47	V22
LED4	IO_L18P_T2U_N10_AD2P_47	V21
FPGA_DONE	DONE_0	N7
TEST_LED1	IO_L18P_T2U_N10_AD2P_67	D20
TEST_LED2	IO_L18N_T2U_N11_AD2N_67	D21

Part 16 Buttons

The AXKU041 development board has two buttons, one of which is a reset button. 1 user button, user button and reset button are connected to IO of FPGA BANK47. User key low level effective, for customers to achieve some functions of the board; The reset button is used to reset the system

Figure 16-1 shows the connection of keys.

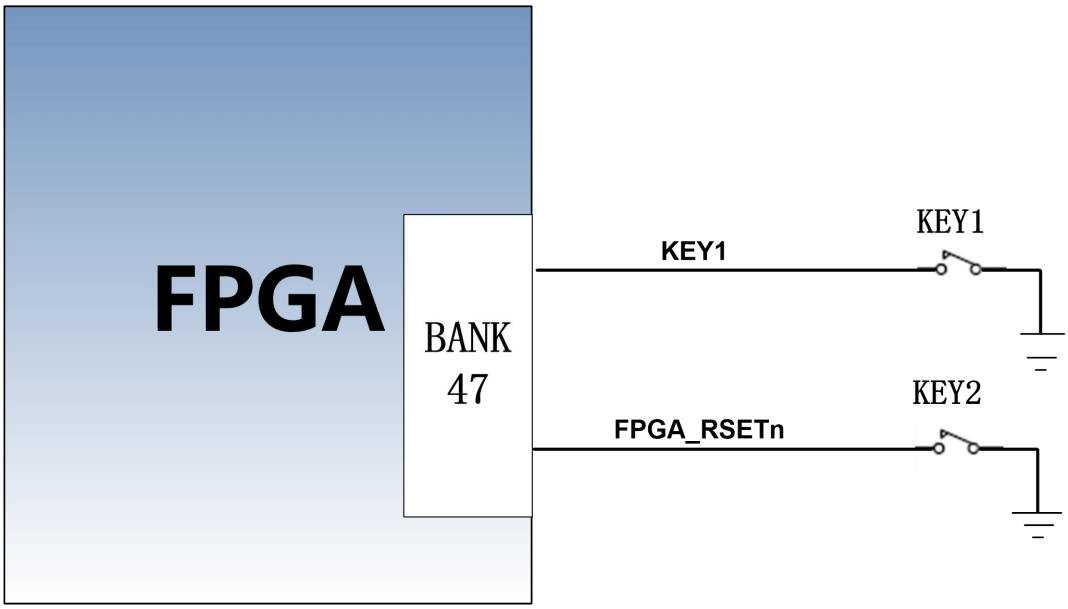


Figure 16-1

Signal Name	PIN Name	FPGA PIN
KEY1	IO_T1U_N12_47	Y22
FPGA_RSETn	IO_T2U_N12_47	Y21

Part 17 Power Supply

The power input voltage of the development board is DC12V, and the external +12V power supply supplies power to the board. For external power supply, please use the power supply provided by the development board. Do not use the power supply of other specifications, so as not to damage the development board

Figure 17-1 shows the schematic diagram of power supply design on the board:

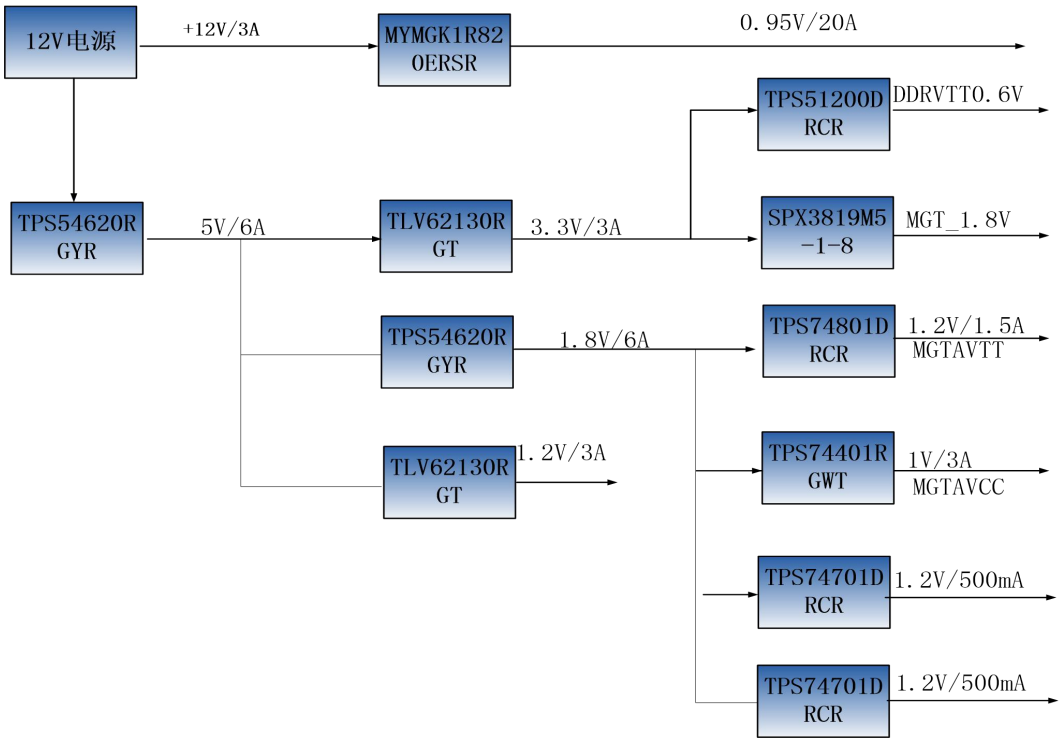


Figure 17-1

The following table describes the functions of each power supply:

power supply	function
+0.95V	FPGA core voltage
+3.3V	FPGA chip IO voltage, FMC, optical fiber, LED lamp, SD card, level conversion chip
+1.8V	HDMI chip, level converter chip voltage, power supply voltage
1.2V/1.5A, 1.2V/500mA	DDR4, FPGA chip, VOLTAGE on FMC, auxiliary voltage, network port chip

MGTAVCC(+1.0V)	FPGA voltage
MGTAVTT(+1.2V)	FPGA voltage
DDRVTT（0.6V）	DDR4 Pull-up voltage
MGT_1.8V (+1.2V)	FPGA GTH boosting voltage

Part 18 FAN

Since FPGA generates a lot of heat when it works normally, we added a heat sink and fan to the chip on the board to prevent the chip from overheating. The control of the fan is controlled by THE FPGA chip, and the control pin is connected to the IO of BANK48. If the IO level output is high, the MOSFET tube is on, and the fan works. Figure 18-1 shows the fan module design:

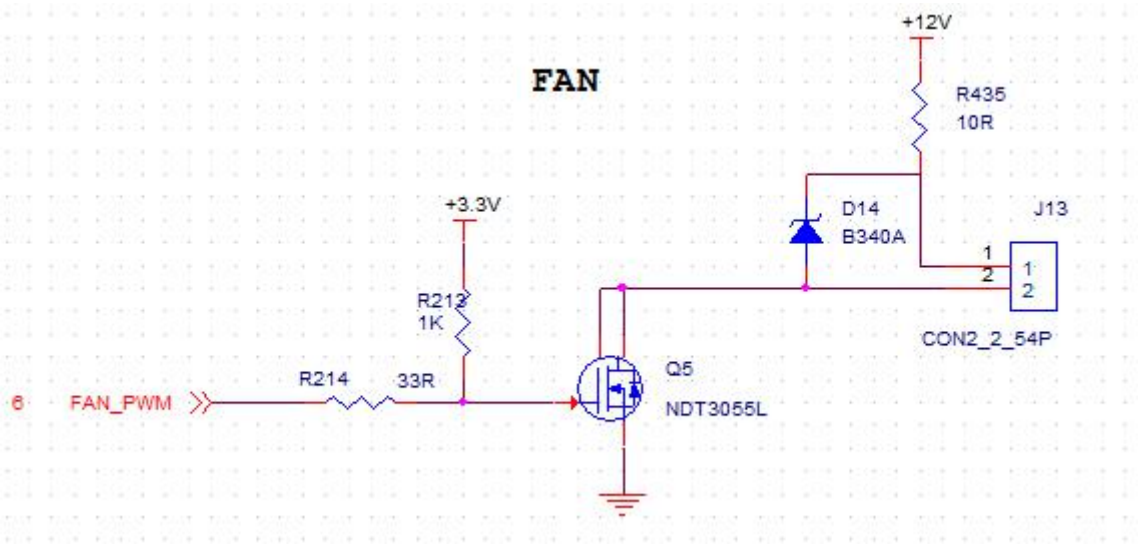
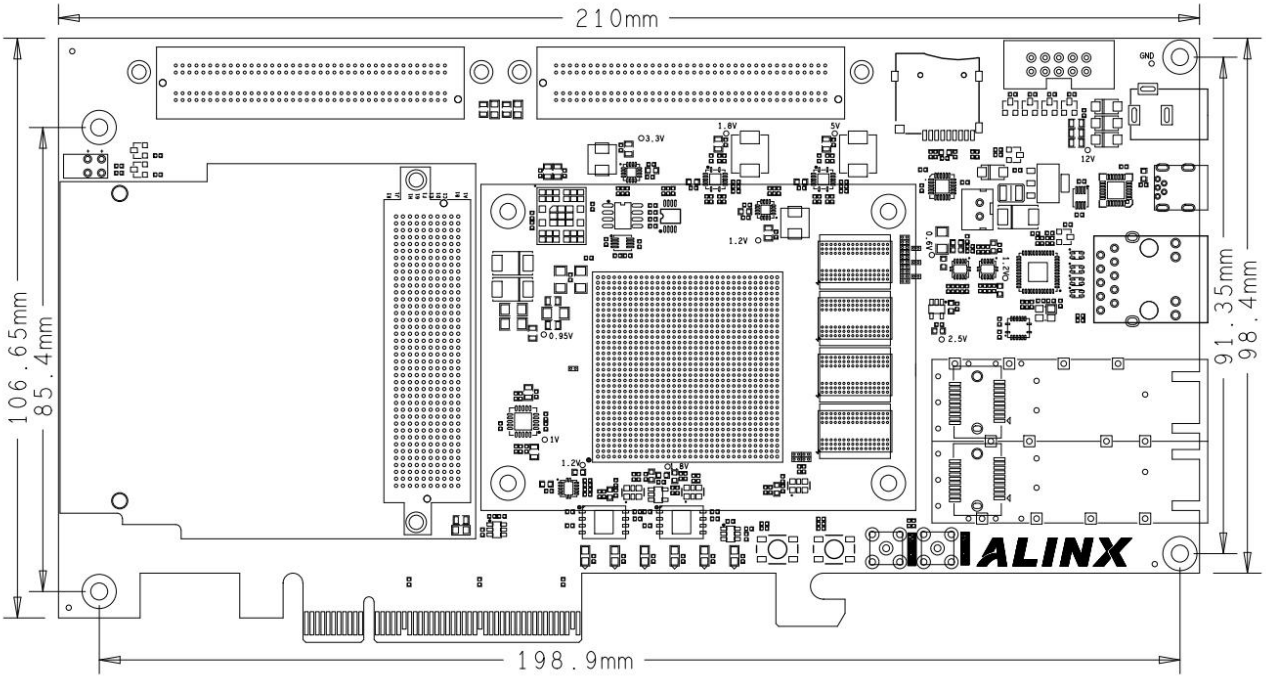


Figure 18-1

Signal Name	PIN Name	FPGA PIN	Description
FAN_PWM	IO_T1U_N12_48	AE31	Fan control pin

Part 19 Structural dimension drawing



front（Top View）