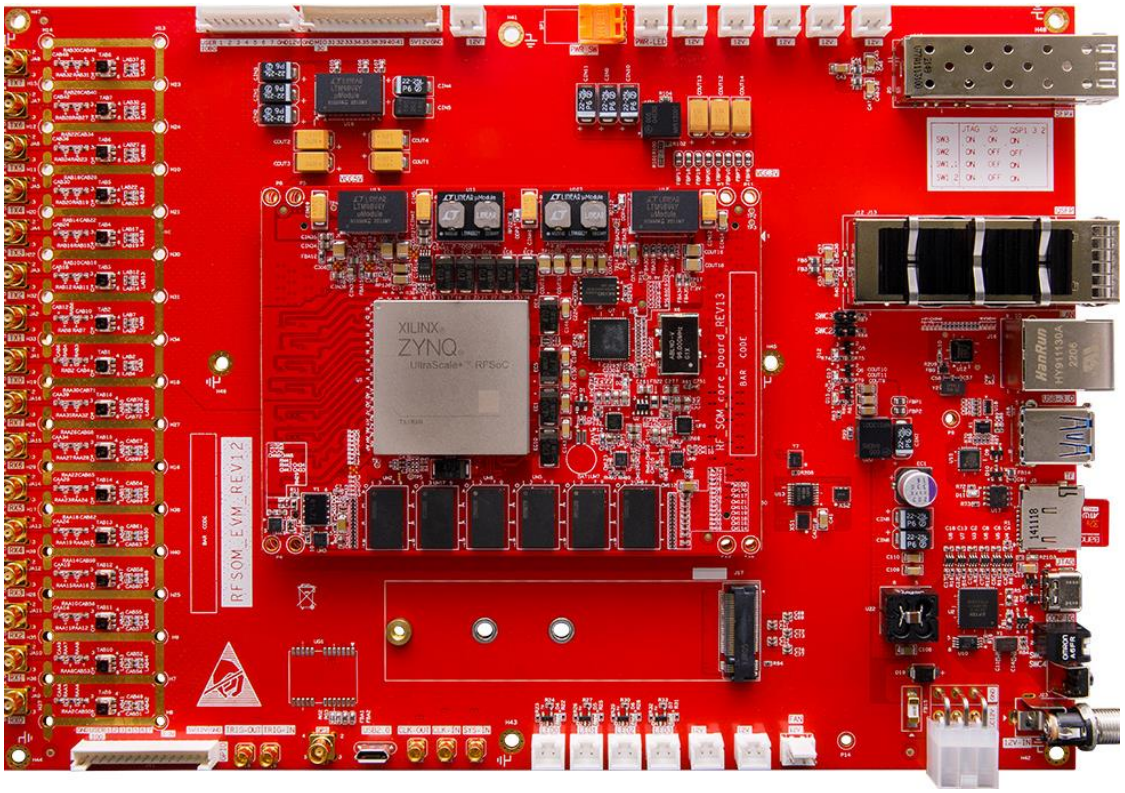
RFEVM development platform

AXRF47 User Manual

Rev. 1.0



Version Record

Version	Date	Release By	Description
Rev 1.0	2024/3/11	Kathy Xia	First Release

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Part 1: Development Board Introduction

The AXRF47 development board consists of an ACRF47 SOM and a base board, which are connected by a high-speed inter-board connector.

The ACRF47 module adopts Zynq UltraScale+ RFSoc Gen3 series ZU47DR FPGA main chip of Xilinx Company, which supports 8-channel 14-bit RF-ADC of maximum sampling rate up to 5GSPS and supports 8-channel 14-bit RF-DAC of maximum sampling rate up to 9.84 GSPS. It reduces the complexity of the RF signal processing chain, maximizes input/output channel density without sacrificing bandwidth, takes advantage of heterogeneous processing capabilities, and has lower power consumption (eliminating ADC/DAC components and eliminating the power of the FPGA-to-analog interface). Offering a comprehensive RF signal chain with an ARM Cortex-A53 processing subsystem, UltraScale+ programmable logic, and the highest signal processing bandwidth available in a Zynq UltraScale+ device, which meets the needs of wireless, cable TV access, test and measurement, early warning/radar, and other high-performance RF applications.

The carrier board expands abundant peripheral interfaces for the SOM module, including one M.2 SSD interface, one USB3.0 interface, one Gigabit Ethernet interface, one JTAG/UART interface, one TF card interface, one SFP interface and one QSFP interface.

The following figure shows the structure of the entire development system:

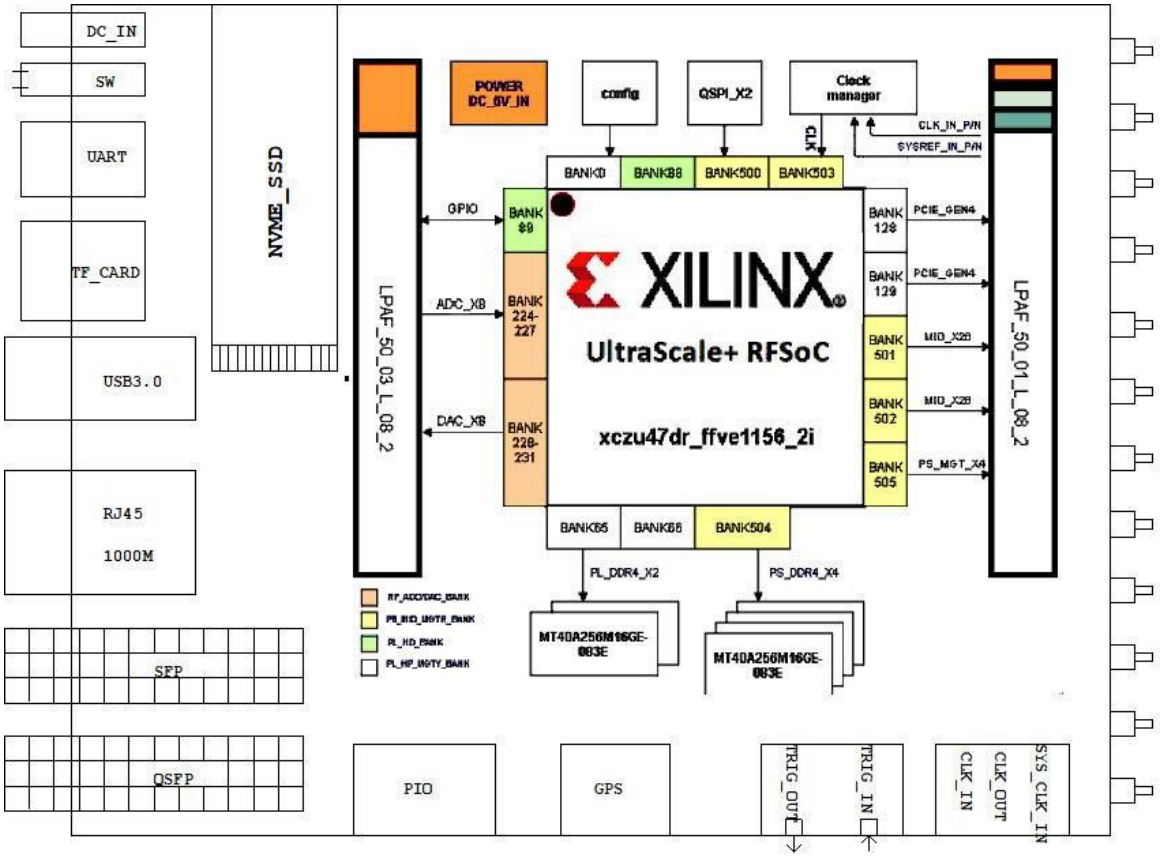

Figure 1: Structure of AXRF47 Development Board

Through Figure 1, we can see the interfaces and functions that the RFEVM development platform can

contain.

- **ACRF47 SOM**

It is composed of ZU47DR + 4GB DDR4 (PS) + 2GB DDR4 (PL) + 1Gb QSPI Flash. In addition, the SOM module provides a dual-crystal oscillator clock source, a single-ended 33.3333MHz active crystal oscillator is provided for the PS system, and a crystal 32.76MHz drives the internal RTC circuit of the RFSOC.

- **M.2 interface**

One PCIe x2 standard M.2 interface is used to connect M.2 SSD.

- **USB3.0 interface**

One USB3.0 interface supports three modes of HOST and SLAVE.

- **Gigabit Ethernet interface**

One 10M/100M/1,000M Ethernet RJ45 interface is used for Ethernet data exchange with computers or other network devices.

- **JTAG & UART interface**

The JTAG & UART debugging interface is a Type-C interface, which is shared by JTAG and UART to Download and debug the FPGA program.

- **Micro SD deck**

One Micro SD deck for storing operating system images and file systems.

- **QSFP28 optical interface**

One QSFP28 optical interface supports communication rate of 40G/100G.

- **SFP optical interface**

One SFP interface supports 10G communication rate.

- **Expand IO**

Three groups of expansion IO, two groups of PL-side expansion IO and one group of PS-side expansion IO, which can be customized by users.

- **LED**

4 expandable LED straight pins for user customization.

- **Key**

A reset button.

Part 2: ACRF47 SOM Module

Part 2.1: Introduction

The ZYNQ chip of ACRF47 SOM module is based on Zynq UltraScale+ RFSoC Gen3 series ZU47DR-2FFVE1156I of XILINX.

This module uses six DDR4 chips MT40A512M16 from Micron, in which four DDR4 chips are mounted on the PS side to form a 64-bit data bus width and two pieces of DDR4 are mounted on the PL side to form a 32-bit data bus width. DDR4 capacity is 1GB per chip. DDR4 SDRAM can run up to 1200MHz (2400Mbps data rate). In addition, 1Gbit QSPI FLASH is also integrated on the module for boot storage configuration and system files.

To connect with the base board, the two 400Pin board-to-board connectors of this module expand the USB3.0 interface, Gigabit Ethernet interface, SD card interface, M.2 interface and the remaining MIO interface at the PS end, and expand four pairs of PS MGT high-speed transceiver interfaces; As well as 1 QSFP28 interface, 1 SFP interface and other IO at the PL end.

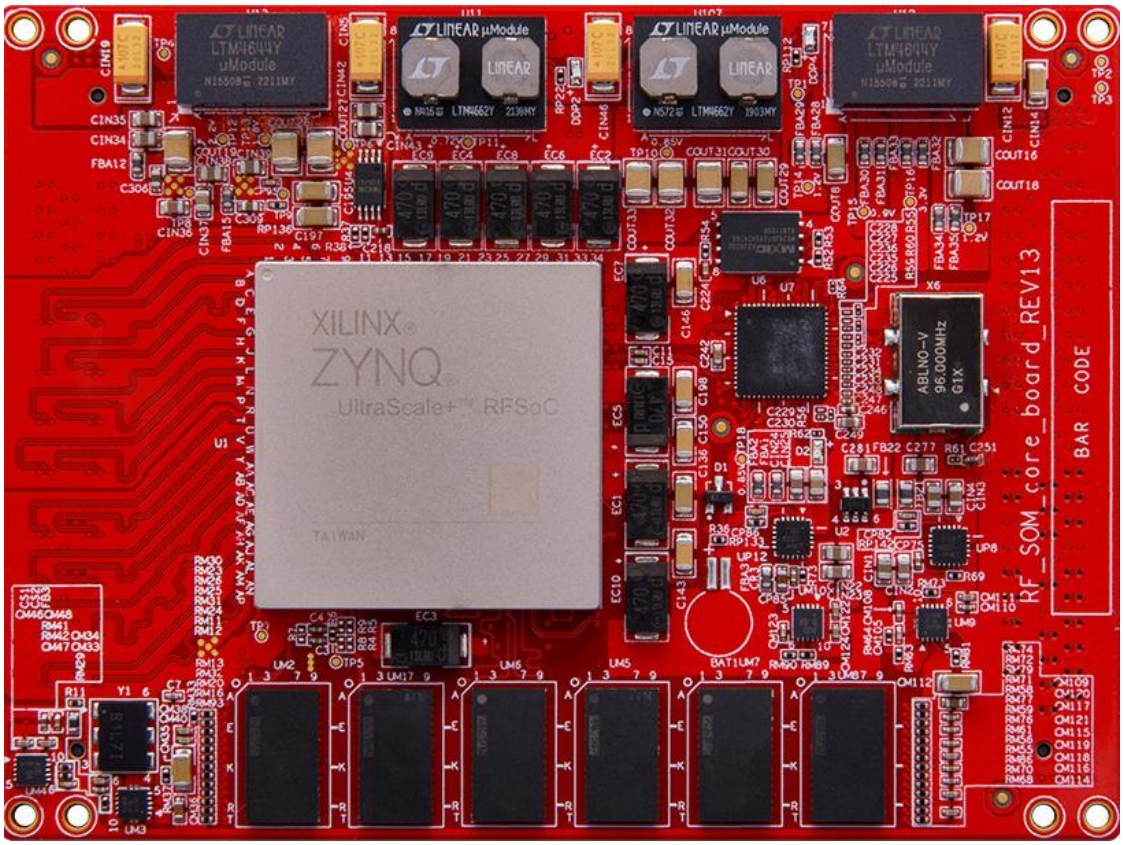

Figure 2: Front view of ACRF47 module

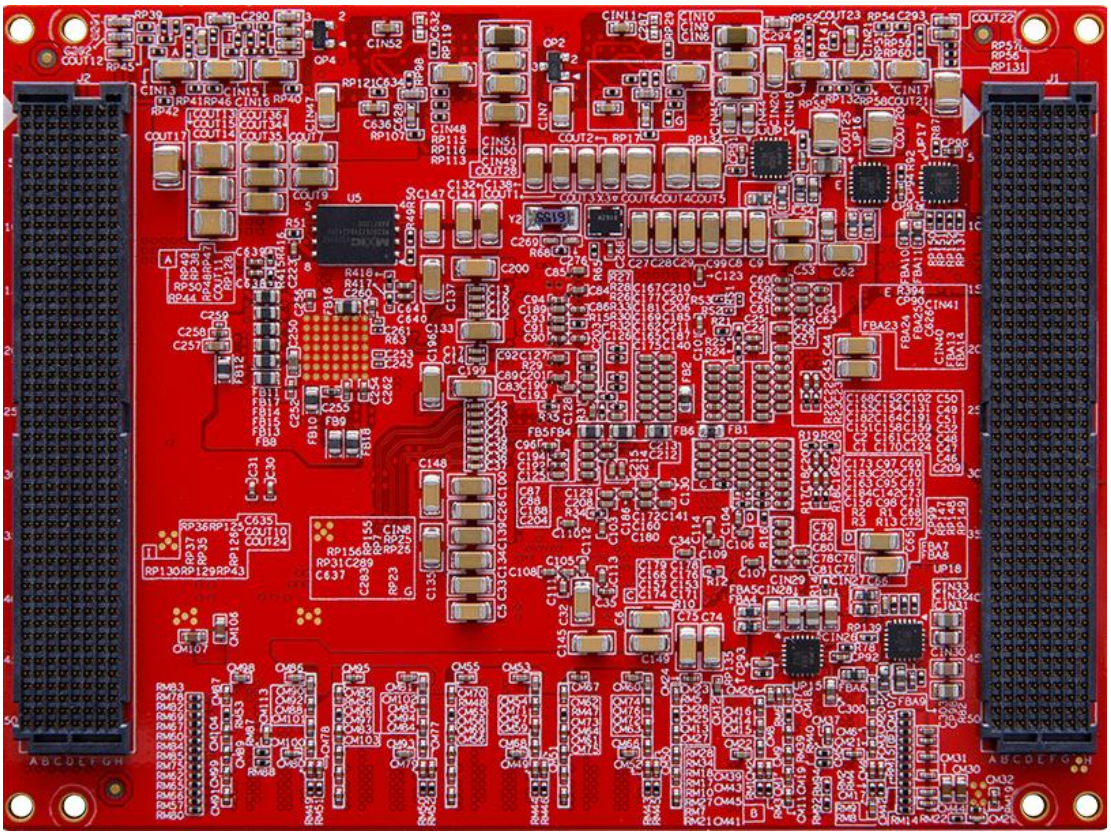

Figure 3: Back view of ACRF47 module

Part 2.2: Zynq Chip

The ACRF47 module uses a Zynq UltraScale+ RFSoC Gen3 series chip from Xilinx, model ZU47DR-2FFVE1156I. FPGA resources in the programmable logic section can provide high-throughput digital signal processing (DSP) and IP cores, such as digital up/down conversion (DUC/DDC) cores. FPGA acceleration is made easier by the software radio development architecture application programming interface and the FPGA infrastructure. This helps you get up and running quickly so you can focus on value-added IP. An FPGA system for common functions such as Fast Fourier Transform (FFT) and Finite Impulse Response (FIR) filters is a good place to start. You can then add your own IP blocks to the modular architecture using your preferred hardware description language (HDL). In addition to the FPGA architecture portion of the system, the Xilinx UltraScale+ RFSoC is equipped with four on-board application processing units (APUs) and two real-time processing units (RPUs). For applications that require an on-board embedded operating system for standalone operation.

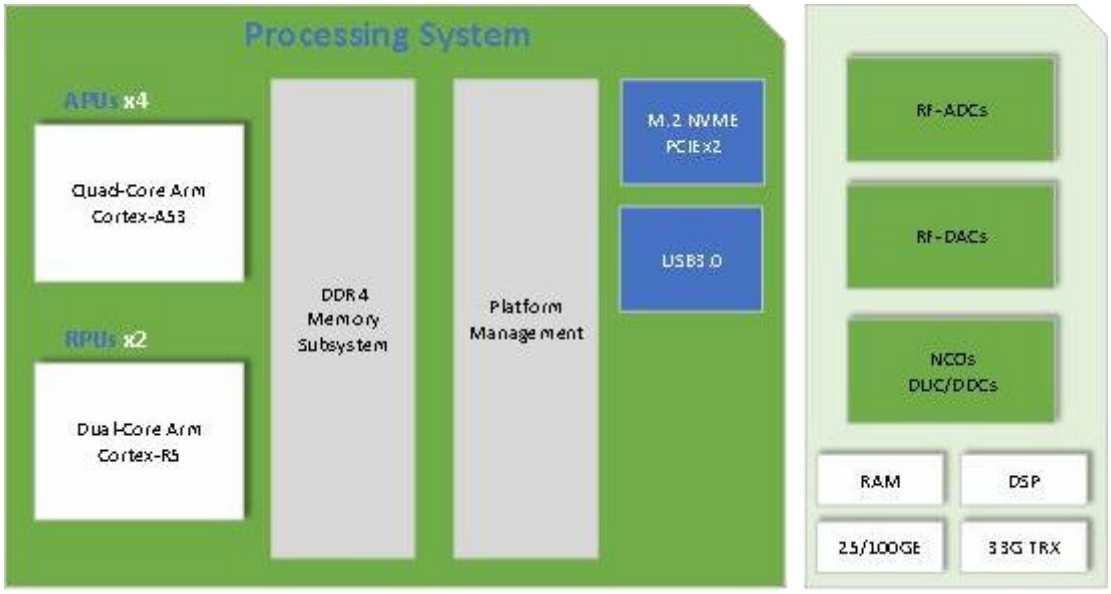

Figure 4: Block diagram of RFSOM hardware system

ACRF47 can support full differential extraction of AD/DA channels. Users can define RF conditioning circuits as required, support DC and AC coupling, and support PA \ LNA amplifier conditioning circuits. It can also support optional RF front-end, LO converter, duplexer, PA, LNA, etc.

Part 2.3: DDR4 SDRAM

The ACRF47 module is equipped with six Micron 1GB DDR4 chips, model MT40A512M16GE-083E, in which four DDR4 chips are mounted on the PS side, forming 64bit data bus bandwidth. Two pieces of DDR4 chips are mounted on the PL side to form 32bit data bus bandwidth. The maximum operating speed of DDR4 SDRAM on the PS side can reach 1200MHz (data rate 2400Mbps), and four DDR4 storage systems directly connected to the memory interface of the bank 504 of the PS. The maximum running speed of DDR SDRAM on the PL side can reach 1200MHz (data rate 2400Mbps), and two DDR4 chips are connected to the BANK65 and BANK66 interfaces of the FPGA. The specific configuration of PS-side and PL-side DDR4 SDRAM is shown in the following table.

Location	Tag number	Chip model	Capacity	Manufacturer
PS	UM5,UM6,UM7,UM8	MT40A512M16GE-083E	512x16bit	Micron
PL	UM1,UM2	MT40A512M16GE-083E	512x16bit	Micron

Table 1: DDR4 SDRAM Configuration

The hardware connection mode of DDR4 on the PS side is shown in figure 5:

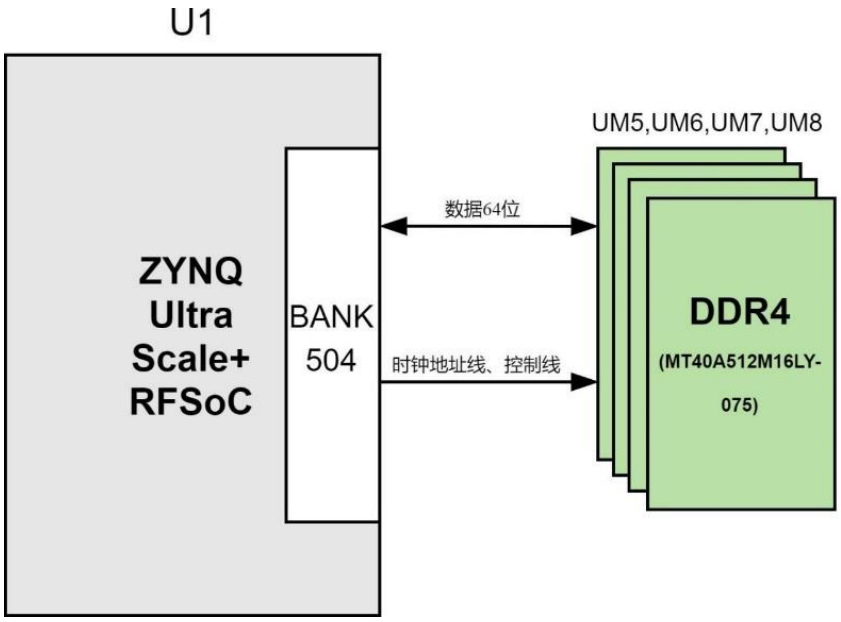

Figure 5: Schematic diagram of PS-side DDR4 SDRAM connection

The hardware connection mode of DDR4 SDRAM on the PL is shown in figure 6:

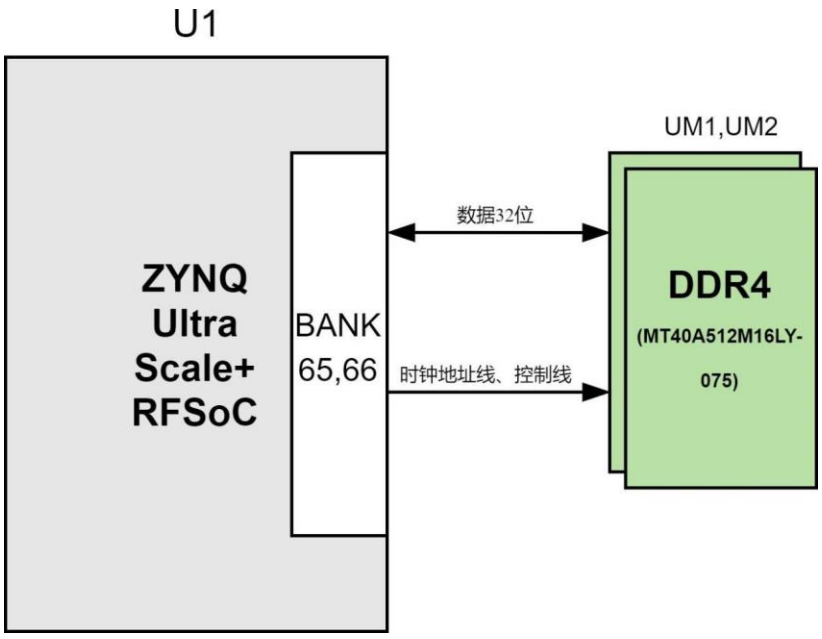

Figure 6 Schematic diagram of PL-side DDR4 SDRAM connection

Part 2.4: QSPI Flash

The ACRF47 module is equipped with two 512Mbit QUAD SPI FLASH chips to form an 8-bit bandwidth data bus. The FLASH model is MT25QU512ABBIEW9-0SIT, which uses 1.8V CMOS Voltage standard. Due to the non-volatile nature of QSPI FLASH, it can be used as the boot device of the system to store the boot image of the system. These images mainly include FPGA bit files, ARM application code and its user data files. See the following table for the specific model and related features of QSPI Flash.

Location	Tag number	Chip model	Capacity	Manufacturer
PS	U5,U6	MT25QU512ABBIEW9-0SIT	512M bit	Micron

Table 2: QSPI Flash Models and Parameters

The QSPI FLASH is connected to the MIO of BANK500, the PS part of the ZYNQ chip. In the system design, it is necessary to configure these MIO functions of PS end as QSPI Flash interfaces.

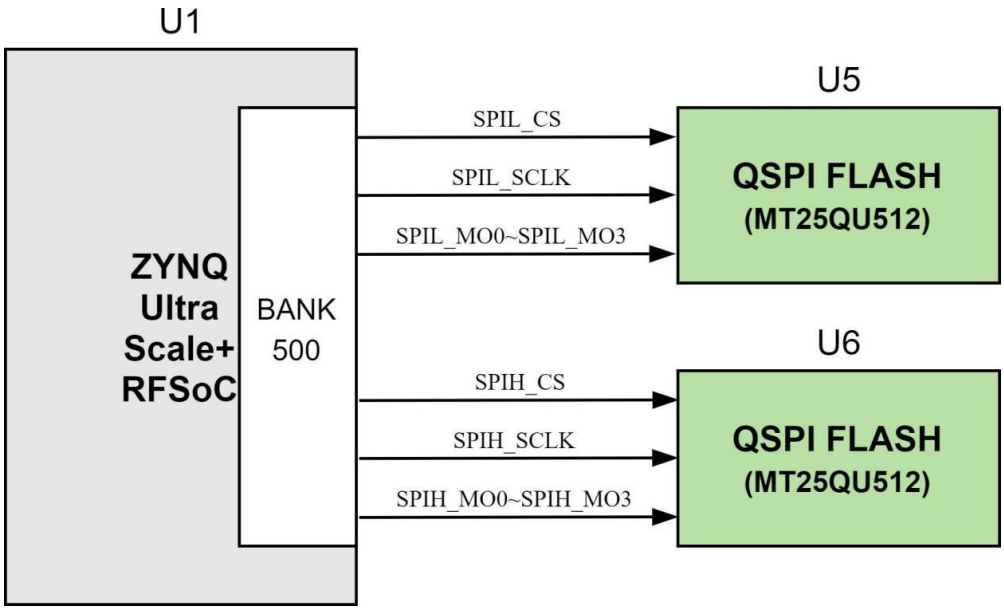

Figure 7: QSPI FLASH Connection Diagram

Signal name	Pin name	Pin number
SPIL_SCLK	PS_MIO0	J17
SPIL_MO1	PS_MIO1	J18
SPIL_MO2	PS_MIO2	J16
SPIL_MO3	PS_MIO3	K16
SPIL_MO0	PS_MIO4	G15
SPIL_CS	PS_MIO5	H18
SPIH_CS	PS_MIO7	K17
SPIH_MO0	PS_MIO8	E15
SPIH_MO1	PS_MIO9	F15
SPIH_MO2	PS_MIO10	C15
SPIH_MO3	PS_MIO11	G16
SPIH_SCLK	PS_MIO12	B15

Table 3: Configuring Chip Pin Assignments

Part 2.5: EEPROM

The ACRF47 module has an EEPROM on board, the model is AT24CM01, the capacity is 1Mbit, and it is connected to the PS end for communication through the IIC bus.

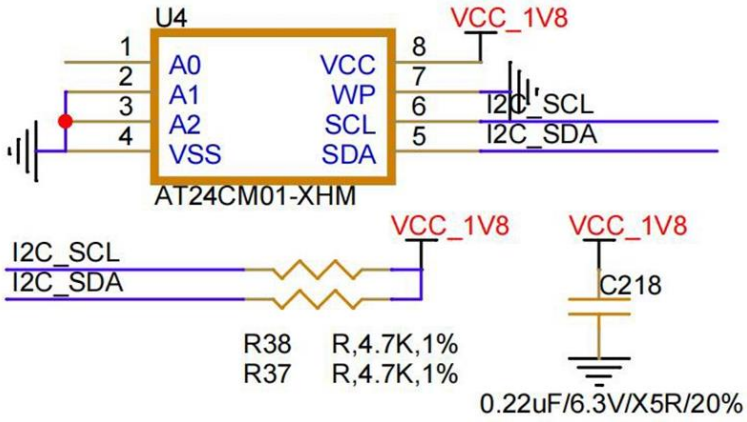

Figure 8: EEPROM Hardware Schematic

Signal name	Pin name	Pin number	Remark
IIC_SDA	PS_MIO25	B17	I2C Data Signal
IIC_SCL	PS_MIO24	A17	I2C Clock Signal

Table 4: EEPROM Pin Assignment

Part 2.6: Clock Configuration

Dual crystal oscillator clock is provided on SOM module. The system clock uses 33.3333MHz active crystal oscillator by default. The package is 3.2x2.5mm. Crystal 32.768 KHz, driving the ACRF47 internal RTC circuit. The schematic diagram of the clock circuit design is shown in the following figure:

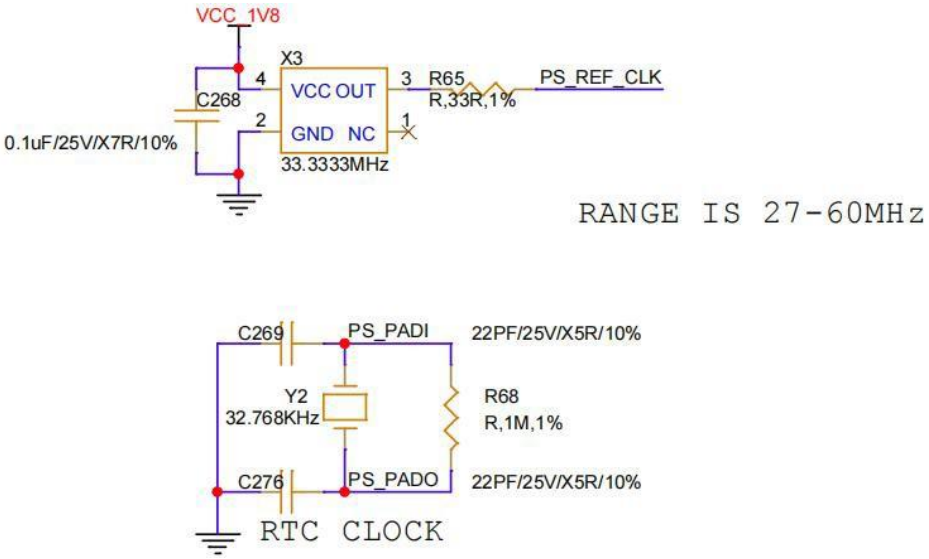

Figure 9: Schematic diagram of crystal oscillator

The module system uses LMK04828 clock chip to distribute the clock required by each module, and the main crystal oscillator uses 19.2MHz high stability OCXO. Support GTY recovery clock, support input of external reference clock and SYSREF input, and realize parallel connection of multiple modules to form a larger-scale coherent RF channel.

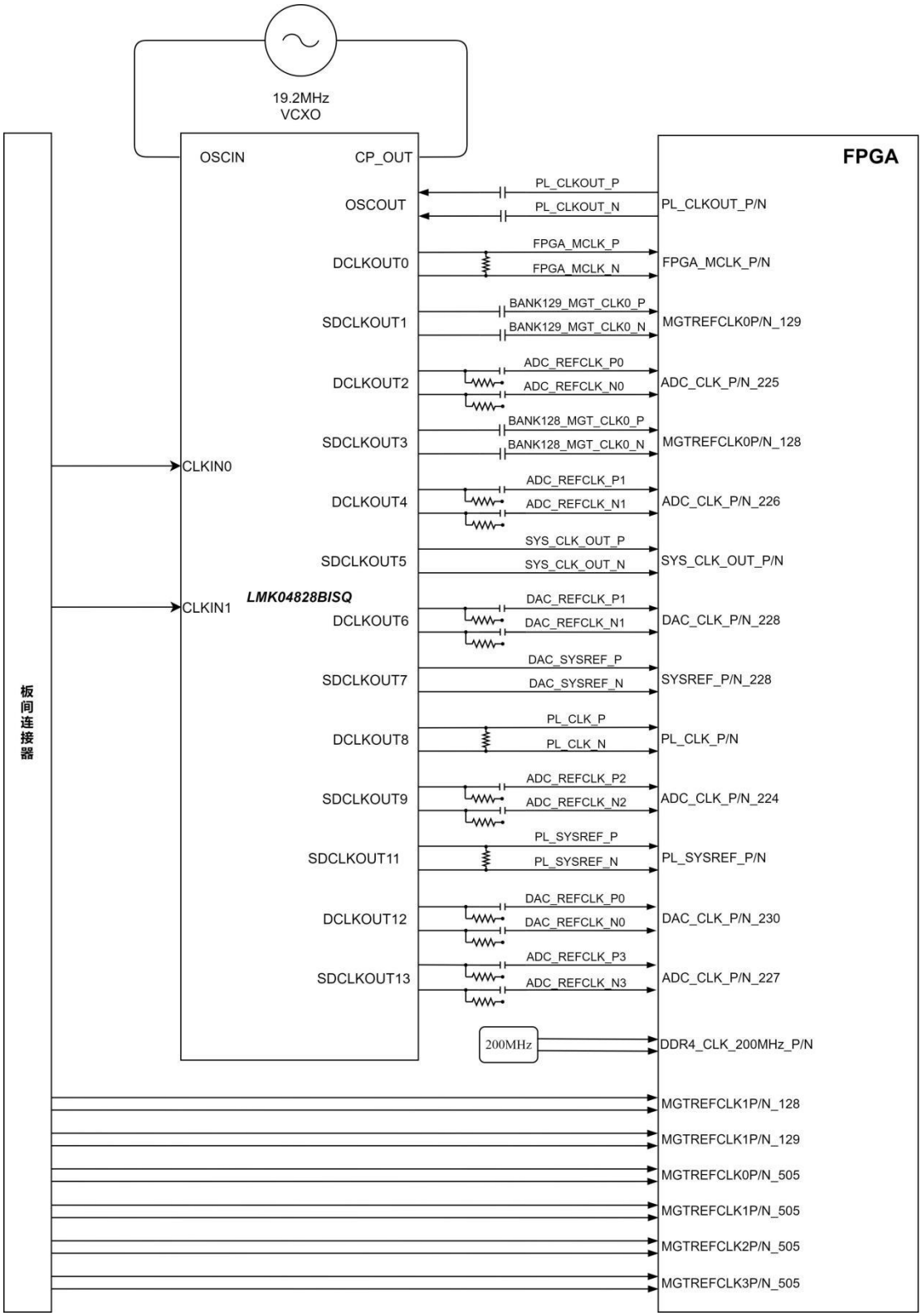

Figure 10: Schematic diagram of clock distribution connection

Part 2.7: PS-GTR Interface

The PS-side GTR high-speed BANK of the ACRF47 module is not used and is pulled out through the connector. It supports a data rate of up to 6.0 Gb/s and can be used as x1, x2 and x4 of PCIE Gen2. As well as can also be used as a SATA interface, supporting 1.5Gb/s, 3.0Gb/s, 6Gb/s data rates, and DP interface and USB3.0 interface and other applications.

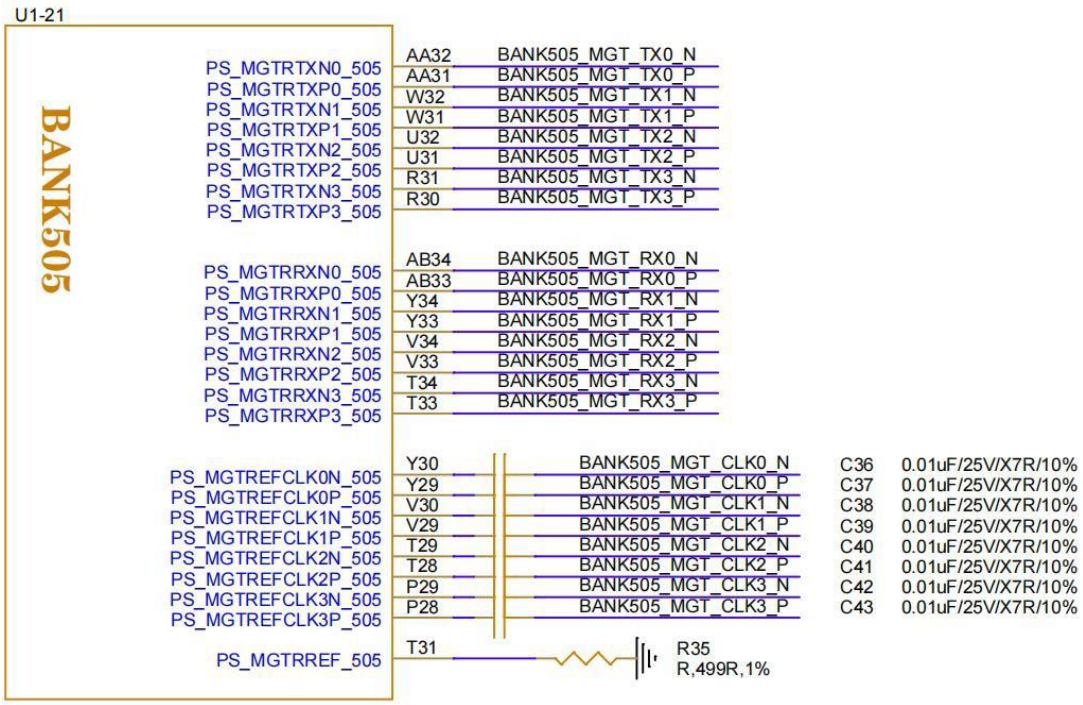

Figure 11: Mapping Diagram of GTR High-speed Transceiver at PS End

Part 2.8: PCIE Gen4 Connector (Requires PCIe carrier card)

The ACRF47 supports the GTY high-speed transceiver, which enables PCIe x8 Gen4.0 at data rates up to 16.0 Gb/s, as well as 100G optical interface interconnects. It is convenient for users to develop for the second time, and the design risk is small, convenient, and flexible.

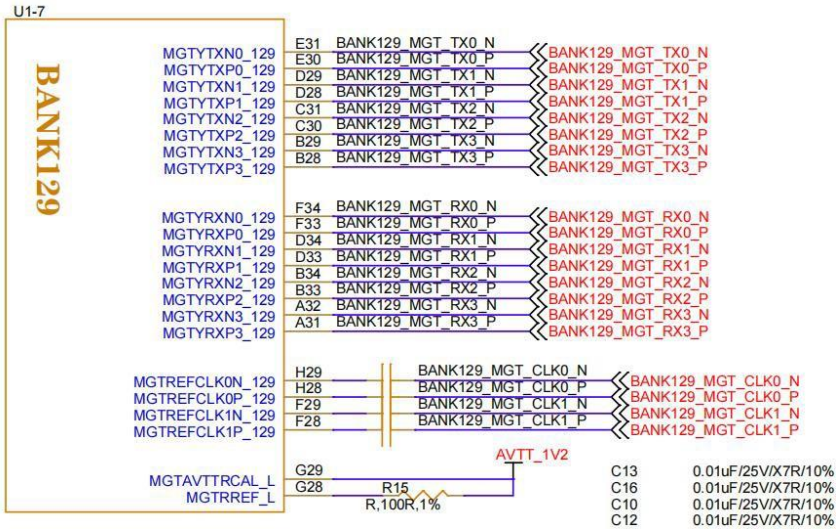

Figure 12: High Speed Transceiver Map

Part 2.9: RF-ADC Interface

The FPGA chip used in the ACRF47 module is the only single-chip adaptive radio platform of Zynq UltraScale+ RFSoC Gen3 series in the industry, which integrates a 14-bit RF-ADC. The maximum sampling rate is up to 5GSPS, and the VCM signal is also brought out to the connector, making it easier for the user to adjust the common-mode voltage.

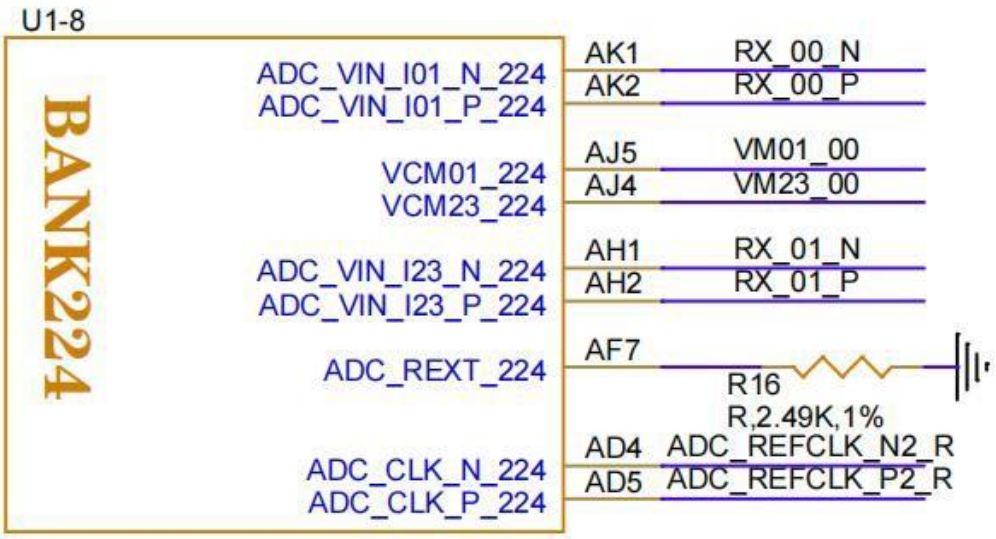

Figure 13: RF-to-ADC Interface Schematic

Part 2.10: RF-DAC Interface

The FPGA chip used in the core module of ACRF47 is the only single-chip adaptive radio platform of Zynq UltraScale+ RFSoC Gen3 series in the industry. The chip integrates a 14-bit RF-DAC with a maximum sampling rate of 9.85 GSPS.

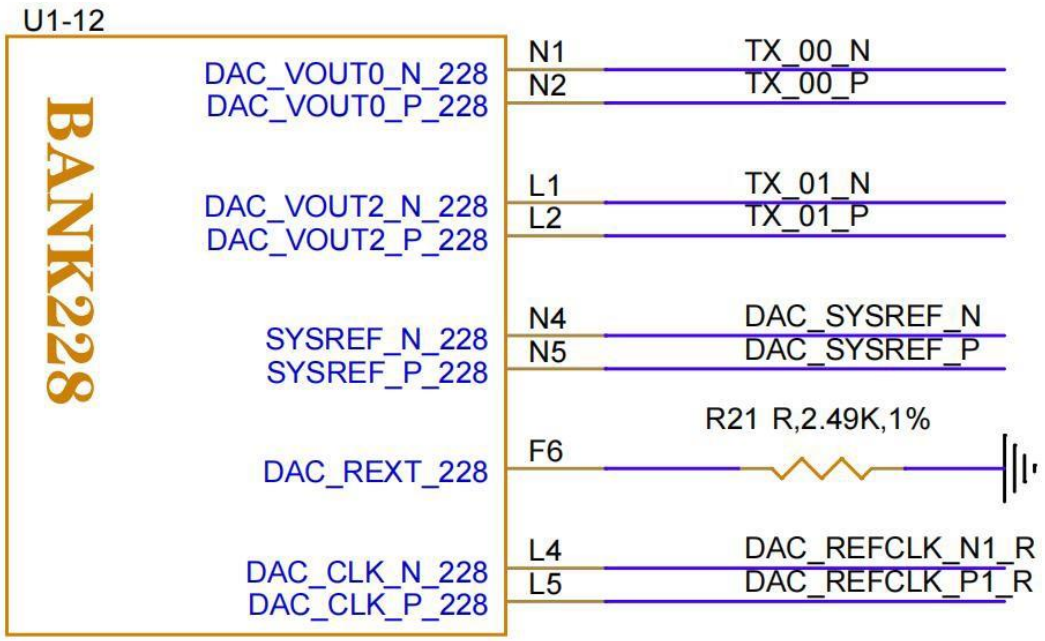

Figure 14: RF-to-DAC Interface Schematic

Part 2.11: Power Source

The ACRF47 module is powered by DC 5V, and the power is supplied to the module through the connector in base board. The ACRF47 module typically consumes 60W. The 5V system power supply drives the FPGA and other circuits on the board by converting different voltages through the buck regulator. The power supply of the ADC and DAC on the board is provided by the linear low-voltage LDO, which has good power supply rejection (PSRR).

The extended IO BANK interface level of the core module is shown in the figure below:

BANK	Level (V)	Remark
BANK89	Supplied from the base board	HD _ BANK supports 1.2 ~ 3.3V (HD I/O only) at ± 5%
BANK128	MGTY	PCIE Gen4 signal
BANK129	MGTY	PCIE Gen4 signal
BANK501	Supplied from the base board	MIO BANK supports 1.8V, 2.5V, and 3.3V at ± 5%
BANK502	Supplied from the base board	MIO BANK supports 1.8V, 2.5V, and 3.3V at ± 5%
BANK503	1.8 V fixed	Configure pin output, mode selection, system reset signal
BANK505	PS_MGTR	Without any definition, the high-speed signal pin and clock signal are all pulled out to the connector.

Table 5: Extended IO BANK interface level of the core module

The power supply design block diagram of the ACRF47 core module is shown below:

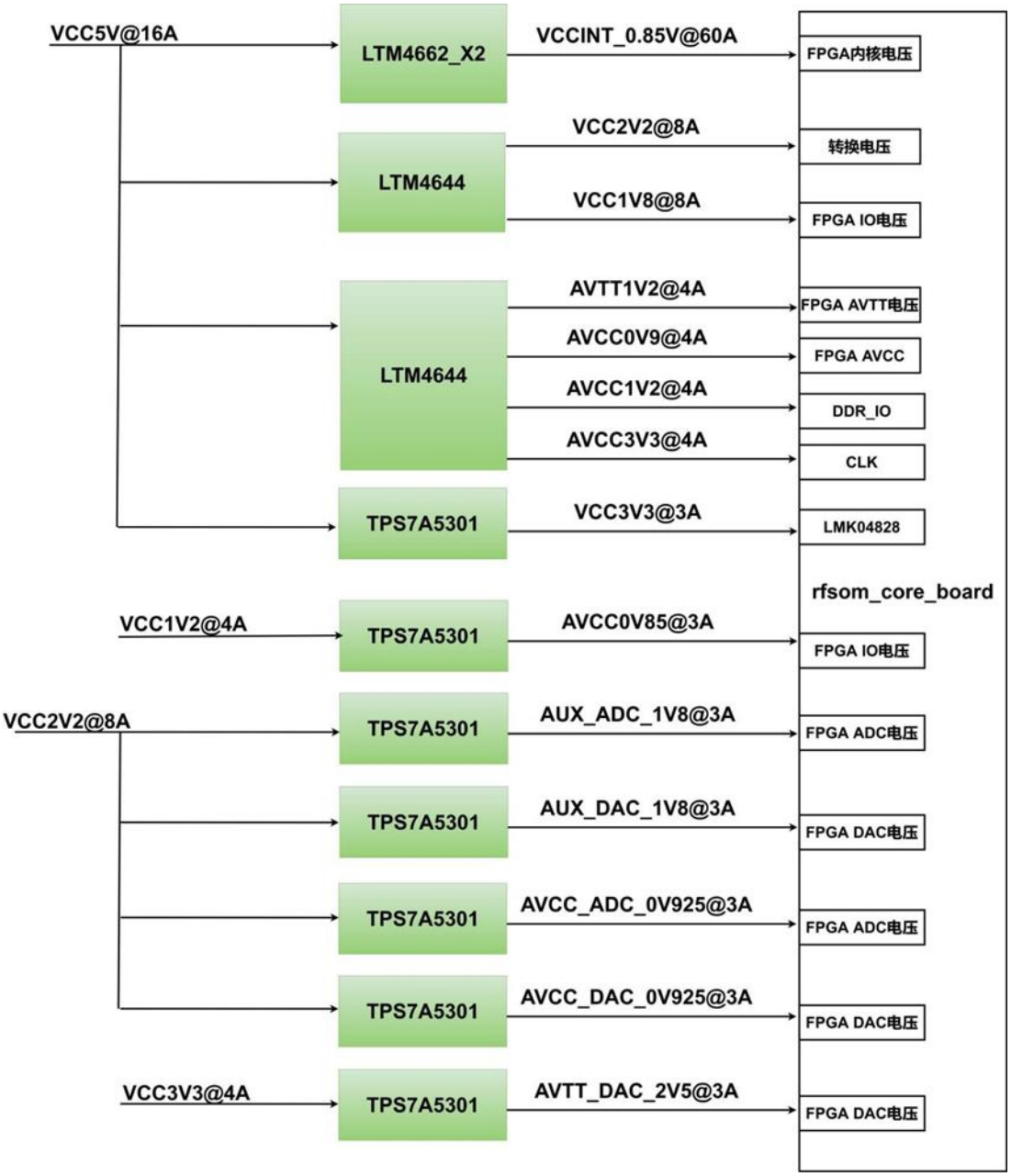

Figure 15: Design block diagram of ACRF47 module power supply

Part 2.12: Structure Diagram

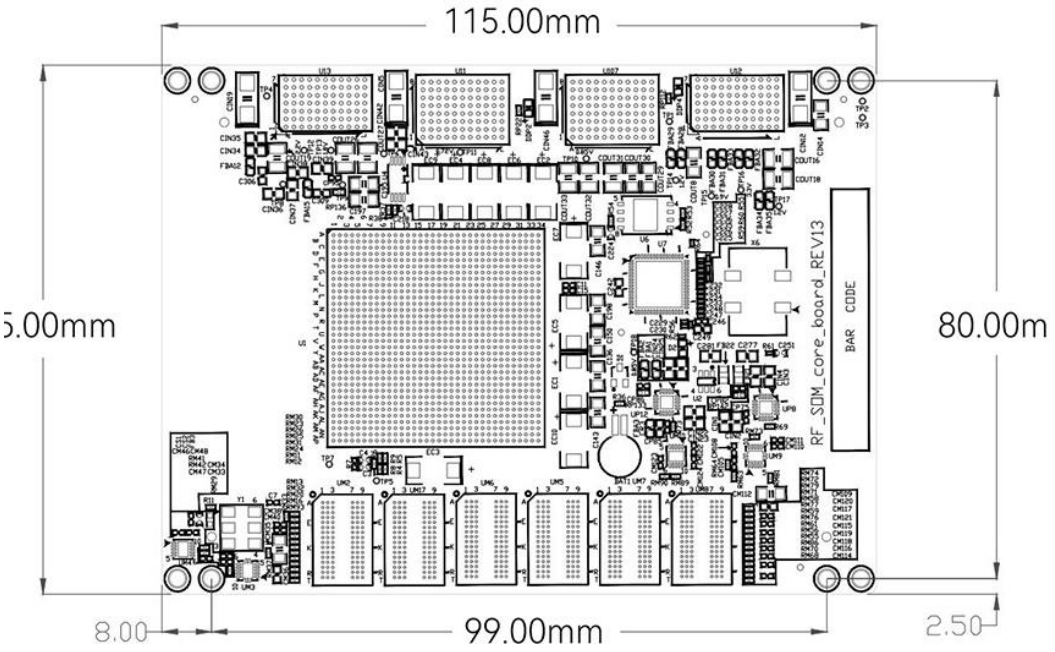

Figure 16: Front view of ACRF47 core module

Part 2.13: Connector Pin Definition

Two high-speed expansion ports are extended on the module, and two 400Pin inter-board connectors (J1, J2) are used to connect with the base board. The connector is the LPAM_50_01_0_L_08_2_K_TR connector of Samtec.

The connector signals are defined as follows:

Mark Number	Signal Network	Mark Number	Signal Network	Mark Number	Signal Network	Mark Number	Signal Network
A1	GND	B1	VCC_5V	C1	VCC_5V	D1	VCC_5V
A2	GND	B2	VCC_5V	C2	VCC_5V	D2	VCC_5V
A3	GND	B3	GND	C3	GND	D3	GND
A4	GND	B4	GND	C4	GND	D4	GND
A5	GND	B5	GND	C5	GND	D5	GND
A6	GND	B6	GND	C6	GND	D6	GND
A7	GND	B7	BANK89_IO_L1P	C7	BANK89_IO_L1N	D7	GND
A8	GND	B8	GND	C8	GND	D8	BANK89_IO_L2P

A9	GND	B9	BANK89_IO_L3P	C9	BANK89_IO_L3N	D9	GND
A10	GND	B10	GND	C10	GND	D10	BANK89_IO_GC_L5P
A11	GND	B11	BANK89_IO_GC_L7P	C11	BANK89_IO_GC_L7N	D11	GND
A12	GND	B12	GND	C12	GND	D12	BANK89_IO_GC_L6P
A13	GND	B13	BANK89_IO_L4P	C13	BANK89_IO_L4N	D13	GND
A14	GND	B14	GND	C14	GND	D14	BANK89_IO_L9P
A15	GND	B15	GND	C15	GND	D15	GND
A16	GND	B16	GND	C16	GND	D16	GND
A17	GND	B17	GND	C17	GND	D17	GND
A18	GND	B18	TX_06_P	C18	TX_06_N	D18	GND
A19	GND	B19	GND	C19	GND	D19	GND
A20	GND	B20	GND	C20	GND	D20	GND
A21	GND	B21	GND	C21	GND	D21	GND
A22	GND	B22	TX_04_P	C22	TX_04_N	D22	GND
A23	GND	B23	GND	C23	GND	D23	GND
A24	GND	B24	GND	C24	GND	D24	GND
A25	GND	B25	GND	C25	GND	D25	GND
A26	GND	B26	TX_02_P	C26	TX_02_N	D26	GND
A27	GND	B27	GND	C27	GND	D27	GND
A28	GND	B28	GND	C28	GND	D28	GND
A29	GND	B29	GND	C29	GND	D29	GND
A30	GND	B30	TX_00_P	C30	TX_00_N	D30	GND
A31	GND	B31	GND	C31	GND	D31	GND
A32	GND	B32	GND	C32	GND	D32	GND
A33	GND	B33	GND	C33	GND	D33	NC
A34	GND	B34	RX_06_P	C34	RX_06_N	D34	GND
A35	GND	B35	GND	C35	GND	D35	GND

A36	GND	B36	GND	C36	GND	D36	GND
A37	GND	B37	GND	C37	GND	D37	NC
A38	GND	B38	RX_04_P	C38	RX_04_N	D38	GND
A39	GND	B39	GND	C39	GND	D39	GND
A40	GND	B40	GND	C40	GND	D40	GND
A41	GND	B41	GND	C41	GND	D41	NC
A42	GND	B42	RX_02_P	C42	RX_02_N	D42	GND
A43	GND	B43	GND	C43	GND	D43	GND
A44	GND	B44	GND	C44	GND	D44	GND
A45	GND	B45	GND	C45	GND	D45	NC
A46	GND	B46	RX_00_P	C46	RX_00_N	D46	GND
A47	GND	B47	GND	C47	GND	D47	GND
A48	GND	B48	GND	C48	GND	D48	GND
A49	GND	B49	GND	C49	GND	D49	GND
A50	GND	B50	GND	C50	GND	D50	GND

Table 5: Signal Definition of J1 Connector

Mark Number	Signal Network	Mark Number	Signal Network	Mark Number	Signal Network	Mark Number	Signal Network
E1	VCC_5V	F1	VCC_5V	G1	VCC_5V	H1	GND
E2	VCC_5V	F2	VCC_5V	G2	VCC_5V	H2	GND
E3	GND	F3	GND	G3	GND	H3	GND
E4	GND	F4	GND	G4	GND	H4	GND
E5	GND	F5	GND	G5	GND	H5	GND
E6	GND	F6	GND	G6	GND	H6	GND
E7	GND	F7	BANK89_IO_L12P	G7	BANK89_IO_L12N	H7	GND
E8	BANK89_IO_L2N	F8	GND	G8	GND	H8	GND
E9	GND	F9	BANK89_IO_GC_L8P	G9	BANK89_IO_GC_L8N	H9	GND
E10	BANK89_IO_GC_L5N	F10	GND	G10	GND	H10	GND

E11	GND	F11	BANK89_IO_L10P	G11	BANK89_IO_L10N	H11	GND
E12	BANK89_IO_GC_L6N	F12	GND	G12	GND	H12	GND
E13	GND	F13	BANK89_IO_L11P	G13	BANK89_IO_L11N	H13	GND
E14	BANK89_IO_L9N	F14	GND	G14	GND	H14	GND
E15	GND	F15	GND	G15	GND	H15	GND
E16	GND	F16	GND	G16	GND	H16	GND
E17	GND	F17	GND	G17	GND	H17	GND
E18	GND	F18	TX_07_P	G18	TX_07_N	H18	GND
E19	GND	F19	GND	G19	GND	H19	GND
E20	GND	F20	GND	G20	GND	H20	GND
E21	GND	F21	GND	G21	GND	H21	GND
E22	GND	F22	TX_05_P	G22	TX_05_N	H22	GND
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E26	GND	F26	TX_03_P	G26	TX_03_N	H26	GND
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E28	GND	F28	GND	G28	GND	H28	GND
E29	GND	F29	GND	G29	GND	H29	GND
E30	GND	F30	TX_01_P	G30	TX_01_N	H30	GND
E31	GND	F31	GND	G31	GND	H31	GND
E32	GND	F32	GND	G32	GND	H32	GND
E33	GND	F33	GND	G33	GND	H33	GND
E34	GND	F34	RX_07_P	G34	RX_07_N	H34	GND
E35	NC	F35	GND	G35	GND	H35	GND
E36	GND	F36	GND	G36	GND	H36	GND
E37	GND	F37	GND	G37	GND	H37	GND
E38	GND	F38	RX_05_P	G38	RX_05_N	H38	GND

E39	NC	F39	GND	G39	GND	H39	GND
E40	GND	F40	GND	G40	GND	H40	GND
E41	GND	F41	GND	G41	GND	H41	GND
E42	GND	F42	RX_03_P	G42	RX_03_N	H42	GND
E43	NC	F43	GND	G43	GND	H43	GND
E44	GND	F44	GND	G44	GND	H44	GND
E45	GND	F45	GND	G45	GND	H45	GND
E46	GND	F46	RX_01_P	G46	RX_01_N	H46	GND
E47	NC	F47	GND	G47	GND	H47	GND
E48	GND	F48	GND	G48	GND	H48	GND
E49	GND	F49	GND	G49	GND	H49	GND
E50	GND	F50	GND	G50	GND	H50	GND

Table 6: J1 Connector Signal Definition

Mark Number	Signal Network	Mark Number	Signal Network	Mark Number	Signal Network	Mark Number	Signal Network
E1	VCCO_501	F1	VCC_5V	G1	VCC_5V	H1	GND
E2	VCCO_501	F2	VCC_501	G2	VCC_5V	H2	GND
E3	GND	F3	GND	G3	GND	H3	GND
E4	GND	F4	CLKIN0_P	G4	CLKIN0_N	H4	GND
E5	SYSREF_IN_N	F5	GND	G5	GND	H5	GND
E6	GND	F6	GND	G6	GND	H6	GND
E7	GND	F7	BANK501_PS_MIO37	G7	BANK501_PS_MIO34	H7	GND
E8	BANK501_PS_MIO36	F8	GND	G8	GND	H8	GND
E9	GND	F9	BANK501_PS_MIO41	G9	BANK501_PS_MIO38	H9	GND
E10	BANK501_PS_MIO39	F10	GND	G10	GND	H10	GND
E11	GND	F11	BANK501_PS_MIO43	G11	BANK501_PS_MIO44	H11	GND
E12	BANK501_PS_MIO45	F12	GND	G12	GND	H12	GND

E13	GND	F13	BANK501_PS_MIO48	G13	BANK501_PS_MIO51	H13	GND
E14	BANK501_PS_MIO47	F14	GND	G14	GND	H14	GND
E15	GND	F15	BANK501_PS_MIO58	G15	BANK501_PS_MIO60	H15	GND
E16	BANK501_PS_MIO59	F16	GND	G16	GND	H16	GND
E17	GND	F17	BANK501_PS_MIO63	G17	BANK501_PS_MIO62	H17	GND
E18	BANK501_PS_MIO55	F18	GND	G18	GND	H18	GND
E19	GND	F19	BANK501_PS_MIO64	G19	BANK501_PS_MIO65	H19	GND
E20	BANK501_PS_MIO71	F20	GND	G20	GND	H20	GND
E21	GND	F21	BANK501_PS_MIO75	G21	BANK501_PS_MIO70	H21	GND
E22	BANK501_PS_MIO74	F22	GND	G22	GND	H22	GND
E23	GND	F23	JTAG_TDI	G23	PS_ERROR	H23	GND
E24	BANK501_PS_MIO77	F24	GND	G24	GND	H24	GND
E25	GND	F25	PS_MODE2	G25	PS_MODE0	H25	GND
E26	PS_MODE1	F26	GND	G26	GND	H26	GND
E27	GND	F27	NC	G27	NC	H27	GND
E28	JTAG_TCK	F28	GND	G28	GND	H28	GND
E29	GND	F29	BANK129_MGT_RX1_P	G29	BANK129_MGT_RX1_N	H29	GND
E30	BANK129_MGT_RX2_N	F30	GND	G30	GND	H30	GND
E31	GND	F31	BANK129_MGT_TX2_P	G31	BANK129_MGT_TX2_N	H31	GND
E32	BANK129_MGT_TX3_N	F32	GND	G32	GND	H32	GND
E33	GND	F33	BANK505_MGT_CLK0_P	G33	BANK505_MGT_CLK0_N	H33	GND
E34	BANK129_MGT_TX0_N	F34	GND	G34	GND	H34	GND
E35	GND	F35	BANK505_MGT_CLK3_P	G35	BANK505_MGT_CLK3_N	H35	GND
E36	BANK505_MGT_CLK2_N	F36	GND	G36	GND	H36	GND
E37	GND	F37	BANK128_MGT_RX1_P	G37	BANK128_MGT_RX1_N	H37	GND

E38	BANK128_MGT_RX2_N	F38	GND	G38	GND	H38	GND
E39	GND	F39	BANK128_MGT_TX2_P	G39	BANK128_MGT_TX2_N	H39	GND
E40	BANK128_MGT_CLK1_N	F40	GND	G40	GND	H40	GND
E41	GND	F41	BANK128_MGT_TX0_P	G41	BANK128_MGT_TX0_N	H41	GND
E42	BANK128_MGT_TX1_N	F42	GND	G42	GND	H42	GND
E43	GND	F43	BANK505_MGT_TX2_P	G43	BANK505_MGT_TX2_N	H43	GND
E44	BANK505_MGT_TX1_N	F44	GND	G44	GND	H44	GND
E45	GND	F45	BANK505_MGT_RX2_P	G45	BANK505_MGT_RX2_N	H45	GND
E46	BANK505_MGT_RX3_N	F46	GND	G46	GND	H46	GND
E47	GND	F47	BANK129_MGT_CLK1_N	G47	BANK129_MGT_CLK1_P	H47	GND
E48	BANK505_MGT_RX0_N	F48	GND	G48	GND	H48	GND
E49	GND	F49	GND	G49	GND	H49	GND
E50	GND	F50	GND	G50	GND	H50	GND

Table 7: Definition of J2 connector signal

Part 3: Base Board

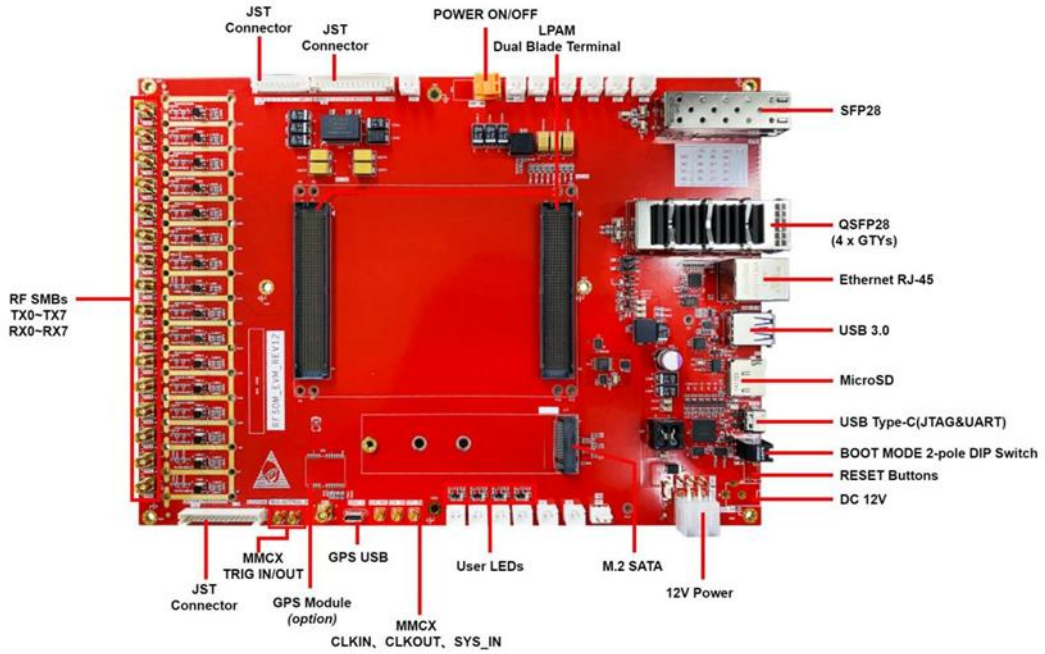

Figure 17: AXRF47 base board

Part 3.1: Introduction

Through the previous function introduction, we can understand the functions of the carrier board.

- 1× M.2 interface
- 1× USB3.0 interface
- 1× Gigabit Ethernet interface
- Type-C interface for 1× JTAG & UART
- 1× Micro SD deck
- 1× SFP optical port
- 1× QSFP28 optical port
- 2 sets of PL extended IOx8, 1 set of PS extended IO
- 4× LEDs

Part 3.2: M.2 Interface

The AXRF47 development board is equipped with a PCIE x2 standard M.2 interface for connecting M.2 SSDs. The M.2 interface uses the M key slot, which only supports PCI-E and does not support SATA. Users need to select the PCIE-type SSD when selecting the SSD.

The PCIE signal is directly connected to the BANK505 PS MGT transceiver of the ZU47DR, and the two TX signals and RX signals are connected to the LANE0 and LANE1 of the MGT in the form of differential signals. The clock of PCIE is provided by a 100MHz differential clock, and the M.2 circuit design diagram is shown below:

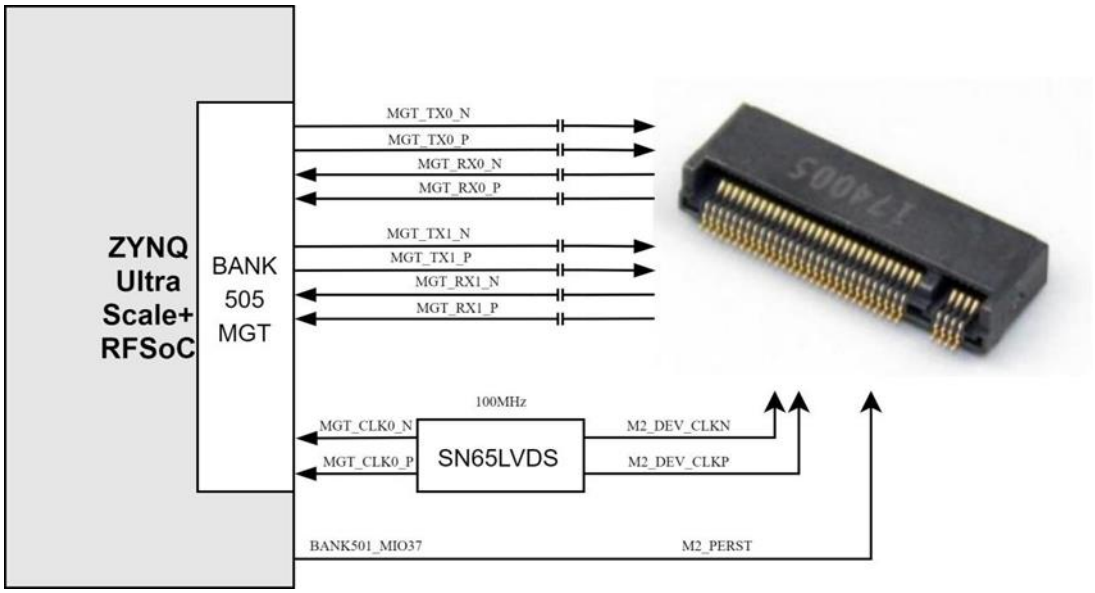

Figure 17: M.2 Interface Design Diagram

Signal name	ZYNQ pin number	M.2 CONNECTOR J17	
		Pin number	Name
MGT_TX0_N	AA32	47	PETn0
MGT_TX0_P	AA31	49	PETp0
MGT_TX1_N	W32	35	PETn1
MGT_TX1_P	W31	37	PETp1
MGT_RX0_N	AB34	41	PERn0
MGT_RX0_P	AB33	43	PERp0
MGT_RX1_N	Y34	29	PERn1
MGT_RX1_P	Y33	31	PERp1
MGT_CLK0_N	Y30		
MGT_CLK0_P	Y29		

Table 8: ZYNQ pin assignment of M.2 interface

Part 3.3: USB3.0 Interface

One USB3.0 interface on the AXRF47 carrier board supports HOST and SLAVE operation modes, and the data transmission rate is up to 5.0 Gb/s. USB3.0 is directly connected with the external Type-A interface, and USB2.0 relates to the external USB3320C chip through the ULPI interface to realize high-speed USB3.0 and USB2.0 data communication. The schematic diagram of USB3.0 connection is as follows:

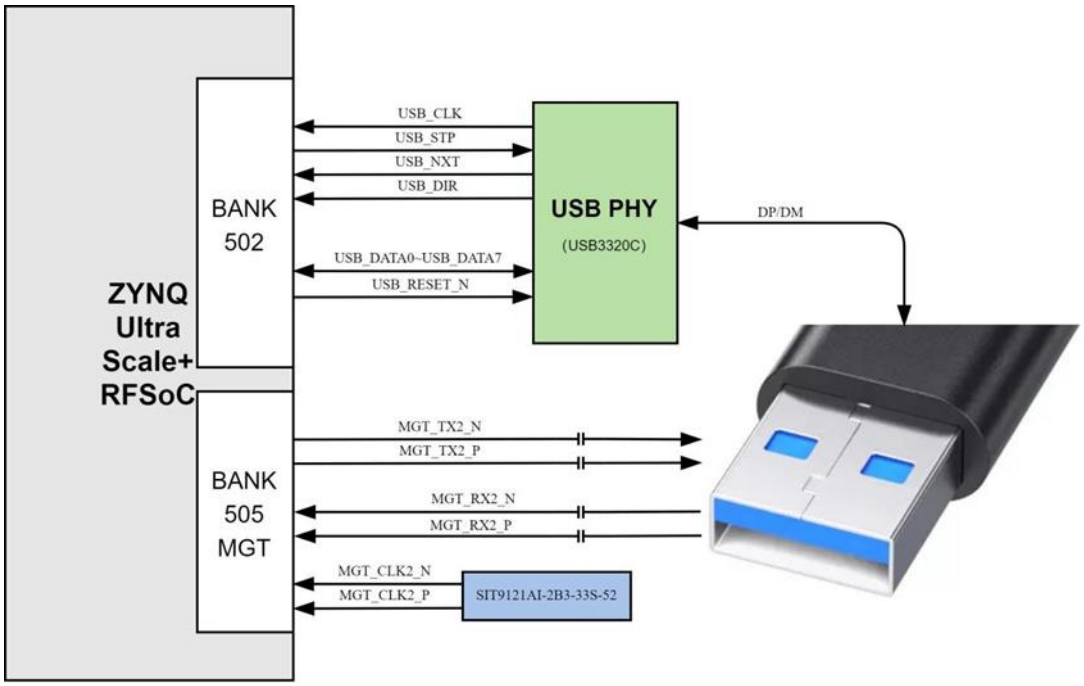

Figure 18: Schematic diagram of USB3.0 interface

Signal name	Pin name	ZYNQ pin number	Remark
USB_TX_N	BANK505_MGT_TX2_N	U32	USB3.0 data transmission negative
USB_TX_P	BANK505_MGT_TX2_P	U31	USB3.0 Data Sending Positive
USB_RX_N	BANK505_MGT_RX2_N	V34	USB3.0 data transfer negative
USB_RX_P	BANK505_MGT_RX2_P	V33	USB3.0 Data Transfer Positive
USB_DATA0	BANK502_PS_MIO56	G23	USB2.0 Data Bit0
USB_DATA1	BANK502_PS_MIO57	F23	USB2.0 Data Bit1
USB_DATA2	BANK502_PS_MIO54	H23	USB2.0 Data Bit2
USB_DATA3	BANK502_PS_MIO59	D23	USB2.0 Data Bit3
USB_DATA4	BANK502_PS_MIO60	A23	USB2.0 Data Bit4
USB_DATA5	BANK502_PS_MIO61	E22	USB2.0 Data Bit5
USB_DATA6	BANK502_PS_MIO62	B23	USB2.0 Data Bit6
USB_DATA7	BANK502_PS_MIO63	C23	USB2.0 Data Bit 7
USB_STP	BANK502_PS_MIO58	B22	USB2.0 stop signal
USB_DIR	BANK502_PS_MIO53	F22	USB2.0 data direction signal
USB_CLK	BANK502_PS_MIO52	G22	USB2.0 clock signal

USB_NXT	BANK502_PS_MIO55	D22	USB2.0 next data signal
USB_RESET_N	BANK501_PS_MIO36	C18	USB2.0 reset signal

Table 9: USB Interface Pin Assignment

Part 3.4: Gigabit Ethernet Interface

The AXRF47 carrier board has a 1-way Gigabit Ethernet interface connected to the PS side. The Ethernet chip uses the fourth generation AR8035 chip of Atheros Company to provide network communication services for users. The Ethernet PHY chip at the PS end is connected to the MIO of BANK502 at the PS end of ZYNQ. AR8035 chip supports 10/100/1,000 Mbps network transmission rate and communicates with MAC layer of ZYNQ system through RGMII interface. The schematic diagram of Gigabit Ethernet PHY chip connection is shown in the figure below:

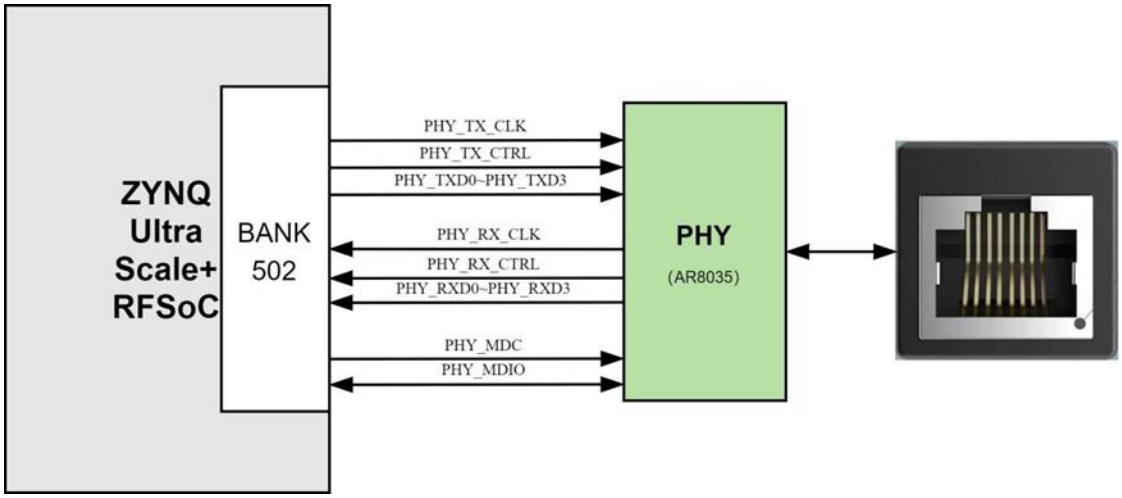

Figure 19: Ethernet Connection Diagram

Signal name	Pin name	Pin number	AR8035 PHY U12	
			Pin number	Pin name
PHY_TX_CLK	BANK502_PS_MIO64	D24	33	GTX_CLK
PHY_TXD0	BANK502_PS_MIO65	C24	34	TXD0
PHY_TXD1	BANK502_PS_MIO66	F24	35	TXD1
PHY_TXD2	BANK502_PS_MIO67	F25	36	TXD2
PHY_TXD3	BANK502_PS_MIO68	E25	37	TXD3
PHY_TX_CTRL	BANK502_PS_MIO69	E24	32	TX_EN
PHY_RX_CLK	BANK502_PS_MIO70	B25	31	RX_CLK
PHY_RXD0	BANK502_PS_MIO71	A24	29	RXD0
PHY_RXD1	BANK502_PS_MIO72	C25	28	RXD1

PHY_RXD2	BANK502_PS_MIO73	A25	26	RXD2
PHY_RXD3	BANK502_PS_MIO74	C26	25	RXD3
PHY_RX_CTRL	BANK502_PS_MIO75	B26	30	RX_DV
PHY_MDC	BANK502_PS_MIO76	E26	40	MDC
PHY_MDIO	BANK502_PS_MIO77	D26	39	MDIO
PS_POR_B	BANK501_PS_MIO44	C20	1	RSTn

Table 10: AR8035 PHY connected to XCZU47DR RFSoC

Part 3.5: Micro SD Deck

The AXRF47 carrier board includes a Micro SD card interface to provide user access to SD card memory for storing BOOT programs, the Linux operating system kernel, file systems, and other user data files. The SD card IO signal is connected to the MIO signal of PS BANK501, and the connection between PS and SD card connectors is shown in Figure 20.

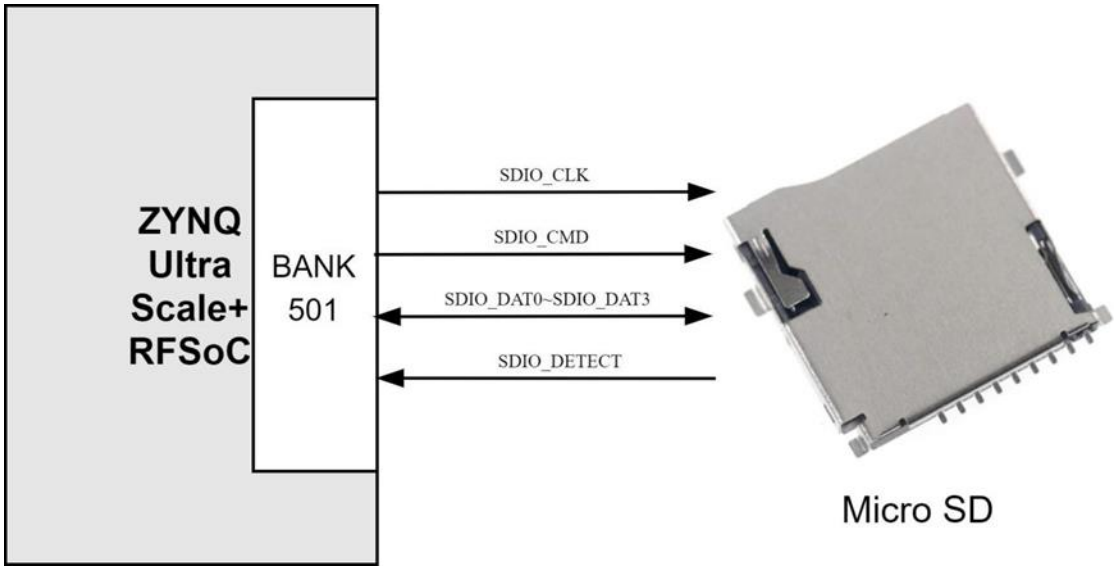

Figure 20: Schematic diagram of SD card connection

Signal name	Pin name	Pin number	Remark
SDIO_CLK	BANK501_PS_MIO51	B21	SD clock signal
SDIO_CMD	BANK501_PS_MIO50	A22	SD command signal
SDIO_DAT0	BANK501_PS_MIO46	A20	SD Data Bit 0
SDIO_DAT1	BANK501_PS_MIO47	D21	SD Data Bit 1
SDIO_DAT2	BANK501_PS_MIO48	C21	SD data Bit2
SDIO_DAT3	BANK501_PS_MIO49	E21	SD Data Bit 3

SDIO_DETECT	BANK501_PS_MIO45	B20	SD card detection signal

Table 11. SD Card Pin Assignment

Part 3.6: Fiber Optical Interface

There are two optical interfaces, one SFP interface and one QSFP28 interface on the AXRF47 carrier board. The two optical fiber interfaces are respectively connected with the GTY transceivers on BANK128 and BAN129 of ZYNQ. The two reference clocks of BANK128 are 156.25 MHz provided by the LMK04828 chip of the ACRF47 module and the differential crystal oscillator on the carrier board respectively.

The QSFP28 interface connection diagram is shown in the figure below:

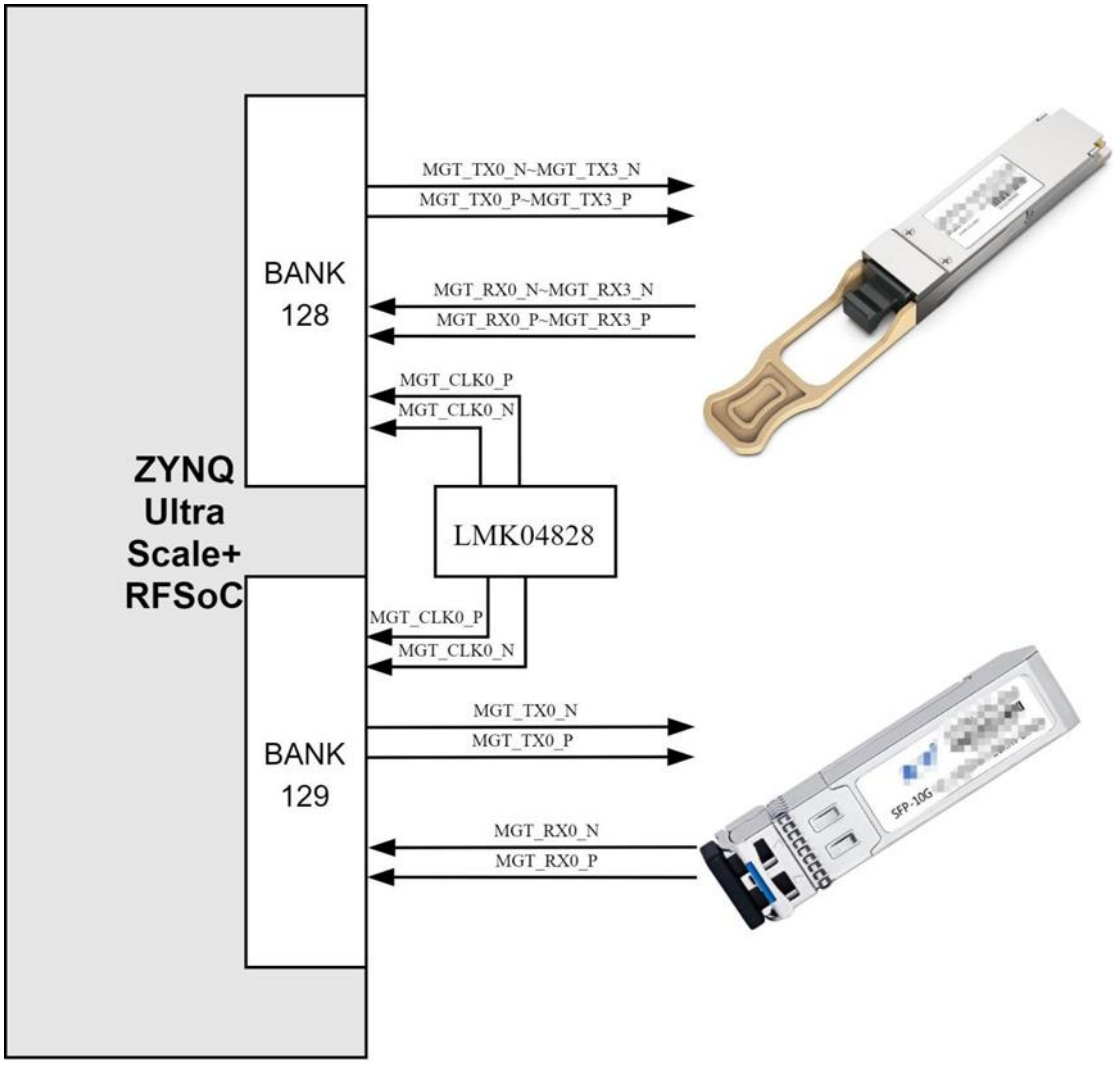

Figure 21: Schematic diagram of fiber design

Signal name	ZYNQ pin name	ZYNQ pin number	Remark
QSFP_RX0_N	MGTYRXN0_128	P34	
QSFP_RX0_P	MGTYRXP0_128	P33	

QSFP_RX1_N	MGTYRXN1_128	M34	
QSFP_RX1_P	MGTYRXP1_128	M33	
QSFP_RX2_N	MGTYRXN2_128	K34	
QSFP_RX2_P	MGTYRXP2_128	K33	
QSFP_RX3_N	MGTYRXN3_128	H34	
QSFP_RX3_P	MGTYRXP3_128	H33	
QSFP_TX0_N	MGTYTXN0_128	N31	
QSFP_TX0_P	MGTYTXP0_128	N30	
QSFP_TX1_N	MGTYTXN1_128	L31	
QSFP_TX1_P	MGTYTXP1_128	L30	
QSFP_TX2_N	MGTYTXN2_128	J31	
QSFP_TX2_P	MGTYTXP2_128	J30	
QSFP_TX3_N	MGTYTXN3_128	G31	
QSFP_TX3_P	MGTYTXP3_128	G30	

Table 12: QSFP interface pin assignment

ZYNQ pin name	ZYNQ pin number	Remark
MGTREFCLK0N_128	M29	SDCLKOUT3 output for LMK04828 Default configuration 156.25 MHz
MGTREFCLK0P_128	M28	SDCLKOUT3 output for LMK04828 Default configuration 156.25 MHz
MGTREFCLK1N_128	K29	Carrier board 156.25 MHz differential output
MGTREFCLK1P_128	K28	Carrier board 156.25 MHz differential output
MGTREFCLK0N_129	H29	SDCLKOUT1 output for LMK04828 Default configuration 156.25 MHz
MGTREFCLK0P_129	H28	SDCLKOUT1 output for LMK04828 Default configuration 156.25 MHz

Table 13: BANK128 Reference Clock Distribution

Signal name	ZYNQ pin name	ZYNQ pin number	Remark

SFP_RX0_N	MGTYRXN0_129	F34	
SFP_RX0_P	MGTYRXP0_129	F33	
SFP_TX0_N	MGTYTXN0_129	E31	
SFP_TX0_P	MGTYTXP0_129	E30	

Table 14: SFP Interface Pin Assignment

Low speed control IO processing:

QSFP low speed IO signal name	Remark	SFP low speed IO signal name	Remark
SCL	Pull up 3.3 V	TX_FULT	Pull up 3.3 V
SDA	Pull up 3.3 V	TX_DISABLE	Grounding
ModSelL	Pull up 3.3 V	RATE_SELECT0	Pull up 3.3 V
ResetL	Pull up 3.3 V	RATE_SELECT1	Pull up 3.3 V
ModPrsl	Pull up 3.3 V	LOS	Pull up 3.3 V
intL	Pull up 3.3 V		
LPMode	Grounding		

Table 15: Optical fiber low-speed IO signal processing mode

Part 3.7: JTAG & UART Interface

A JTAG & UART interface is reserved on the AXRF47 carrier board, which is used to download and debug FPGA programs or solidify programs to FLASH. Here we use FTDI's fifth USB device chip FT2232H chip, which is a USB2.0 high-speed to UART/FIFO chip with two multi-protocol synchronous serial engines allowing the use of JTAG. Capable of being configured over a variety of industry standard serial or parallel interfaces.

The schematic diagram of JTAG & UART connection is shown in the figure below:

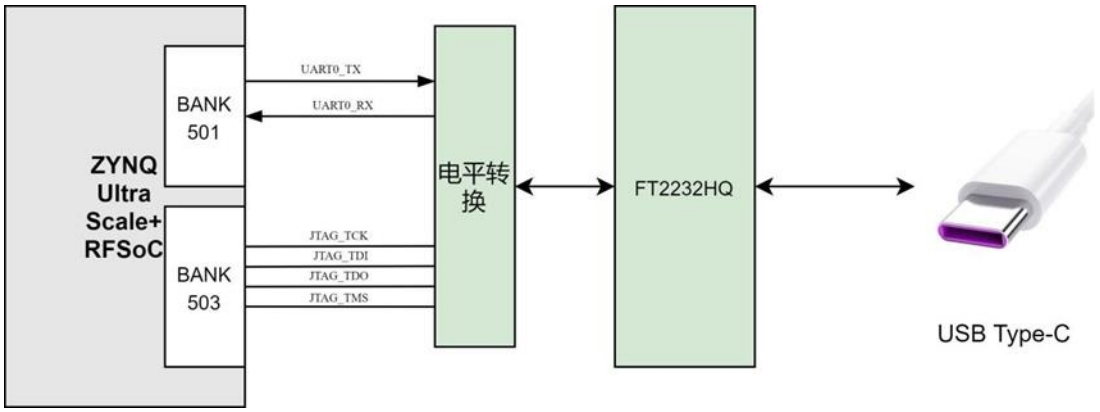

Figure 22: JTAG & UART Connector Connection Diagram

Signal name	Pin name	Pin number	Remark
UART0_TX	BANK501_PS_MIO43	A19	PS Uart data output
UART0_RX	BANK501_PS_MIO42	E20	PS Uart data input

Table 16: UART Interface Pin Assignment

Part 3.8: GPS Module (optional)

The AXRF47 carrier board can be optionally equipped with the GPS module NEO-M8N, a high-performance GNSS receiver module with superior positioning accuracy and sensitivity. The module uses the latest u-blox M8 chip, supports GPS, GLONASS, BeiDou, Galileo and other satellite systems, and can provide global positioning data. The schematic diagram of GPS connection is shown in the figure below:

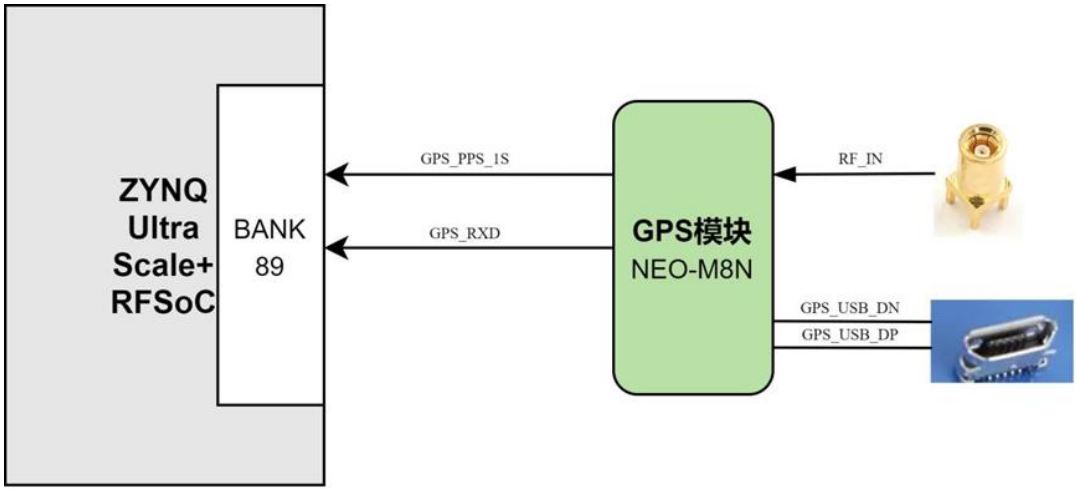

Figure 23: Schematic diagram of GPS module connection

Signal name	Pin name	Pin number	Remark
GPS_PPS_1S	IO_L10P_AD2P_89	K11	TIMEPLUSE
GPS_TXD	IO_L9P_AD3P_89	H10	TXD_MISO

Table 17: GPS Module Pin Assignment

Part 3.9: Extended IO and LEDs

The AXRF47 carrier board is extended with two sets of PL-side IO (x8) and one set of PS-side IO (x10).

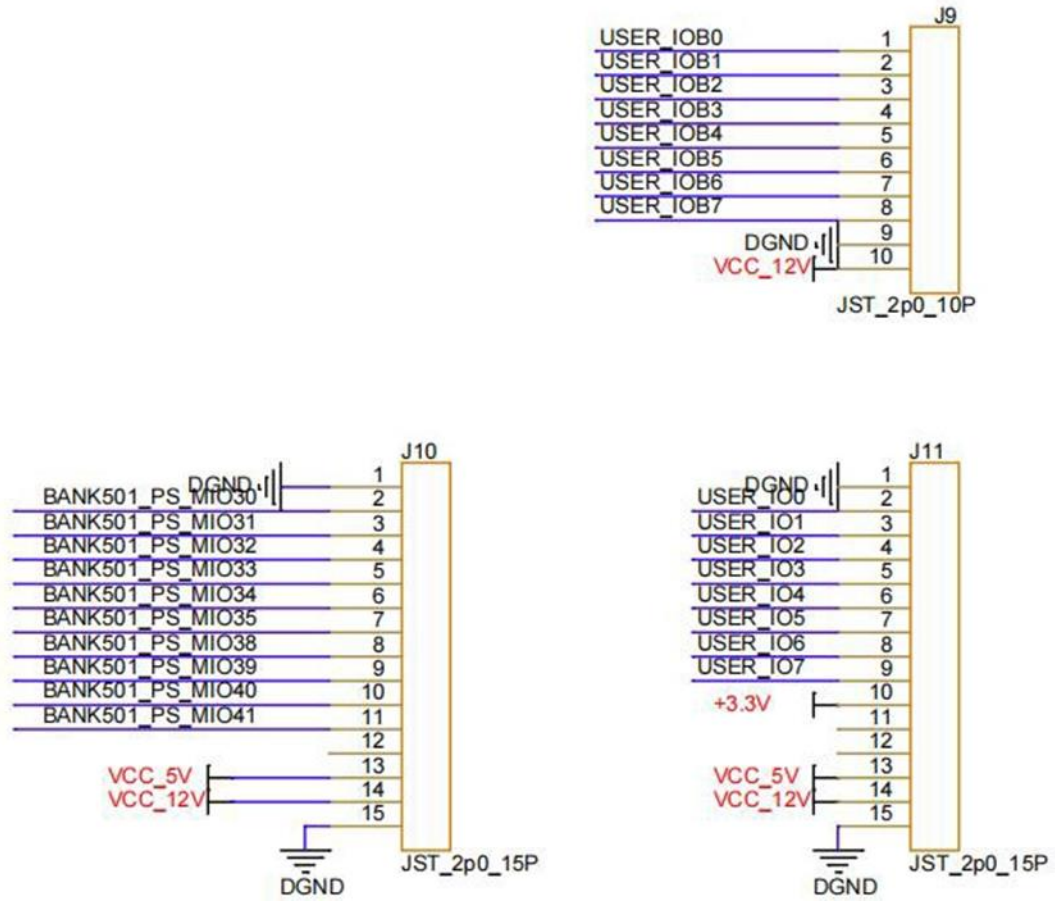

Figure 24: Extended IO Circuit Connection Diagram

Signal name	Pin name	Pin number	Remark
USER_IO0	IO_L6N_HDGC_AD6N_89	E9	
USER_IO1	IO_L5P_HDGC_AD7P_89	E11	
USER_IO2	IO_L5N_HDGC_AD7N_89	D11	
USER_IO3	IO_L4P_AD8P_89	D9	
USER_IO4	IO_L4N_AD8N_89	C9	
USER_IO5	IO_L3P_AD9P_89	A10	
USER_IO6	IO_L3N_AD9N_89	A9	
USER_IO7	IO_L2P_AD10P_89	C10	

Table 18: J11 Extended IO Pin Assignment

Signal name	Pin name	Pin number	Remark
USER_IOB0	IO_L10N_AD2N_89	K10	

USER_IOB1	IO_L11P_AD1P_89	J11	
USER_IOB2	IO_L11N_AD1N_89	H11	
USER_IOB3	IO_L8P_HDGC_AD4P_89	G11	
USER_IOB4	IO_L8N_HDGC_AD4N_89	G10	
USER_IOB5	IO_L7P_HDGC_AD5P_89	F10	
USER_IOB6	IO_L7N_HDGC_AD5N_89	F9	
USER_IOB7	IO_L6P_HDGC_AD6P_89	E10	

Table 19: J9 Extended IO Pin Assignment

Signal name	Pin name	Pin number	Remark
BANK501_PS_MIO30	PS_MIO30	H20	
BANK501_PS_MIO31	PS_MIO31	G20	
BANK501_PS_MIO32	PS_MIO32	F19	
BANK501_PS_MIO33	PS_MIO33	G21	
BANK501_PS_MIO34	PS_MIO34	D18	
BANK501_PS_MIO35	PS_MIO35	F20	
BANK501_PS_MIO38	PS_MIO38	B18	
BANK501_PS_MIO39	PS_MIO39	D19	
BANK501_PS_MIO40	PS_MIO40	A18	
BANK501_PS_MIO41	PS_MIO41	C19	

Table 20: J10 Extended IO Pin Assignment

Four user-defined LEDs can be extended on the AXRF47 card, and four extended IOs are introduced 2 PIN TJC3 straight on the header.

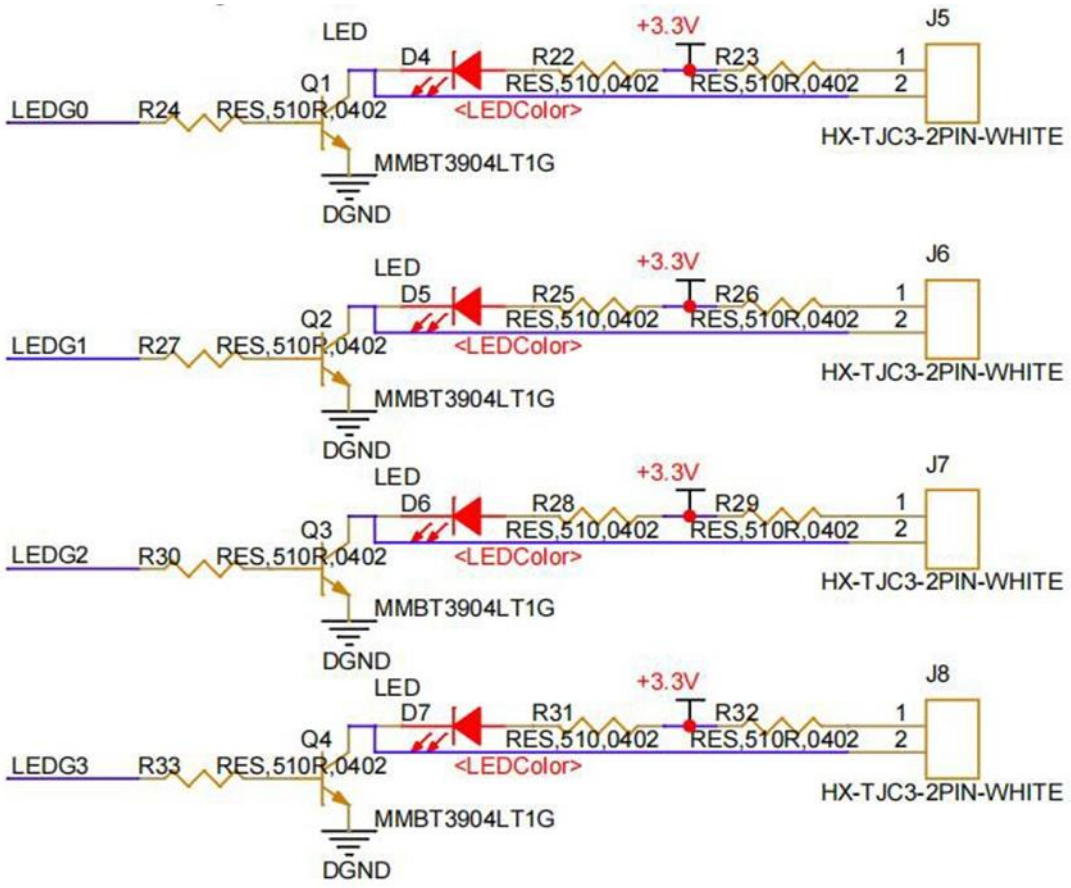

Figure 25: Schematic diagram of LED lamp expansion IO circuit

Signal name	Pin name	Pin number	Remark
LEDG0	IO_L9N_AD3N_89	H9	
LEDG1	IO_L1N_AD11N_89	B11	
LEDG2	IO_L2N_AD10N_89	B10	
LEDG3	IO_L1P_AD11P_89	C11	

Table 21: LED lamp expansion IO pin assignment

Part 3.10: Dip Switch Configuration

The AXRF47 development board has a 2-position dial switch SWC1 and two jumper caps to configure the boot mode of the ZYNQ system. The RFEVM development platform supports three boot modes, namely JTAG debug mode, QSPI FLASH and SD card boot mode. The ACRF47 chip will detect the level of (PS _ MODE0 ~ 3) after power-on to determine the startup mode. The user can select a different start mode through the dial switch SWC1.

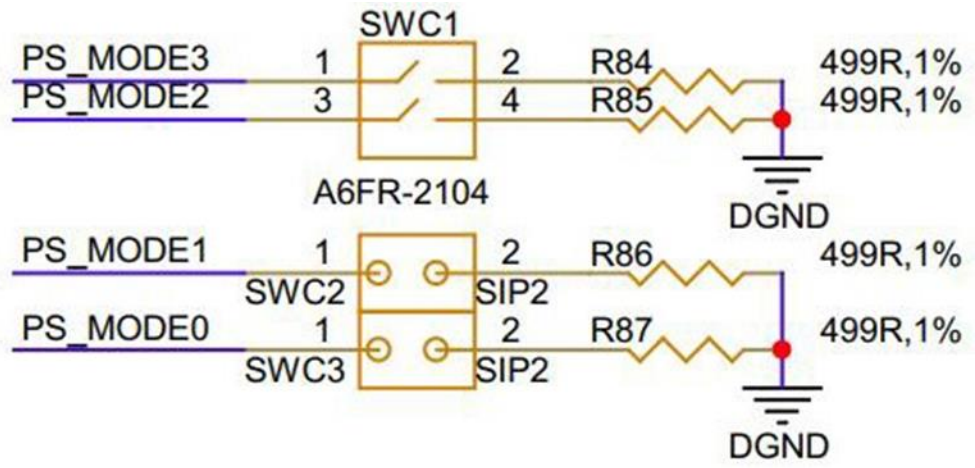

Figure 26: PS _ MODE Circuit Schematic

The default configuration is that SWC3 is short-circuited through the jumper cap, i.e. PS _ MODE0 = 0, and SWC2 is pulled up by default, i.e. PS_MODE1=1.

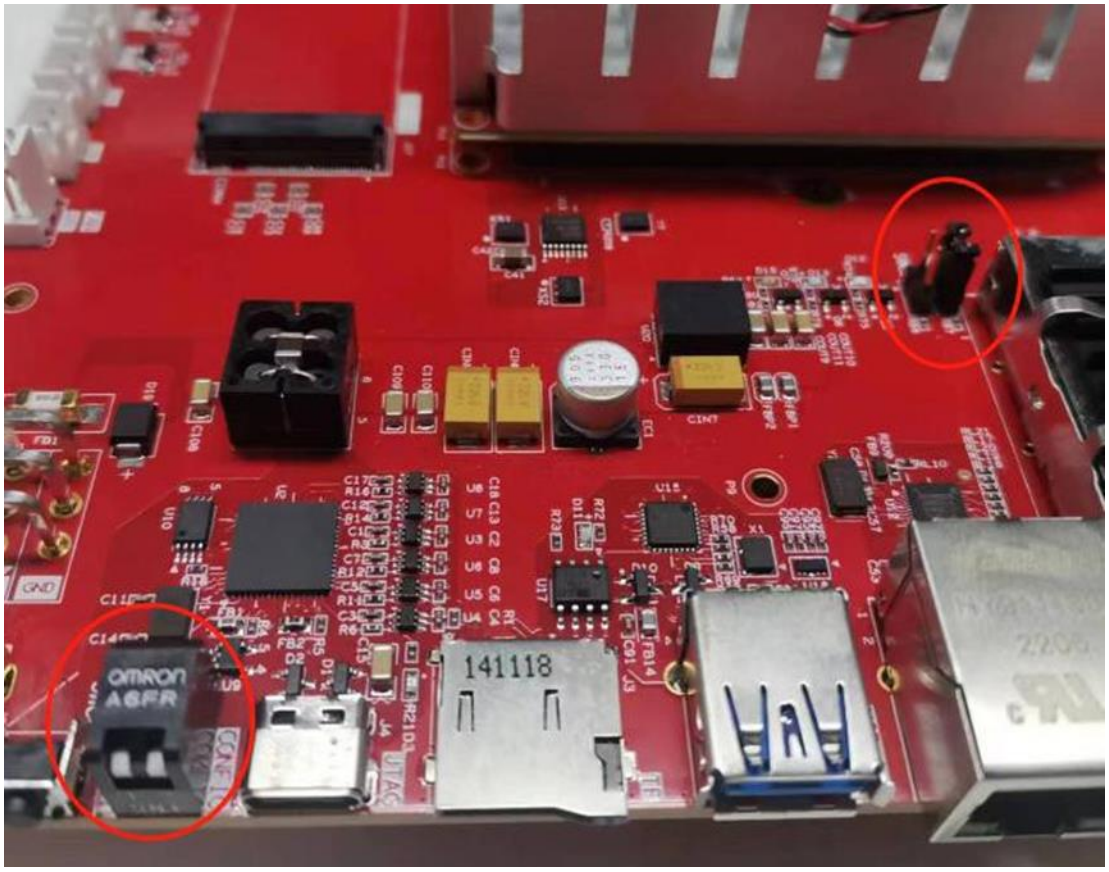

Figure 27 jumper cap diagram

The SWC1startup mode configuration is shown in the following table.

Dial SWC1 position (1,2)	MODE[3:0]	Start mode
ON，ON	*0000*	*JTAG*

ON，ON	0010	QSPI
ON，OFF	*0110*	*EMMC*
OFF，OFF	1110	SD

Table 22: SWC1 Startup Mode Configuration

Note: In the SD card boot mode, the JTAG function can still be used normally.

Part 3.11: Power Source

The power input voltage of the AXRF47 development board is DC12V, which is generated by multiple power chips on the carrier board +5V, +1.8V, +3.3V power supply.

The power supply design block diagram is shown in the following figure:

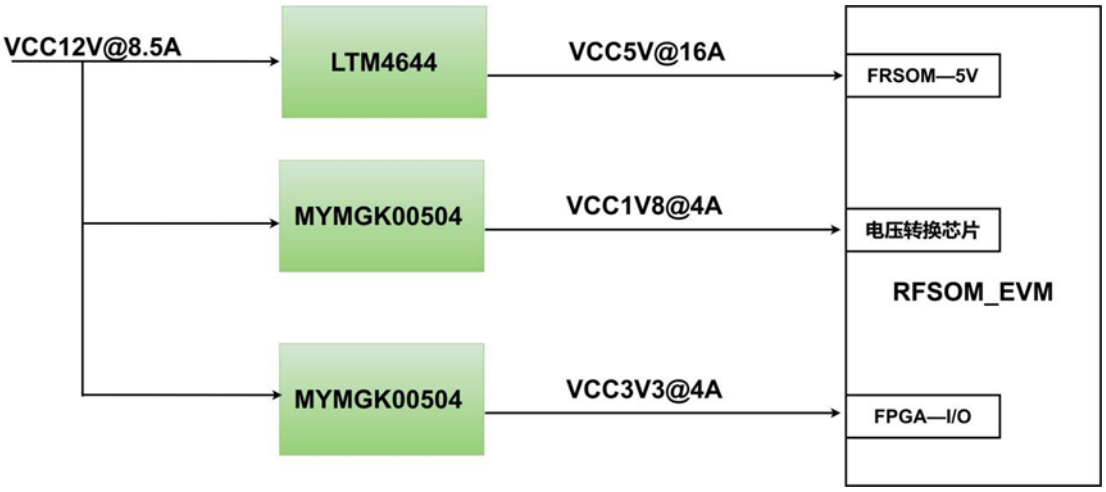

Figure 28: AXRF47 Carrier Board Power Interface Section

Part 3.12: Structural Dimension Diagram

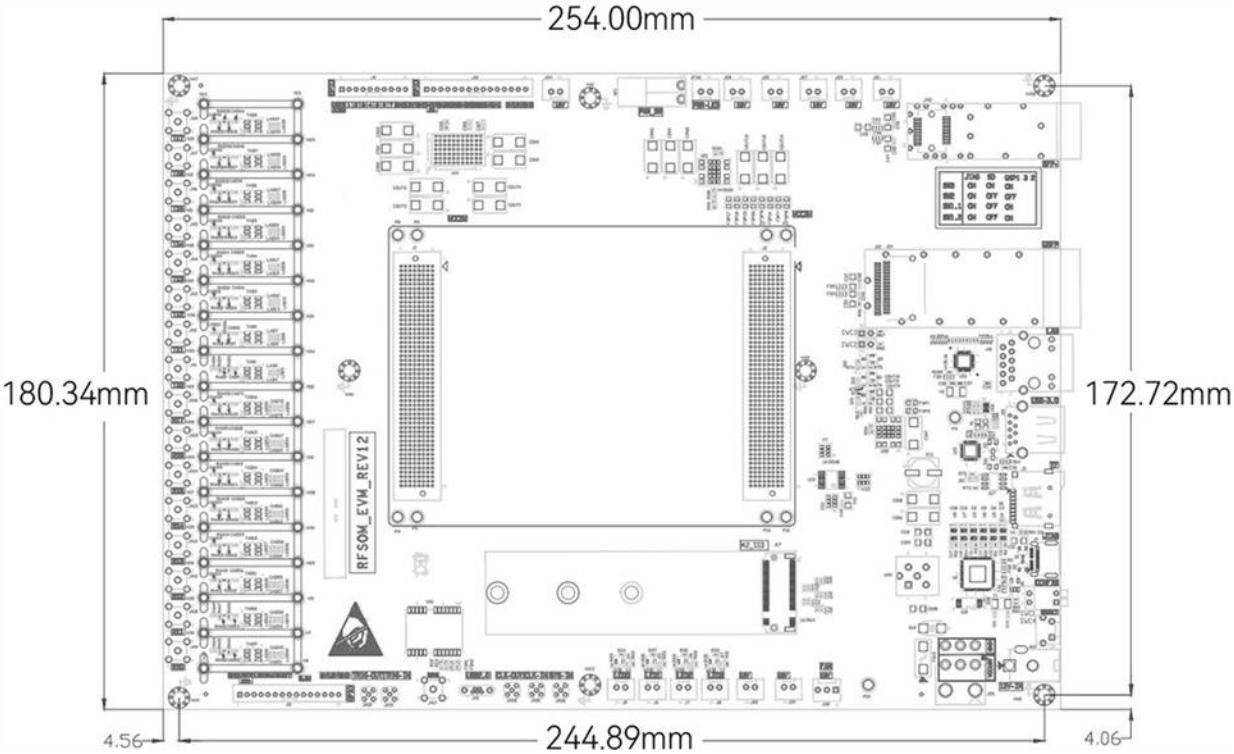

Figure 29: Front view of AXRF47