

**ZYNQ UltraScale+ MPSoC
FPGA Development Board
AXU2CGB-E
User Manual**



Version Record

| Version | Date | Release By | Description |
|---------|------------|------------|-------------|
| Rev 1.0 | 2022-09-08 | | |

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This MPSoCs FPGA development platform adopts the core board + carrier board mode, which is convenient for users to use the core board for secondary development. The core board uses XILINX Zynq UltraScale+ CEG chip ZU2CG solution, uses Processing System(PS)+Programmable Logic(PL) technology to integrate dual-core ARM ARM Cortex-A53 and FPGA programmable logic on a single chip. In addition, the PS side of the core board has 4 pieces of 1GB high-speed DDR4 SDRAM chips, 1 piece of 8GB eMMC memory chip and 1 piece of 256Mb QSPI FLASH chip.

In the design of carrier board, we have extended a wealth of interfaces for users, such as 1 SATA M.2 interface, 1 DP interface, 4 USB 3.0 Interface, 2 Gigabit Ethernet interfaces, 1 SD card slot, 2-Channel 40-pin expansion header, 2-Channel CAN bus interfaces, 2-Channel RS485 bus interfaces, 1 MIPI Camera Interface. It meets users' requirements for high-speed data exchange, data storage, Video transmission processing, deep learning, artificial intelligence and industrial control. It is a "professional" ZYNQ development platform. For high-speed data transmission and exchange, pre-verification and post-application of data processing is possible. This product is very suitable for students, engineers and other groups engaged in MPSoCs development.



Part 1: FPGA Development Board Introduction

The entire structure of the AXU2CGB-E FPGA development board is inherited from our consistent core board + carrier board model. A high-speed inter-board connector is used between the core board and the carrier board.

The core board is mainly composed of the smallest system of XCZU2CG + 4 DDR4 + eMMC + QSPI FLASH, ACU2CG uses Xilinx's Zynq UltraScale+ MPSoCs CG chip, the model number is XCZU2CG-1SFVC784E. XCZU2CG chip can be divided into processor system part Processor System (PS) and programmable logic part Programmable Logic (PL). On the PS side of the ZU2CG chip, there are 4 DDR4, each with a capacity of up to 512MB. The 8GB eMMC FLASH memory chip and a 256Mb QSPI FLASH which are on the PS side, used to statically store the operating system, file system and user data of MPSoCs.

The AXU2CGB-E carrier board expands its rich peripheral interface, including 1 SATA M.2 interface, 1 DP interface, 4 USB 3.0 Interface, 2 Gigabit Ethernet interfaces, 1 SD card slot, 2-Channel 40-pin expansion header, 2-Channel CAN bus interfaces, 2-Channel RS485 bus interfaces, 1 MIPI Camera Interface and some keys and LEDs.

The following figure shows the structure of the entire development system:

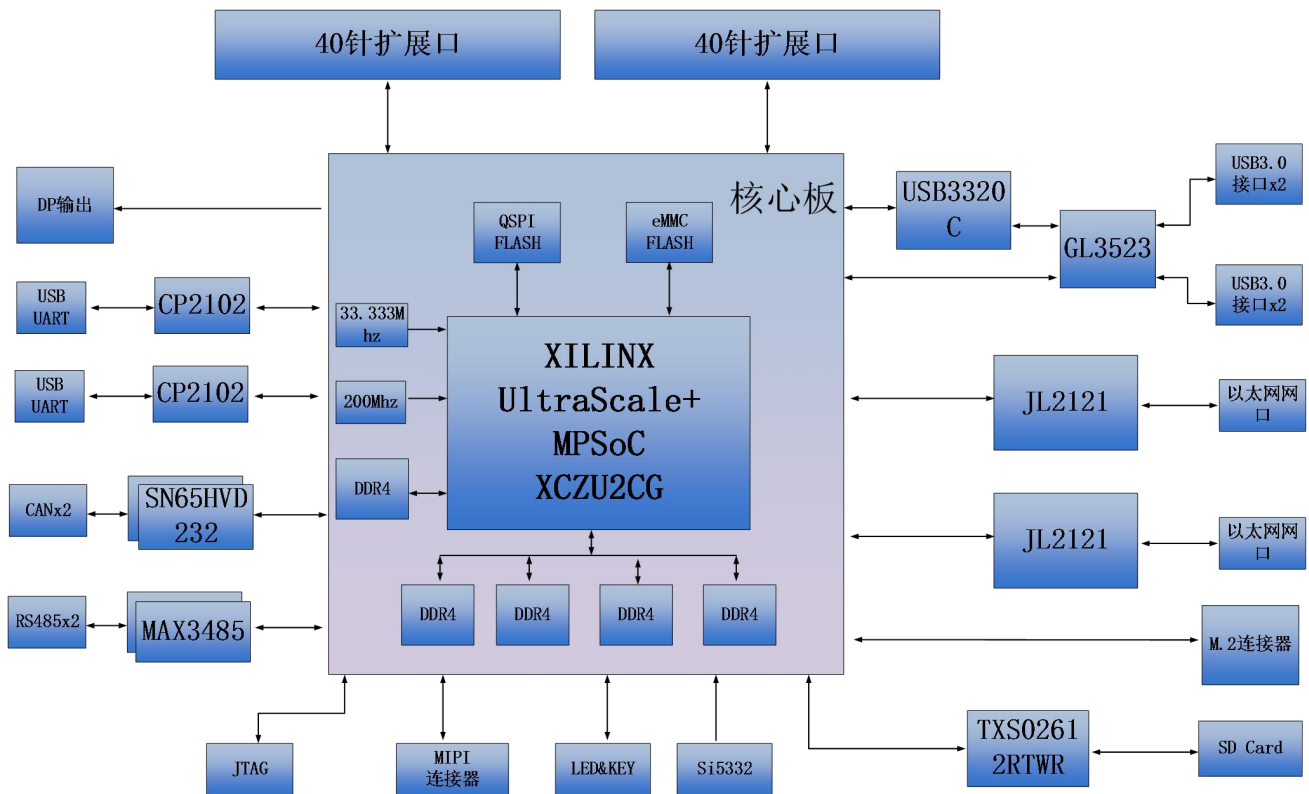


Figure 1-1-1: The Schematic Diagram of the AXU2CGB-E

Through this diagram, you can see the interfaces and functions that the AXU2CGB-E FPGA Development Board contains:

➤ ACU2CG core board

It consists of ACU2CG +4GB DDR4 (PS) +8GB eMMC FLASH + 256Mb QSPI FLASH, and there are 2 crystal oscillators to provide the clock, a single-ended 33.3333MHz crystal oscillator for the PS system, and a differential 200MHz crystal oscillator for the PL logic DDR reference clock.

➤ M.2 Interface1 PCIe1 standard M.2 interface, used to connect M.2 SSD solid state drives, with a communication speed of up to 6Gbps.

➤ DP Output Interface

1 standard Display Port output display interface, used for video image display. Supports up to 4K@30Hz or 1080P@60Hz output

➤ USB 3.0 Interface

4-channel USB3.0 HOST interface, USB interface type is TYPE A. Used to connect external USB peripherals, such as connecting a mouse, keyboard, U disk, etc.

➤ Gigabit Ethernet Interface

2-Channel 10/100M/1000M Ethernet RJ45 interface for Ethernet data exchange with computers or other network devices. The network interface chip uses JLSemi JL2121-N040I industrial grade GPHY chip.

➤ USB Uart Interface

Two Uart to USB ports, one for PS and one for PL. It is used to communicate with the computer, which is convenient for users to debug. The serial port chip adopts Silicon Labs CP2102GM's USB-UAR chip, and the USB interface adopts MINI USB interface.

➤ SD Card Slot Interface

1 Micro SD card holder, used to store operating system image and file system.

➤ 40-pin expansion port

2 40-pin 0.1-inch pitch expansion port can be connected to various ALINX modules (binocular camera, TFT LCD screen, high-speed AD module, etc.). The expansion port contains 1-channel 5V power supply, 2-channel 3.3V power supply, 3-channel way ground, 34 IOs port.

➤ CAN Communication Interface

Two-way CAN bus interface, using TI's SN65HVD232 chip, the interface uses 4Pin green terminal blocks.

➤ 485 Communication Interface

Two-way 485 communication interface, using MAX3485 chip of MAXIM company. The interface uses 6Pin green terminal blocks.

➤ MIPI Interface

MIPI camera input interfaces, used to connect MIPI camera module (AN5641).

- JTAG debug port
A 10-pin 0.1 spacing standard JTAG ports for FPGA program download and debugging. Users can debug and download the ZU2CG system through the XILINX downloader.
- Temperature and humidity sensor chip LM75
On-board temperature and humidity sensor chip LM75, used to detect the temperature and humidity of the surrounding environment around the FPGA development board
- EEPROM
One EEPROM 24LC04 with IIC interface
- Real Time Clock (RTC)
1 built-in RTC real-time clock
- LED Lights
5 LEDs, include 2 LEDs on the core board, 3 LED on the carrier board. There are 1 power indicator and 1 DONE Configuration indicator on the core board, 1 power indicator on the carrier board. There are 1 power indicator and 2 user indicators on the carrier board.
- KEYS
3 KEYS, include 1 Rest KEY and 2 User KEYS.

Part 2: ACU2CG core board

Part 2.1: ACU2CG core board Introduction

ACU2CG (core board model, the same below) FPGA core board, ZYNQ chip is based on XCZU2CG-1SFVC784E of XILINX company Zynq UltraScale+ MPSoCs CG series.

This core board uses 4 Micron DDR4 chips MT40A512M16GE on the PS side, to form a 64-bit data bus bandwidth and 2GB capacity. The highest operating speed of DDR4 SDRAM on the PS side can reach 1200MHz (data rate 2400Mbps). In addition, a 256MBit QSPI FLASH and an 8GB eMMC FLASH chip are also integrated on the core board to start storage configuration and system files.

In order to connect with the carrier board, the four board-to-board connectors of this core board expand the PS side USB2.0 interface, Gigabit Ethernet interface, SD card interface and other remaining MIO ports; also expand 4 pairs of PS MGT high-speed transceiver interface; and almost all IO ports on the PL side (HP I/O: 96, HD I/O: 84). The wiring between the XCZU2CG chip and the interface has been processed with equal length and differential, and the core board size is only 3.15*2.36 (inch), which is very suitable for secondary development.

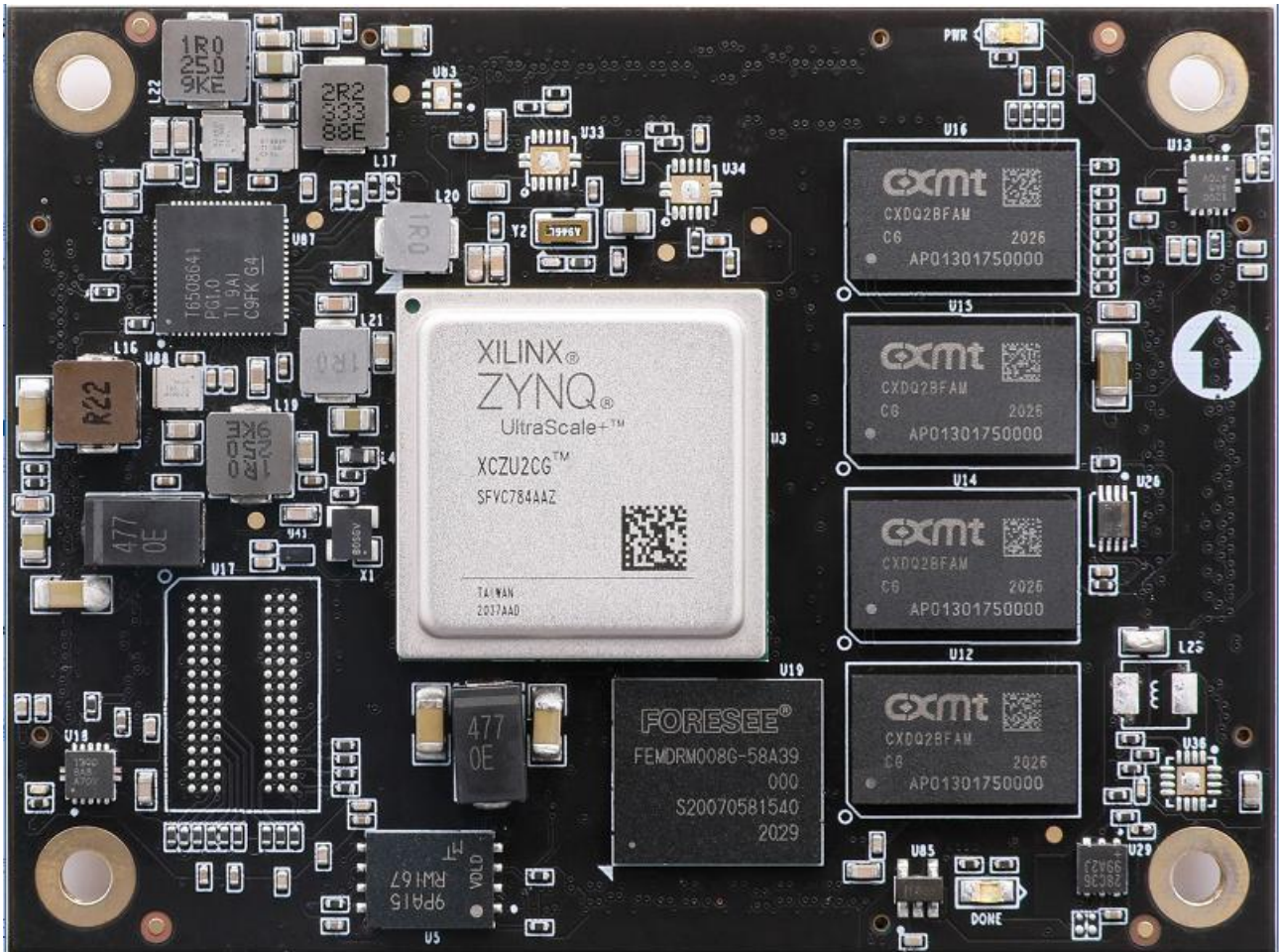


Figure 2-1-1: ACU2CG Core Board (Front View)

Part 2.2: ZYNQ Chip

The FPGA core board ACU2CG uses Xilinx's Zynq UltraScale+ MPSoCs CG series chip, module XCZU2CG-1SFVC784E. The PS system of the ZU2CG chip integrates 2 ARM Cortex™-A53 processors with a speed of up to 1.2Ghz and supports Level 2 Cache; it also contains 2 Cortex-R5 processors with a speed of up to 500Mhz

The ZU2CG chip supports 32-bit or 64-bit DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 memory chips, with rich high-speed interfaces on the PS side such as PCIE Gen2, USB3.0, SATA 3.1, DisplayPort; it also supports USB2.0 , Gigabit Ethernet, SD/SDIO, I2C, CAN, UART, GPIO and other interfaces. The PL end contains a wealth of programmable logic units, DSP and internal RAM.

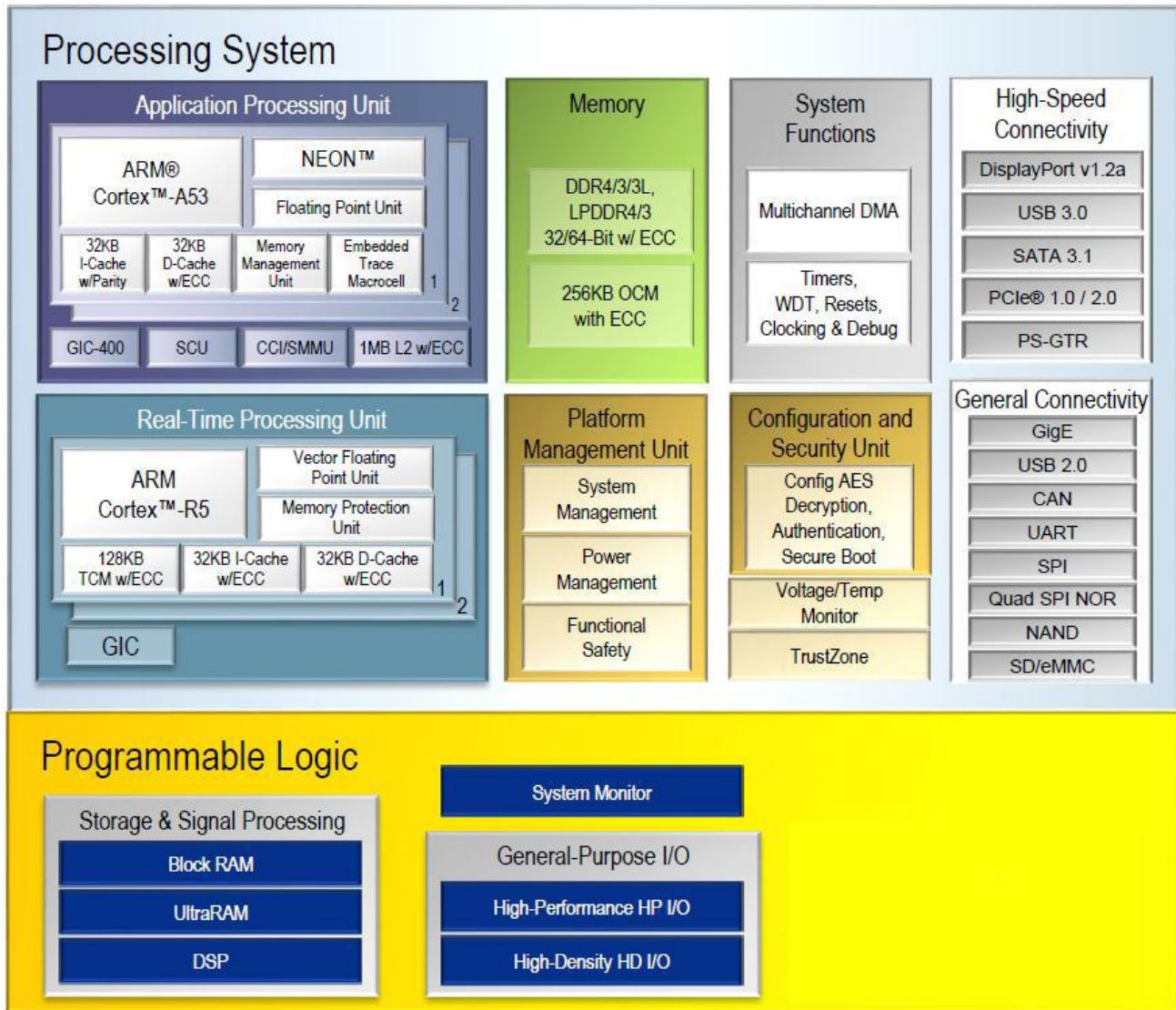


Figure 2-2-1: Overall Block Diagram of the ZYNQ ZU2CG Chip

The main parameters of the PS system part are as follows:

- ARM quad-core Cortex™-A53 processor, speed up to 1.2GHz, each CPU 32KB level 1 instruction and data cache, 1MB level 2 cache, shared by 2 CPUs
- ARM dual-core Cortex-R5 processor, speed up to 500MHz, each CPU 32KB level 1 instruction and data cache, and 128K tightly coupled memory.
- External storage interface, support 32/64bit DDR4/3/3L, LPDDR4/3 interface

- Static storage interface, support NAND, 2xQuad-SPI FLASH.
- High-speed connection interface, support PCIe Gen2 x 4, 2 x USB3.0, Sata 3.1, Display Port, 4 x Tri-mode Gigabit Ethernet
- Common connection interfaces: 2 x USB2.0, 2 x SD/SDIO, 2 x UART, 2 x CAN 2.0B, 2 x I2C, 2 x SPI, 4 x 32b GPIO
- Power management: Supports the division of four parts of power supply Full/Low/PL/Battery.
- Encryption algorithm: support RSA, AES and SHA.
- System monitoring: 10-bit 1Mbps AD sampling for temperature and voltage detection.

The main parameters of the PL logic part are as follows:

- Logic Cells: 103K
- Flip-flops: 94K
- Look-up-tables (LUTs): 47K
- Block RAM: 5.3MB
- Clock Management Units (CMTs): 3
- 18x25MACCs: 240

XCZU2CG-1SFVC784E chip speed grade is -1, industrial grade, package is SFVC784

Part 2.3: DDR4 DRAM

The ACU2CG core board is equipped with 4 Micron (Micron) 512MB DDR4 chips, model is PANGO CXDQ2BFAM-CG (Compatible with MT40A256M16GE-083E), to form a 64-bit data bus bandwidth and 2GB capacity. The maximum operating speed of the DDR4 SDRAM on the PS side can reach 1200MHz (data rate 2400Mbps), and the 4 DDR4 storage systems

are directly connected to the memory interface of the PS BANK504. The highest operating speed of the DDR4 SDRAM on the PL side can reach 1066MHz (data rate 2133Mbps), and four DDR4 storage systems are directly connected to the memory interface of PS's BANK504. The specific configuration of DDR4 SDRAM is shown in Table 2-3-1 below:

| Bit Number | Chip Model | Capacity | Factory |
|-----------------|--------------|--------------|---------|
| U12,U14,U15,U16 | CXDQ2BFAM-CG | 256M x 16bit | PANGO |

Table 2-3-1: DDR4 SDRAM Configuration

The hardware design of DDR4 requires strict consideration of signal integrity. We have fully considered the matching resistor/terminal resistance, trace impedance control, and trace length control in circuit design and PCB design to ensure high-speed and stable operation of DDR4.

The hardware connection of DDR4 SDRAM on the PS Side is shown in Figure 2-3-1:

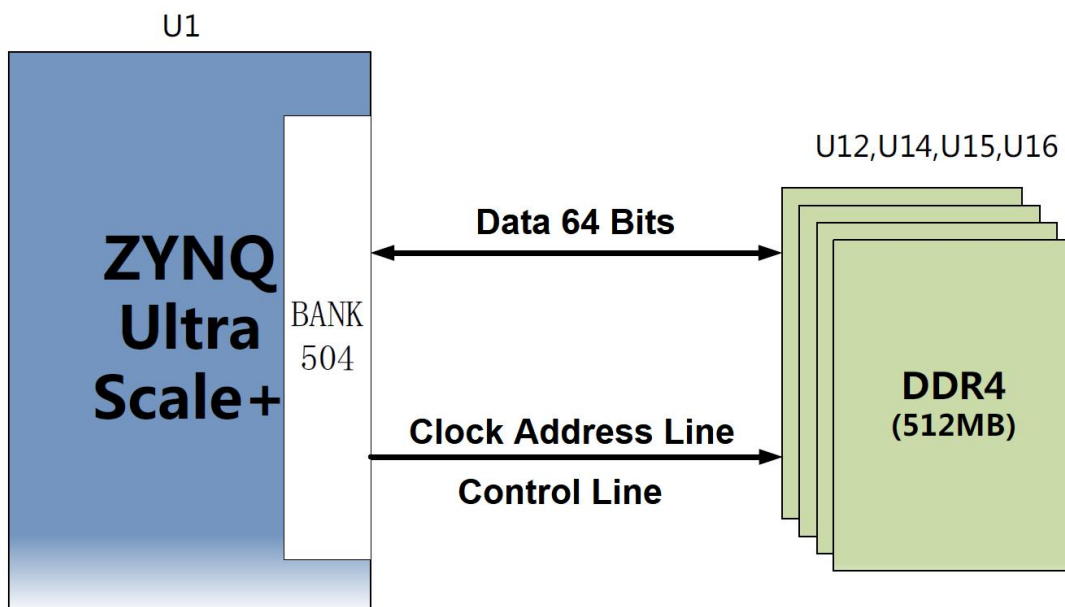


Figure 2-3-1: DDR4 DRAM schematic diagram on the PS Side

PS Side DDR4 DRAM pin assignment:

| Signal Name | Pin Name | Pin Number |
|----------------|-------------------|------------|
| PS_DDR4_DQS0_P | PS_DDR_DQS_P0_504 | AF21 |
| PS_DDR4_DQS0_N | PS_DDR_DQS_N0_504 | AG21 |
| PS_DDR4_DQS1_P | PS_DDR_DQS_P1_504 | AF23 |
| PS_DDR4_DQS1_N | PS_DDR_DQS_N1_504 | AG23 |
| PS_DDR4_DQS2_P | PS_DDR_DQS_P2_504 | AF25 |
| PS_DDR4_DQS2_N | PS_DDR_DQS_N2_504 | AF26 |
| PS_DDR4_DQS3_P | PS_DDR_DQS_P3_504 | AE27 |
| PS_DDR4_DQS3_N | PS_DDR_DQS_N3_504 | AF27 |
| PS_DDR4_DQS4_P | PS_DDR_DQS_P4_504 | N23 |
| PS_DDR4_DQS4_N | PS_DDR_DQS_N4_504 | M23 |
| PS_DDR4_DQS5_P | PS_DDR_DQS_P5_504 | L23 |
| PS_DDR4_DQS5_N | PS_DDR_DQS_N5_504 | K23 |
| PS_DDR4_DQS6_P | PS_DDR_DQS_P6_504 | N26 |
| PS_DDR4_DQS6_N | PS_DDR_DQS_N6_504 | N27 |
| PS_DDR4_DQS7_P | PS_DDR_DQS_P7_504 | J26 |
| PS_DDR4_DQS7_N | PS_DDR_DQS_N7_504 | J27 |
| PS_DDR4_DQ0 | PS_DDR_DQ0_504 | AD21 |
| PS_DDR4_DQ1 | PS_DDR_DQ1_504 | AE20 |
| PS_DDR4_DQ2 | PS_DDR_DQ2_504 | AD20 |
| PS_DDR4_DQ3 | PS_DDR_DQ3_504 | AF20 |
| PS_DDR4_DQ4 | PS_DDR_DQ4_504 | AH21 |
| PS_DDR4_DQ5 | PS_DDR_DQ5_504 | AH20 |
| PS_DDR4_DQ6 | PS_DDR_DQ6_504 | AH19 |
| PS_DDR4_DQ7 | PS_DDR_DQ7_504 | AG19 |
| PS_DDR4_DQ8 | PS_DDR_DQ8_504 | AF22 |
| PS_DDR4_DQ9 | PS_DDR_DQ9_504 | AH22 |
| PS_DDR4_DQ10 | PS_DDR_DQ10_504 | AE22 |
| PS_DDR4_DQ11 | PS_DDR_DQ11_504 | AD22 |
| PS_DDR4_DQ12 | PS_DDR_DQ12_504 | AH23 |
| PS_DDR4_DQ13 | PS_DDR_DQ13_504 | AH24 |
| PS_DDR4_DQ14 | PS_DDR_DQ14_504 | AE24 |
| PS_DDR4_DQ15 | PS_DDR_DQ15_504 | AG24 |

| | | |
|--------------|-----------------|------|
| PS_DDR4_DQ16 | PS_DDR_DQ16_504 | AC26 |
| PS_DDR4_DQ17 | PS_DDR_DQ17_504 | AD26 |
| PS_DDR4_DQ18 | PS_DDR_DQ18_504 | AD25 |
| PS_DDR4_DQ19 | PS_DDR_DQ19_504 | AD24 |
| PS_DDR4_DQ20 | PS_DDR_DQ20_504 | AG26 |
| PS_DDR4_DQ21 | PS_DDR_DQ21_504 | AH25 |
| PS_DDR4_DQ22 | PS_DDR_DQ22_504 | AH26 |
| PS_DDR4_DQ23 | PS_DDR_DQ23_504 | AG25 |
| PS_DDR4_DQ24 | PS_DDR_DQ24_504 | AH27 |
| PS_DDR4_DQ25 | PS_DDR_DQ25_504 | AH28 |
| PS_DDR4_DQ26 | PS_DDR_DQ26_504 | AF28 |
| PS_DDR4_DQ27 | PS_DDR_DQ27_504 | AG28 |
| PS_DDR4_DQ28 | PS_DDR_DQ28_504 | AC27 |
| PS_DDR4_DQ29 | PS_DDR_DQ29_504 | AD27 |
| PS_DDR4_DQ30 | PS_DDR_DQ30_504 | AD28 |
| PS_DDR4_DQ31 | PS_DDR_DQ31_504 | AC28 |
| PS_DDR4_DQ32 | PS_DDR_DQ32_504 | T22 |
| PS_DDR4_DQ33 | PS_DDR_DQ33_504 | R22 |
| PS_DDR4_DQ34 | PS_DDR_DQ34_504 | P22 |
| PS_DDR4_DQ35 | PS_DDR_DQ35_504 | N22 |
| PS_DDR4_DQ36 | PS_DDR_DQ36_504 | T23 |
| PS_DDR4_DQ37 | PS_DDR_DQ37_504 | P24 |
| PS_DDR4_DQ38 | PS_DDR_DQ38_504 | R24 |
| PS_DDR4_DQ39 | PS_DDR_DQ39_504 | N24 |
| PS_DDR4_DQ40 | PS_DDR_DQ40_504 | H24 |
| PS_DDR4_DQ41 | PS_DDR_DQ41_504 | J24 |
| PS_DDR4_DQ42 | PS_DDR_DQ42_504 | M24 |
| PS_DDR4_DQ43 | PS_DDR_DQ43_504 | K24 |
| PS_DDR4_DQ44 | PS_DDR_DQ44_504 | J22 |
| PS_DDR4_DQ45 | PS_DDR_DQ45_504 | H22 |
| PS_DDR4_DQ46 | PS_DDR_DQ46_504 | K22 |
| PS_DDR4_DQ47 | PS_DDR_DQ47_504 | L22 |
| PS_DDR4_DQ48 | PS_DDR_DQ48_504 | M25 |
| PS_DDR4_DQ49 | PS_DDR_DQ49_504 | M26 |
| PS_DDR4_DQ50 | PS_DDR_DQ50_504 | L25 |

| | | |
|--------------|-----------------|------|
| PS_DDR4_DQ51 | PS_DDR_DQ51_504 | L26 |
| PS_DDR4_DQ52 | PS_DDR_DQ52_504 | K28 |
| PS_DDR4_DQ53 | PS_DDR_DQ53_504 | L28 |
| PS_DDR4_DQ54 | PS_DDR_DQ54_504 | M28 |
| PS_DDR4_DQ55 | PS_DDR_DQ55_504 | N28 |
| PS_DDR4_DQ56 | PS_DDR_DQ56_504 | J28 |
| PS_DDR4_DQ57 | PS_DDR_DQ57_504 | K27 |
| PS_DDR4_DQ58 | PS_DDR_DQ58_504 | H28 |
| PS_DDR4_DQ59 | PS_DDR_DQ59_504 | H27 |
| PS_DDR4_DQ60 | PS_DDR_DQ60_504 | G26 |
| PS_DDR4_DQ61 | PS_DDR_DQ61_504 | G25 |
| PS_DDR4_DQ62 | PS_DDR_DQ62_504 | K25 |
| PS_DDR4_DQ63 | PS_DDR_DQ63_504 | J25 |
| PS_DDR4_DM0 | PS_DDR_DM0_504 | AG20 |
| PS_DDR4_DM1 | PS_DDR_DM1_504 | AE23 |
| PS_DDR4_DM2 | PS_DDR_DM2_504 | AE25 |
| PS_DDR4_DM3 | PS_DDR_DM3_504 | AE28 |
| PS_DDR4_DM4 | PS_DDR_DM4_504 | R23 |
| PS_DDR4_DM5 | PS_DDR_DM5_504 | H23 |
| PS_DDR4_DM6 | PS_DDR_DM6_504 | L27 |
| PS_DDR4_DM7 | PS_DDR_DM7_504 | H26 |
| PS_DDR4_A0 | PS_DDR_A0_504 | W28 |
| PS_DDR4_A1 | PS_DDR_A1_504 | Y28 |
| PS_DDR4_A2 | PS_DDR_A2_504 | AB28 |
| PS_DDR4_A3 | PS_DDR_A3_504 | AA28 |
| PS_DDR4_A4 | PS_DDR_A4_504 | Y27 |
| PS_DDR4_A5 | PS_DDR_A5_504 | AA27 |
| PS_DDR4_A6 | PS_DDR_A6_504 | Y22 |
| PS_DDR4_A7 | PS_DDR_A7_504 | AA23 |
| PS_DDR4_A8 | PS_DDR_A8_504 | AA22 |
| PS_DDR4_A9 | PS_DDR_A9_504 | AB23 |
| PS_DDR4_A10 | PS_DDR_A10_504 | AA25 |
| PS_DDR4_A11 | PS_DDR_A11_504 | AA26 |
| PS_DDR4_A12 | PS_DDR_A12_504 | AB25 |
| PS_DDR4_A13 | PS_DDR_A13_504 | AB26 |

| | | |
|-----------------|--------------------|------|
| PS_DDR4_WE_B | PS_DDR_A14_504 | AB24 |
| PS_DDR4_CAS_B | PS_DDR_A15_504 | AC24 |
| PS_DDR4_RAS_B | PS_DDR_A16_504 | AC23 |
| PS_DDR4_ACT_B | PS_DDR_ACT_N_504 | Y23 |
| PS_DDR4_ALERT_B | PS_DDR_ALERT_N_504 | U25 |
| PS_DDR4_BA0 | PS_DDR_BA0_504 | V23 |
| PS_DDR4_BA1 | PS_DDR_BA1_504 | W22 |
| PS_DDR4_BG0 | PS_DDR_BG0_504 | W24 |
| PS_DDR4_CS0_B | PS_DDR_CS_N0_504 | W27 |
| PS_DDR4_ODT0 | PS_DDR_ODT0_504 | U28 |
| PS_DDR4_PARITY | PS_DDR_PARITY_504 | V24 |
| PS_DDR4_RESET_B | PS_DDR_RST_N_504 | U23 |
| PS_DDR4_CLK0_P | PS_DDR_CK0_P_504 | W25 |
| PS_DDR4_CLK0_N | PS_DDR_CK0_N_504 | W26 |
| PS_DDR4_CKE0 | PS_DDR_CKE0_504 | V28 |

Part 2.4: QSPI Flash

The FPGA core board ACU2CG is equipped with one 256Mbit Quad-SPI FLASH chip to form an 8-bit bandwidth data bus, the flash model is MT25QU256ABA1EW9, which uses the 1.8V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, it can be used as a boot device for the system to store the boot image of the system. These images mainly include FPGA bit files, ARM application code, and other user data files. The specific models and related parameters of QSPI FLASH are shown in Table 2-4-1.

| Position | Model | Capacity | Factory |
|----------|------------------|----------|---------|
| U5 | MT25QU256ABA1EW9 | 256Mbit | Winbond |

Table 2-4-1: QSPI FLASH Specification

QSPI FLASH is connected to the GPIO port of the BANK500 in the PS section of the ZYNQ chip. In the system design, the GPIO port functions of these PS ports need to be configured as the QSPI FLASH interface. Figure

2-4-1 shows the QSPI Flash in the schematic.

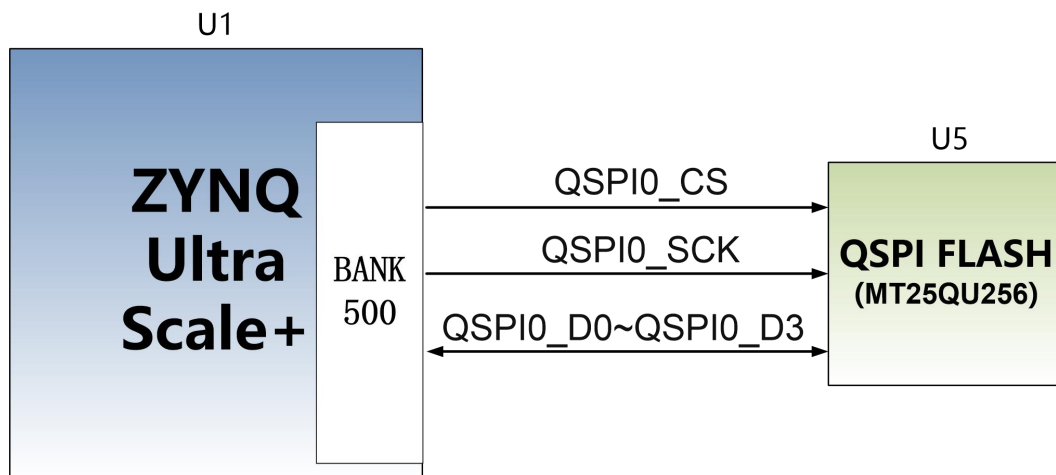


Figure 2-4-1: QSPI Flash in the schematic

Configure chip pin assignments:

| Signal Name | Pin Name | Pin Number |
|-----------------|-------------|------------|
| MIO0_QSPI0_SCLK | PS_MIO0_500 | AG15 |
| MIO1_QSPI0_IO1 | PS_MIO1_500 | AG16 |
| MIO2_QSPI0_IO2 | PS_MIO2_500 | AF15 |
| MIO3_QSPI0_IO3 | PS_MIO3_500 | AH15 |
| MIO4_QSPI0_IO0 | PS_MIO4_500 | AH16 |
| MIO5_QSPI0_SS_B | PS_MIO5_500 | AD16 |

Part 2.5: eMMC Flash

The ACU2CG core board is equipped with a large-capacity 8GB eMMC FLASH chip, the model is FEMDRM008G-58A39 (Compatible with MTFC8GAKAJCN-4M), it supports the HS-MMC interface of the JEDEC e-MMC V5.0 standard, and the level supports 1.8V or 3.3V. The data width of eMMC FLASH and ZYNQ connection is 8bit. Due to the large-capacity and non-volatile characteristics of eMMC FLASH, it can be used as a large-capacity storage device in the ZYNQ system, such as storing ARM applications, system files and other user data files. The specific models and related parameters of eMMC FLASH are shown in Table 2-5-1.

| Position | Model | Capacity | Factory |
|----------|------------------|----------|---------|
| U19 | FEMDRM008G-58A39 | 8G Byte | FORESEE |

Table 2-5-1: eMMC FLASH Specification

The eMMC FLASH is connected to the GPIO port of the BANK500 of the PS part of the ZYNQ UltraScale+. In the system design, it is necessary to configure the GPIO port function of the PS side as an EMMC interface. Figure 2-5-1 shows the part of eMMC Flash in the schematic diagram.

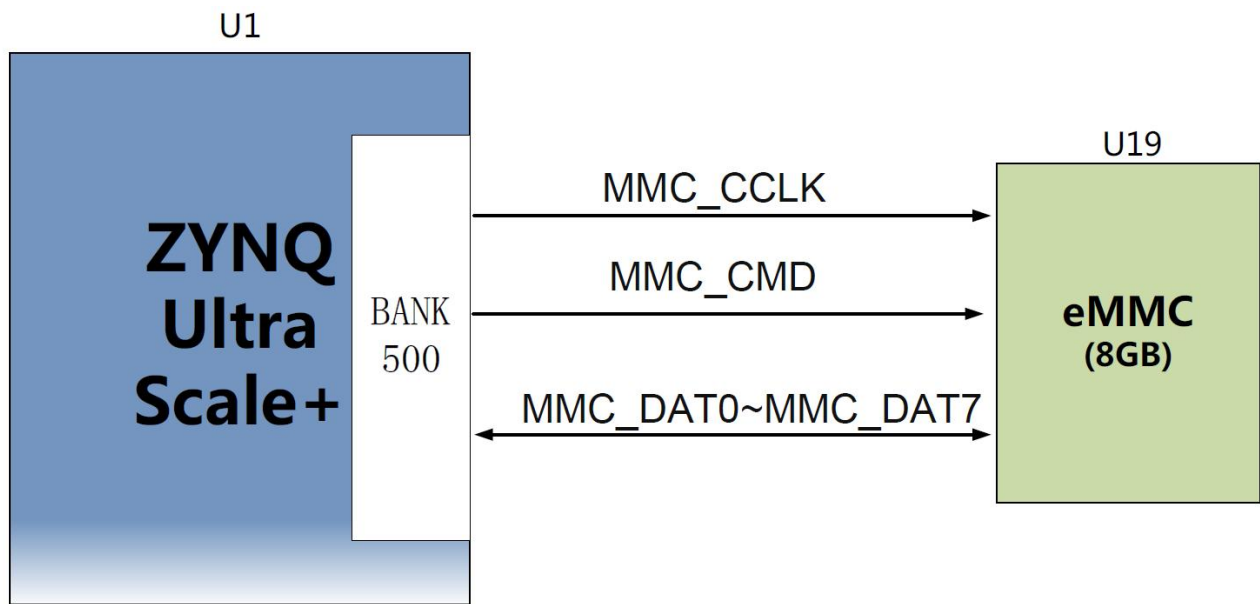


Figure 2-5-1: QSPI Flash in the schematic

Configuration Chip pin assignment:

| Signal Name | Pin Name | Pin Number |
|-------------|--------------|------------|
| MMC_DAT0 | PS_MIO13_500 | AH18 |
| MMC_DAT1 | PS_MIO14_500 | AG18 |
| MMC_DAT2 | PS_MIO15_500 | AE18 |
| MMC_DAT3 | PS_MIO16_500 | AF18 |
| MMC_DAT4 | PS_MIO17_500 | AC18 |
| MMC_DAT5 | PS_MIO18_500 | AC19 |
| MMC_DAT6 | PS_MIO19_500 | AE19 |
| MMC_DAT7 | PS_MIO20_500 | AD19 |
| MMC_CMD | PS_MIO21_500 | AC21 |

| | | |
|----------|--------------|------|
| MMC_CCLK | PS_MIO22_500 | AB20 |
| MMC_RSTN | PS_MIO23_500 | AB18 |

Part 2.6: Clock configuration

The core board provides reference clock and RTC real-time clock for PS system and PL logic respectively, so that PS system and PL logic can work independently. The schematic diagram of the clock circuit design is shown in Figure 2-6-1:

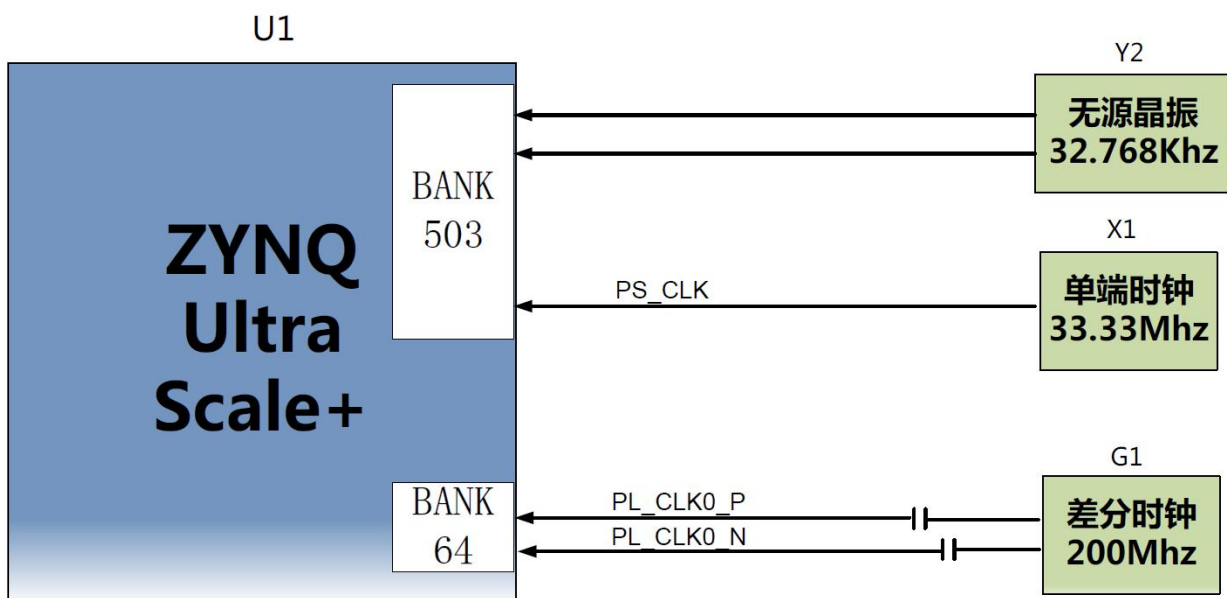


Figure 2-6-1: Core Board Clock Source

PS System RTC Real Time Clock

The passive crystal Y2 on the core board provides a 32.768KHz real-time clock source for the PS system. The crystal is connected to the PS_PADI_503 and PS_PADO_503 pins of BANK503 of the ZYNQ chip. The schematic diagram is shown in Figure 2-6-2:

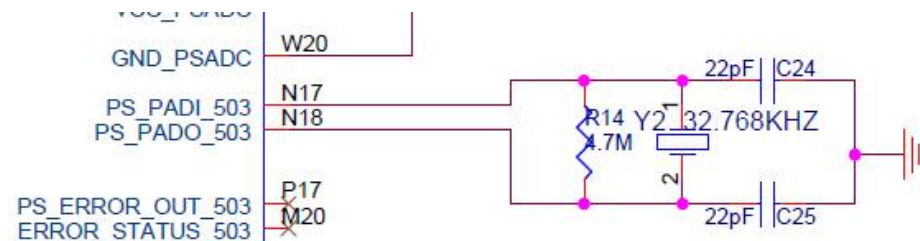


Figure 2-6-2: Passive Crystal Oscillator for RTC

Clock pin assignment:

| Signal Name | Pin |
|-------------|-----|
| PS_PADI_503 | N17 |
| PS_PADO_503 | N18 |

PS System Clock Source

The X1 crystal on the core board provides a 33.333MHz clock input for the PS part. The clock input is connected to the PS_REF_CLK_503 pin of BANK503 of the ZYNQ chip. The schematic diagram is shown in Figure 2-6-3:

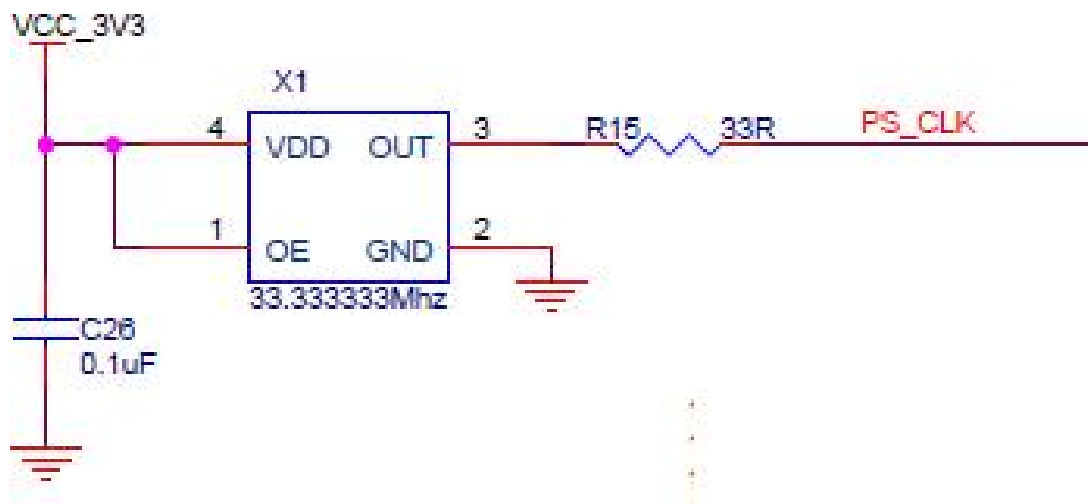


Figure 2-6-3: Active Crystal in PS part

Clock pin assignment:

| Signal Name | Pin |
|-------------|-----|
| PS_CLK | R16 |

PL System Clock Source

The core board provides a differential 200MHz PL system clock source for the reference clock of the DDR4 controller. The crystal oscillator output is connected to the global clock (MRCC) of PL BANK64. This global clock can be used to drive the DDR4 controller and user logic circuits in the FPGA. The schematic diagram of this clock source is shown in Figure 2-6-4

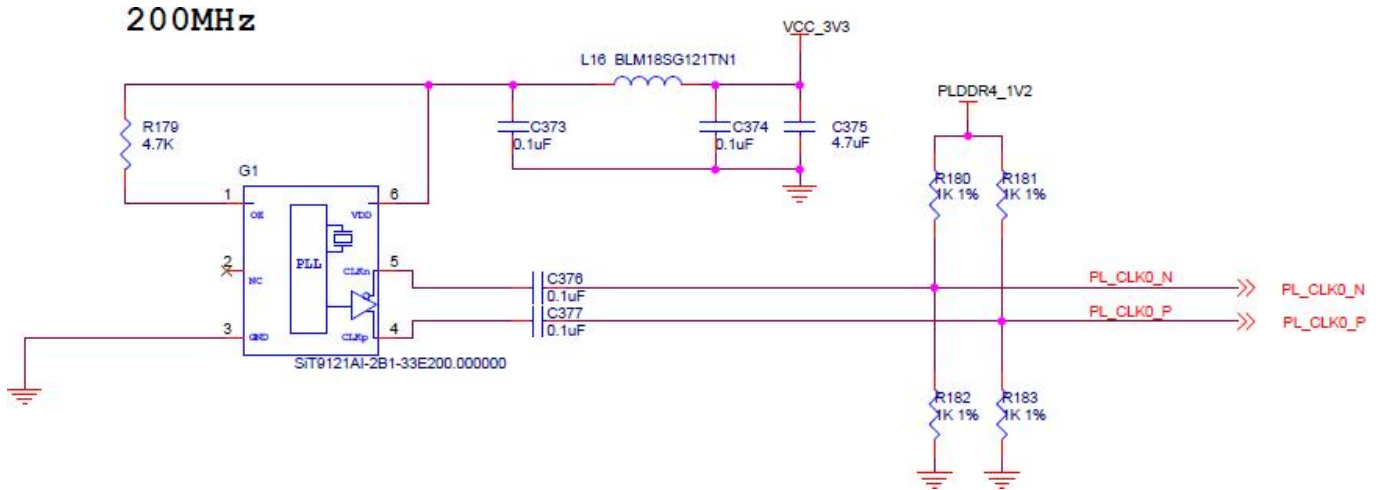


Figure 2-6-4: PL system clock source

Clock pin assignment:

| Signal Name | Pin |
|-------------|-----|
| PL_CLK0_P | AE5 |
| PL_CLK0_N | AF5 |

Part 2.7: LED

There is a red power indicator (PWR) and a configuration LED (DONE) on the ACU2CG core board. When the core board is powered on, the power indicator will light up; after the FPGA configuration program, the configuration LED light will light up. The LED Schematic in the Core Board is shown in Figure 2-7-1:

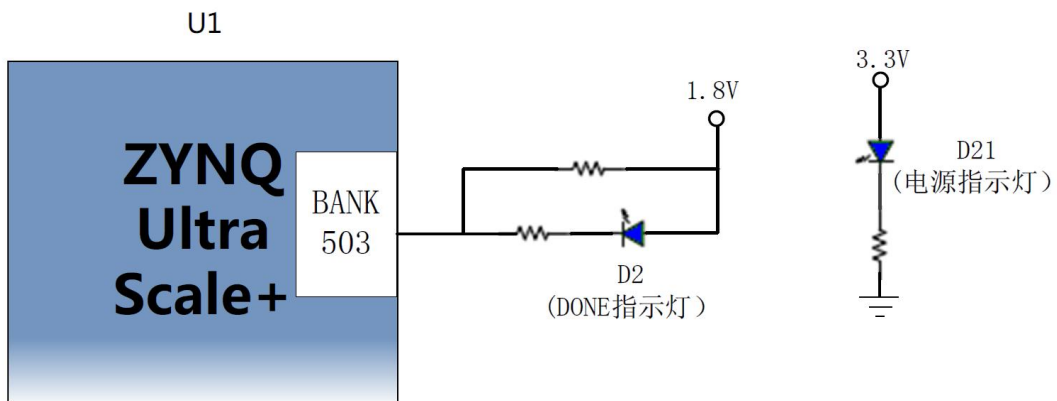
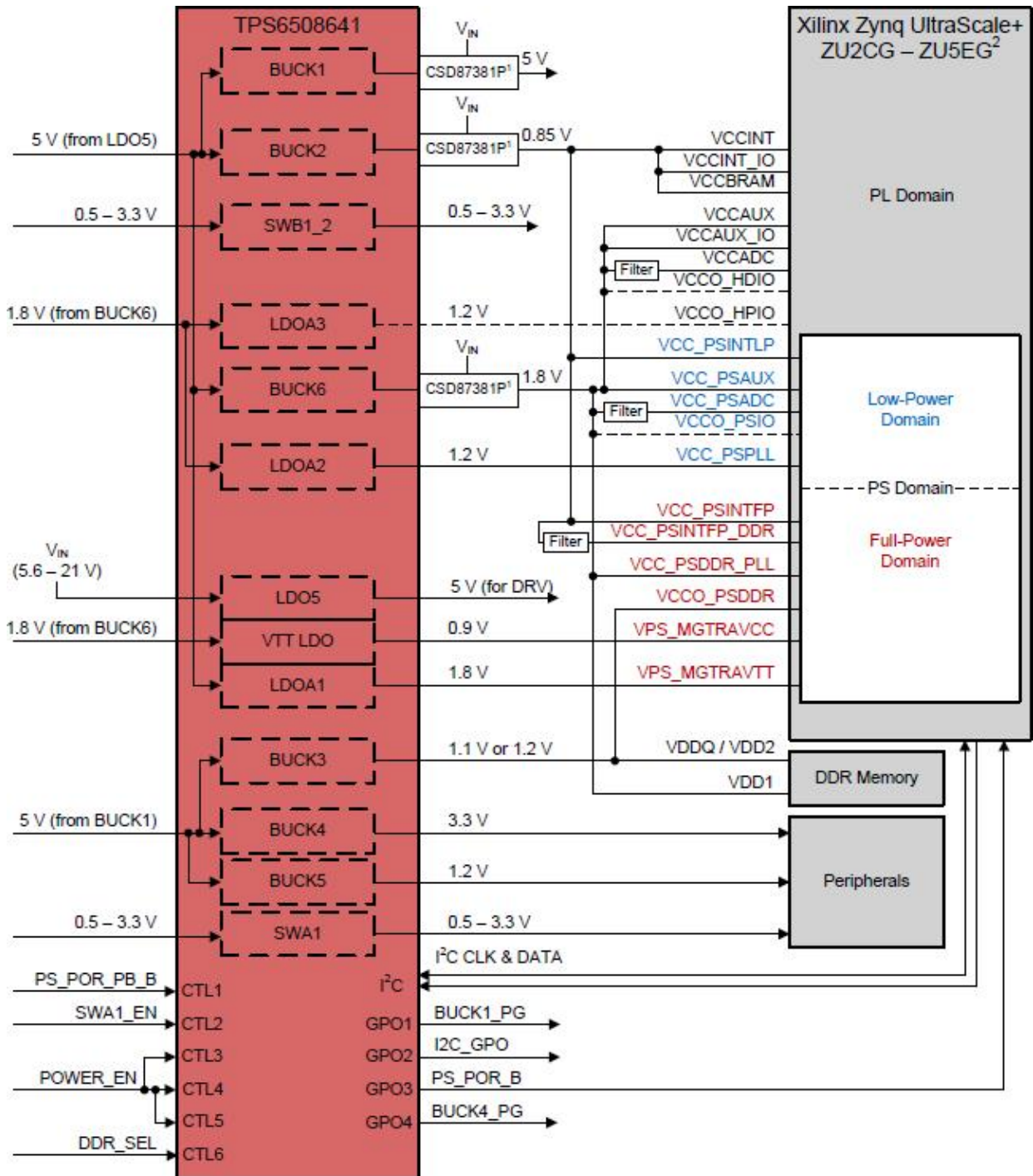


Figure 2-7-1: LED Schematic in the Core Board

Part 2.8: Power Supply

The power supply voltage of the ACU2CG core board is DC12V, which is supplied by connecting the carrier board. The core board uses a PMIC chip TPS6508641 to generate all the power required by the XCZU2CG chip. For the TPS6508641 power supply design, please refer to the power supply chip manual. The design block diagram is as follows:



In addition, the VCCIO power supply of BANK65 and BANK66 of XCZU2CG chip is provided by the carrier board, which is convenient for users to modify, but the maximum power supply cannot exceed 1.8V.

Part 2.9: ACU2CG Core Board Form Factor

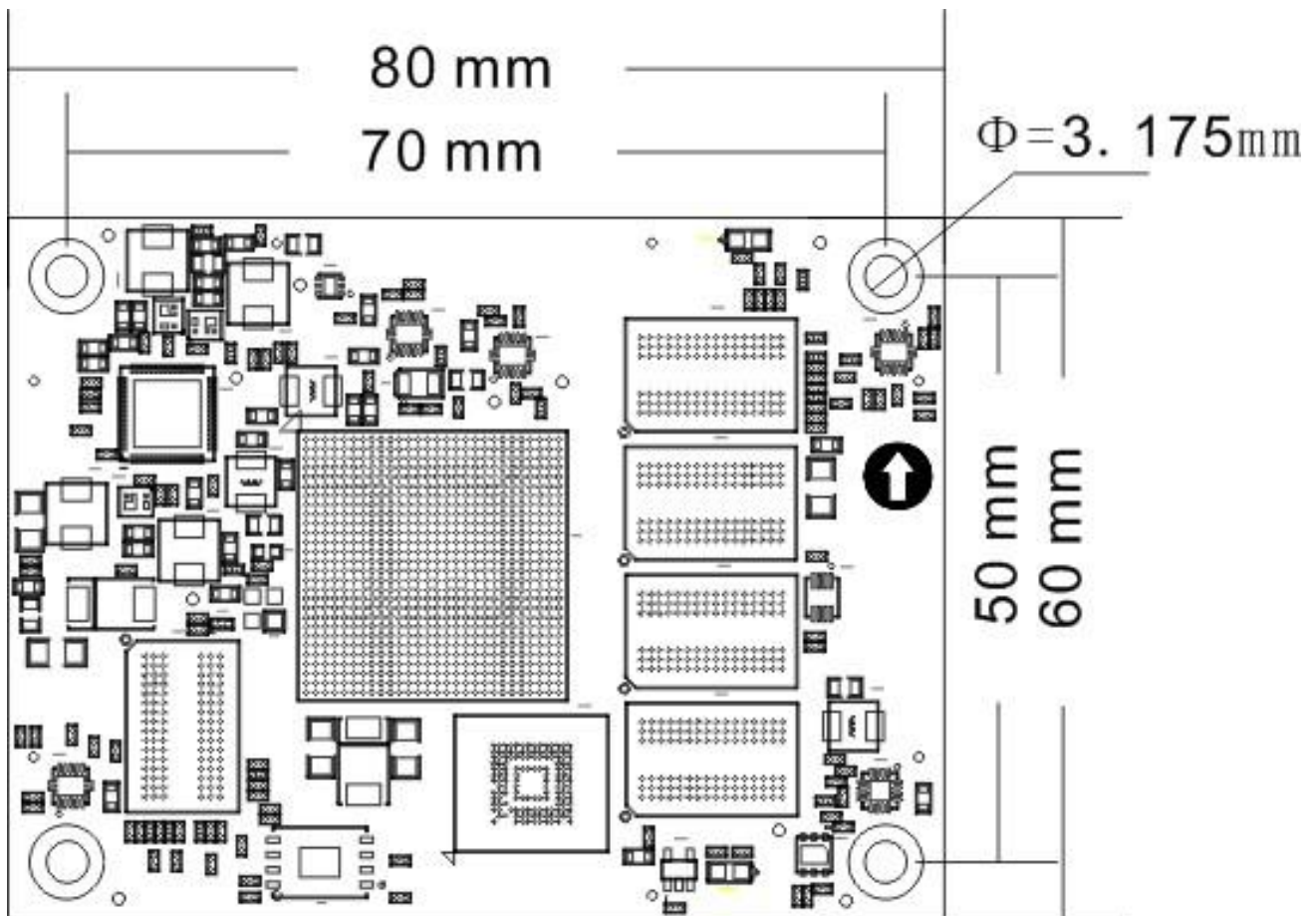


Figure 2-9-1: ACU2CG Core Board Form Factor

Part 2.10: Board to Board Connectors pin assignment

The core board has a total of four high-speed expansion ports. It uses four 120-pin inter-board connectors (J29/J30/J31/J32) to connect to the carrier board.

The connectors used is Panasonic AXK5A2137YG, and the corresponding connector model in the carrier board is Panasonic AXK6A2337YG. Among

them, J29 is connected to the IO of BANK65 and BANK66, J30 is connected to the IO of BANK25, BANK26, BANK66 and the transceiver signal of BANK505 MGT, J31 is connected to the IO of BANK24 and BANK44, J32 is connected to the MIO, VCCO_65, VCCO_66 and +12V power supply of PS.

Among them, the IO level standard of BANK43~46 is 3.3V, and the level standard of BANK65 and BANK66 is determined by the VCCO_65 and VCCO_66 power supply of the carrier board, but cannot exceed +1.8V; the level standard of MIO is also 1.8V.

Pin assignment of board to board connector J29

| J29 Pin | Signal Name | Pin Number | J29 Pin | Signal Name | Pin Number |
|---------|-------------|------------|---------|-------------|------------|
| 1 | B65_L2_N | V9 | 2 | B65_L22_P | K8 |
| 3 | B65_L2_P | U9 | 4 | B65_L22_N | K7 |
| 5 | GND | - | 6 | GND | - |
| 7 | B65_L4_N | T8 | 8 | B65_L20_P | J6 |
| 9 | B65_L4_P | R8 | 10 | B65_L20_N | H6 |
| 11 | GND | - | 12 | GND | - |
| 13 | B65_L1_N | Y8 | 14 | B65_L6_N | T6 |
| 15 | B65_L1_P | W8 | 16 | B65_L6_P | R6 |
| 17 | GND | - | 18 | GND | - |
| 19 | B65_L7_P | L1 | 20 | B65_L17_P | N9 |
| 21 | B65_L7_N | K1 | 22 | B65_L17_N | N8 |
| 23 | GND | - | 24 | GND | - |
| 25 | B65_L15_P | N7 | 26 | B65_L9_P | K2 |
| 27 | B65_L15_N | N6 | 28 | B65_L9_N | J2 |
| 29 | GND | - | 30 | GND | - |
| 31 | B65_L16_P | P7 | 32 | B65_L3_N | V8 |
| 33 | B65_L16_N | P6 | 34 | B65_L3_P | U8 |
| 35 | GND | - | 36 | GND | - |
| 37 | B65_L14_P | M6 | 38 | B65_L19_P | J5 |

| | | | | | |
|-----|-----------|----|-----|-----------|----|
| 39 | B65_L14_N | L5 | 40 | B65_L19_N | J4 |
| 41 | GND | - | 42 | GND | - |
| 43 | B65_L5_N | T7 | 44 | B65_L18_P | M8 |
| 45 | B65_L5_P | R7 | 46 | B65_L18_N | L8 |
| 47 | GND | - | 48 | GND | - |
| 49 | B65_L11_N | K3 | 50 | B65_L8_P | J1 |
| 51 | B65_L11_P | K4 | 52 | B65_L8_N | H1 |
| 53 | GND | - | 54 | GND | - |
| 55 | B65_L10_N | H3 | 56 | B65_L24_N | H8 |
| 57 | B65_L10_P | H4 | 58 | B65_L24_P | H9 |
| 59 | GND | - | 60 | GND | - |
| 61 | B66_L3_P | F2 | 62 | B65_L12_P | L3 |
| 63 | B66_L3_N | E2 | 64 | B65_L12_N | L2 |
| 65 | GND | - | 66 | GND | - |
| 67 | B66_L1_P | G1 | 68 | B65_L13_N | L6 |
| 69 | B66_L1_N | F1 | 70 | B65_L13_P | L7 |
| 71 | GND | - | 72 | GND | - |
| 73 | B66_L6_P | G5 | 74 | B65_L21_P | J7 |
| 75 | B66_L6_N | F5 | 76 | B65_L21_N | H7 |
| 77 | GND | - | 78 | GND | - |
| 79 | B66_L16_P | G8 | 80 | B65_L23_P | K9 |
| 81 | B66_L16_N | F7 | 82 | B65_L23_N | J9 |
| 83 | GND | - | 84 | GND | - |
| 85 | B66_L15_P | G6 | 86 | B66_L5_N | E3 |
| 87 | B66_L15_N | F6 | 88 | B66_L5_P | E4 |
| 89 | GND | - | 90 | GND | - |
| 91 | B66_L4_P | G3 | 92 | B66_L2_P | E1 |
| 93 | B66_L4_N | F3 | 94 | B66_L2_N | D1 |
| 95 | GND | - | 96 | GND | - |
| 97 | B66_L11_P | D4 | 98 | B66_L20_P | C6 |
| 99 | B66_L11_N | C4 | 100 | B66_L20_N | B6 |
| 101 | GND | - | 102 | GND | - |

| | | | | | |
|-----|-----------|----|-----|-----------|----|
| 103 | B66_L12_P | C3 | 104 | B66_L7_P | C1 |
| 105 | B66_L12_N | C2 | 106 | B66_L7_N | B1 |
| 107 | GND | - | 108 | GND | - |
| 109 | B66_L13_N | D6 | 110 | B66_L10_P | B4 |
| 111 | B66_L13_P | D7 | 112 | B66_L10_N | A4 |
| 113 | GND | - | 114 | GND | - |
| 115 | B66_L8_N | A1 | 116 | B66_L9_P | B3 |
| 117 | B66_L8_P | A2 | 118 | B66_L9_N | A3 |
| 119 | GND | - | 120 | GND | - |

Pin assignment of board to board connector J30

| J30 Pin | Signal Name | Pin Number | J30 Pin | Signal Name | Pin Number |
|---------|-------------|------------|---------|-------------|------------|
| 1 | B66_L14_P | E5 | 2 | FPGA_TDI | R18 |
| 3 | B66_L14_N | D5 | 4 | FPGA_TCK | R19 |
| 5 | GND | - | 6 | GND | - |
| 7 | B66_L22_P | C8 | 8 | FPGA_TDO | T21 |
| 9 | B66_L22_N | B8 | 10 | FPGA_TMS | N21 |
| 11 | GND | - | 12 | GND | - |
| 13 | B66_L19_N | A5 | 14 | B66_L21_N | A6 |
| 15 | B66_L19_P | B5 | 16 | B66_L21_P | A7 |
| 17 | GND | - | 18 | GND | - |
| 19 | B66_L24_P | C9 | 20 | B66_L17_P | F8 |
| 21 | B66_L24_N | B9 | 22 | B66_L17_N | E8 |
| 23 | GND | - | 24 | GND | - |
| 25 | B66_L23_N | A8 | 26 | B25_L9_P | C11 |
| 27 | B66_L23_P | A9 | 28 | B25_L9_N | B10 |
| 29 | GND | - | 30 | GND | - |
| 31 | B25_L5_N | F10 | 32 | B25_L10_P | B11 |
| 33 | B25_L5_P | G11 | 34 | B25_L10_N | A10 |
| 35 | GND | - | 36 | GND | - |
| 37 | B66_L18_N | D9 | 38 | B25_L12_P | D12 |

| | | | | | |
|-----|------------|-----|-----|------------|-----|
| 39 | B66_L18_P | E9 | 40 | B25_L12_N | C12 |
| 41 | GND | - | 42 | GND | - |
| 43 | B25_L4_N | H12 | 44 | B25_L11_P | A12 |
| 45 | B25_L4_P | J12 | 46 | B25_L11_N | A11 |
| 47 | GND | - | 48 | GND | - |
| 49 | B26_L11_P | K14 | 50 | B25_L6_N | F11 |
| 51 | B26_L11_N | J14 | 52 | B25_L6_P | F12 |
| 53 | GND | - | 54 | GND | - |
| 55 | B26_L10_N | H13 | 56 | B26_L6_N | E13 |
| 57 | B26_L10_P | H14 | 58 | B26_L6_P | E14 |
| 59 | GND | - | 60 | GND | - |
| 61 | B26_L7_N | F13 | 62 | B26_L3_N | A13 |
| 63 | B26_L7_P | G13 | 64 | B26_L3_P | B13 |
| 65 | GND | - | 66 | GND | - |
| 67 | B26_L9_N | G14 | 68 | B26_L2_N | A14 |
| 69 | B26_L9_P | G15 | 70 | B26_L2_P | B14 |
| 71 | GND | - | 72 | GND | - |
| 73 | B26_L5_N | D14 | 74 | B26_L4_N | C13 |
| 79 | B26_L5_P | D15 | 76 | B26_L4_P | C14 |
| 77 | GND | - | 78 | GND | - |
| 79 | B26_L1_P | B15 | 80 | B26_L12_P | L14 |
| 81 | B26_L1_N | A15 | 82 | B26_L12_N | L13 |
| 83 | GND | - | 84 | GND | - |
| 85 | 505_CLK2_P | C21 | 86 | 505_CLK1_P | E21 |
| 87 | 505_CLK2_P | C22 | 88 | 505_CLK1_P | E22 |
| 89 | GND | - | 90 | GND | - |
| 91 | 505_CLK0_P | F23 | 92 | 505_CLK3_P | A21 |
| 93 | 505_CLK0_N | F24 | 94 | 505_CLK3_N | A22 |
| 95 | GND | - | 96 | GND | - |
| 97 | 505_TX3_P | B23 | 98 | 505_TX1_P | D23 |
| 99 | 505_TX3_N | B24 | 100 | 505_TX1_N | D24 |
| 101 | GND | - | 102 | GND | - |

| | | | | | |
|-----|-----------|-----|-----|-----------|-----|
| 103 | 505_RX3_P | A25 | 104 | 505_TX0_P | E25 |
| 105 | 505_RX3_N | A26 | 106 | 505_TX0_N | E26 |
| 107 | GND | - | 108 | GND | - |
| 109 | 505_TX2_P | C25 | 110 | 505_RX1_P | D27 |
| 111 | 505_TX2_N | C26 | 112 | 505_RX1_N | D28 |
| 113 | GND | - | 114 | GND | - |
| 115 | 505_RX2_P | B27 | 116 | 505_RX0_P | F27 |
| 117 | 505_RX2_N | B28 | 118 | 505_RX0_N | F28 |
| 119 | GND | - | 120 | GND | - |

Pin assignment of board to board connector J31

| J31 Pin | Signal Name | Pin Number | J31 Pin | Signal Name | Pin Number |
|---------|-------------|------------|---------|-------------|------------|
| 1 | B24_L10_P | Y14 | 2 | B24_L7_P | AA13 |
| 3 | B24_L10_N | Y13 | 4 | B24_L7_N | AB13 |
| 5 | GND | - | 6 | GND | - |
| 7 | B24_L6_P | AC14 | 8 | B44_L6_P | AC12 |
| 9 | B24_L6_N | AC13 | 10 | B44_L6_N | AD12 |
| 11 | GND | - | 12 | GND | - |
| 13 | B24_L5_P | AD15 | 14 | B44_L7_P | AD11 |
| 15 | B24_L5_N | AD14 | 16 | B44_L7_N | AD10 |
| 17 | GND | - | 18 | GND | - |
| 19 | B24_L1_P | AE15 | 20 | B44_L8_N | AC11 |
| 21 | B24_L1_N | AE14 | 22 | B44_L8_P | AB11 |
| 23 | GND | - | 24 | GND | - |
| 25 | B24_L12_P | Y12 | 26 | B24_L2_P | AG14 |
| 27 | B24_L12_N | AA12 | 28 | B24_L2_N | AH14 |
| 29 | GND | - | 30 | GND | - |
| 31 | B24_L3_P | AG13 | 32 | - | - |
| 33 | B24_L3_N | AH13 | 34 | - | - |
| 35 | GND | - | 36 | GND | - |
| 37 | B44_L12_N | AB9 | 38 | B44_L9_P | AA11 |

| | | | | | |
|-----|------------|------|-----|------------|------|
| 39 | B44_L12_P | AB10 | 40 | B44_L9_N | AA10 |
| 41 | GND | - | 42 | GND | - |
| 43 | B44_L10_N | Y10 | 44 | B44_L3_P | AH12 |
| 45 | B44_L10_P | W10 | 46 | B44_L3_N | AH11 |
| 47 | GND | - | 48 | GND | - |
| 49 | B24_L11_N | W11 | 50 | B44_L1_N | AH10 |
| 51 | B24_L11_P | W12 | 52 | B44_L1_P | AG10 |
| 53 | GND | - | 54 | GND | - |
| 55 | B24_L9_N | W13 | 56 | B24_L4_P | AE13 |
| 57 | B24_L9_P | W14 | 58 | B24_L4_N | AF13 |
| 59 | GND | - | 60 | GND | - |
| 61 | B24_L8_P | AB15 | 62 | B44_L5_P | AE12 |
| 63 | B24_L8_N | AB14 | 64 | B44_L5_N | AF12 |
| 65 | GND | - | 66 | GND | - |
| 67 | B44_L2_N | AG11 | 68 | B44_L4_N | AF10 |
| 69 | B44_L2_P | AF11 | 70 | B44_L4_P | AE10 |
| 71 | GND | - | 72 | GND | - |
| 73 | VBAT_IN | Y18 | 74 | B44_L11_P | Y9 |
| 75 | MR | - | 76 | B44_L11_N | AA8 |
| 77 | GND | - | 78 | GND | - |
| 79 | - | - | 80 | PS_POR_B | P16 |
| 81 | - | - | 82 | - | - |
| 83 | GND | - | 84 | GND | - |
| 86 | - | - | 86 | - | - |
| 87 | - | - | 88 | - | - |
| 89 | GND | - | 90 | GND | - |
| 91 | 224_CLK0_P | Y6 | 92 | 224_CLK1_P | V6 |
| 93 | 224_CLK0_N | Y5 | 94 | 224_CLK1_N | V5 |
| 95 | GND | - | 96 | GND | - |
| 97 | 224_RX3_P | P2 | 98 | 224_TX3_P | N4 |
| 99 | 224_RX3_N | P1 | 100 | 224_TX3_N | N3 |
| 101 | GND | - | 102 | GND | - |

| | | | | | |
|-----|-----------|----|-----|-----------|----|
| 103 | 224_RX2_P | T2 | 104 | 224_TX2_P | R4 |
| 105 | 224_RX2_N | T1 | 106 | 224_TX2_N | R3 |
| 107 | GND | - | 108 | GND | - |
| 109 | 224_RX1_P | V2 | 110 | 224_TX1_P | U4 |
| 111 | 224_RX1_N | V1 | 112 | 224_TX1_N | U3 |
| 113 | GND | - | 114 | GND | - |
| 115 | 224_RX0_P | Y2 | 116 | 224_TX0_P | W4 |
| 117 | 224_RX0_N | Y1 | 118 | 224_TX0_N | W3 |
| 119 | GND | - | 120 | GND | - |

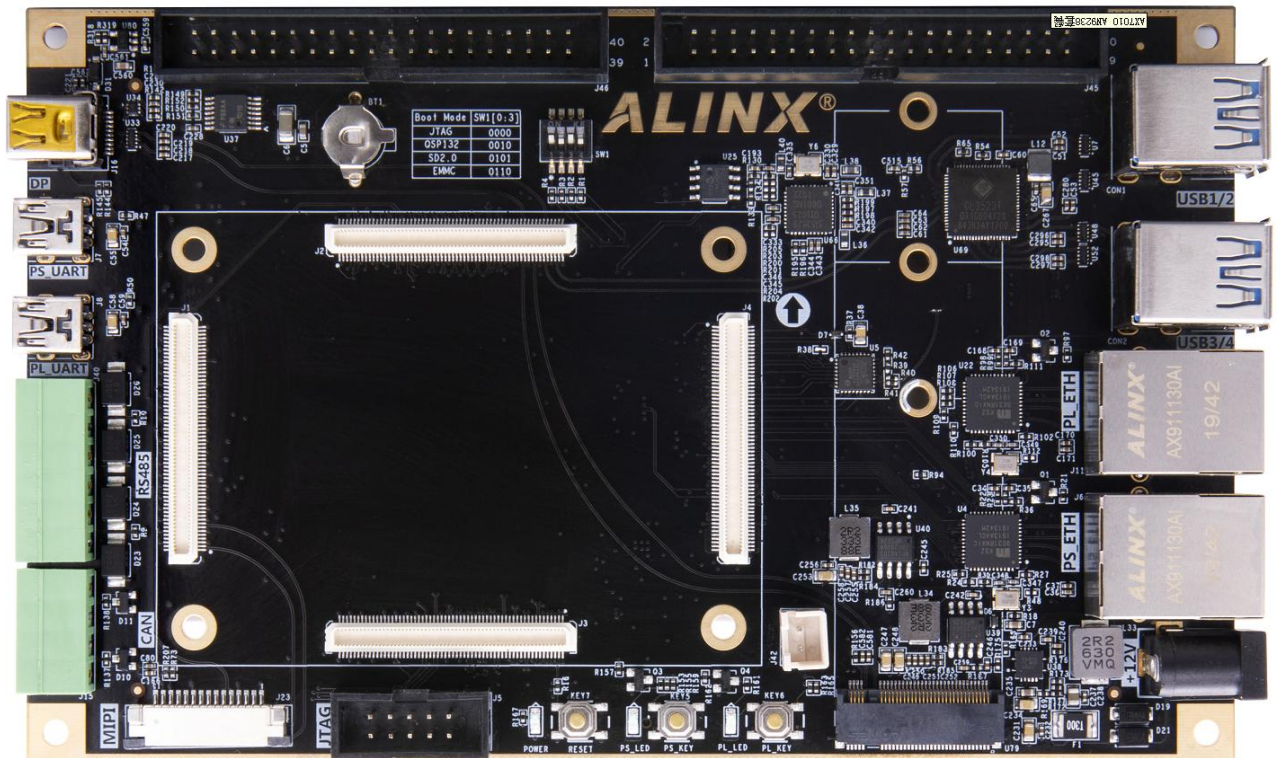
Pin assignment of board to board connector J32

| J32 Pin | Signal Name | Pin Number | J32 Pin | Signal Name | Pin Number |
|---------|-------------|------------|---------|-------------|------------|
| 1 | PS_MIO35 | H17 | 2 | PS_MIO30 | F16 |
| 3 | PS_MIO29 | G16 | 4 | PS_MIO31 | H16 |
| 5 | GND | - | - | GND | - |
| 7 | - | - | 8 | PS_MIO58 | F18 |
| 9 | - | - | 10 | PS_MIO53 | D16 |
| 11 | GND | - | 12 | GND | - |
| 13 | PS_MODE0 | P19 | 14 | PS_MIO52 | G18 |
| 15 | PS_MODE1 | P20 | 16 | PS_MIO55 | B16 |
| 17 | GND | - | 18 | GND | - |
| 19 | PS_MODE2 | R20 | 20 | PS_MIO56 | C16 |
| 21 | PS_MODE3 | T20 | 22 | PS_MIO57 | A16 |
| 23 | GND | - | 24 | GND | - |
| 25 | PS_MIO36 | K17 | 26 | PS_MIO54 | F17 |
| 27 | PS_MIO37 | J17 | 28 | PS_MIO27 | J15 |
| 29 | GND | - | 30 | GND | - |
| 31 | - | - | 32 | PS_MIO28 | K15 |
| 33 | PS_MIO77 | F20 | 34 | PS_MIO59 | E17 |
| 35 | GND | - | 36 | GND | - |
| 37 | PS_MIO76 | B20 | 38 | PS_MIO60 | C17 |

| | | | | | |
|-----|----------|------|-----|----------|-----|
| 39 | - | - | 40 | PS_MIO61 | D17 |
| 41 | GND | - | 42 | GND | - |
| 43 | PS_MIO39 | H19 | 44 | PS_MIO62 | A17 |
| 45 | PS_MIO38 | H18 | 46 | PS_MIO63 | E18 |
| 47 | GND | - | 48 | GND | - |
| 49 | - | - | 50 | PS_MIO65 | A18 |
| 51 | PS_MIO40 | K18 | 52 | PS_MIO66 | G19 |
| 53 | GND | - | 54 | GND | - |
| 55 | PS_MIO44 | J20 | 56 | PS_MIO67 | B18 |
| 57 | PS_MIO45 | K20 | 58 | PS_MIO68 | C18 |
| 59 | GND | - | 60 | GND | - |
| 61 | PS_MIO47 | H21 | 62 | PS_MIO64 | E19 |
| 63 | PS_MIO48 | J21 | 64 | PS_MIO69 | D19 |
| 65 | GND | - | 66 | GND | - |
| 67 | PS_MIO41 | J19 | 68 | PS_MIO74 | D20 |
| 69 | PS_MIO32 | J16 | 70 | PS_MIO73 | G21 |
| 71 | GND | - | 72 | GND | - |
| 73 | PS_MIO46 | L20 | 74 | PS_MIO72 | G20 |
| 75 | PS_MIO50 | M19 | 76 | PS_MIO71 | B19 |
| 77 | GND | - | 78 | GND | - |
| 79 | PS_MIO49 | M18 | 80 | PS_MIO75 | A19 |
| 81 | PS_MIO34 | L17 | 82 | PS_MIO70 | C19 |
| 83 | GND | - | 84 | GND | - |
| 85 | PS_MIO26 | L15 | 86 | PS_MIO43 | K19 |
| 87 | PS_MIO24 | AB19 | 88 | PS_MIO51 | L21 |
| 89 | GND | - | 90 | GND | - |
| 91 | PS_MIO25 | AB21 | 92 | PS_MIO42 | L18 |
| 93 | - | - | 94 | PS_MIO33 | L16 |
| 95 | GND | - | 96 | GND | - |
| 97 | - | - | 98 | - | - |
| 99 | VCCO_65 | - | 100 | VCCO_66 | - |
| 101 | VCCO_65 | - | 102 | VCCO_66 | - |

| | | | | | |
|-----|---------|---|-----|---------|---|
| 103 | VCCO_65 | - | 104 | VCCO_66 | - |
| 105 | GND | - | 106 | GND | - |
| 107 | +12V | - | 108 | +12V | - |
| 109 | +12V | - | 110 | +12V | - |
| 111 | +12V | - | 112 | +12V | - |
| 113 | +12V | - | 114 | +12V | - |
| 115 | +12V | - | 116 | +12V | - |
| 117 | +12V | - | 118 | +12V | - |
| 119 | +12V | - | 120 | +12V | - |

Part 3: Carrier Board



Part 3.1: Carrier Board Introduction

Through the previous function introduction, you can understand the function of the carrier board part

- 1-Channel M.2 interface
- 1-Channel DP output interface
- 4 USB 3.0 Interfaces
- 2-Channel 10/100M/1000M Ethernet RJ-45 interface
- 2-Channel USB Uart Interfaces
- 1-Channel Micro SD card slot
- 1-Channel MIPI camera interface
- 2-Channel 40-pin expansion port
- 2-Channel CAN communication interfaces
- 2-Channel 485 communication interfaces

- JTAG debugging interface
- 1-Channel temperature sensor
- 1-Channel EEPROM
- 1-Channel RTC real-time clock
- 3 LED lights
- 3 Keys

Part 3.2: M.2 Interface

The AXU2CGB-E development board is equipped with a PCIe x1 standard M.2 interface for connecting M.2 SSD solid state drives, with a communication speed of up to 6Gbps. The M.2 interface uses the M key slot, which only supports PCI-E, not SATA. When users choose SSD solid state drives, they need to choose PCIe type SSD solid state drives.

The PCIe signal is directly connected to the BANK505 PS MGT transceiver of ZU2CG, and the TX signal and RX signal of one channel are connected to the LANE1 of MGT in a differential signal mode. The PCIe clock is provided by the Si5332 chip, the frequency is 100Mhz, and the schematic diagram of the M.2 circuit design is shown in Figure 3-2-1:

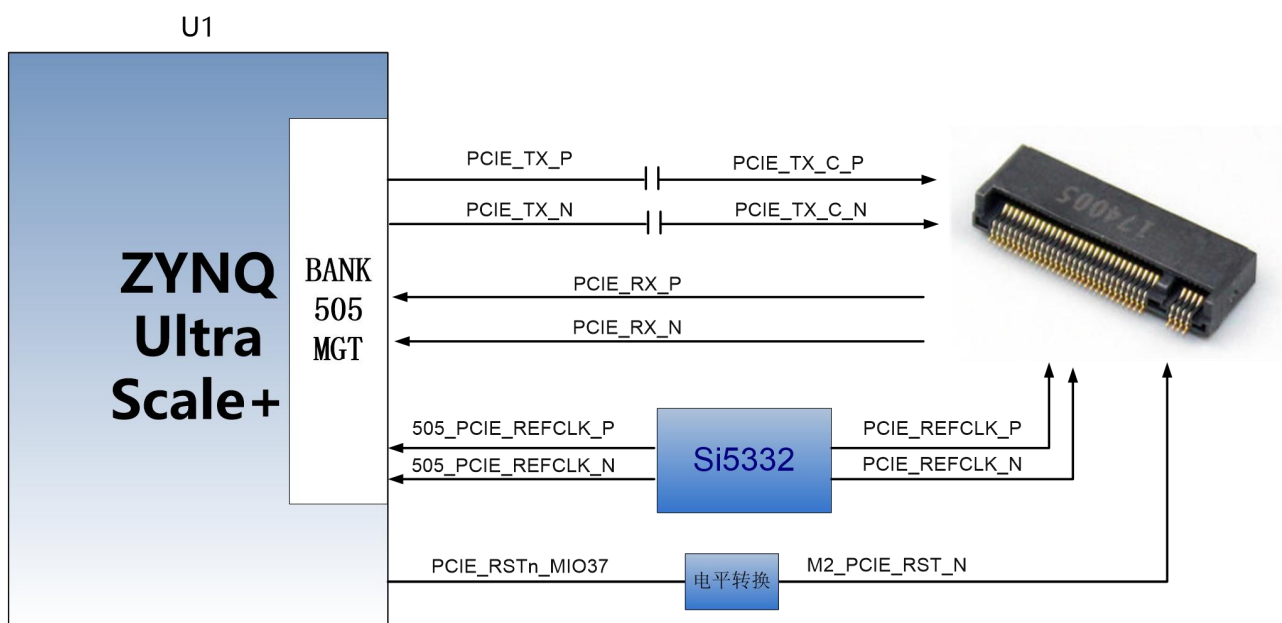


Figure 3-2-1: M.2 Interface Schematic

The pin assignment of M.2 interface ZYNQ is as follows:

| Signal Name | Pin Name | Pin Number | Description |
|-------------------|--------------|------------|-------------------------------|
| PCIE_TX_P | 505_TX0_P | E25 | PCIE Data Transmit Positive |
| PCIE_TX_N | 505_TX0_N | E26 | PCIE Data Transmit Negative |
| PCIE_RX_P | 505_RX0_P | F27 | PCIE Data Receive Positive |
| PCIE_RX_N | 505_RX0_N | F28 | PCIE Data Receive Negative |
| 505_PCIE_REFCLK_P | 505_CLK0_P | F23 | PCIE Reference Clock Positive |
| 505_PCIE_REFCLK_N | 505_CLK0_N | F24 | PCIE Reference Clock Negative |
| PCIE_RSTn_MIO37 | PS_MIO37_501 | J17 | PCIE Reset Signal |

Part 3.3: DP Interface

The AXU2CGB-E development board has a standard DisplayPort output display interface for video image display. The interface supports VESA DisplayPort V1.2a output standard, up to 4K x 2K@30Fps output, supports Y-only, YCbCr444, YCbCr422, YCbCr420 and RGB video formats, each color supports 6, 8, 10, or 12 bits.

The DisplayPort data transmission channel is directly driven and output by the BANK505 PS MGT of ZU2CG, and the LANE2 and LANE3 TX signals of MGT are connected to the DP connector in a differential signal mode. The DisplayPort auxiliary channel is connected to the MIO pin of the PS. The schematic diagram of the DP output interface design is shown in Figure 3-3-1:

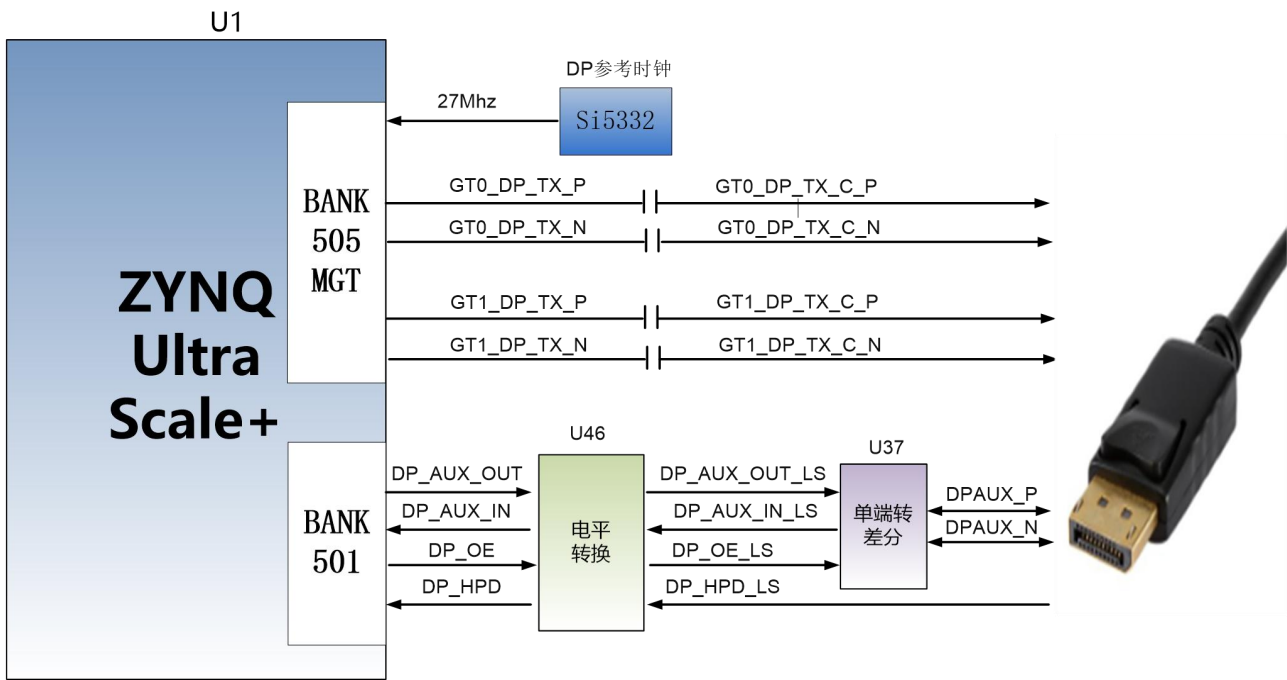


Figure 3-3-1: DP interface design Schematic

The DisplayPort interface ZYNQ pin assignment is as follows:

| Signal Name | ZYNQ Pin Number | ZYNQ Pin Number | Description |
|-------------|-----------------|-----------------|--|
| GT0_DP_TX_P | 505_TX3_P | B23 | Low bits of DP Data Transmit Positive |
| GT0_DP_TX_N | 505_TX3_N | B24 | Low bits of DP Data Transmit Negative |
| GT1_DP_TX_P | 505_TX2_P | C25 | High bits of DP Data Transmit Positive |
| GT1_DP_TX_N | 505_TX2_N | C26 | High bits of DP Data Transmit Negative |
| 505_CLK1_P | 505_CLK2_P | C21 | DP Reference Clock Positive |
| 505_CLK1_N | 505_CLK2_N | C22 | DP Reference Clock Negative |
| DP_AUX_OUT | PS_MIO27 | J15 | DP Auxiliary Data Output |
| DP_AUX_IN | PS_MIO30 | F16 | DP Auxiliary Data Input |
| DP_OE | PS_MIO29 | G16 | DP Auxiliary Data Output Enable |
| DP_HPDP | PS_MIO28 | K15 | DP Insertion Signal Detection |

Part 3.4: USB3.0 interface

There are 4 USB3.0 ports on the AXU2CGB-E carrier board, supporting the HOST working mode, and the data transmission speed is up to 5.0Gb/s. USB3.0 is connected through the PIPE3 interface, and USB2.0 is connected to the external USB3320C chip through the ULPI interface to realize high-speed USB3.0 and USB2.0 data communication.

The USB interface is a flat USB interface (USB Type A), which is convenient for users to connect different USB Slave peripherals (such as USB mouse, keyboard or U disk) at the same time. The schematic diagram of USB3.0 connection is shown as 3-4-1:

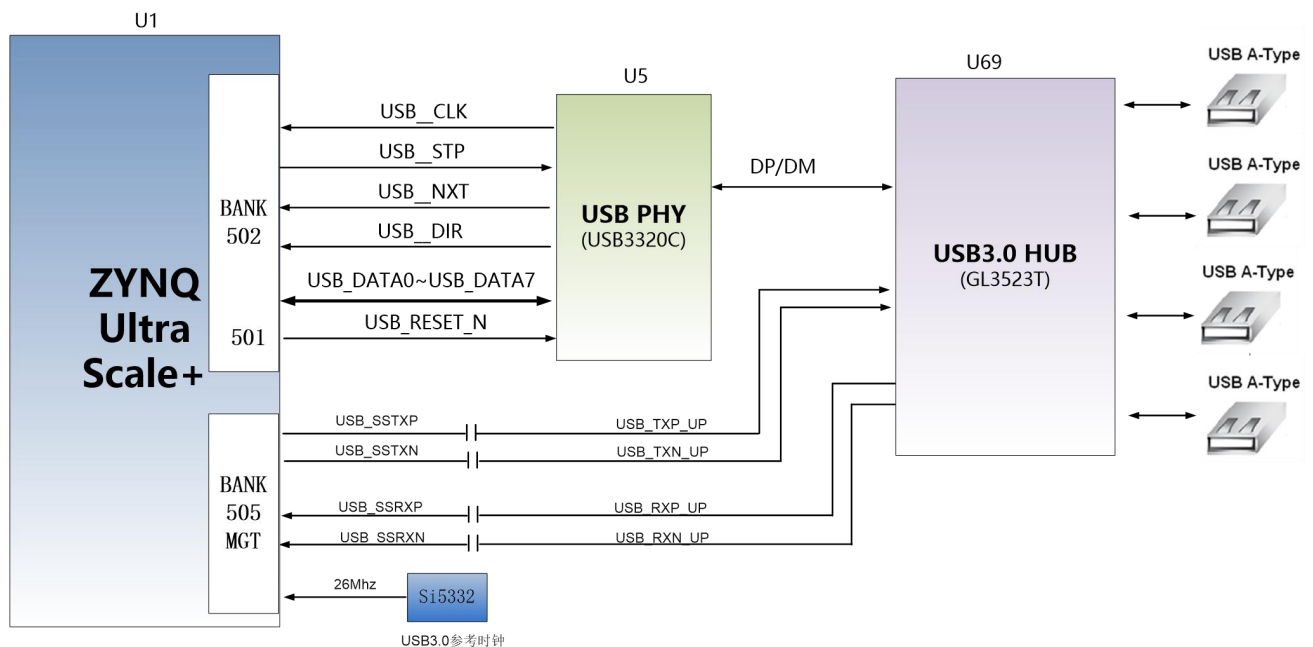


Figure 3-4-1: USB3.0 Interface Schematic

USB Interface Pin Assignment:

| Signal Name | Pin Name | Pin Number | Description |
|-------------|-----------|------------|-------------------------------|
| USB_SSTXP | 505_TX1_P | D23 | USB3.0 Data Transmit Positive |
| USB_SSTXN | 505_TX1_N | D24 | USB3.0 Data Transmit Negative |
| USB_SSRXP | 505_RX1_P | D27 | USB3.0 Data Receive Positive |
| USB_SSRXN | 505_RX1_N | D28 | USB3.0 Data Receive Negative |
| USB_DATA0 | PS_MIO56 | C16 | USB2.0 Data Bit0 |

| | | | |
|-------------|----------|-----|------------------------------|
| USB_DATA1 | PS_MIO57 | A16 | USB2.0 Data Bit1 |
| USB_DATA2 | PS_MIO54 | F17 | USB2.0 Data Bit2 |
| USB_DATA3 | PS_MIO59 | E17 | USB2.0 Data Bit3 |
| USB_DATA4 | PS_MIO60 | C17 | USB2.0 Data Bit4 |
| USB_DATA5 | PS_MIO61 | D17 | USB2.0 Data Bit5 |
| USB_DATA6 | PS_MIO62 | A17 | USB2.0 Data Bit6 |
| USB_DATA7 | PS_MIO63 | E18 | USB2.0 Data Bit7 |
| USB_STP | PS_MIO58 | F18 | USB2.0 Stop Signal |
| USB_DIR | PS_MIO53 | D16 | USB2.0 Data Direction Signal |
| USB_CLK | PS_MIO52 | G18 | USB2.0 Clock Signal |
| USB_NXT | PS_MIO55 | B16 | USB2.0 Next Data Signal |
| USB_RESET_N | PS_MIO31 | H16 | USB2.0 Reset Signal |

Part 3.5: Gigabit Ethernet Interface

There are 2 Gigabit Ethernet ports on the AXU2CGB-E carrier board, one is connected to the PS end, and the other is connected to the PL end. The GPHY chip uses JLSemi JL2121-N040I Ethernet GPHY chip to provide users with network communication services. The Ethernet PHY chip on the PS side is connected to the MIO interface of the BANK502 of the PS side of ZYNQ. The Ethernet PHY chip on the PL side is connected to the IO of the BANK66. The JL2121-N040I chip supports 10/100/1000 Mbps network transmission rate, and communicates with the MAC layer of the ZU2CG system through the RGMII interface. JL2121-N040I supports MDI/MDX adaptation, various speed adaptation, Master/Slave adaptation, and MDIO bus for PHY register management.

When the JL2121-N040I is powered on, it will detect the level status of some specific IOs to determine its own operating mode. Table 3-5-1 describes the default settings after the GPHY chip is powered on.

| Configuration Pin | Instructions | Configuration value |
|-----------------------|--------------------------|---------------------|
| RXD3_ADR0 RXC_ADR1 | MDIO/MDC Mode PHYaddress | PHY Address 001 |

| | | |
|------------|--------------------|-------|
| RXCTL_ADR2 | | |
| RXD1_TXDLY | TX clock 2ns delay | delay |
| RXD0_RXDLY | RX clock 2ns delay | delay |

Table 3-5-1: PHY chip default configuration value

When the network is connected to Gigabit Ethernet, the data transmission of ZYNQ and PHY chip JL2121-N040I is communicated through the RGMII bus, the transmission clock is 125Mhz, and the data is sampled on the rising edge and falling samples of the clock.

When the network is connected to 100M Ethernet, the data transmission of ZYNQ and PHY chip JL2121-N040I is communicated through RMII bus, and the transmission clock is 25Mhz. Data is sampled on the rising edge and falling samples of the clock.

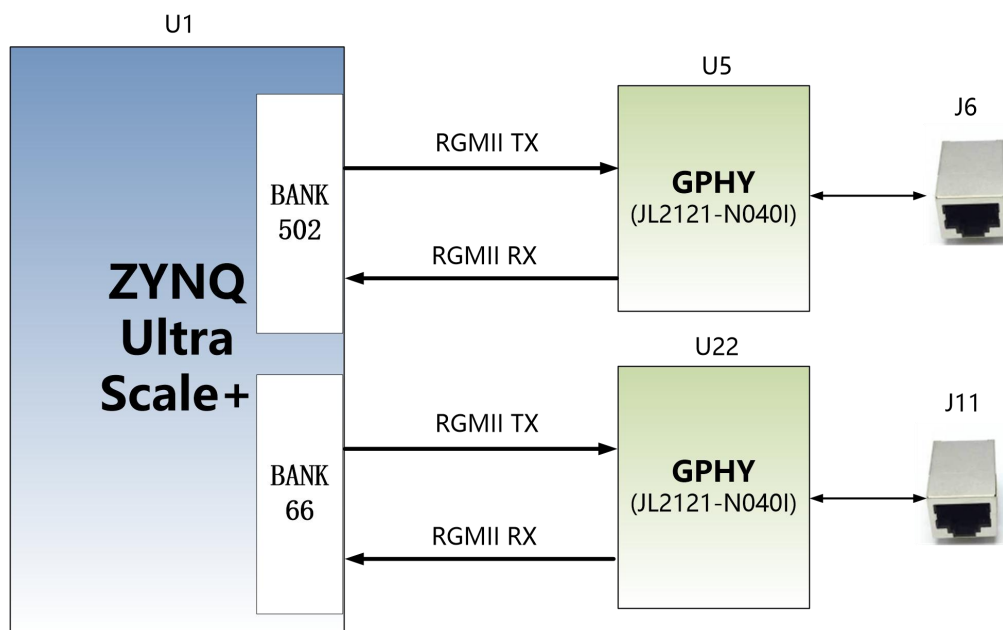


Figure 3-5-1: ZYNQ PS system and GPHY connection diagram

The Gigabit Ethernet pin assignments are as follows:

| Signal Name | Pin Name | Pin Number | Description |
|-------------|----------|------------|-------------|
|-------------|----------|------------|-------------|

| | | | |
|------------|-----------|-----|-----------------------------------|
| PHY1_TXCK | PS_MIO64 | E19 | Ethernet 1 RGMII Transmit Clock |
| PHY1_TXD0 | PS_MIO65 | A18 | Ethernet 1 Transmit data bit0 |
| PHY1_TXD1 | PS_MIO66 | G19 | Ethernet 1 Transmit data bit1 |
| PHY1_TXD2 | PS_MIO67 | B18 | Ethernet 1 Transmit data bit2 |
| PHY1_TXD3 | PS_MIO68 | C18 | Ethernet 1 Transmit data bit3 |
| PHY1_TXCTL | PS_MIO69 | D19 | Ethernet 1 Transmit Enable Signal |
| PHY1_RXCK | PS_MIO70 | C19 | Ethernet 1 RGMII Receive Clock |
| PHY1_RXD0 | PS_MIO71 | B19 | Ethernet 1 Receive Data Bit0 |
| PHY1_RXD1 | PS_MIO72 | G20 | Ethernet 1 Receive Data Bit1 |
| PHY1_RXD2 | PS_MIO73 | G21 | Ethernet 1 Receive Data Bit2 |
| PHY1_RXD3 | PS_MIO74 | D20 | Ethernet 1 Receive Data Bit3 |
| PHY1_RXCTL | PS_MIO75 | A19 | Ethernet 1 Receive Enable Signal |
| PHY1_MDC | PS_MIO76 | B20 | Ethernet 1 MDIO Clock Management |
| PHY1_MDIO | PS_MIO77 | F20 | Ethernet 1 MDIO Management Data |
| PHY2_TXCK | B66_L17_N | E8 | Ethernet 2 RGMII Transmit Clock |
| PHY2_TXD0 | B66_L18_P | E9 | Ethernet 2 Transmit data bit0 |
| PHY2_TXD1 | B66_L18_N | D9 | Ethernet 2 Transmit data bit1 |
| PHY2_TXD2 | B66_L23_P | A9 | Ethernet 2 Transmit data bit2 |
| PHY2_TXD3 | B66_L23_N | A8 | Ethernet 2 Transmit data bit3 |
| PHY2_TXCTL | B66_L24_N | B9 | Ethernet 2 Transmit Enable Signal |
| PHY2_RXCK | B66_L14_P | E5 | Ethernet 2 RGMII Receive Clock |
| PHY2_RXD0 | B66_L19_N | A5 | Ethernet 2 Receive Data Bit0 |
| PHY2_RXD1 | B66_L19_P | B5 | Ethernet 2 Receive Data Bit1 |
| PHY2_RXD2 | B66_L17_P | F8 | Ethernet 2 Receive Data Bit2 |
| PHY2_RXD3 | B66_L24_P | C9 | Ethernet 2 Receive Data Bit3 |
| PHY2_RXCTL | B66_L22_N | B8 | Ethernet 2 Receive Enable Signal |
| PHY2_MDC | B66_L21_N | A6 | Ethernet 2 MDIO Clock Management |
| PHY2_MDIO | B66_L22_P | C8 | Ethernet 2 MDIO Management Data |
| PHY2_RESET | B66_L14_N | D5 | Ethernet 2 Reset Signal |

Part 3.6: USB to Serial Port

The AXU2CGB-E carrier board is equipped with two Uart to USB ports, one is connected to the PS end, and one is connected to the PL end.

The conversion chip uses Silicon Labs CP2102GM's USB-UAR chip, and

the USB interface is a MINI USB interface. You can use a USB cable to connect it to the PC's USB port for serial data communication. The schematic diagram of the USB Uart circuit design is shown in the figure below:

The schematic diagram of the USB Uart circuit design is shown in Figure 3-6-1:

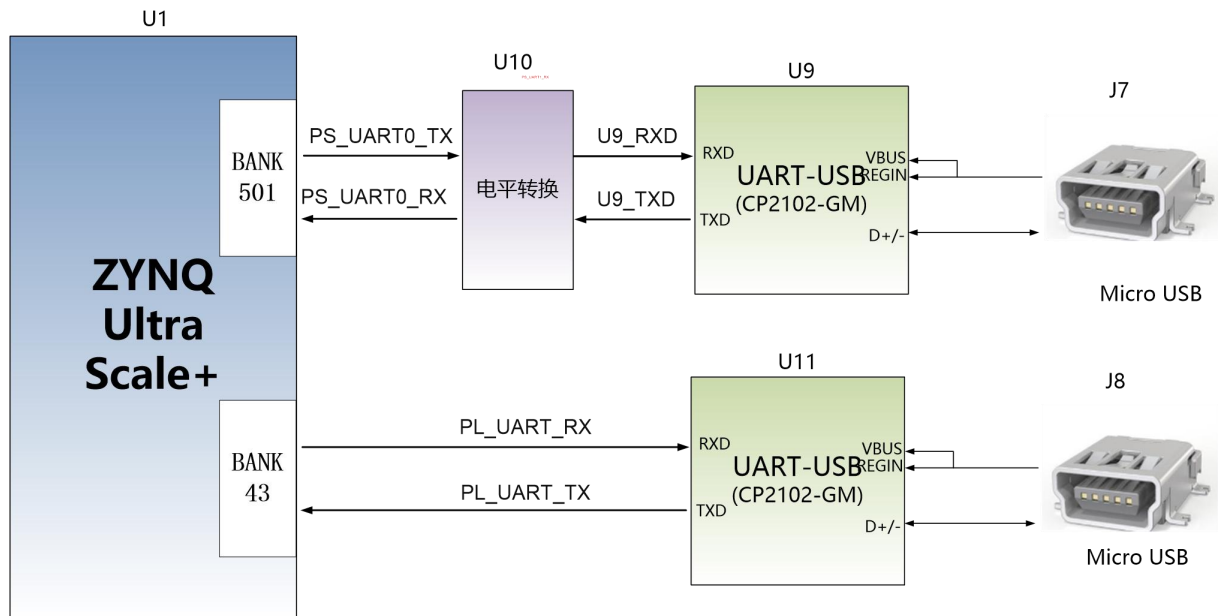


Figure 3-6-1: USB to serial port schematic

USB to serial port ZYNQ pin assignment:

| Signal name | Pin Name | Pin Number | Description |
|-------------|----------|------------|---------------------|
| PS_UART0_TX | PS_MIO43 | K19 | PS Uart Data Output |
| PS_UART0_RX | PS_MIO42 | L18 | PS Uart Data Input |
| PL_UART_TX | B43_L3_P | AH12 | PL Uart Data Output |
| PL_UART_RX | B43_L3_N | AH11 | PL Uart Data Input |

Part 3.7: SD Card Slot Interface

The AXU2CGB-E FPGA Development Board contains a Micro SD card interface to provide user access to the SD card memory, the BOOT program for the ZU2CG chip, the Linux operating system kernel, the file

system and other user data files.

The SDIO signal is connected to the IO signal of the PS BANK501 of ZU2CG. Since the VCCMIO of the BANK is set to 1.8V, but the data level of the SD card is 3.3V, connected through the TXS02612 level shifter. The schematic of the Zynq7000 PS and SD card connector is shown in Figure 3-10-1:

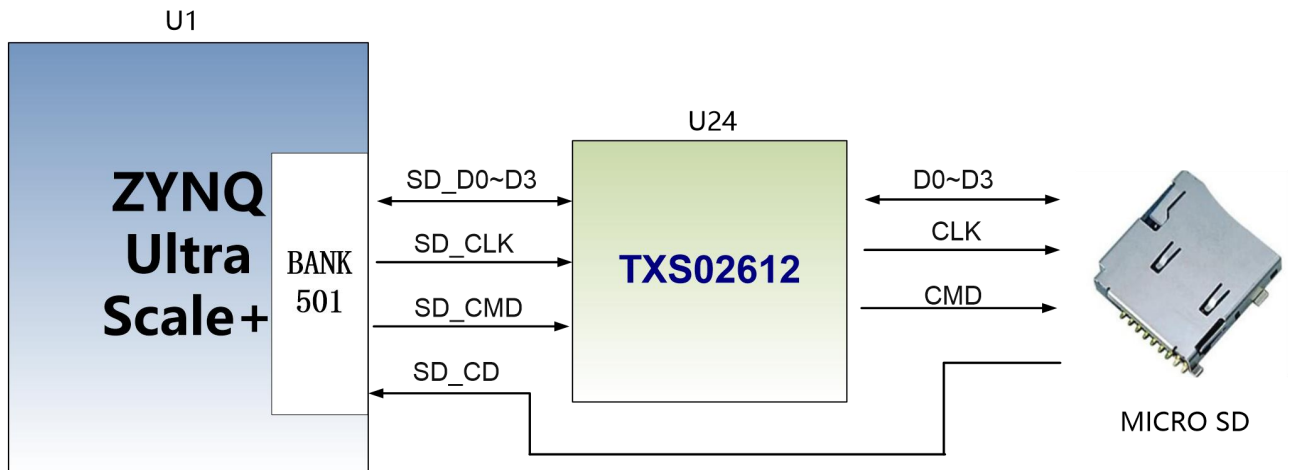


Figure 3-7-1: SD Card Connection Diagram

SD card slot pin assignment:

| Signal Name | Pin Name | Pin Number | Description |
|-------------|----------|------------|--------------------------|
| SD_CLK | PS_MIO51 | I21 | SD Clock Signal |
| SD_CMD | PS_MIO50 | M19 | SD Command Signal |
| SD_D0 | PS_MIO46 | L20 | SD Data0 |
| SD_D1 | PS_MIO47 | H21 | SD Data1 |
| SD_D2 | PS_MIO48 | J21 | SD Data2 |
| SD_D3 | PS_MIO49 | M18 | SD Data3 |
| SD_CD | PS_MIO45 | K20 | SD card insertion signal |

Part 3.8: Expansion Header

The AXU2CGB-E board is reserved with two 0.1-inch standard pitch 40-pin expansion ports J45 and J46, which are used to connect the ALINX modules or the external circuit designed by the user. The expansion port has 40 signals, of

which 1-channel 5V power supply, 2-channel 3.3 V power supply, 3-channel ground and 34 IOs. **Do not directly connect the IO directly to the 5V device to avoid burning the FPGA. If you want to connect 5V equipment, you need to connect level conversion chip.**

J45 Expansion Header Pin Assignment

| J45 Pin | Signal Name | Pin Number | J45 Pin | Signal Name | Pin Number |
|---------|-------------|------------|---------|-------------|------------|
| 1 | GND | - | 2 | +5V | - |
| 3 | B45_L9_N | B10 | 4 | B45_L9_P | C11 |
| 5 | B45_L5_N | F10 | 6 | B45_L5_P | G11 |
| 7 | B45_L12_N | C12 | 8 | B45_L12_P | D12 |
| 9 | B45_L11_N | A11 | 10 | B45_L11_P | A12 |
| 11 | B45_L6_N | F11 | 12 | B45_L6_P | F12 |
| 13 | B46_L6_N | E13 | 14 | B46_L6_P | E14 |
| 15 | B46_L3_N | A13 | 16 | B46_L3_P | B13 |
| 17 | B46_L2_N | A14 | 18 | B46_L2_P | B14 |
| 19 | B46_L4_N | C13 | 20 | B46_L4_P | C14 |
| 21 | B46_L12_N | L13 | 22 | B46_L12_P | L14 |
| 23 | B45_L4_N | H12 | 24 | B45_L4_P | J12 |
| 25 | B46_L11_N | J14 | 26 | B46_L11_P | K14 |
| 27 | B46_L10_N | H13 | 28 | B46_L10_P | H14 |
| 29 | B46_L7_N | F13 | 30 | B46_L7_P | G13 |
| 31 | B46_L9_N | G14 | 32 | B46_L9_P | G15 |
| 33 | B46_L5_N | D14 | 34 | B46_L5_P | D15 |
| 35 | B46_L1_N | A15 | 36 | B46_L1_P | B15 |
| 37 | GND | - | 38 | GND | - |
| 39 | +3.3V | - | 40 | +3.3V | - |

J46 Expansion Header Pin Assignment

| J46 Pin | Signal Name | Pin Number | J46 Pin | Signal Name | Pin Number |
|---------|-------------|------------|---------|-------------|------------|
| 1 | GND | - | 2 | +5V | - |
| 3 | B43_L2_N | AG11 | 4 | B43_L2_P | AF11 |
| 5 | B44_L8_N | AB14 | 6 | B44_L8_P | AB15 |
| 7 | B44_L9_N | W13 | 8 | B44_L9_P | W14 |
| 9 | B44_L11_N | W11 | 10 | B44_L11_P | W12 |

| | | | | | |
|----|-----------|------|----|-----------|------|
| 11 | B43_L10_N | Y10 | 12 | B43_L10_P | W10 |
| 13 | B43_L12_N | AB9 | 14 | B43_L12_P | AB10 |
| 15 | B44_L3_N | AH13 | 16 | B44_L3_P | AG13 |
| 17 | B44_L12_N | AA12 | 18 | B44_L12_P | Y12 |
| 19 | B44_L1_N | AE14 | 20 | B44_L1_P | AE15 |
| 21 | B44_L5_N | AD14 | 22 | B44_L5_P | AD15 |
| 23 | B44_L6_N | AC13 | 24 | B44_L6_P | AC14 |
| 25 | B44_L10_N | Y13 | 26 | B44_L10_P | Y14 |
| 27 | B44_L2_N | AH14 | 28 | B44_L2_P | AG14 |
| 29 | B43_L8_N | AC11 | 30 | B43_L8_P | AB11 |
| 31 | B43_L7_N | AD10 | 32 | B43_L7_P | AD11 |
| 33 | B43_L6_N | AD12 | 34 | B43_L6_P | AC12 |
| 35 | B44_L7_N | AB13 | 36 | B44_L7_P | AA13 |
| 37 | GND | - | 38 | GND | - |
| 39 | +3.3V | - | 40 | +3.3V | - |

Part 3.9: CAN communication interface

There are 2 CAN communication interfaces on the AXU2CGB-E carrier board, which are connected to the MIO interface of the BANK501 on the PS system side. The CAN transceiver chip selected TI's SN65HVD232C chip for user CAN communication services. The connection of the CAN transceiver chip on the PS side is show as Figure 3-9-1

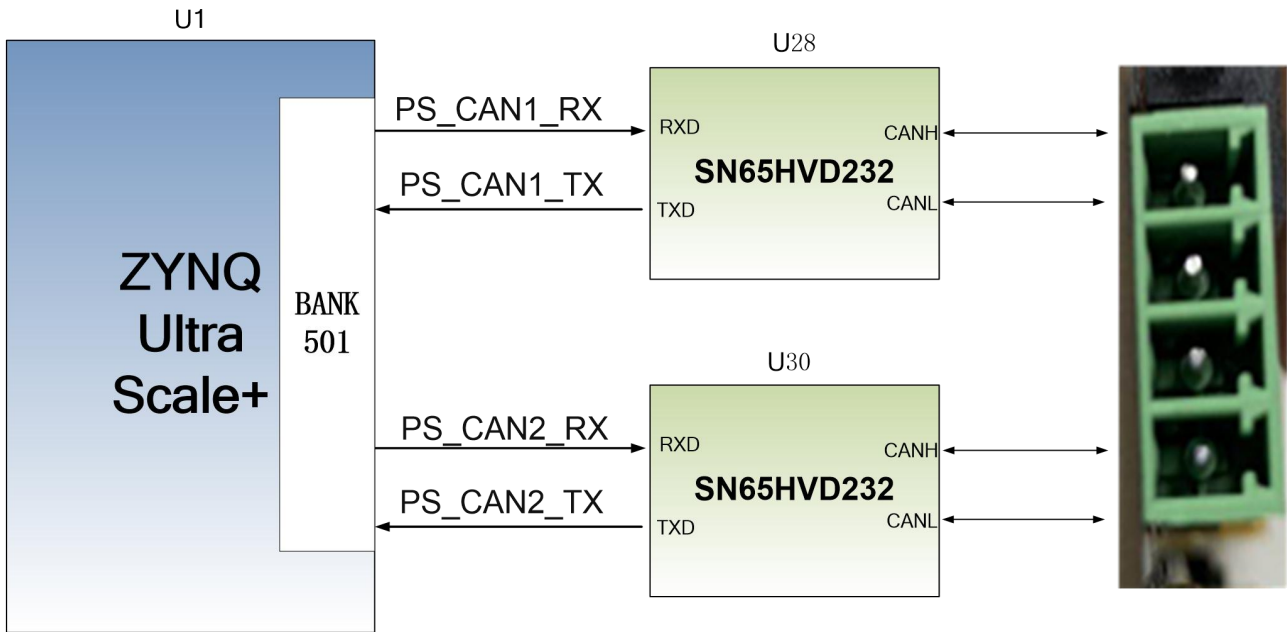


Figure 3-9-1: Connection diagram of CAN transceiver chip on PS side

The CAN communication pin assignments are as follows:

| Signal Name | ZYNQ Pin Name | ZYNQ Pin Number | Description |
|-------------|---------------|-----------------|------------------|
| PS_CAN1_TX | PS_MIO32 | J16 | CAN1 Receiver |
| PS_CAN1_RX | PS_MIO33 | L16 | CAN1 Transmitter |
| PS_CAN2_TX | PS_MIO39 | H19 | CAN2 Receiver |
| PS_CAN2_RX | PS_MIO38 | H18 | CAN2 Transmitter |

Part 3.10: 485 communication interface

There are two 485 communication interfaces on the AXU2CGB-E carrier board. The 485 communication port 1 is connected to the IO interface of BANK43~45 on the PL system. The 485 transceiver chip selects the MAX3485 chip from MAXIM for the user's 485 communication service.

Figure 3-10-1 is the connection diagram of the 485 transceiver chip on the PL side

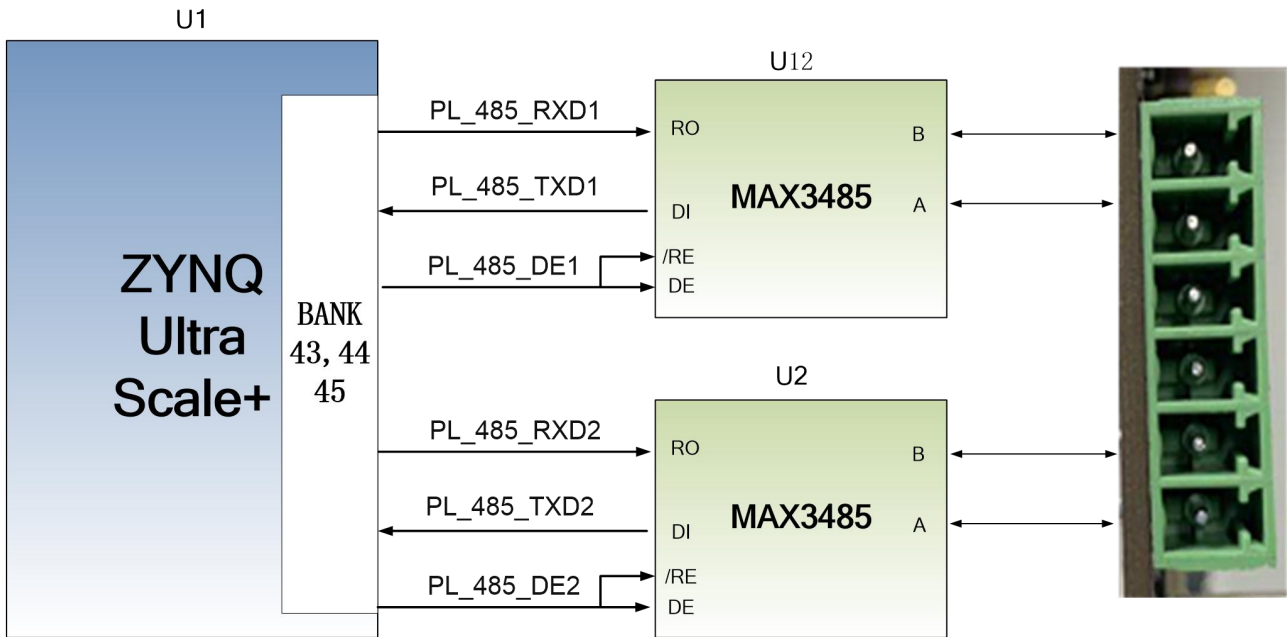


Figure 3-10-1: 485 Communication on the PL Side

The 485 communication pins are assigned as follows:

| Signal Name | Pin Name | Pin Number | Description |
|-------------|-----------|------------|---|
| PL_485_TXD1 | B43_L1_N | AH10 | The 1 st Channel 485 Transceiver |
| PL_485_RXD1 | B44_L4_P | AE13 | The 1 st Channel 485 Receiver |
| PL_485_DE1 | B45_L10_P | B11 | The 1 st Channel 485 Transmit Enable |
| PL_485_TXD2 | B43_L1_N | AG10 | The 2 nd Channel 485 Transceiver |
| PL_485_RXD2 | B44_L4_N | AF13 | The 2 nd Channel 485 Receiver |
| PL_485_DE2 | B45_L10_N | A10 | The 2 nd Channel 485 Transmit Enable |

Part 3.11: MIPI camera interface

The AXU2CGB-E carrier board includes a MIPI camera interface, which can be used to connect with the ALINX Brand MIPI OV5640 camera module AN5641. MIPI interface 15PIN FPC connector, 2 LANE data and 1 pair of clock, connected to the differential IO pin of BANK65, the level standard is 1.2V; other control signals are connected to the IO of BANK43, level standard It is 3.3V.

The circuit schematic of the MIPI interface part is shown in Figure 3-11-1

below:

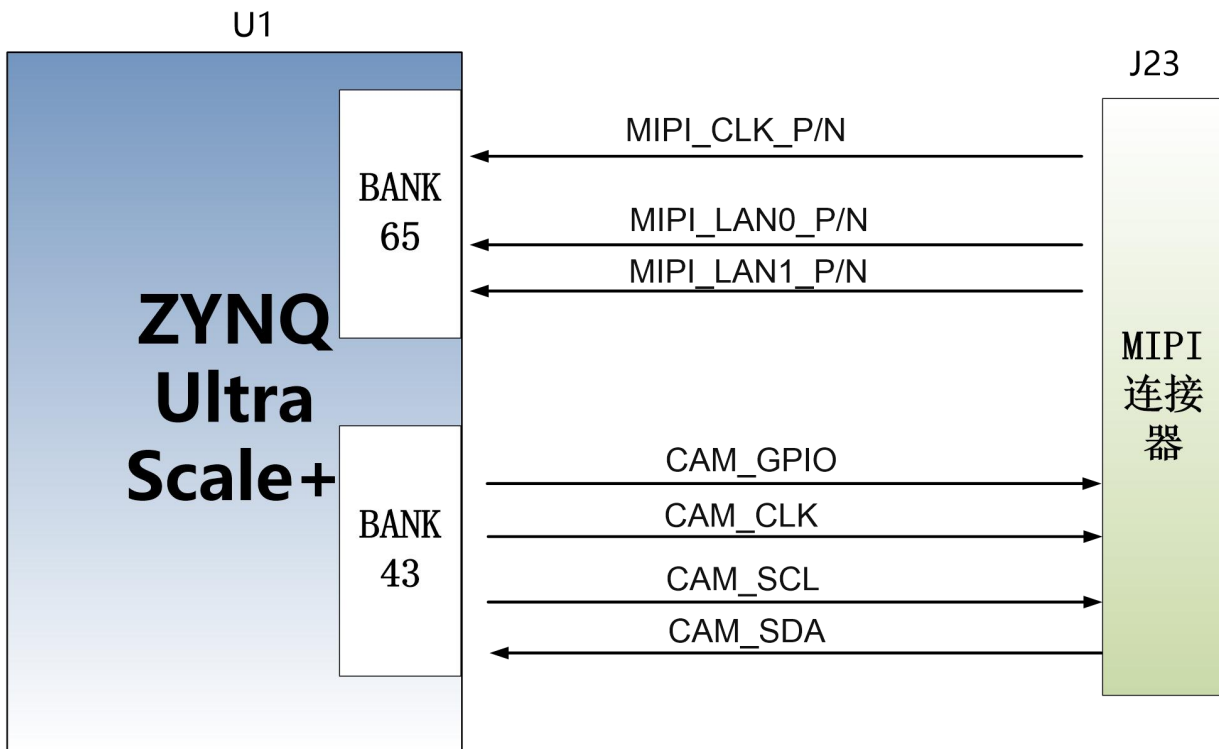


Figure 3-11-1: MIPI camera interface design schematic

MIPI interface pin assignment

| Signal Name | ZYNQ Pin Name | ZYNQ Pin Number | Description |
|-------------|---------------|-----------------|--------------------------------|
| MIPI_CLK_P | B65_L1_P | W8 | MIPI Input Clock Positive |
| MIPI_CLK_N | B65_L1_N | Y8 | MIPI Input Clock Negative |
| MIPI_LAN0_P | B65_L2_P | U9 | MIPI Input Data LANE0 Positive |
| MIPI_LAN0_N | B65_L2_N | V9 | MIPI Input Data LANE0 Negative |
| MIPI_LAN1_P | B65_L3_P | U8 | MIPI Input Data LANE1 Positive |
| MIPI_LAN1_N | B65_L3_N | V8 | MIPI Input Data LANE1 Negative |
| CAM_GPIO | B43_L4_P | AE10 | GPIO Control of Camera |
| CAM_CLK | B43_L4_N | AF10 | Clock Input of Camera |
| CAM_SCL | B43_L11_P | Y9 | I2C Clock of Camera |
| CAM_SDA | B43_L11_N | AA8 | I2C Data of Camera |

Part 3.12: JTAG Debug Port

The JTAG interface is reserved on the AXU2CGB-E expansion board for

downloading ZYNQ UltraScale+ programs or firmware programs to FLASH. In order to not damage the ZYNQ UltraScale+ chip by plugging and unplugging under power, we added a protection diode to the JTAG signal to ensure that the signal voltage is within the range accepted by the FPGA and avoid damage to the ZYNQ UltraScale+ chip.

JTAG Connector

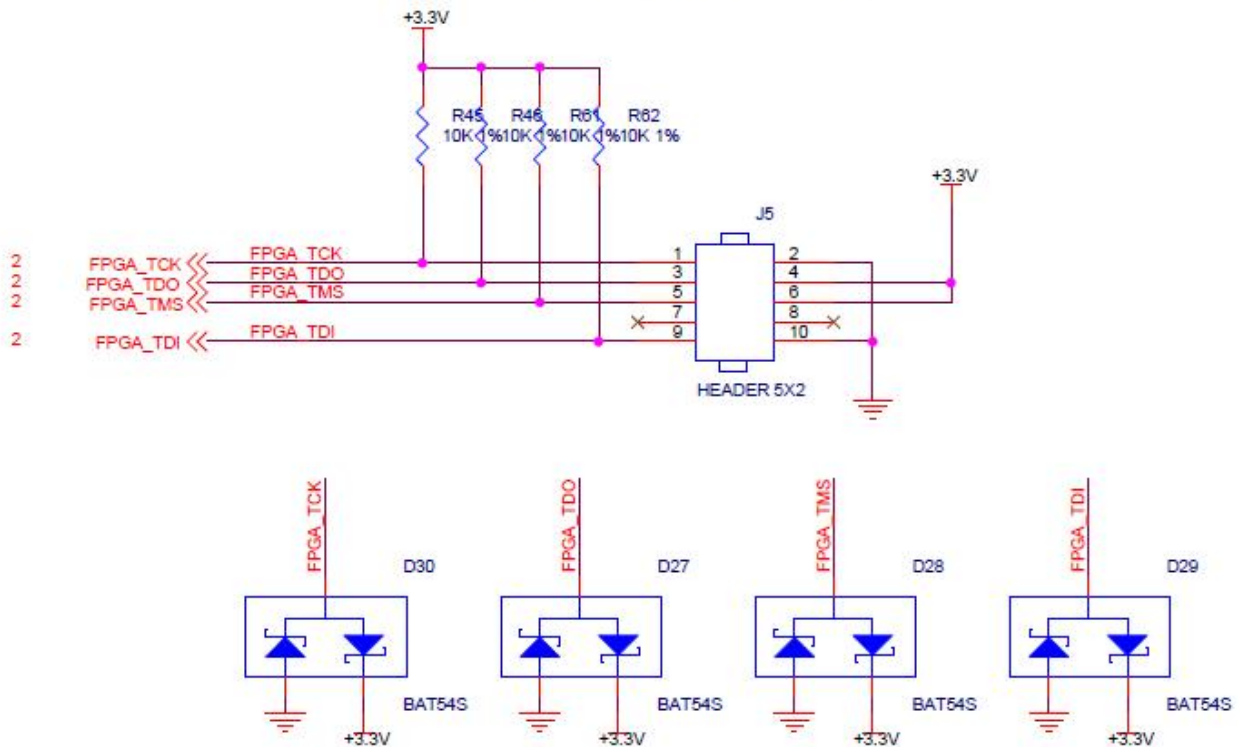


Figure 3-12-1: JTAG Interface Schematic

Part 3.13: Real-time clock

The ZU2CG chip has the function of an RTC real-time clock, with timing functions such as year, month, day, hour, minute, and second, and week. External need to connect a 32.768KHz passive clock to provide an accurate clock source to the internal clock circuit, so that the RTC can accurately provide clock information. At the same time, in order for the real-time clock to operate normally after the product is powered off, it is generally necessary to equip the coin battery (**model LR1130, voltage is 5V**) to supply power to the clock chip.

The BT1 on the development board is a battery Socket. After we put the coin battery, even the system is off, the coin battery can also power the RTC system and provide continuous time information.

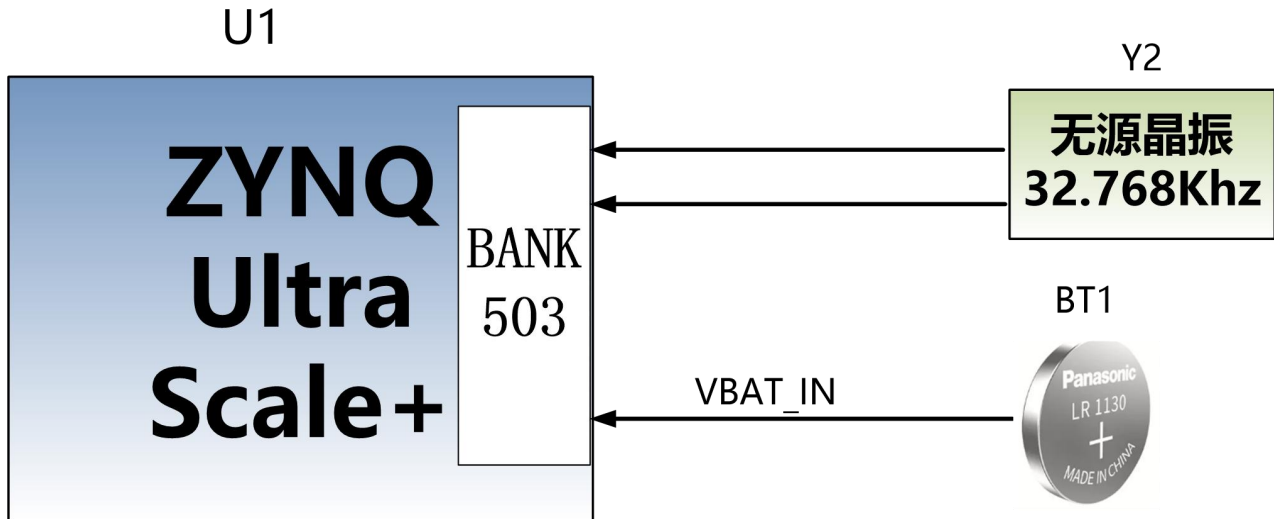


Figure 3-13-1: RTC Schematic

Part 3.14: EEPROM and Temperature sensor

The AXU2CGB-E Fpga development board has an EEPROM onboard. The model of the EEPROM is 24LC04, and the capacity is: 4Kbit ($2 * 256 * 8\text{bit}$), which is connected to the PS terminal through the IIC bus.

A high-precision, low-power, digital temperature sensor chip is installed on the AXU2CGB-E FPGA development board, and the model is LM75 from ON Semiconductor. The temperature accuracy of the LM75 chip is 0.5 degrees.

The EEPROM and temperature sensor are mounted on the Bank500 MIO of ZYNQ UltraScale+ through the I2C bus. Figure 3-14-1 is the schematic diagram of EEPROM and temperature sensor

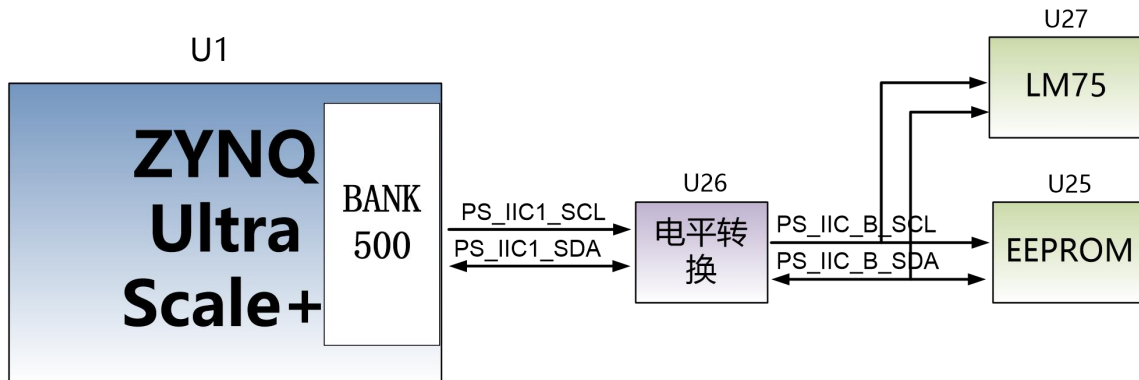


Figure 3-14-1: EEPROM and Sensor connection diagram

EEPROM pin assignment:

| Signal Name | ZYNQ Pin Name | ZYNQ Pin Number | Description |
|-------------|---------------|-----------------|------------------|
| PS_IIC1_SCL | PS_MIO24 | AB19 | IIC Clock Signal |
| PS_IIC1_SDA | PS_MIO25 | AB21 | IIC Data Signal |

Part 3.15: User LEDs

There are 3 LEDs on the AXU2CGB-E Carrier board. including 1 power indicator light, 1 User LED Controlled by PS side, and 1 User LED Controlled by PL side. The user can control the user LED on and off through the program. When the IO voltage of the connected user LED light is low, the user LED light is off, and when the connected IO voltage is high, the user LED will be lit. The schematic diagram of the user's LED light hardware connection is shown in Figure 3-15-1:

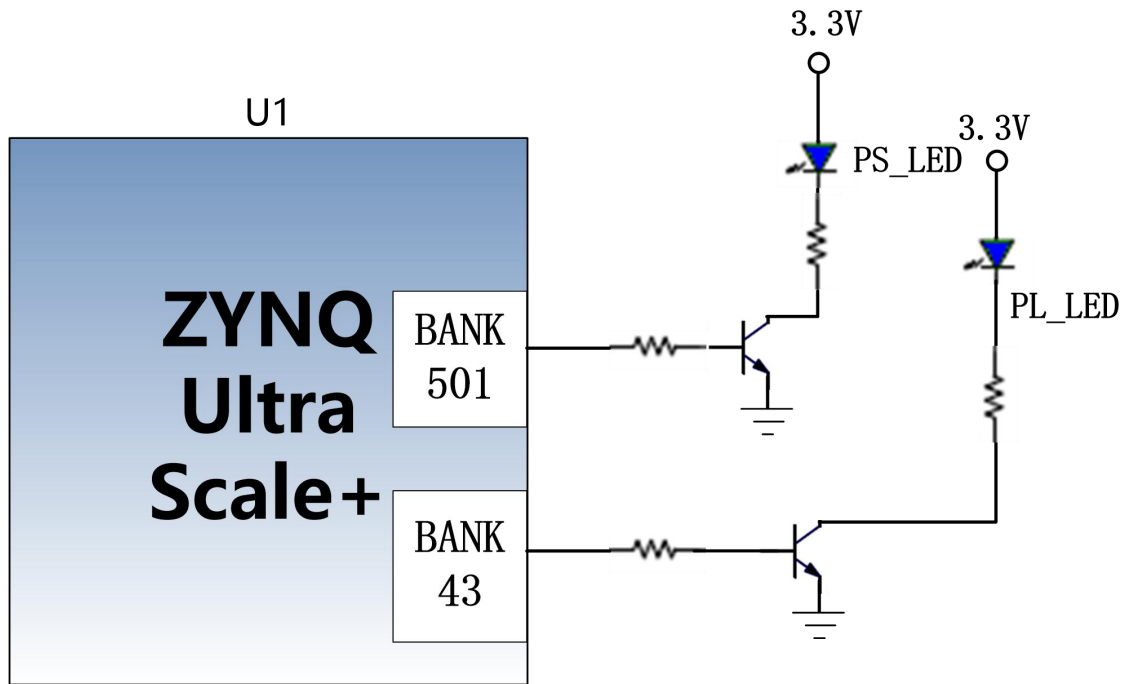


Figure 3-15-1: The User LEDs Hardware Connection Diagram

Pin assignment of user LED lights

| Signal Name | ZYNQ Pin Name | ZYNQ Pin Number | Description |
|-------------|---------------|-----------------|---------------------------|
| PS_LED1 | PS_MIO40 | K18 | User LED controlled by PS |
| PL_LED1 | B43_L5_P | AE12 | User LED controlled by PL |

Part 3.16: Keys

There are 1 reset KEY RESET and 2 user buttons on the AXU2CGB-E carrier board. The reset signal is connected to the reset chip input of the core board ACU3EG, and the user can use this reset KEY to reset the ZYNQ system. One user KEY is connected to the MIO of the PS, and one is connected to the IO of the PL. The reset KEY and the user KEYS are both low-level active. The connection diagram of the user key is shown in Figure 3-16-1:

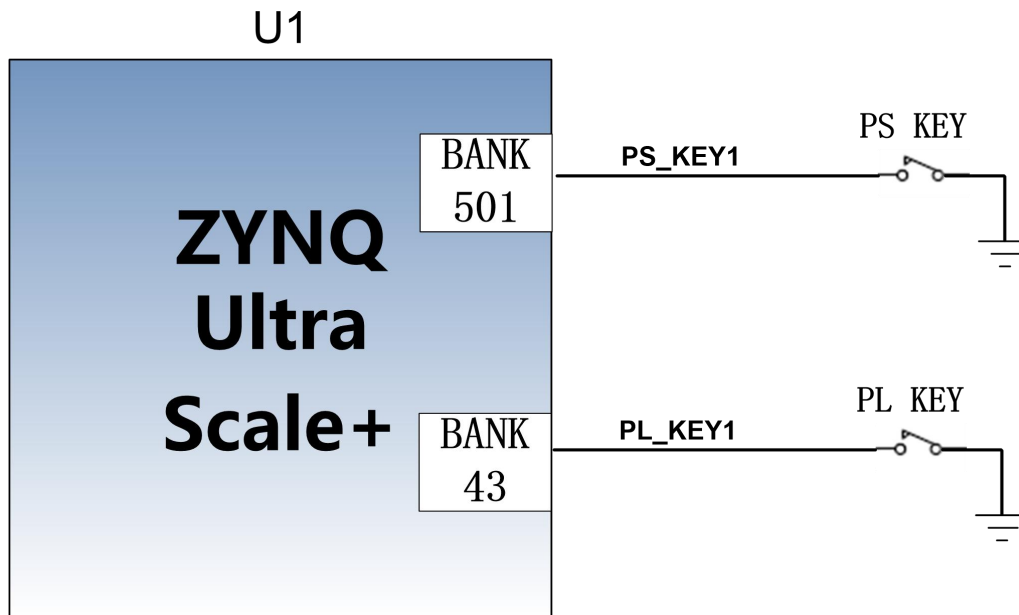


Figure 3-16-1: Rest keys connection diagram

ZYNQ pin assignment of keys

| Signal Name | ZYNQ Pin Name | ZYNQ Pin Number | Description |
|-------------|---------------|-----------------|---------------|
| PS_KEY1 | PS_MIO26 | L15 | PS KEY1 Input |
| PL_KEY1 | B43_L5_N | AF12 | PL KEY1 Input |

Part 3.17: DIP Switch Configuration

There is a 4-digit DIP switch SW1 on the FPGA development board to configure the startup mode of the ZYNQ system. The AXU2CGB-E system development platform supports 4 startup modes. The 4 startup modes are JTAG debug mode, QSPI FLASH, EMMC and SD2.0 card startup mode. After ZU2CG chip is powered on, it will detect the level of (PS_MODE0~3) to determine the startup mode. The user can select different startup modes through the DIP switch SW1 on the expansion board. The SW1 startup mode configuration is shown in the following table 3-17-1.

| SW1 | Dial Position (1, 2, 3, 4) | MODE[3:0] | Start mode |
|-----|----------------------------|-----------|------------|
|-----|----------------------------|-----------|------------|

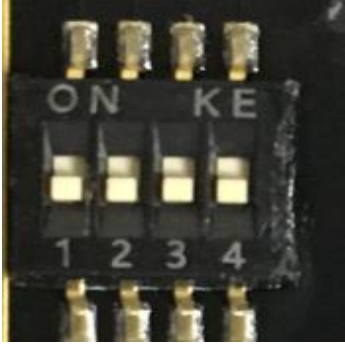
| | | | |
|---|------------------|------|------------|
|  | ON, ON, ON, ON | 0000 | PS JTAG |
| | ON, ON, OFF, ON | 0010 | QSPI FLASH |
| | ON, OFF, ON, OFF | 0101 | SD Card |
| | ON, OFF, OFF, ON | 0110 | EMMC |

Table 3-17-1

Part 3.18: Power Supply

The power input voltage of the AXU2CGB-E development board is DC12V. In the carrier board, the DC12V is converted into +5V, +3.3V, and +1.8V through one-way DC/DC power chip TPS54620 and two-way DC/DC power chip MP1482. In addition, the Carrier board generates +1.2V through LDO to supply power to the core board BANK65, and the power supply of BANK66 is +1.8V. The schematic diagram of the power supply design on the board is shown in Figure 3-18-1:

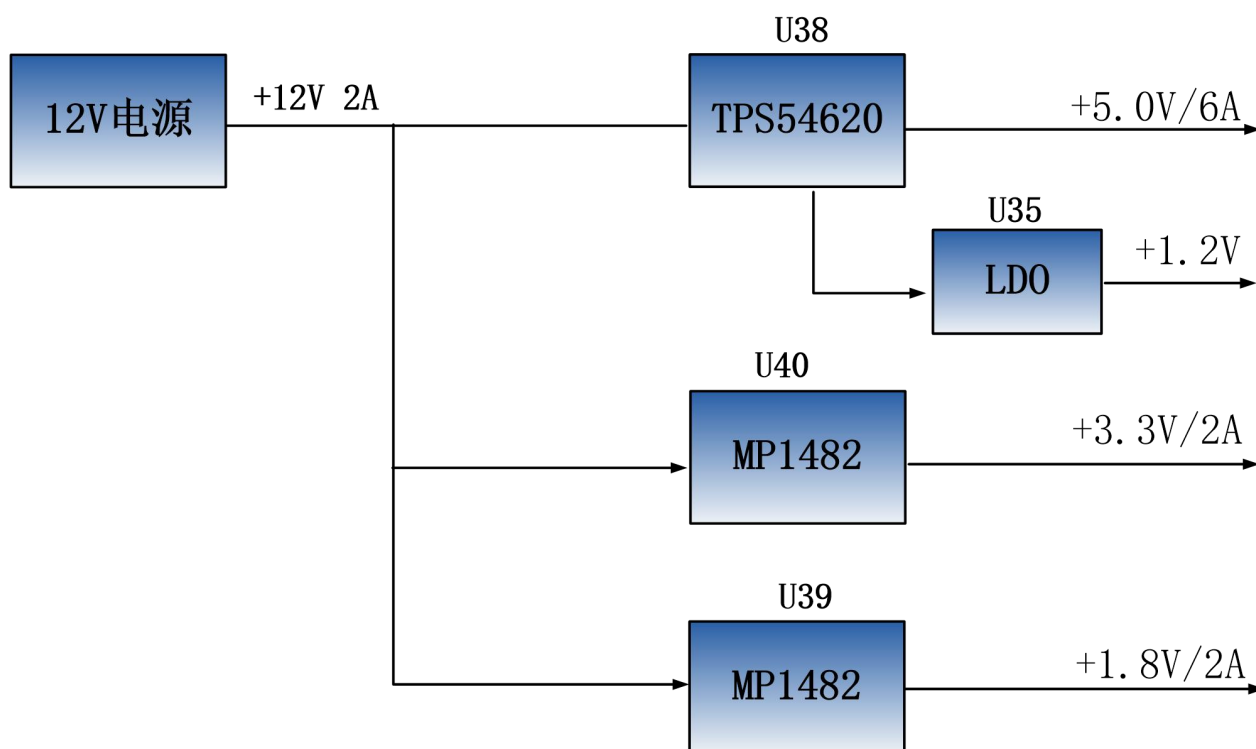


Figure 3-18-1: Carrier Board Power Schematic

The functions of each power distribution are shown in the following table:

| Power | Function |
|-------|--|
| +5.0V | USB power supply |
| +1.8V | Ethernet, USB2.0, BANK66 of Core Board |
| +3.3V | Ethernet, USB2.0, SD, DP, CAN, RS485 |
| +1.2V | BANK65 of Core Board |

Part 3.19: ALINX Customized Fan

Because AXU2CGB-E generates a lot of heat when it works normally, we add a heat sink and fan to the chip on the board to prevent the chip from overheating. The control of the fan is controlled by the ZYNQ chip. The control pin is connected to the IO of the BANK43 (AA11). If the IO level output is high, the MOSFET is turned on and the fan is working. If the IO level output is low, the fan stops. The fan design on the board is shown in Figure 3-19-1.

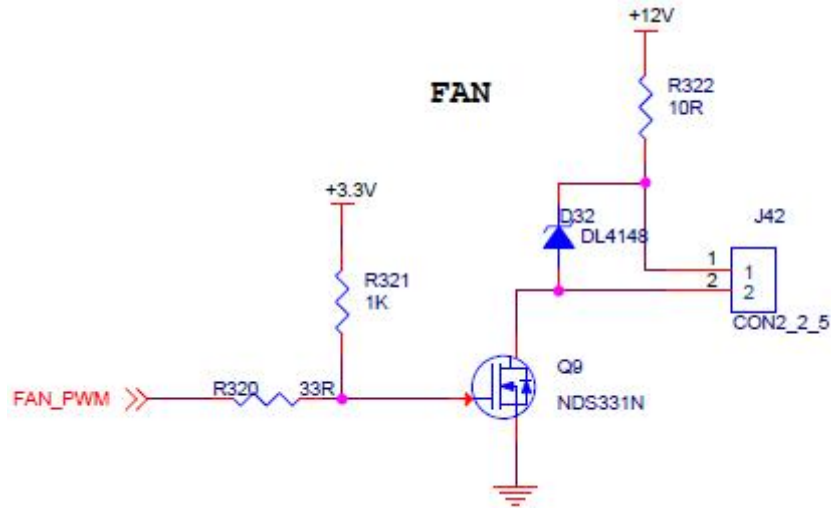


Figure 3-19-1: Fan Design Schematic

The fan has been screwed to the AXU2CGB-E FPGA development board before leaving the factory. The power of the fan is connected to the socket of J24. The red is positive and the black is negative.

Part 3.20: Carrier Board Size Dimension

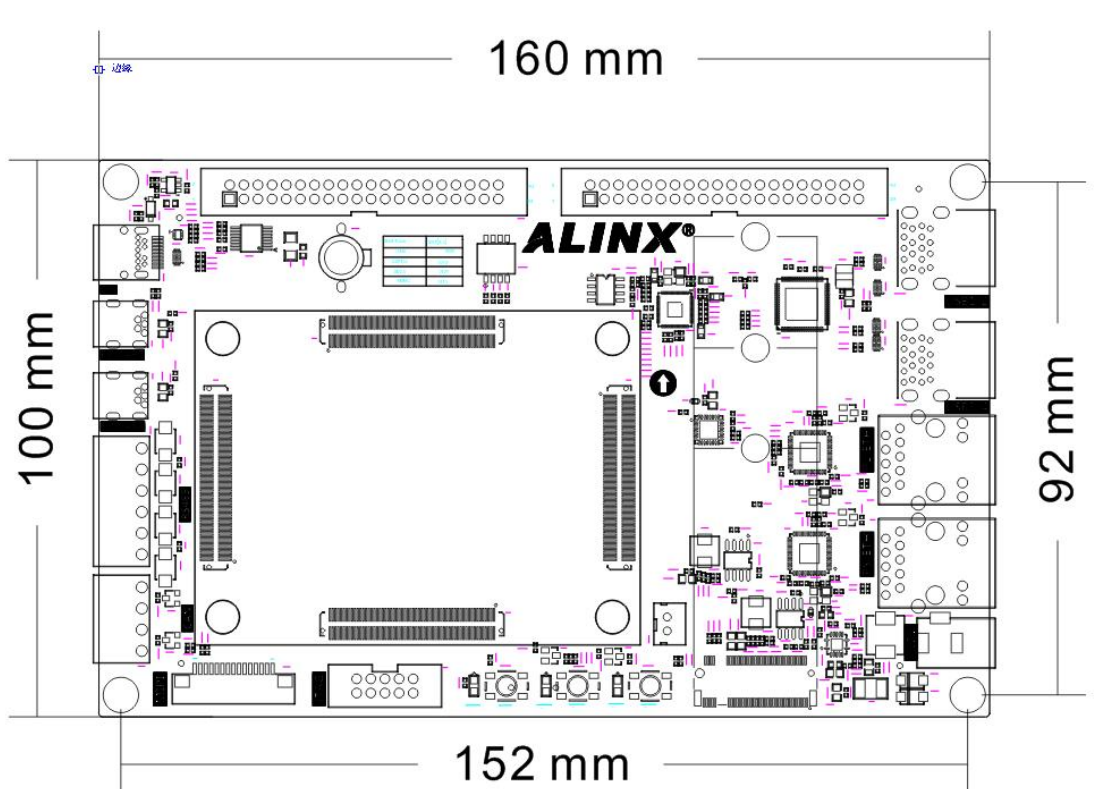


Figure 3-20-1: Top View