FH1219 Module
User Manual

Rev 1.0

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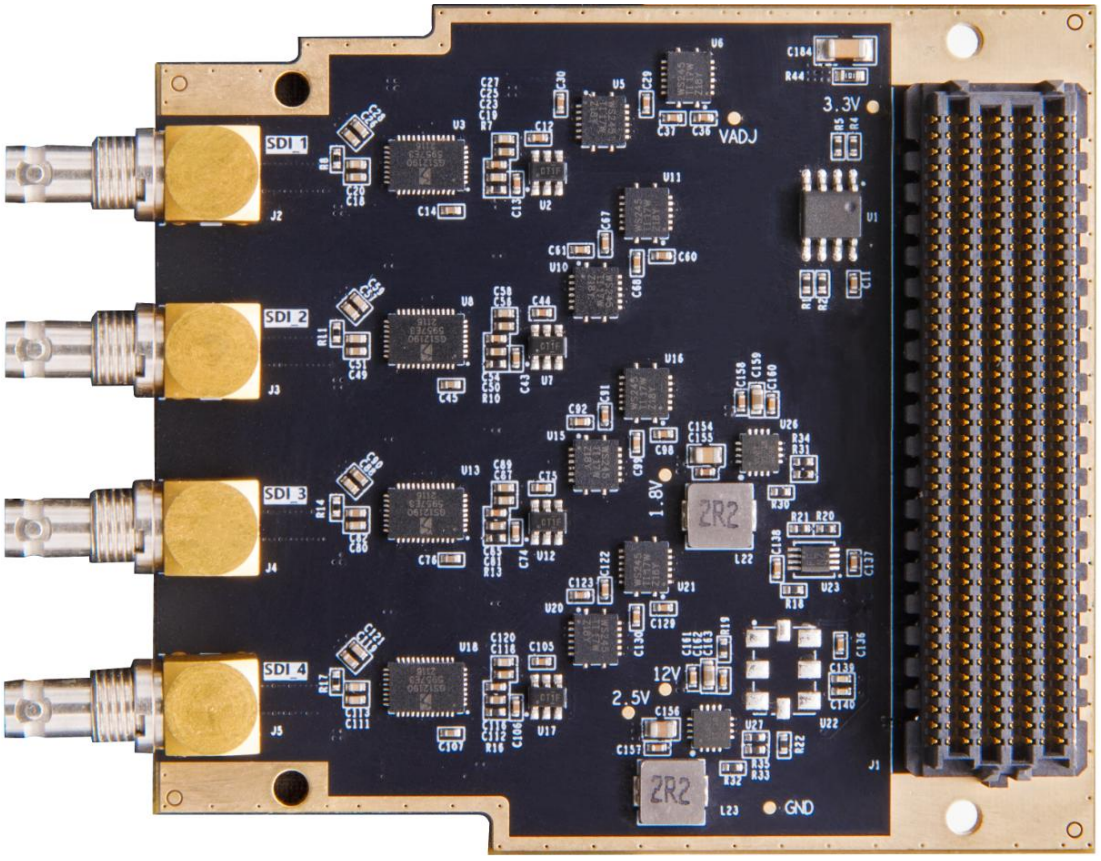
1.0	2022/11/11	First Release

Part 1 Introduction of FMC Module FH1219

There are four 12G SDI interfaces in FH1219, each of which can be configured as an input or output separately. Each SDI supports a data rate of up to 11.88 Gbps, and the input and output of four SDI video signals are connected to the HDBNC connector (model: HDBNC-J-P-GN-RA-BH1) through a 75 ohm wiring impedance. Using SEMTECH's bidirectional 12G UHD-SDI chip GS12190 to achieve SDI clock recovery, signal driving, and signal equalization, the output SDI signal and the recovered SDI signal are connected to the FPGA's GTX/GTH transceiver through the FMC HPC connector (model: ASP-134488-01).

The picture of FH1219 module is as follows:



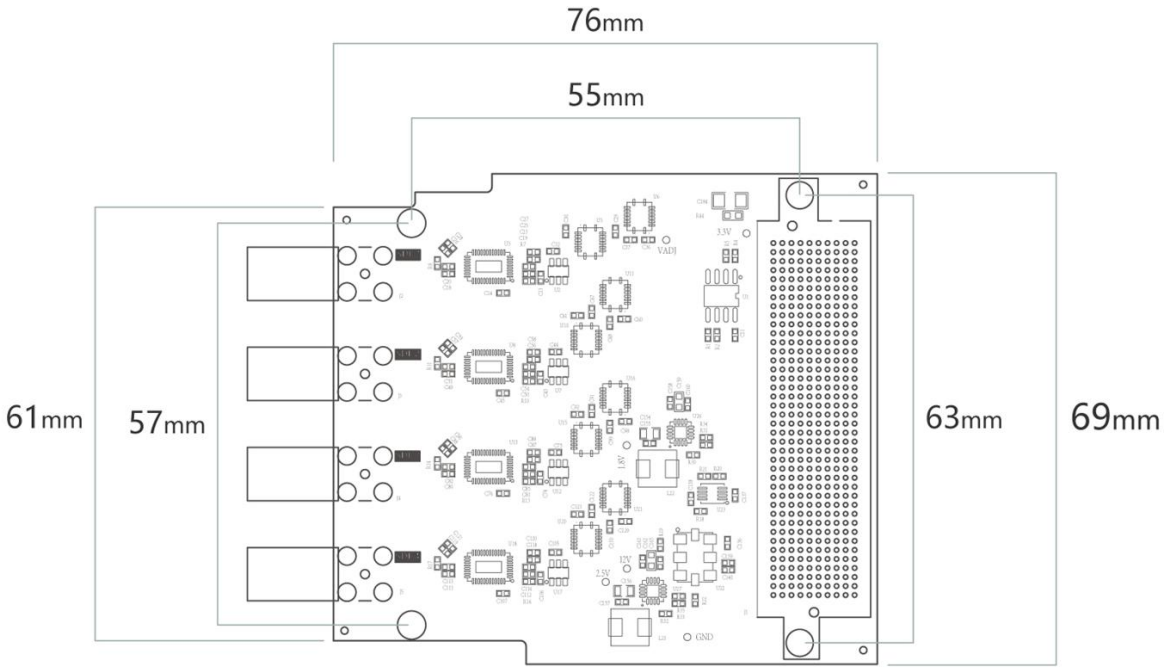
Module FH1219

1.1 Parameters of Module FH1219

The following are the detailed parameters of the FH1219 module:

- Support 4-way bidirectional SDI, support SD/HD/3G/6G/12G SDI rate, and support up to 4K/60 frames of video input or output
- 4 HDBNC SDI interfaces
- FMC HPC interface, compatible with ANSI/VITA57.1 FMC standard
- Two reference clocks 148.5Mhz and 148.35Mhz
- Industrial grade, operating temperature -40°C~85°C

1.2 Structure diagram of the Module FH1219

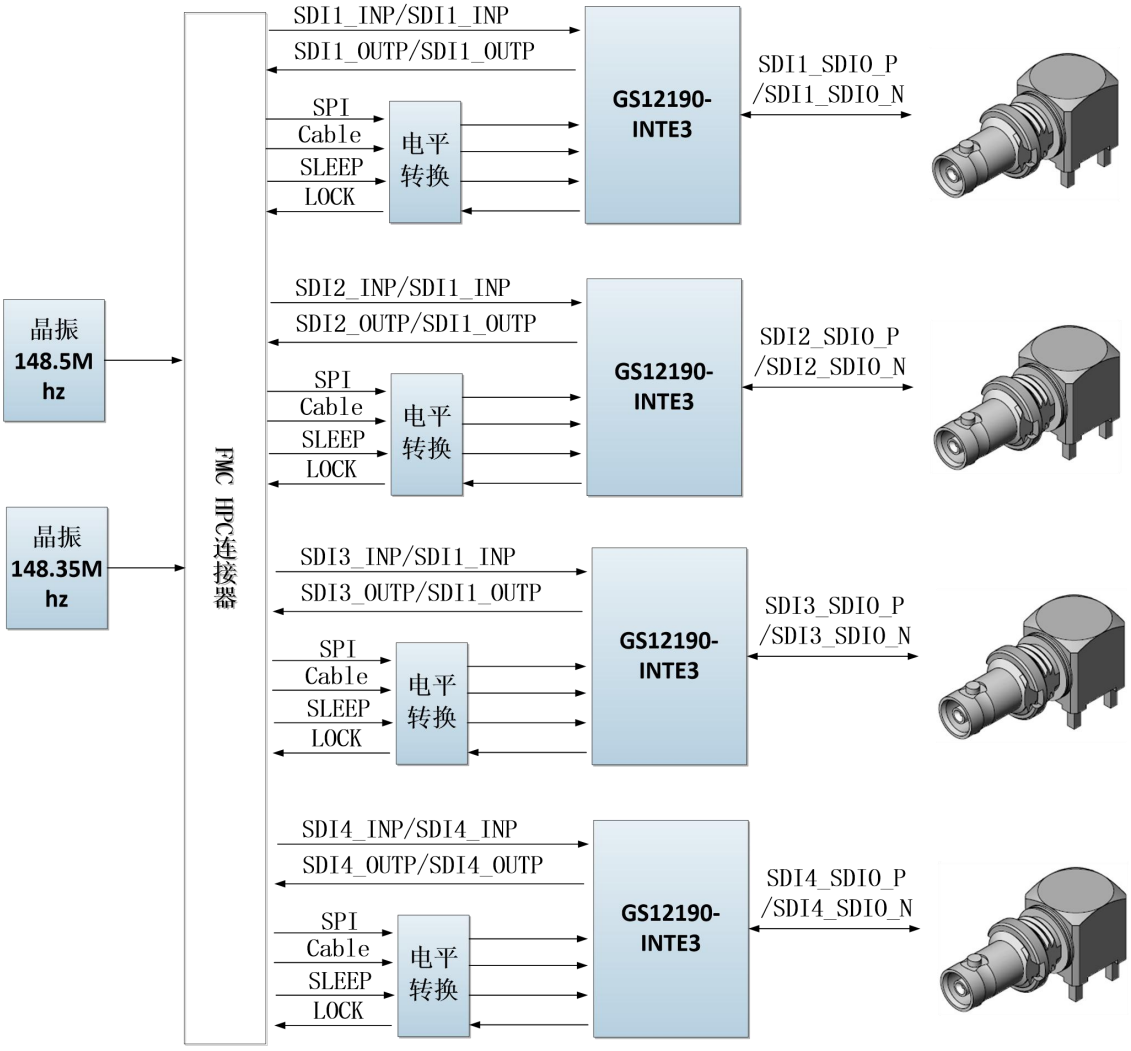


Structure diagram of the module FH1219

Part 2 Module Function Description

2.1 Schematic Diagram of Module FH1219

The schematic design diagram of the module FH1219 is as follows:



2.2 Pin assignment for module FMC HPC:

The following only lists the signals of the power supply and interface, and the signals of GND are not listed. For specific users, please refer to the schematic diagram.

Pin No.	Signal Name	Description
C30	FMC_SCL	FMC I2C Clock
C31	FMC_SDA	FMC I2C Data
C34	GA0	EEPROM Address Selection A0

C35	+12V	Power supply 12V
C37	+12V	Power supply 12V
D4	FMC_GBTCLK0_M2C_P	Transceiver reference clock 0 input P
D5	FMC_GBTCLK0_M2C_N	Transceiver reference clock 0 input N
D8	SDI_CLK1_P	SDI reference clock 0 input P
D9	SDI_CLK1_N	SDI reference clock 0 input N
D11	FMC_570_SDA	SI570 clock chip I2C data
D12	FMC_570_SCL	SI570 clock chip I2C clock
D20	FMC_REC_CLOCK_P	SDI reference clock FPGA output P
D21	FMC_REC_CLOCK_N	SDI reference clock FPGA output N
D29	FMC_TCK	FMC JTAG TCK
D30	FMC_TDI	FMC JTAG TDI
D31	FMC_TDO	FMC JTAG TDO
D32	+3.3V	Power supply 3.3V
D33	FMC_TMS	FMC JTAG TMS
D35	GA1	EEPROM address selection A1
G6	SDI_CLK0_P	SDI reference clock 0 input P
G7	SDI_CLK0_N	SDI reference clock 0 input N
G9	FMC_SDI4_CS	SPI film selection for the fourth SDI
G10	FMC_SDI4_SDIN	SPI data input for the fourth SDI
G12	FMC_SDI4_LOS	Loss signal of the fourth SDI
G13	FMC_SDI4_LOCK	Lock signal of the fourth SDI
G15	FMC_SDI3_CS	SPI Film Selection for Third SDI
G16	FMC_SDI3_SDIN	SPI data input for the third SDI
G18	FMC_SDI3_LOS	Loss signal of the third SDI
G19	FMC_SDI3_LOCK	Lock signal of the third SDI
G21	FMC_SDI2_CS	SPI film selection for the second SDI
G22	FMC_SDI2_SDIN	SPI data input for the second SDI
G24	FMC_SDI2_LOS	Loss signal of the second SDI
G25	FMC_SDI2_LOCK	Lock signal of the second SDI
G27	FMC_SDI1_CS	SPI Film Selection for First SDI
G28	FMC_SDI1_SDIN	SPI data input for the first SDI
G30	FMC_SDI1_LOS	Loss signal of the first SDI
G31	FMC_SDI1_LOCK	Lock signal of the first SDI
G39	VADJ	Power supply VADJ
H2	GND	GND
H7	FMC_SDI4_CABLE	Input and output selection of the fourth SDI
H8	FMC_SDI4_SLEEP	Sleep mode selection for the fourth SDI
H10	FMC_SDI4_SCLK	Clock of SPI of the fourth SDI
H11	FMC_SDI4_SDOUT	SPI data output of the fourth SDI
H13	FMC_SDI3_CABLE	Input and output selection of the third SDI
H14	FMC_SDI3_SLEEP	Sleep mode selection for the third SDI
H16	FMC_SDI3_SCLK	SPI time of the third SDI

H17	FMC_SDI3_SDOUT	SPI data output of the third SDI
H19	FMC_SDI2_CABLE	Input and output selection of the second SDI
H20	FMC_SDI2_SLEEP	Sleep mode selection for the second SDI
H22	FMC_SDI2_SCLK	Clock of SPI for the second SDI
H23	FMC_SDI2_SDOUT	SPI data output of the second SDI
H25	FMC_SDI1_CABLE	Input and output selection of the first SDI
H26	FMC_SDI1_SLEEP	Sleep mode selection for the first SDI
H28	FMC_SDI1_SCLK	SPI clock from the first SDI
H29	FMC_SDI1_SDOUT	SPI data output of the first SDI
H40	VADJ	Power supply VADJ
A2	FMC_DP1_M2C_P	Not used
A3	FMC_DP1_M2C_N	Not used
A6	FMC_DP2_M2C_P	Not used
A7	FMC_DP2_M2C_N	Not used
A10	FMC_DP3_M2C_P	Not used
A11	FMC_DP3_M2C_N	Not used
A14	SDI3_OUTP	Data output from the third SDI P
A15	SDI3_OUTN	Data output from the third SDI N
A18	SDI1_OUTP	Data input from the first SDI P
A19	SDI1_OUTN	Data input from the first SDI N
A22	FMC_DP1_C2M_P	Not used
A23	FMC_DP1_C2M_N	Not used
A26	FMC_DP2_C2M_P	Not used
A27	FMC_DP2_C2M_N	Not used
A30	FMC_DP3_C2M_P	Not used
A31	FMC_DP3_C2M_N	Not used
A34	SDI3_INP	Data input from the third SDI P
A35	SDI3_INN	Data output from the third SDI N
A38	SDI1_INP	Data input from the first SDI P
A39	SDI1_INN	Data output from the first SDI N
B12	SDI4_OUTP	Data input from the fourth SDI P
B13	SDI4_OUTN	Data input from the fourth SDI N
B16	SDI2_OUTP	Data input from the second SDI P
B17	SDI2_OUTN	Data input from the second SDI N
B20	FMC_GBTCLK1_M2C_P	Input Transceiver reference clock 1 P
B21	FMC_GBTCLK1_M2C_N	Input Transceiver reference clock 1 N
B32	SDI4_INP	Data output from the fourth SDI P
B33	SDI4_INN	Data output from the fourth SDI N
B36	SDI2_INP	Data input from the second SDI P
B37	SDI2_INN	Data output from the second SDI N