FH1226 Module
User Manual

Rev 1.0

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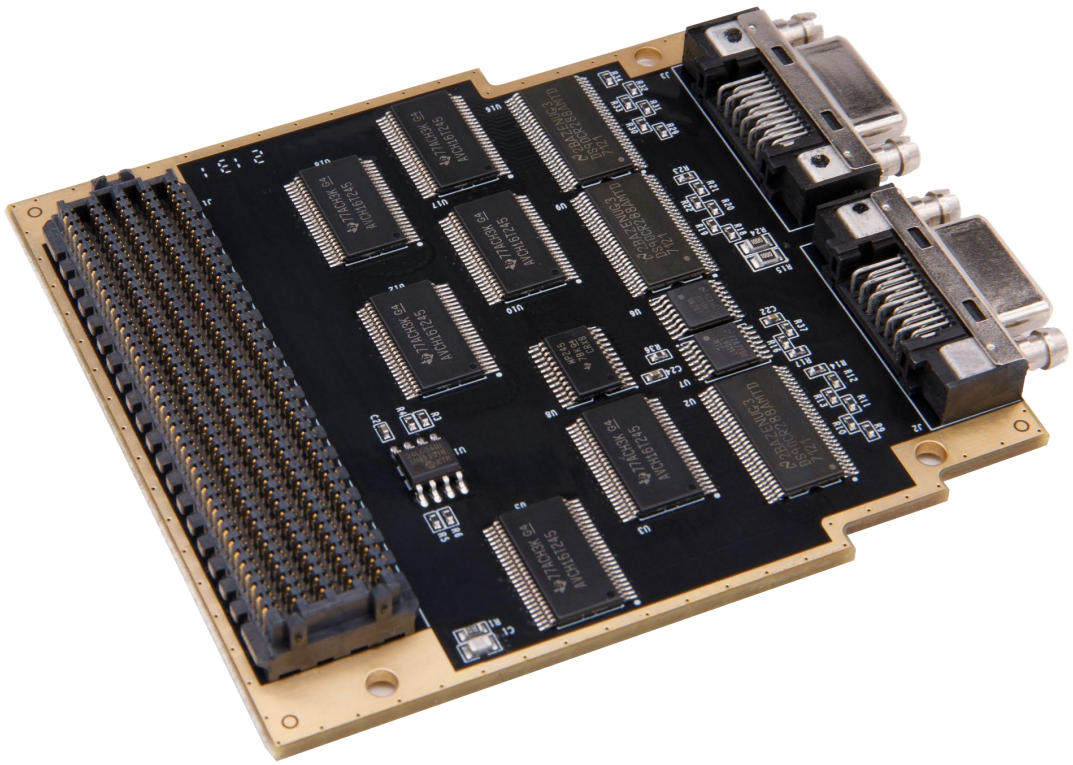
1.0	2022/11/11	First Release

Part 1 Introduction of FMC Module FH1226

The FH1226 supports two standard Camera Link interfaces. At the same time, it supports Base, Medium and Full modes, providing suitable configuration and connection methods for cameras with different speeds. By using DS90CR288A chip, FH1226 converts 4 pairs of LDVS serial data to 28-bit parallel data, the throughput is up to 2.38Gbps. Through the Camera Link interface, the real-time images are transmitted to the FPGA image acquisition card at high speed for real-time data processing, which better provides applications for digital cameras and data acquisition cards.

The picture of module FH1226 is as follows:



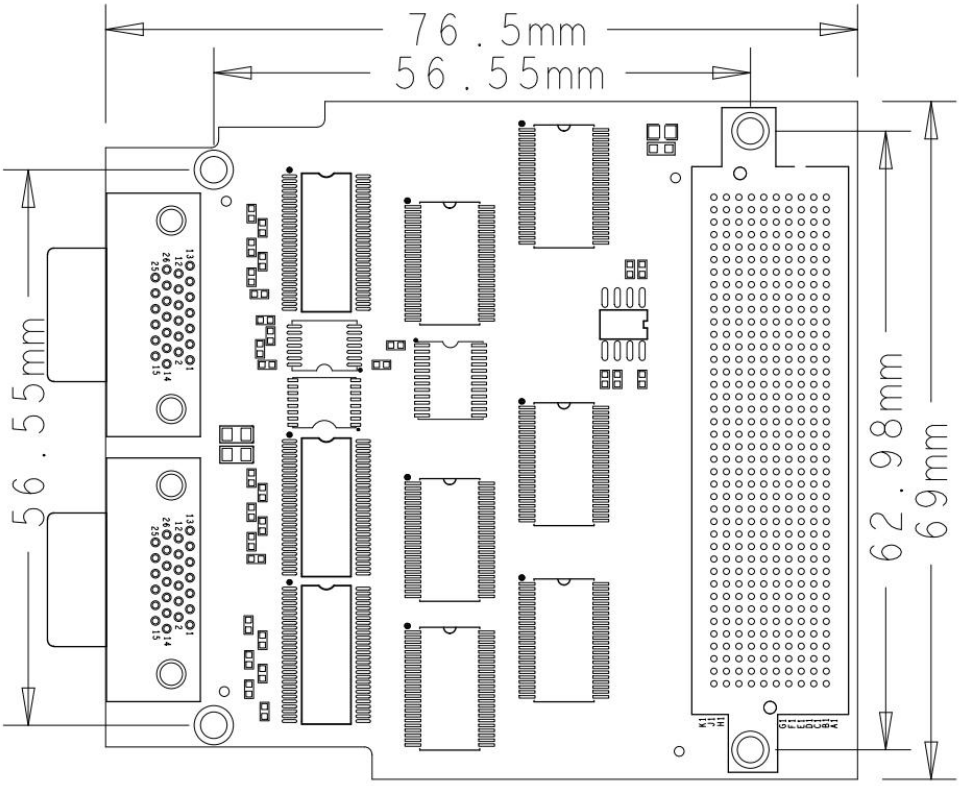
Module FH1226

1.1 Parameters of Module FH1226

The following are the detailed parameters of the module FH1226:

- Support standard Camera Link mode (Base, Medium, Full)
- Camera Link Interface: 2 channels
- 3 LVDS 28-bit channel chips (DS90CR288A)
- LVDS 28-bit data bits, supporting clock conversion from 20 MHZ to 85MHz
- Throughput up to 2.38Gbps
- Bandwidth up to 297.5 Mbytes/sec
- Compatible with TIA/EIA-644 LVDS standard
- Storage temperature -65~150°C, working temperature -10~70°C

1.2 Structure Diagram of Module FH1226

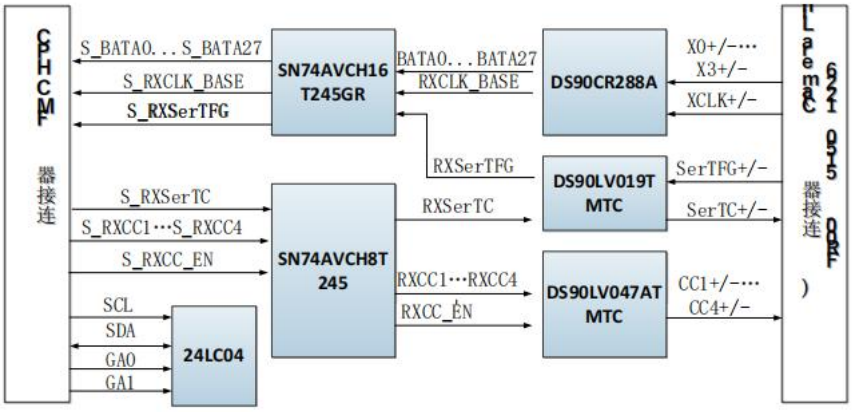


Structure diagram of the module FH1226

Part 2 Functions of Module FH1226

2.1 Schematic Diagram of Module FH1226

The schematic design diagram of the module FH1226 is as follows:



The schematic diagram provided for the specific reference for the complete circuit of the module FH1226.

2.2 Pin assignment of module FMC HPC:

The following only lists the signals of the power supply and interface, and the signals of GND are not listed. For specific information, please refer to the schematic diagram.

Pin No.	Signal Name	Description
C35、C37	12V	Power supply
C39、D32 D36、D38、D40	3.3V	Power supply
E39、F40、 G39、H40	VADJ	Power supply
G22	S_RX_BASE0	TTL level BASE0 data input
H22	S_RX_BASE1	TTL level BASE1 data input
D23	S_RX_BASE2	TTL level BASE2 data input
H23	S_RX_BASE3	TTL level BASE3 data input
D24	S_RX_BASE4	TTL level BASE4 data input
G24	S_RX_BASE5	TTL level BASE5 data input
C26	S_RX_BASE6	TTL level BASE6 data input
D26	S_RX_BASE7	TTL level BASE7 data input
H25	S_RX_BASE8	TTL level BASE8 data input
G25	S_RX_BASE9	TTL level BASE9 data input

H26	S_RX_BASE10	TTL level BASE10 data input
C27	S_RX_BASE11	TTL level BASE11 data input
D27	S_RX_BASE12	TTL level BASE12 data input
G27	S_RX_BASE13	TTL level BASE013 data input
G28	S_RX_BASE14	TTL level BASE14 data input
H28	S_RX_BASE15	TTL level BASE15 data input
G30	S_RX_BASE16	TTL level BASE16 data input
G31	S_RX_BASE17	TTL level BASE17 data input
H31	S_RX_BASE18	TTL level BASE18 data input
H32	S_RX_BASE19	TTL level BASE19 data input
G33	S_RX_BASE20	TTL level BASE20 data input
G34	S_RX_BASE21	TTL level BASE21 data input
H34	S_RX_BASE22	TTL level BASE22 data input
H35	S_RX_BASE23	TTL level BASE23 data input
G36	S_RX_BASE24	TTL level BASE24 data input
G37	S_RX_BASE25	TTL level BASE25 data input
H37	S_RX_BASE26	TTL level BASE26 data input
H38	S_RX_BASE27	TTL level BASE27 data input
C22	S_RXCLK_BASE	TTL level BASE clock data input
H29	S_RXSerTFG	Input serial signal
C23	S_RXSerTC	Output serial signal
G2	S_RXCC1	Output control signal CC1
D20	S_RXCC2	Output control signal CC2
D21	S_RXCC3	Output control signal CC3
G21	S_RXCC4	Output control signal CC3
G3	S_RXCC_EN	CC enable signal
D8	S_RX_MEDIUM0	TTL level MEDIUM0 data input
G6	S_RX_MEDIUM1	TTL level MEDIUM1 data input
G7	S_RX_MEDIUM2	TTL level MEDIUM2 data input
H7	S_RX_MEDIUM3	TTL level MEDIUM3 data input
D9	S_RX_MEDIUM4	TTL level MEDIUM4 data input
H8	S_RX_MEDIUM5	TTL level MEDIUM5 data input
C10	S_RX_MEDIUM6	TTL level MEDIUM6 data input
G9	S_RX_MEDIUM7	TTL level MEDIUM7 data input
G10	S_RX_MEDIUM8	TTL level MEDIUM8 data input
H10	S_RX_MEDIUM9	TTL level MEDIUM9 data input
C11	S_RX_MEDIUM10	TTL level MEDIUM10 data input
C11	S_RX_MEDIUM11	TTL level MEDIUM11 data input
D11	S_RX_MEDIUM12	TTL level MEDIUM12 data input
D12	S_RX_MEDIUM13	TTL level MEDIUM13 data input
G12	S_RX_MEDIUM14	TTL level MEDIUM14 data input
G13	S_RX_MEDIUM15	TTL level MEDIUM15 data input
H16	S_RX_MEDIUM16	TTL level MEDIUM16 data input

H17	S_RX_MEDIUM17	TTL level MEDIUM17 data input
G16	S_RX_MEDIUM18	TTL level MEDIUM18 data input
G18	S_RX_MEDIUM19	TTL level MEDIUM19 data input
D17	S_RX_MEDIUM20	TTL level MEDIUM20 data input
D18	S_RX_MEDIUM21	TTL level MEDIUM21 data input
C15	S_RX_MEDIUM22	TTL level MEDIUM22 data input
D15	S_RX_MEDIUM23	TTL level MEDIUM23 data input
C14	S_RX_MEDIUM24	TTL level MEDIUM24 data input
D14	S_RX_MEDIUM25	TTL level MEDIUM25 data input
H14	S_RX_MEDIUM26	TTL level MEDIUM26 data input
H13	S_RX_MEDIUM27	TTL level MEDIUM27 data input
H4	S_RXCLK_MEDIUM	TTL level MEDIUM clock data input
H20	S_RX2SerTFG	Input serial signal
H19	S_RX2SerTC	Output serial signal
C19	S_RX2CC1	Output control signal CC1
C18	S_RX2CC2	Output control signal CC2
G15	S_RX2CC3	Output control signal CC3
H5	S_RX2CC4	Output control signal CC3
G19	S_RX2CC_EN	CC enable signal
E6	S_RX_Full0	TTL level Full0 data input
E7	S_RX_Full1	TTL level Full1 data input
E9	S_RX_Full2	TTL level Full2 data input
E10	S_RX_Full3	TTL level Full3 data input
F7	S_RX_Full4	TTL level Full4 data input
F8	S_RX_Full5	TTL level Full5 data input
J6	S_RX_Full6	TTL level Full6 data input
J7	S_RX_Full7	TTL level Full7 data input
K7	S_RX_Full8	TTL level Full8 data input
K8	S_RX_Full9	TTL level Full9 data input
E12	S_RX_Full10	TTL level Full10 data input
E13	S_RX_Full11	TTL level Full11 data input
J9	S_RX_Full12	TTL level Full12 data input
J10	S_RX_Full13	TTL level Full13 data input
K10	S_RX_Full14	TTL level Full14 data input
K11	S_RX_Full15	TTL level Full15 data input
F13	S_RX_Full16	TTL level Full16 data input
F14	S_RX_Full17	TTL level Full17 data input
J15	S_RX_Full18	TTL level Full18 data input
J16	S_RX_Full19	TTL level Full19 data input
F16	S_RX_Full20	TTL level Full20 data input
F17	S_RX_Full21	TTL level Full21 data input
K14	S_RX_Full22	TTL level Full22 data input
K13	S_RX_Full23	TTL level Full23 data input

J13	S_RX_Full24	TTL level Full24 data input
J12	S_RX_Full25	TTL level Full25 data input
F11	S_RX_Full26	TTL level Full26 data input
F10	S_RX_Full27	TTL level Full27 data input
F4	S_RX_FullCLK	TTL level Full clock data input