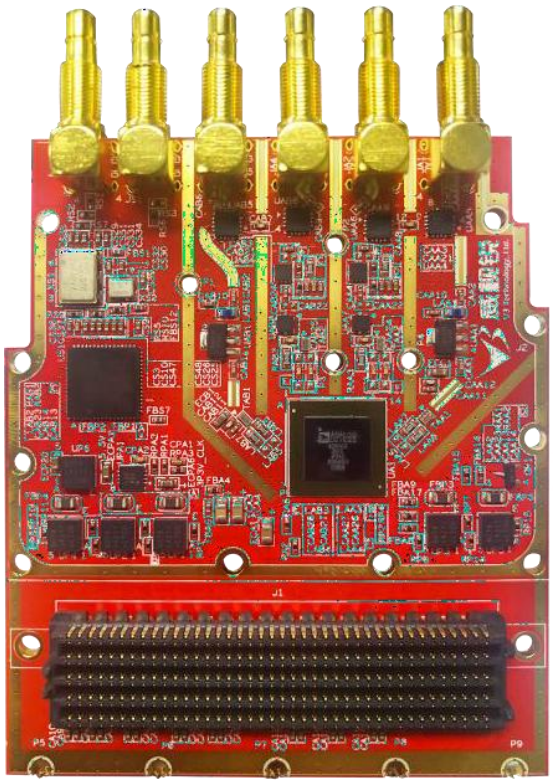
FH7000 Radio Frequency FMC Card

Rev. 3.1



Revision record

Version	Date	Revision Content
1.0	2018 - 1 -24	Initial version
2.0	2018 - 6 -10	Update ad9371 Module to version 2.0
3.0	2018 - 9	Update ad9371 Module to version 3.0
3.1	2020 - 11 - 23	Update software version VIVADO2018.3

Table of Contents

1. Introduction

This document mainly introduces the development process of FH7000 module FPGA, including the following parts:

FPGA generates DDS signal source internally, FPGA JESD204B interface, customized ARM processor based on ZYNQ, and AD9371 configuration. It can achieve the function of sending and receiving single tone signals and can use chip scope to observe the received signals and export them to MATLAB for analysis.

Furthermore, the RF sub board contains an integrated VCO reference clock generation IC selected from TI's LMK04828, which can generate various reference clocks for AD9371 and FPGA JESD204B using a 48MHz reference clock. The FPGA development process allows for user defined sampling clocks, which can be flexibly used in various communication scenarios.

Through this reference routine, users can understand the hardware composition and programming architecture of this system. For FPGA developers, they can use this FPGA project for secondary development to achieve AD9371 airport baseband data transmission.

V3 provides the overall configuration of PS (ZYNQ processor part), PL (ZYNQ logic part), and AD9371. It can output a single tone signal of a specified frequency through FPGA DDS ipCore and obtain the received waveform through chip scope. Finally, an interface is provided to configure LMK04828 and customize the sampling rate, allowing users to customize the required sampling rate as needed. Based on this project, users who develop FPGA baseband algorithms can use it for secondary development.

Users can use this development firmware to directly complete:

1. AD9371 Configuration
2. Initialization of JESD204B
3. DDS ipcore transmitting IQ data
4. Customization of sampling rates

2. RMFC7000 HDL reference design

HDL reference design is an embedded system built around ARM, NIOS-II, or Microblaze processor cores. The functional block diagram is shown below. The digital interface of the device mainly consists of GTX/GTH/GTY high-speed transceivers, and the PL calls the JESD204B IP core and AD9371 for data communication. The SPI interface is used to configure the AD9371 chip and LMK04828 clock chip. In addition, bare metal software programs are provided to support hardware system testing and verification, and AD9371 initialization parameter modification instructions are also provided, which will be explained in the next chapter.

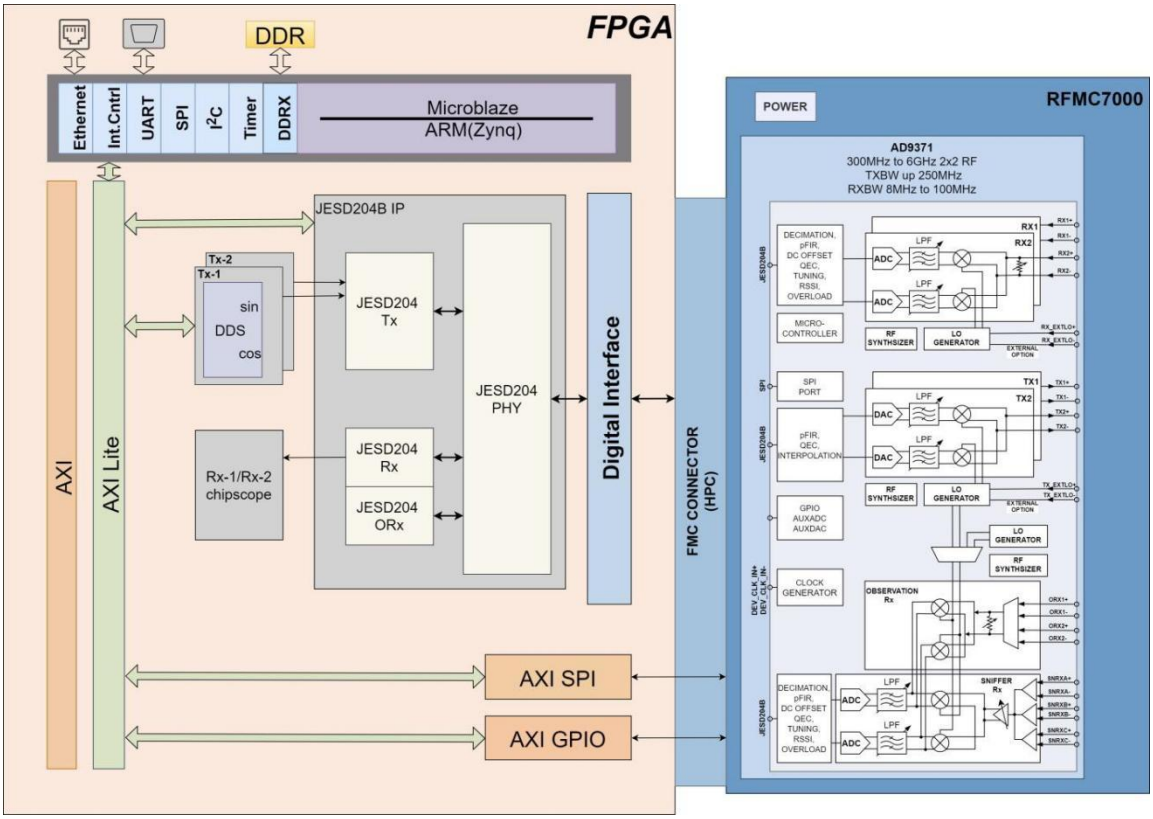


Figure 1 FH7000-HDL Reference Design Block Diagram

Digital interface

The digital interface includes 4 transmitting, 2 receiving, and 2 observation channels

DDS

The DDS IP core generates and sends test data (single tone signal/single frequency signal), and the phase can be configured by the PS; Control and SPI interface.

The device control signal is controlled by the GPIO module; SPI interface is used to configure AD9371 and LMK04828 clock chips;

2.1 FPGA Hardware Engineering Structure

The FPGA project was built using VIVADO 2018.3, and the main project file structure is as follows:

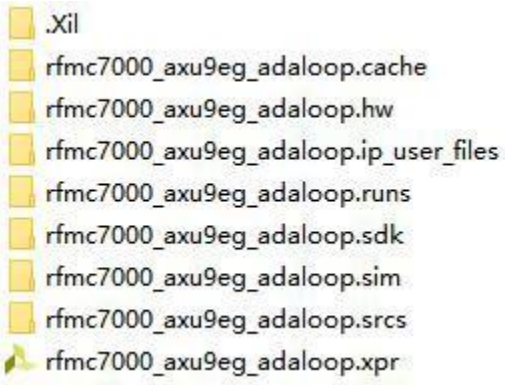


Figure 2 Hardware Engineering Catalog

The main file structure includes run project compilation and generation files, sdk bare metal software engineering, src design source files including HDL code, FPGA constraints, and xpr being the VIVADO project name. Open DeepRed in VIVADO_ FMC9371_ Adaloop.xpr can open the project as shown in the following figure:

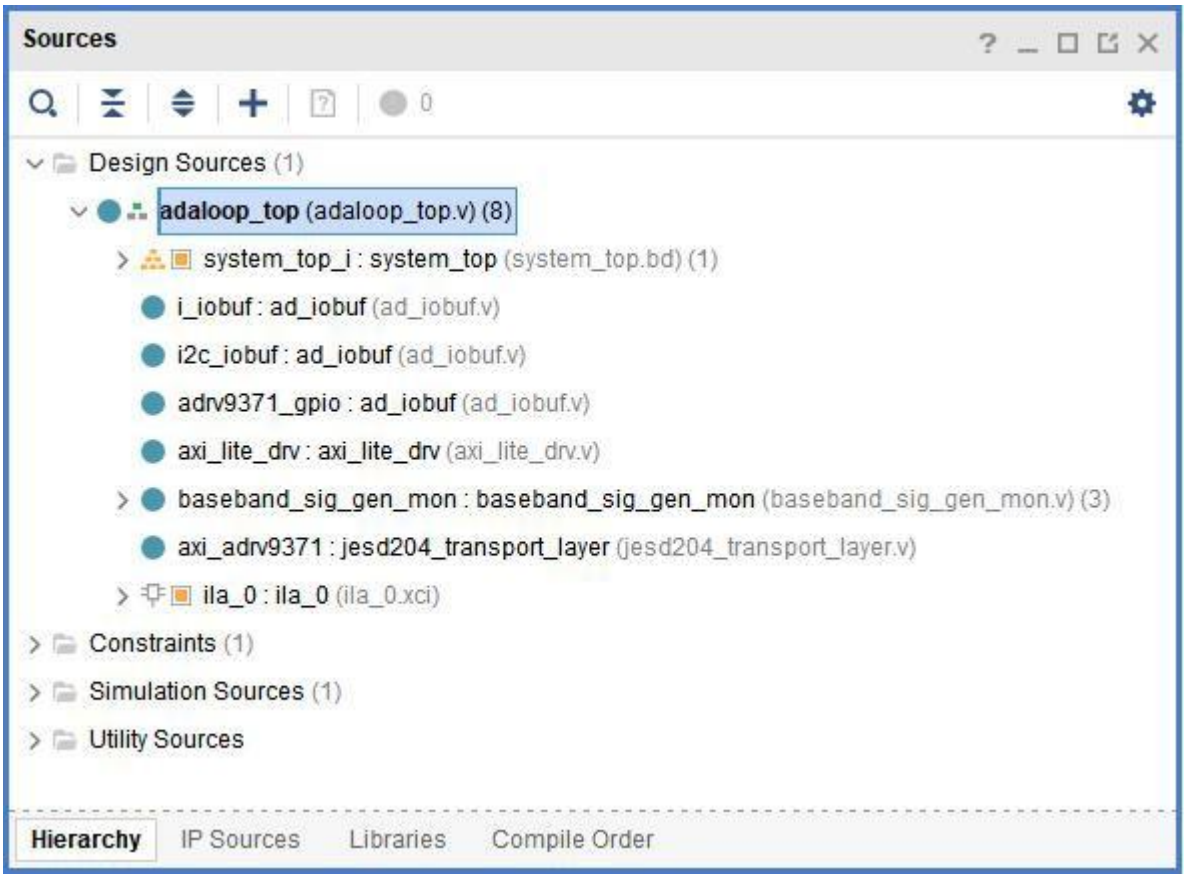


Figure 4 VIVADO Hardware Engineering

Click open block design, open block design. This includes customization of CPUs and peripherals. As shown in the following figure:

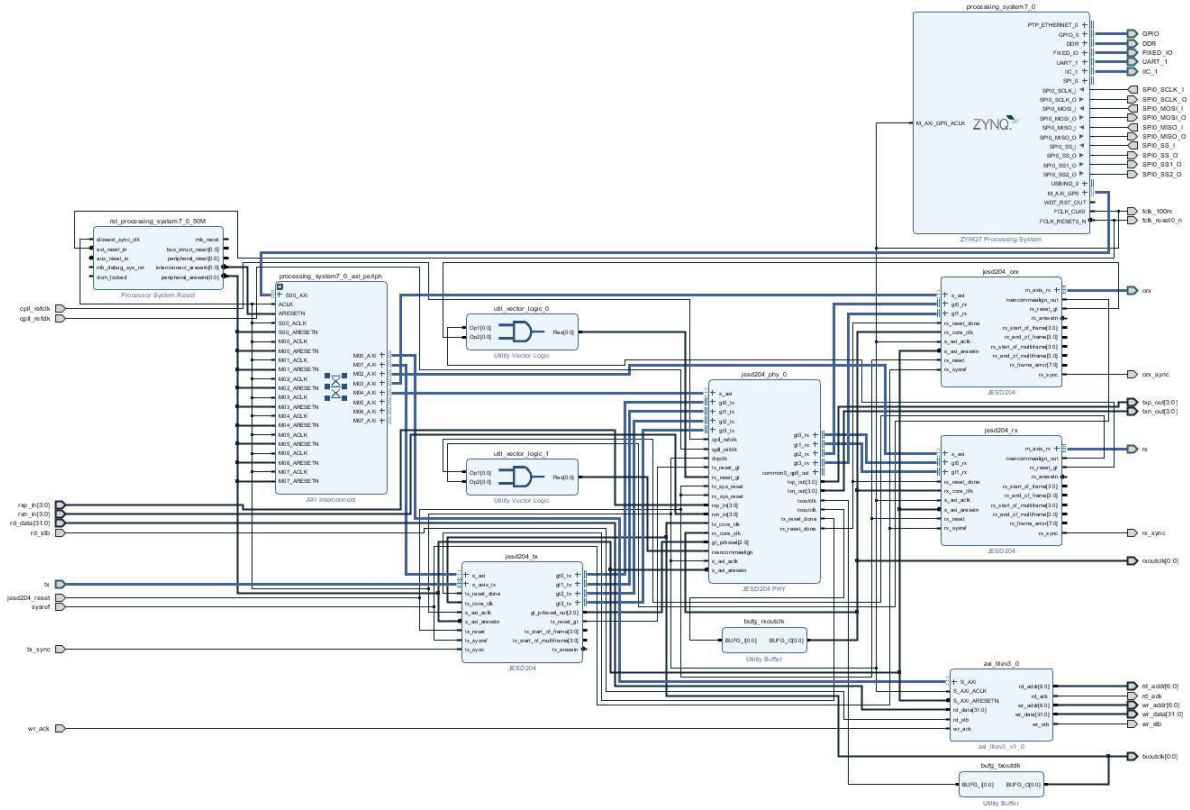


Figure 5 Customization of CPU and Peripheral Devices

Note: Different carrier cards may correspond with different CPU peripherals. In actual use, please customize with your own carrier cards.

2.2 CPU Customized

Double click on each module to see the parameter settings in the module, and double click on processing_ System7_ You can see the customization of the CPU, and users can modify it based on their actual usage of the card. If you do secondary development, it can be used as a reference.

SPI0 is used to configure the AD9371 and LMK04828 clock chips, I2C1 selects EMI reserved read/write eeprom, UART0 is used for serial port modulation, and GPIO controls the switch IO of AD9371.

The interface between PS and PL selects GP for registration of transferring and configuration of each IP. The clock output from PS to PL enables FCLK_ CLK0, FCLK_ CLK0 clock 100MHz is used for GP interface communication, and DMA transmission is not involved in this reference design, so the HP interface is not used. FCLK_ Reset0_ N is used to reset the entire PL system and AXI bus.

2.3 JESD204 Authorization

JESD204B link and configuration, AD9371 adopts the JESD204B protocol and communicates through GTX high-speed serial transceivers. Xilinx provides a complete JESD204B solution, including two parts: JESD204 and JESD204 HPY. JESD204 requires an additional license from Xilinx to use, and JESD204 PHY is included in the VIVADO authorization. Users can register on the xilinx website and receive a free three-month license trial for free. You can also contact We3 Sales for purchase (phone number 010-62670519, QQ120631932). The methods for free trial are as follows:

1 Enter: https://www.xilinx.com/support/licensing_solution_center.html

2 Choose: Access Product Licensing Site

3 Improve user information, next step

4 Enter: Access Product Licensing Site, click “Search Now”

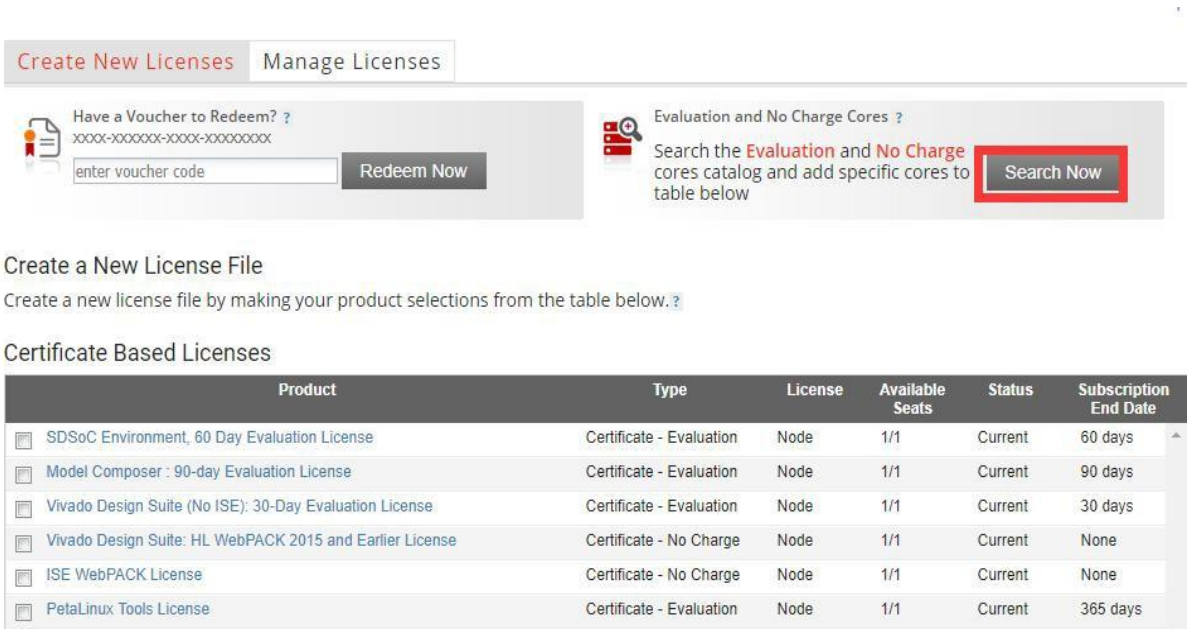


Figure 6 Authorization Center

5 Find JESD and join

6 Generate a license by adding a PC network card MAC to download the license

7 Copy the downloaded license to the. Xilinx directory

8 Click on tools report IP status in VIVADO to see the status of each IP and whether it is authorized.

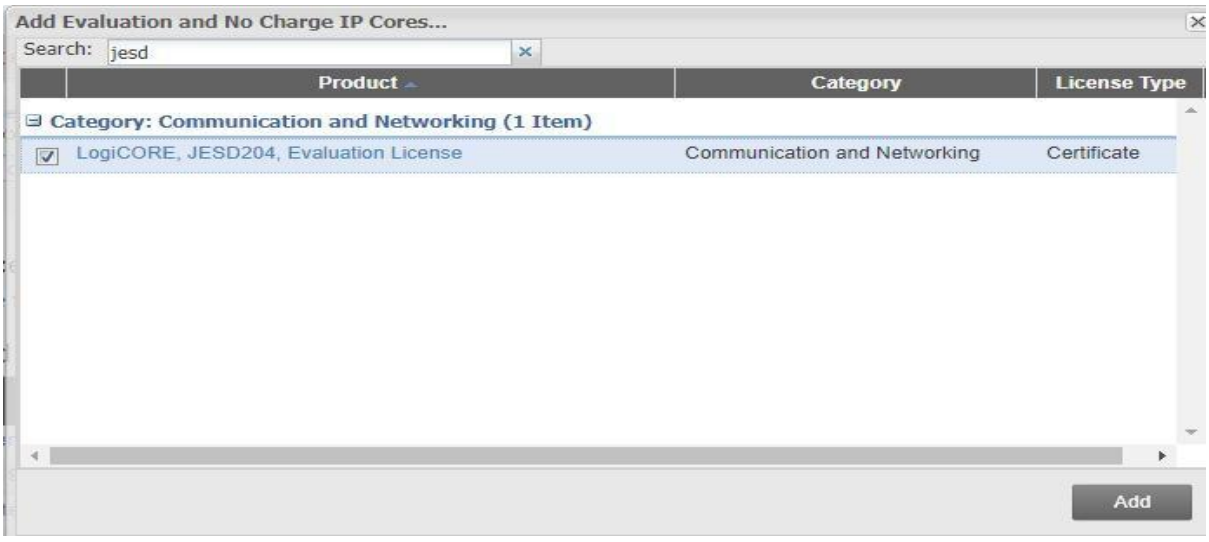


Figure 7 Search JESD204

Certificate Based Licenses

Product	Type	License	Available Seats	Status	Subscription End Date
SDSoC Environment, 60 Day Evaluation License	Certificate - Evaluation	Node	1/1	Current	60 days
Model Composer : 90-day Evaluation License	Certificate - Evaluation	Node	1/1	Current	90 days
Vivado Design Suite (No ISE): 30-Day Evaluation License	Certificate - Evaluation	Node	1/1	Current	30 days
Vivado Design Suite: HL WebPACK 2015 and Earlier License	Certificate - No Charge	Node	1/1	Current	None
ISE WebPACK License	Certificate - No Charge	Node	1/1	Current	None
PetaLinux Tools License	Certificate - Evaluation	Node	1/1	Current	365 days
Vivado HLS Evaluation License	Certificate - Evaluation	Node	1/1	Current	30 days
LogiCORE, JESD204, Evaluation License	Certificate - Evaluation	Node / Flo...		Current	120 days

Generate Node-Locked License

Figure 8 Generate License

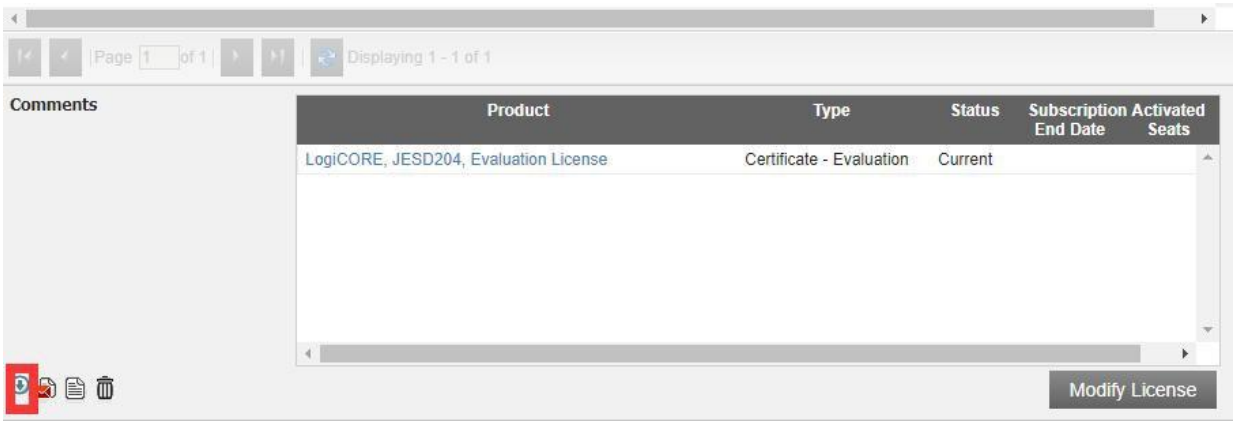


Figure 9 Download license

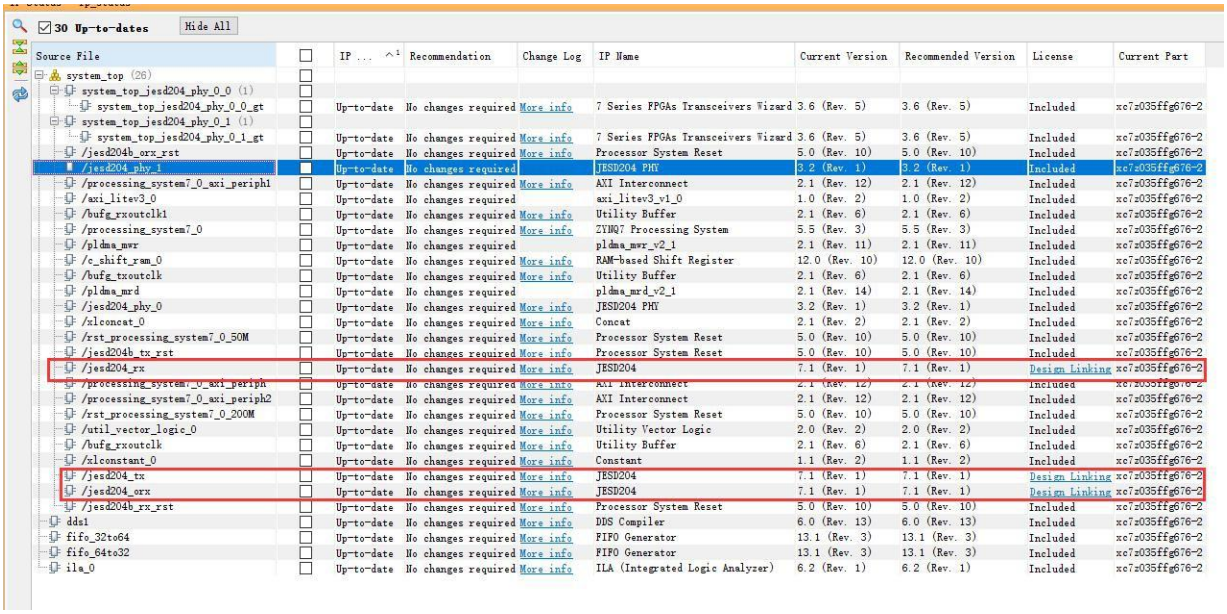
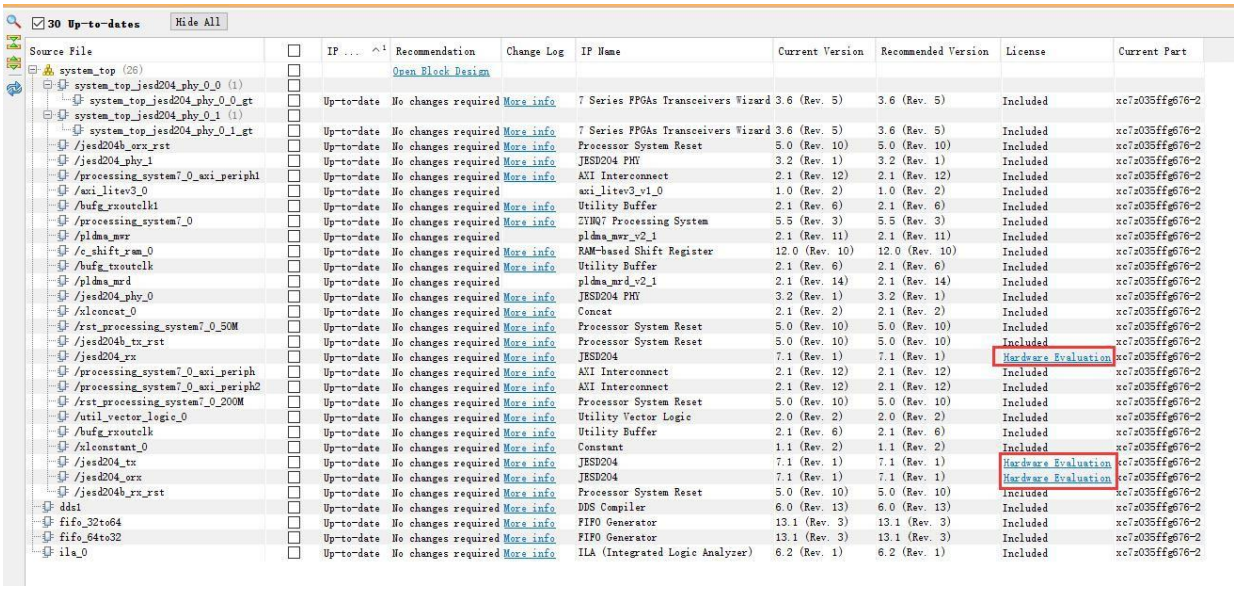


Figure 10 IP Unauthorized Status (Design Linking



30 Up-to-dates | Hide All

Source File	IP ...	Recommendation	Change Log	IP Name	Current Version	Recommended Version	License	Current Part
system_top (26)		Open Block Design						
system_top_jesd204_phy_0_0 (1)								
system_top_jesd204_phy_0_0_gt	Up-to-date	No changes required	More info	7 Series FPGAs Transceivers Wizard	3.6 (Rev. 5)	3.6 (Rev. 5)	Included	xc7z035ffg676-2
system_top_jesd204_phy_0_1 (1)								
system_top_jesd204_phy_0_1_gt	Up-to-date	No changes required	More info	7 Series FPGAs Transceivers Wizard	3.6 (Rev. 5)	3.6 (Rev. 5)	Included	xc7z035ffg676-2
/jesd204b_orx_rst	Up-to-date	No changes required	More info	Processor System Reset	5.0 (Rev. 10)	5.0 (Rev. 10)	Included	xc7z035ffg676-2
/jesd204_phy_1	Up-to-date	No changes required	More info	JESD204 PHY	3.2 (Rev. 1)	3.2 (Rev. 1)	Included	xc7z035ffg676-2
/processing_system7_0_axi_periph1	Up-to-date	No changes required	More info	AXI Interconnect	2.1 (Rev. 12)	2.1 (Rev. 12)	Included	xc7z035ffg676-2
/axi_litev3_0	Up-to-date	No changes required		axi_litev3_v1_0	1.0 (Rev. 2)	1.0 (Rev. 2)	Included	xc7z035ffg676-2
/bufg_rxoutclk1	Up-to-date	No changes required	More info	Utility Buffer	2.1 (Rev. 6)	2.1 (Rev. 6)	Included	xc7z035ffg676-2
/processing_system7_0	Up-to-date	No changes required	More info	ZYNQ7 Processing System	5.5 (Rev. 3)	5.5 (Rev. 3)	Included	xc7z035ffg676-2
/pldma_mwr	Up-to-date	No changes required		pldma_mwr_v2_1	2.1 (Rev. 11)	2.1 (Rev. 11)	Included	xc7z035ffg676-2
/c_shift_ram_0	Up-to-date	No changes required	More info	RAM-based Shift Register	12.0 (Rev. 10)	12.0 (Rev. 10)	Included	xc7z035ffg676-2
/bufg_txoutclk	Up-to-date	No changes required	More info	Utility Buffer	2.1 (Rev. 6)	2.1 (Rev. 6)	Included	xc7z035ffg676-2
/pldma_mrd	Up-to-date	No changes required		pldma_mrd_v2_1	2.1 (Rev. 14)	2.1 (Rev. 14)	Included	xc7z035ffg676-2
/jesd204_phy_0	Up-to-date	No changes required	More info	JESD204 PHY	3.2 (Rev. 1)	3.2 (Rev. 1)	Included	xc7z035ffg676-2
/xlconcat_0	Up-to-date	No changes required	More info	Concat	2.1 (Rev. 2)	2.1 (Rev. 2)	Included	xc7z035ffg676-2
/rst_processing_system7_0_50M	Up-to-date	No changes required	More info	Processor System Reset	5.0 (Rev. 10)	5.0 (Rev. 10)	Included	xc7z035ffg676-2
/jesd204b_tx_rst	Up-to-date	No changes required	More info	Processor System Reset	5.0 (Rev. 10)	5.0 (Rev. 10)	Included	xc7z035ffg676-2
/jesd204_rx	Up-to-date	No changes required	More info	JESD204	7.1 (Rev. 1)	7.1 (Rev. 1)	Hardware Evaluation	xc7z035ffg676-2
/processing_system7_0_axi_periph	Up-to-date	No changes required	More info	AXI Interconnect	2.1 (Rev. 12)	2.1 (Rev. 12)	Included	xc7z035ffg676-2
/processing_system7_0_axi_periph2	Up-to-date	No changes required	More info	AXI Interconnect	2.1 (Rev. 12)	2.1 (Rev. 12)	Included	xc7z035ffg676-2
/rst_processing_system7_0_200M	Up-to-date	No changes required	More info	Processor System Reset	5.0 (Rev. 10)	5.0 (Rev. 10)	Included	xc7z035ffg676-2
/util_vector_logic_0	Up-to-date	No changes required	More info	Utility Vector Logic	2.0 (Rev. 2)	2.0 (Rev. 2)	Included	xc7z035ffg676-2
/bufg_rxoutclk	Up-to-date	No changes required	More info	Utility Buffer	2.1 (Rev. 6)	2.1 (Rev. 6)	Included	xc7z035ffg676-2
/xlconstant_0	Up-to-date	No changes required	More info	Constant	1.1 (Rev. 2)	1.1 (Rev. 2)	Included	xc7z035ffg676-2
/jesd204_tx	Up-to-date	No changes required	More info	JESD204	7.1 (Rev. 1)	7.1 (Rev. 1)	Hardware Evaluation	xc7z035ffg676-2
/jesd204_orx	Up-to-date	No changes required	More info	JESD204	7.1 (Rev. 1)	7.1 (Rev. 1)	Hardware Evaluation	xc7z035ffg676-2
/jesd204b_rx_rst	Up-to-date	No changes required	More info	Processor System Reset	5.0 (Rev. 10)	5.0 (Rev. 10)	Included	xc7z035ffg676-2
dds1	Up-to-date	No changes required	More info	DDS Compiler	6.0 (Rev. 13)	6.0 (Rev. 13)	Included	xc7z035ffg676-2
fifo_32to64	Up-to-date	No changes required	More info	FIFO Generator	13.1 (Rev. 3)	13.1 (Rev. 3)	Included	xc7z035ffg676-2
fifo_64to32	Up-to-date	No changes required	More info	FIFO Generator	13.1 (Rev. 3)	13.1 (Rev. 3)	Included	xc7z035ffg676-2
ila_0	Up-to-date	No changes required	More info	ILA (Integrated Logic Analyzer)	6.2 (Rev. 1)	6.2 (Rev. 1)	Included	xc7z035ffg676-2

Figure 11 IP Authorized Status (Hardware Evaluation)

2.4 JESD 204 Customize

JESD204 is two IP cores, JESD204 and JESD204 PHY. Each port requires a JESD204 IP, which is used to generate or process JESD204 frame formats, TX, RX, and ORX. JESD204 PHY implements the GTX physical layer, which correctly configures the phase-locked loop settings at all levels of GTX hardware based online speed. The connection relationship is shown in the following figure.

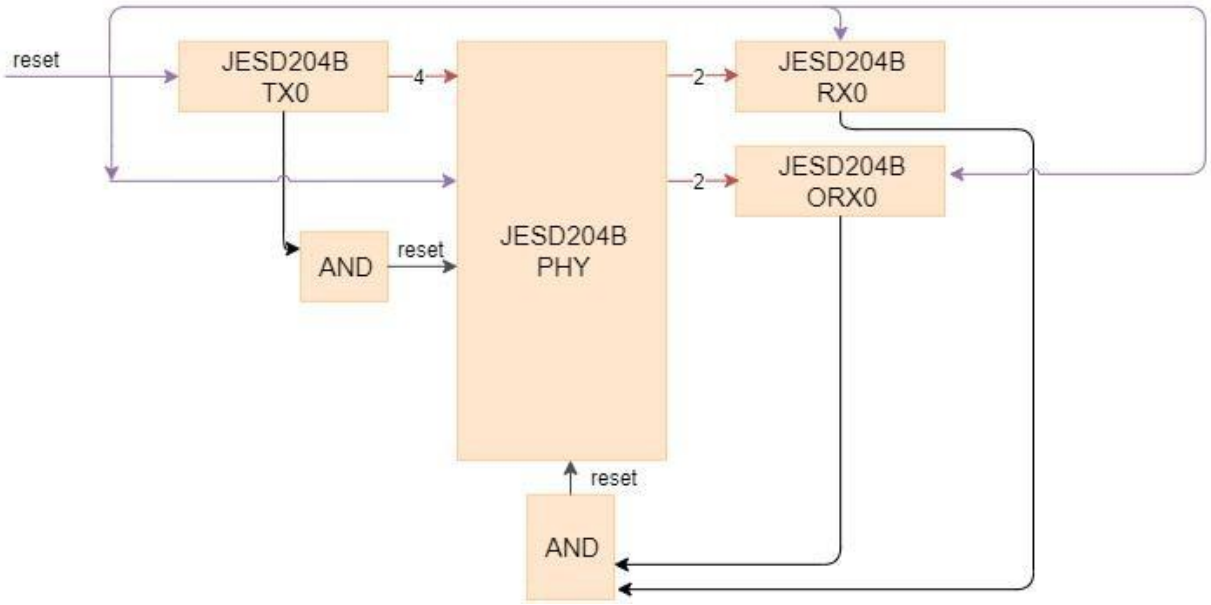


Figure 12 JESD204 Block Diagram

Use four lane sending channels for the TX end, two lane receiving channels for the RX end, and two receiving channels for the ORX end. When the sampling rate is 122.88MHz, txoutclk is 61.44MHz, and rxoutclk is 122.88MHz.

2.5 FPGA Engineering Data Flow

The sending direction is generated by the DDS module for IQ data on the tx end, and the driving clock

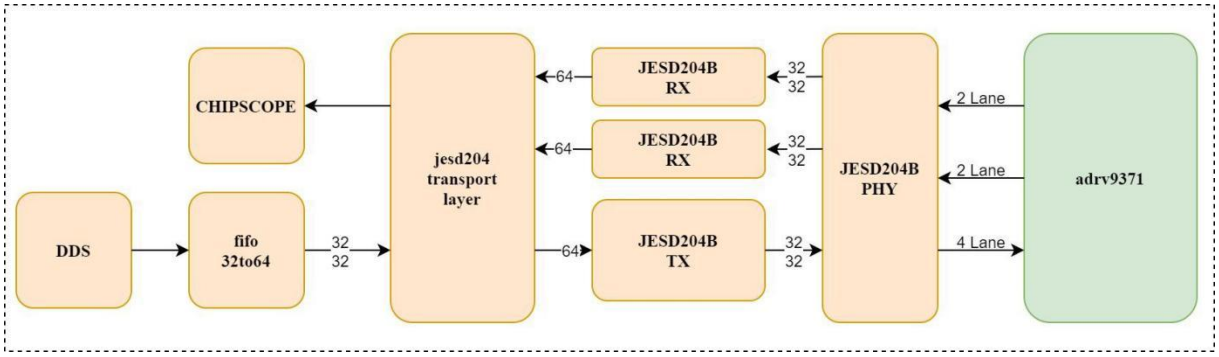
adopts a 122.88MHz rxoutclk. Two channels of IQ data enter fifo separately_ 32to64 converts two channels of IQ data into 64 bit width for Jesd204_ Transport_ Layer module, clock using txoutclk, 61.44MHz, via jesd204_ Transport_ The layer module is converted to the axistream data stream required

for JESD204, with a clock of txoutclk and 61.44MHz.

Enter data into fifo separately_ 32to64 converts two channels of IQ data into 64 bit width for Jesd204_ Transport_ Layer module, clock using txoutclk, 61.44MHz, via jesd204_ Transport_ The layer module is converted to the axistream data stream required for JESD204, with a clock of txoutclk and 61.44MHz.

Receiving direction, rx end axi_ Stream data output from JESD204, rx end rx_ TData width 64 bits, clock rxoutclk, 122.88MHz. Orx end orx_ TData width 64 bits, clock rxoutclk. Rx end data through jesd204_ Transport_ The layer module converts 16 bit IQ data streams and displays them through chipscope

The data flow diagram is shown in the following figure：



3. Bare metal applications

This chapter includes verifying FPGA hardware engineering, GPIO configuration, AD9371 configuration, and register interaction on bare metal.

3.1 Software engineering

Selecting File launch SDK in the VIVADO project will automatically open the software SDK in the project directory. Provided the following engineering:

Adrv9371_ Test generates single tone signals of different frequencies through software configuration of DDS ipcore phase. After configuring AD9371, start to send the single tone signal. Simultaneously start receiving and analyzing data through chipscope. The top-level file is headless. c. The architecture of this file is derived from the NO-OS software program provided by ADI, which has been optimized and modified by Visorai. The NO OS source program can refer to the ADI website link: https://wiki.analog.com/resources/eval/user-guides/mykonos/no-os-setup

3.2 GPIO configuration

First, execute the platform_ Init (void) sets the direction of GPIO and initializes it. Afterwards, set the following IO to the specified level. Secondly, perform external attenuator attenuation setting and DDS output phase stepping. The receiver attenuator is set to maximum attenuation, and the transmission attenuation is set to no

attenuation. For the sake of uniformity in the program, it is named Gain. 0 corresponds to a gain of 0dB with full attenuation, and 63 corresponds to a maximum gain of 31.5dB without attenuation. DDS phase stepping phase, output baseband signal

Assume rxclkout=122.88MHz， Output baseband single tone frequency f_{out} $\frac{122.88}{2^{12}} \times 128 = 3.84\text{MHz}$。

3.2 Configuring Clock Chips

The hardware did not use AD9528 but instead used TI's LMK04828, which is also controlled through the SPI bus.

3.3 AD9371 initial configuration

Initializing AD9371, a user-defined file was used to initialize AD9371. In this project, 122p88. c 122p88. h.

These three files are generated by AD9371 Receiver Evaluation Software. This software can be downloaded at the following link:

http://www.analog.com/cn/license/licensing-agreement/transceiver-evaluation-software.html

The NO-OS program can be found at the following link：

https://wiki.analog.com/resources/eval/user-guides/mykonos/no-os-setup

After opening the AD9371 Receiver Evaluation Software, click on 'connect' and it will prompt that the hardware is not connected. Next, users can customize the working parameters of AD9371. The device clock defaults to 122.88MHz. JESD204B rate calculation method,

- Sending end=sampling rate * bit width/number of channels =122.88MHz*80/4=2457.6Mbps
- Receiving end=sampling rate * bit width/number of channels =122.88MHz*80/2=4915.2Mbps
- ORX reception=sampling rate * bit width/number of channels=122.88MHz*40/2=2457.6Mbps
- Finally, export the C language file and add it to software engineering.

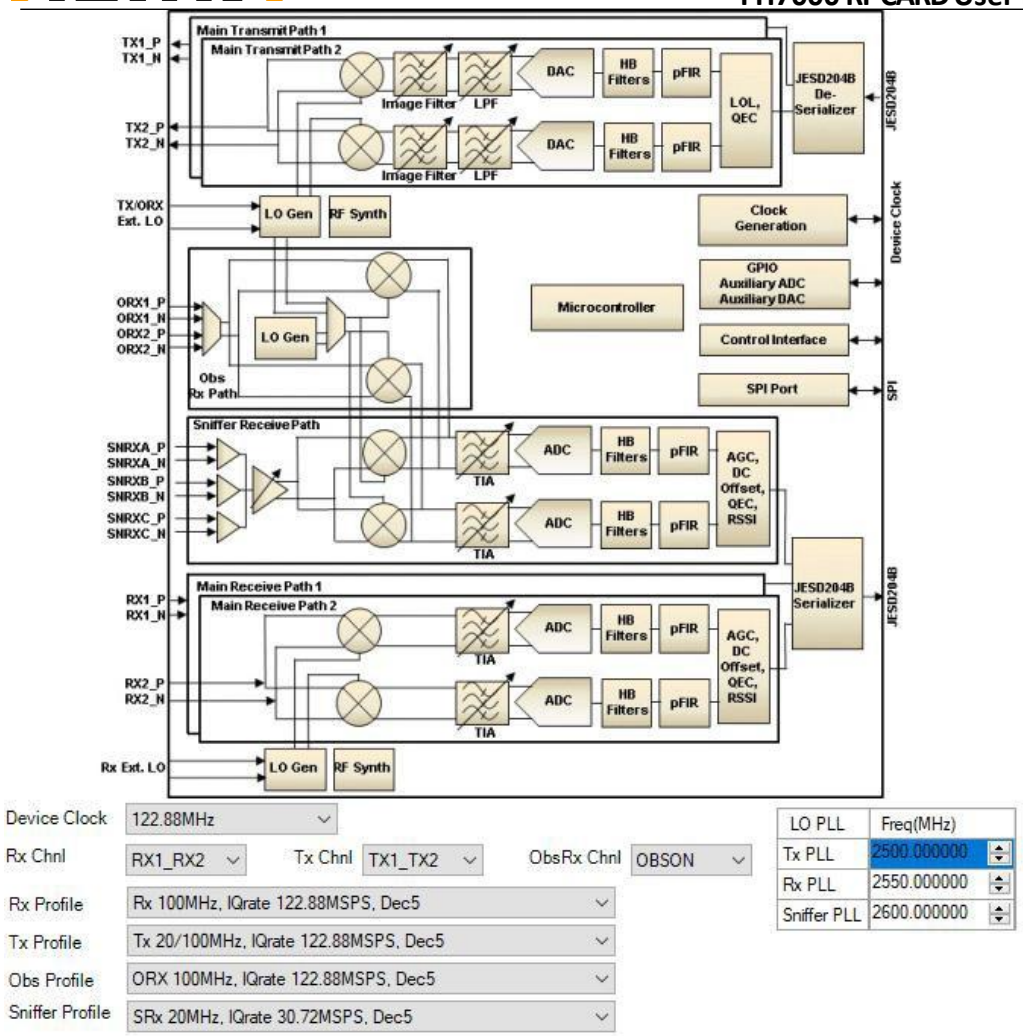


Figure 13 Customized AD9371

Initialization Calibration	Run
Rx QEC	☑
Tx QEC	☑
Internal Tx LOL	☑
External Tx LOL	☐
External Init Attn	0.00

Tracking Calibration	Run
Rx1 QEC	☑
Rx2 QEC	☑
Tx1 LOL	☐
Tx2 LOL	☐
Tx1 QEC	☑
Tx2 QEC	☑

Figure 14 Calibration Selectio

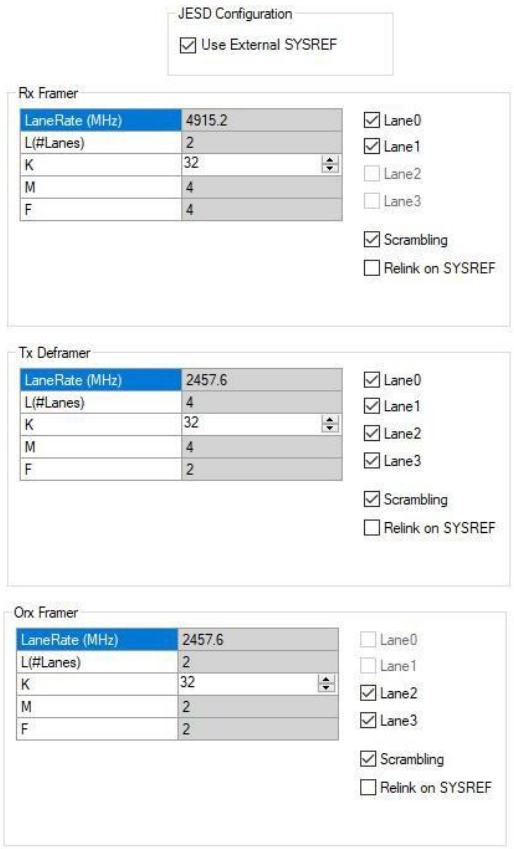


Figure 15 JESD204B Rate Selection

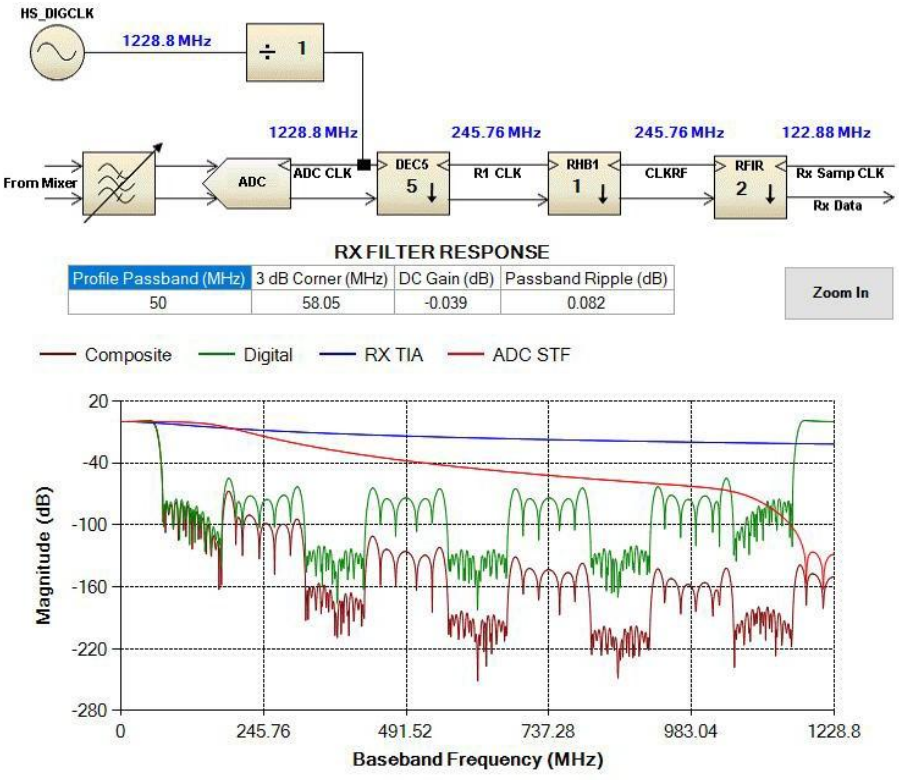


Figure 16 Receive Channel Bandwidth

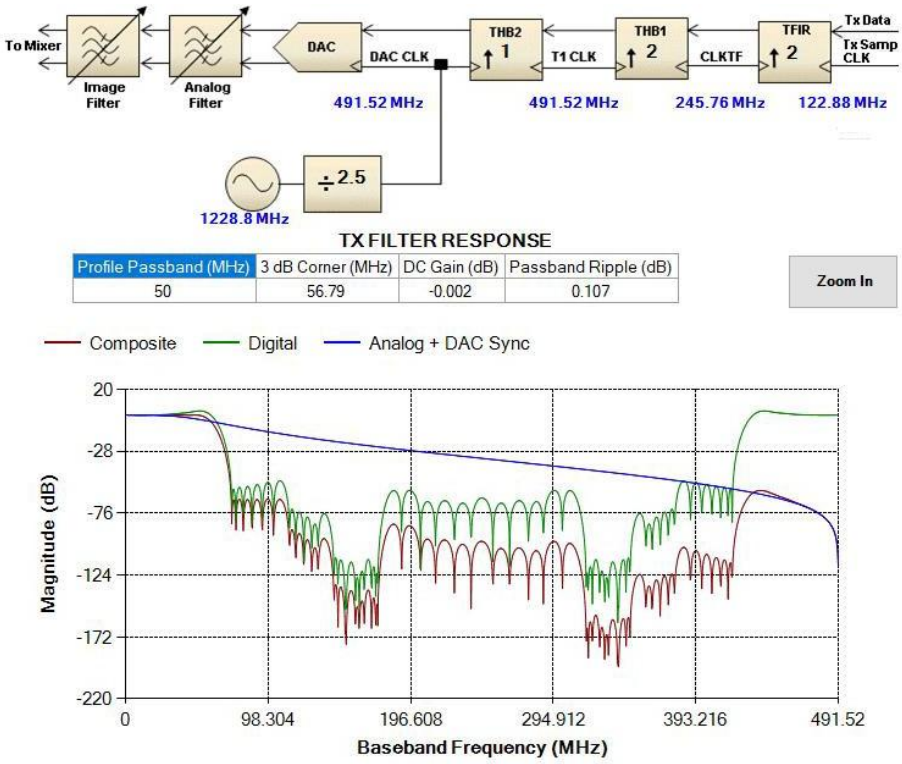


Figure 17 Transmission Channel Bandwidth

The default receiving channel AGC's agcgainUpdateCounter is 0 and changed to 4096. Otherwise, an error will be reported when initializing AD9371.

```
static mykonosAgcCfg_t rxAgcConfig =
{
    255,        /* agcRx1MaxGainIndex */ 195,      /*
    agcRx1MinGainIndex */ 255,/*
    agcRx2MaxGainIndex */ 195,          /*
    agcRx2MinGainIndex: */ 255,         /*
    agcObsRxMaxGainIndex */ 203,        /*
    agcObsRxMinGainIndex */ 1,/* agcObsRxSelect
    */
    1,          /* agcPeakThresholdMode */
    1,          /* agcLowThsPreventGainIncrease */
    //*FIXME*agcGainUpdateCounter=0/ 4096,    /*
    agcGainUpdateCounter */ 4, /*
    agcSlowLoopSettlingDelay */ 2, /*
    agcPeakWaitTime*/
    1, /* agcResetOnRxEnable */
    0, /* agcEnableSyncPulseForGainCounter */ &rxPeakAgc,
    &rxPwrAgc};

static mykonosAgcCfg_t obsRxAgcConfig =
{
    255,        /* agcRx1MaxGainIndex */ 195,      /*
    agcRx1MinGainIndex */ 255,/*
    agcRx2MaxGainIndex */ 195,          /*
    agcRx2MinGainIndex: */ 255,         /*
    agcObsRxMaxGainIndex */ 203,        /*
    agcObsRxMinGainIndex */ 1,/* agcObsRxSelect
```

```
    */
    1,          /* agcPeakThresholdMode */
    1,          /* agcLowThsPreventGainIncrease */
    //*FIXME*agcGainUpdateCounter=0/ 4096,    /*
    agcGainUpdateCounter */
    4,          /* agcSlowLoopSettlingDelay */ 2,   /*
    agcPeakWaitTime */
    1,          /* agcResetOnRxEnable */
    0,          /* agcEnableSyncPulseForGainCounter */
    &obsRxPeakAgc,
    &obsRxPwrAgc
};
```

3.4 AD9371 Modification after initialization

Configure the receive gain function:

```
    if((mykError=MYKONOS_setRx1ManualGain(&mykDevice,200))!=MYKONOS_ERR_OK)
{
        errorString = getMykonosErrorMessage(mykError);
        goto error;
    }

    if((mykError=MYKONOS_setRx2ManualGain(&mykDevice,200))!=MYKONOS_ERR_OK)
{
        errorString = getMykonosErrorMessage(mykError);
        goto error;
    }
```

Configure Send Attenuation Function：

```
    if ((mykError = MYKONOS_setTx1Attenuation(&mykDevice, 10000)) !=
MYKONOS_ERR_OK) {//range=0~41950
        errorString = getMykonosErrorMessage(mykError);
        goto error;
    }

    if ((mykError = MYKONOS_setTx2Attenuation(&mykDevice, 30000)) !=
MYKONOS_ERR_OK) {//range=0~41950
        errorString = getMykonosErrorMessage(mykError);
        goto error;
    }
```

Configuring the transceiver frequency point function: The change of the transceiver frequency point is quite complex, please refer to the RF PLL FREQUENCY CHANGE PROCESS section in the AD9371-User Guide UG-992 document. Instantiate as a function in the test program. The configuration speed is faster within the frequency range of 100MHz, and it will be recalibrated if it exceeds 100MHz.

```
change_rfpll(mykDevice.rx->rxPllLoFrequency_Hz, RX_PLL,2800e6);
change_rfpll(mykDevice.tx->txPllLoFrequency_Hz, TX_PLL,2000e6);
```

3.5 Running reference routines

AD9371 provides a self loopback testing program for testing.

Using a loopback RF cable to loop back TX and RX, you can see the results of loopback through RF.

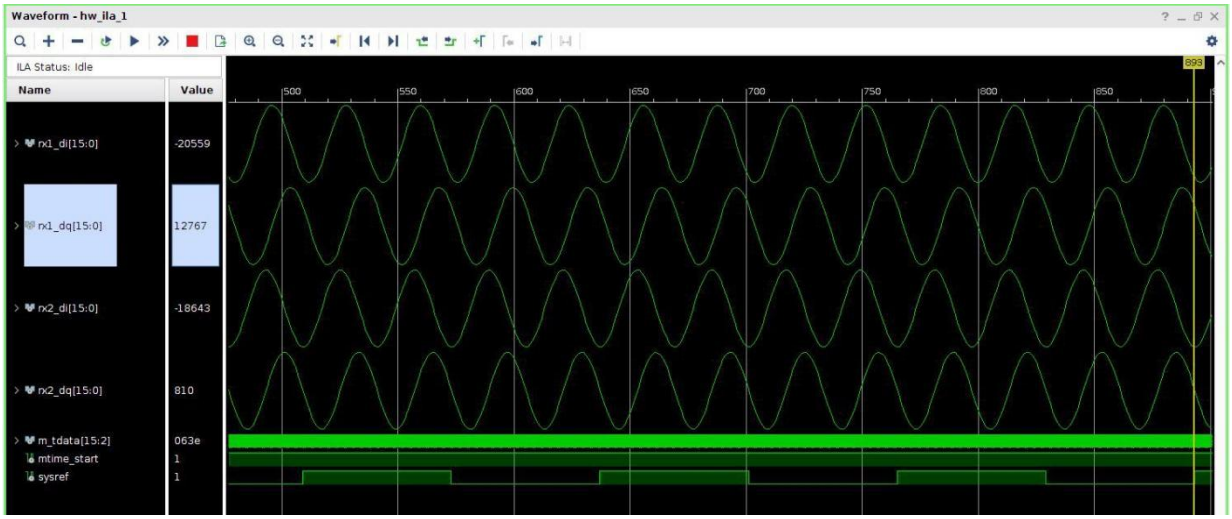


Figure 18 RF Loop Back Test

You can select waveform export and use third-party software for analysis.

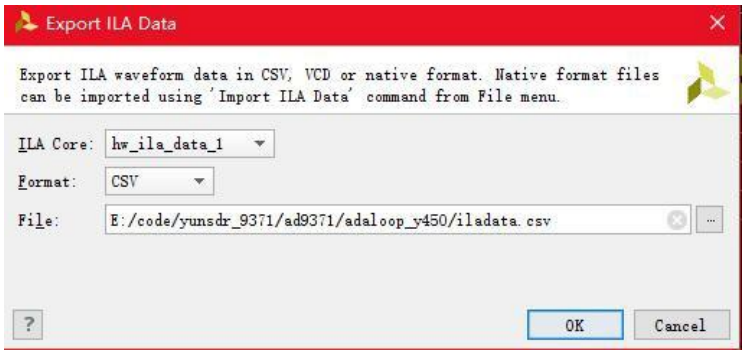


Figure 19 ILA Data Export

For example, using MATLAB for analysis.

```
m = csvread('E:\code\yunsdr_9371\ad9371\adaloop_y450\iladata.csv', 1, 0);
data(:,1)=m(:, 9)+1i*m(:, 8);
data(:,2)=m(:, 11)+1i*m(:, 10);
subplot(231);plot(real(data(:,1)));hold on;plot(imag(data(:,1))); subplot(232);plot(data(:,1));axis equal;
subplot(233);pwelch(data(:,1),[],[],[],122.88e6,'centered','psd');
subplot(234);plot(real(data(:,2)));hold on;plot(imag(data(:,2))); subplot(235);plot(data(:,2));axis equal;
subplot(236);pwelch(data(:,2),[],[],[],122.88e6,'centered','psd');
```

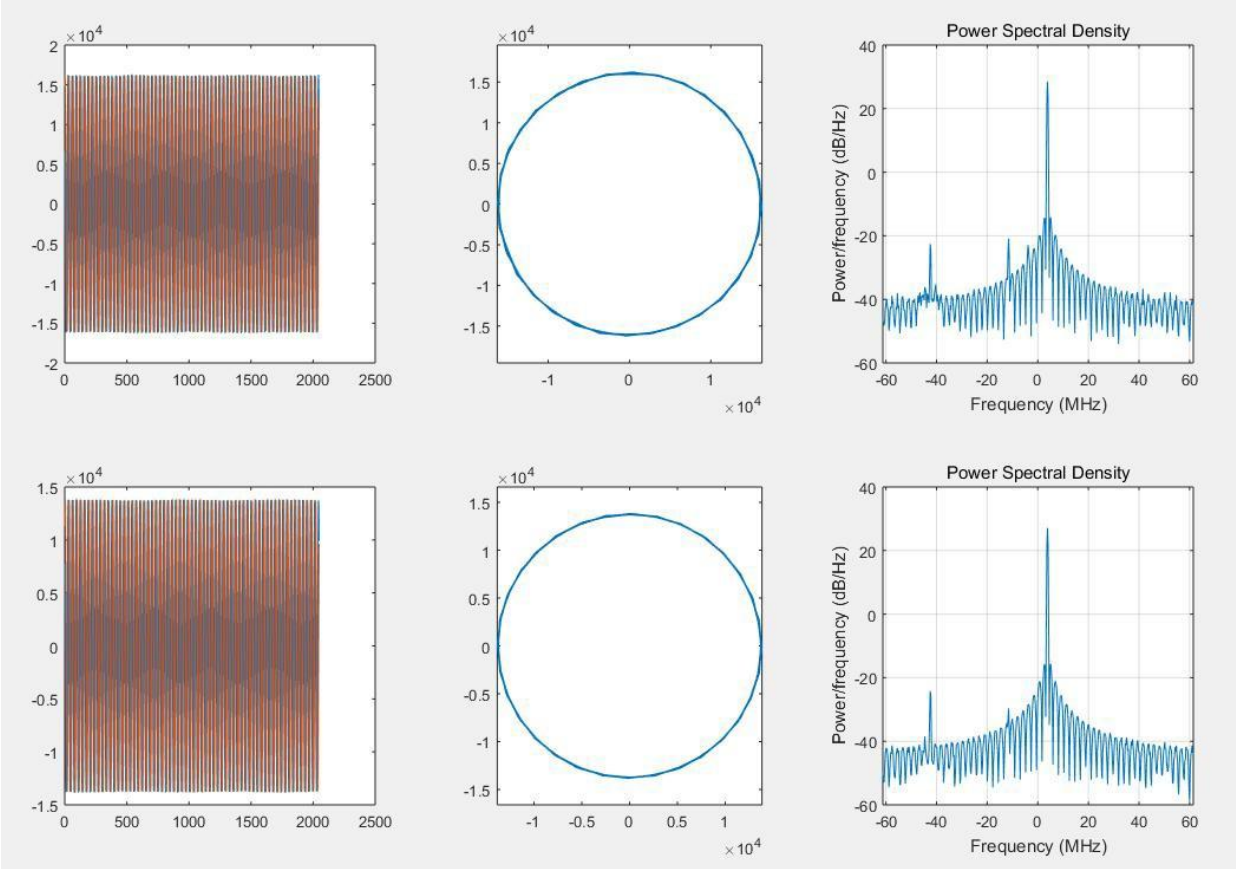


Figure 20 Analysis Results of Matlab Data

4 Customized sampling rate

Customization of sampling rates can be divided into two situations: the customization of sampling rates existing in the AD9371 development and evaluation software (MYK), and the customization of special sampling rates. The existing sampling rates of the AD9371 evaluation software are shown in the following figure:

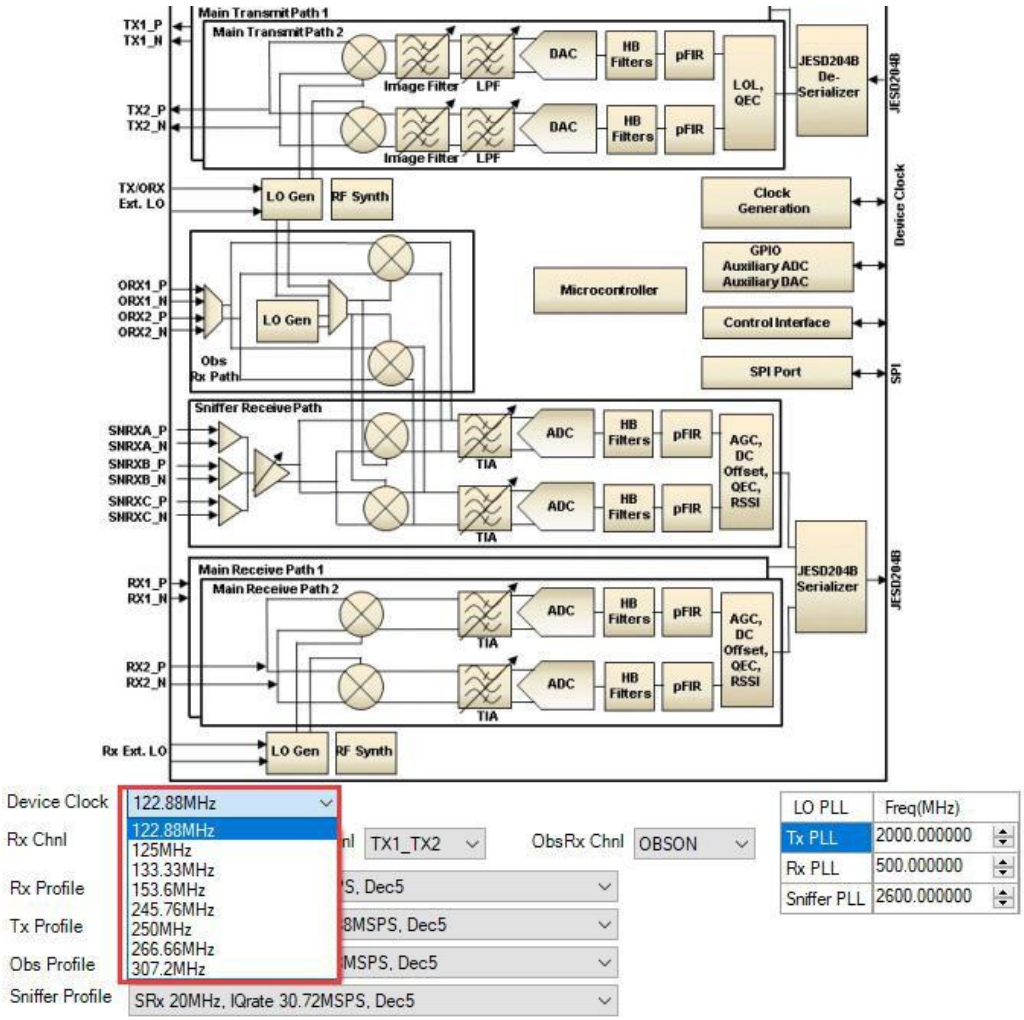


Figure 21 MYK Device Clock List