FMC 4-way high-speed AD Module FL9613 User Manual

Rev 1.0

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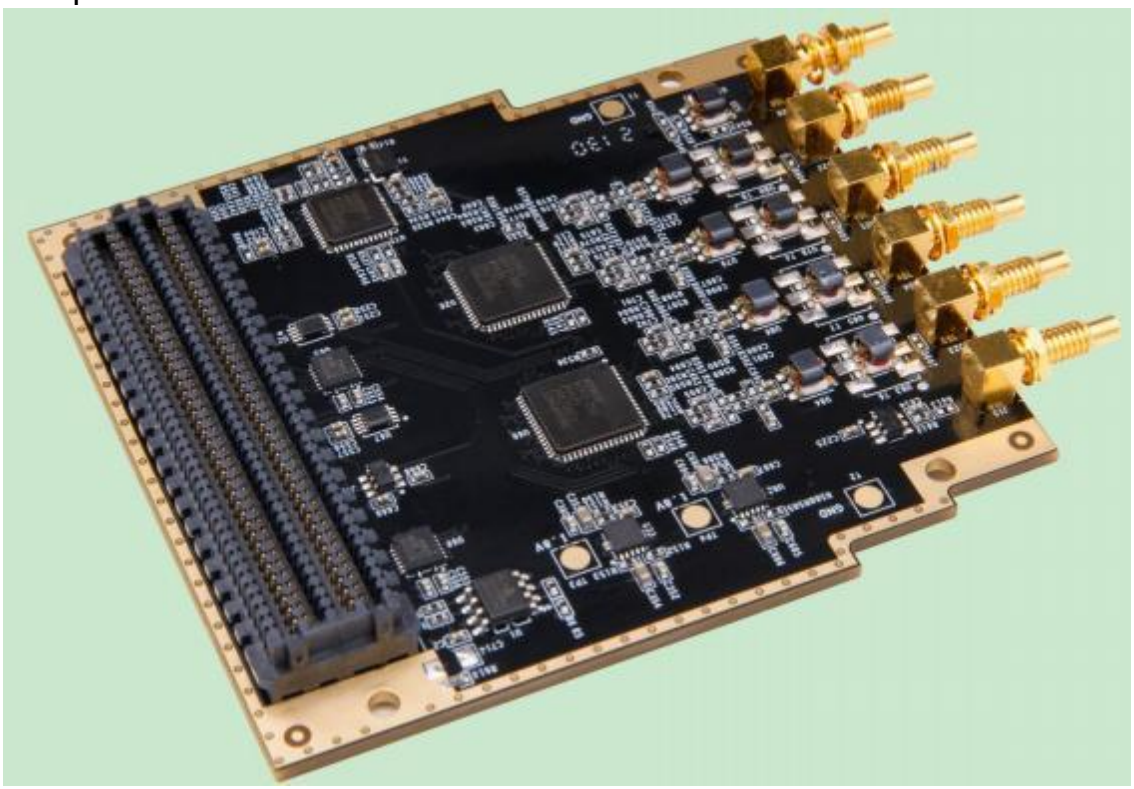
1. Introduction of FMC High Speed AD Module

Alinx FMC high-speed AD module FL9613 is a 4-way 250MSPS, 12-bit analog to digital module. The AD conversion of the FMC module adopts two ADI company's AD9613 chips, each of which supports two AD inputs. Therefore, the two AD9613 chips support a total of four AD inputs simulation. The voltage range of the signal input is 1.7V P-P, and the interface is SSMC.

FL9613 supports external trigger signal input (SSMC interface); Clock mode supports internal reference Clock input, external reference clock input, clock selection can be configured through SPI bus.

The electrical and mechanical design of FL9613 is based on the FMC standard (ANSI/VITA 57.1), which is a standard LPC FMC interface used to connect FPGA development boards. The FMC connector model is ASP_ 134604_ 01

The physical photos of the FL9613 module are as follows:



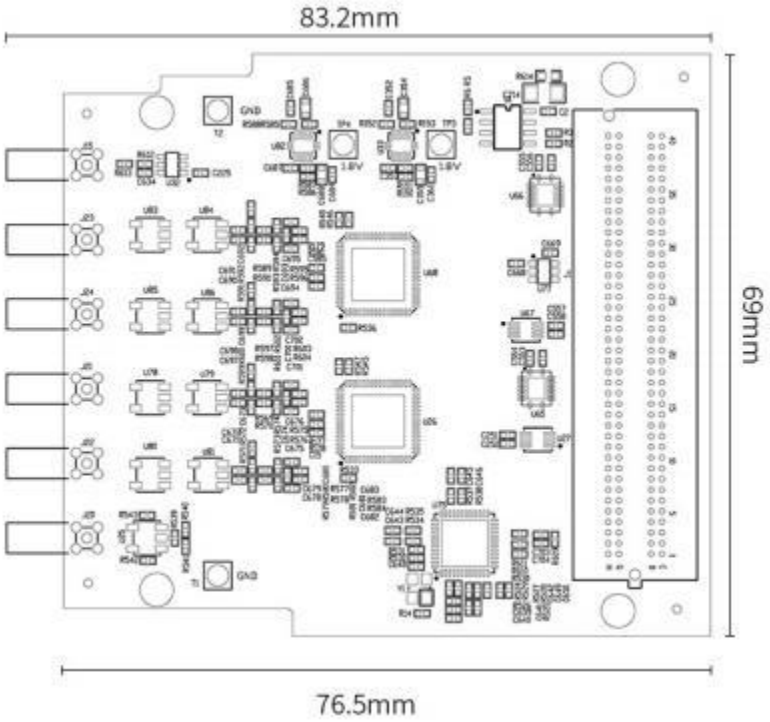
FL9613 Module physical diagram

1.1 Parameter Description of FL9613 Module

The following are the detailed parameters of the FL9613 high-speed AD module:

- AD conversion chip: 2 AD9613 chips
- AD conversion channel: 4 channels;
- AD sampling rate: 250MSPS;
- AD sampling data bits: 12;
- AD analog signal input range: 1.7V P-P;
- AD input impedance: 50 ohms;
- Analog signal input interface: SSMC interface;
- External clock input: 1 channel;
- External trigger signal input: 1 channel
- Digital interface level standard: LVDS level
- Configuration interface: SPI interface;
- Working temperature: -40 °~85 °;

1.2 Structure diagram of FL9613 module



Dimensional structure diagram of FL9613 high-speed AD module

1.3 Installation and usage requirements

The FL9613 module must be used with a development board with FMC interface, and the FMC of the development board must comply with the FMC standard (ANSI/VITA57.1). The development board provides modules with three types of power supplies: 3.3V DC, 12V DC, and VADJ DC through FMC connectors. The voltage range of VADJ allowed by the module is 1.65V~3.3V. Considering the LVDS data communication of FPGA development board, it is generally recommended that the operating voltage of VADJ be+2.5V or 1.8V.

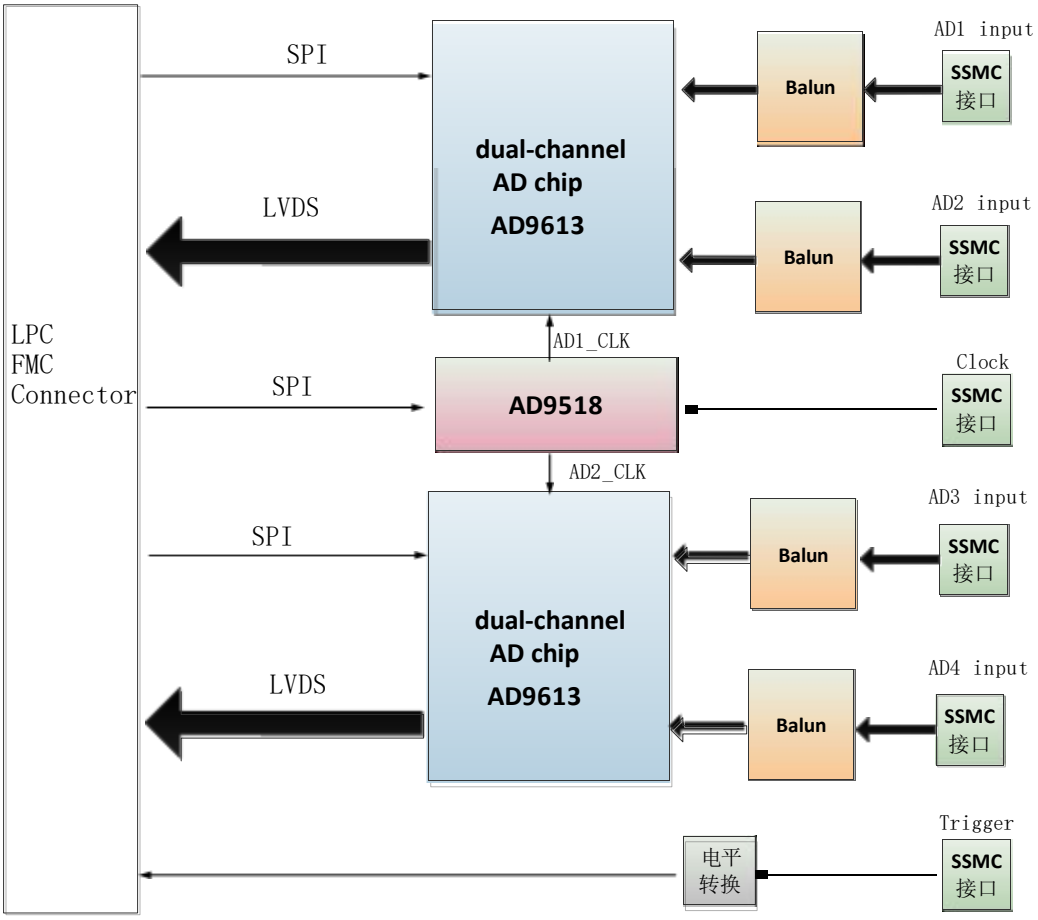
When installing the board, operators should pay attention to accuracy protection. In the absence of static electricity protection. Please do not directly contact the board components.

The output data of the FL9613 module is LVDS signal, and the control signal and trigger signal of the board are LVCMOS signals. The voltage standard depends on the power supply voltage of the VADJ.

2. Functions of FL9613 Module

2.1 Schematic Diagram of FL9613

The schematic design diagram of the FL9613 module is as follows:

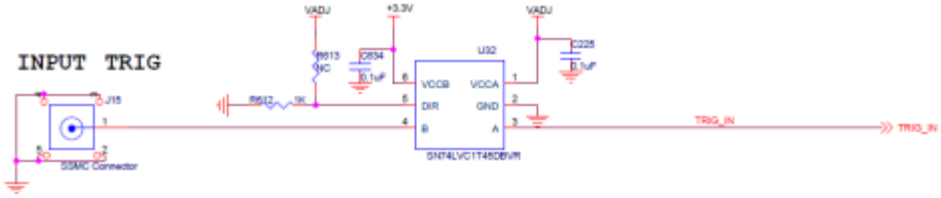


Please refer to the chip manual of AD9213 for the specific reference design of the AD9613 circuit.

2.2 Description of Input interface

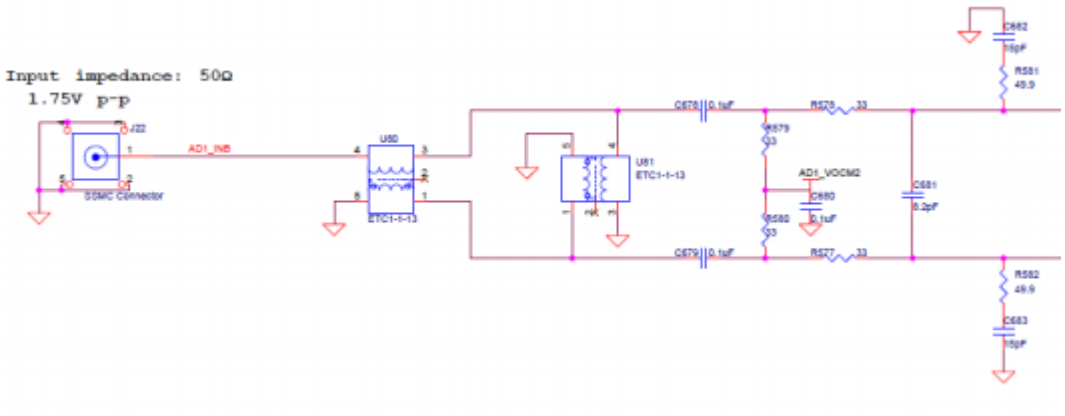
2.2.1 External trigger input interface

External trigger input supports the LVTTL/LVCMOS 3.3V level input method, which is achieved through the level conversion on the board after converting the chip to the level of VADJ, connect it to the FMC connector pins.



2.2.2 Input interface of AD

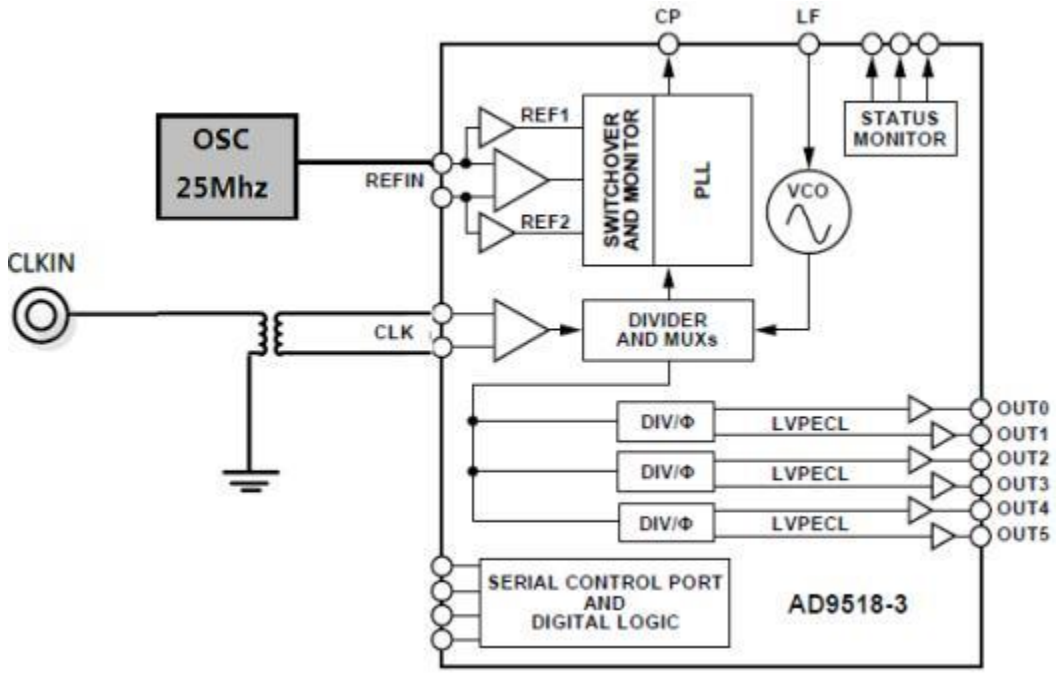
FL9613 is designed with AC coupling input, with a maximum input signal of 300Mhz, an input impedance of 50 ohms, and an analog signal range of 1.7Vp-p.



2.2.3 Clock input

The clock generation module on the board uses the AD9518-3 chip from ADI company, and is designed to use an internal VCO with a frequency range from 1.75G to 2.25G; The internal clock and external reference clock are switched through the program; The clock module configuration is achieved by connecting to the SPI bus of the FMC.

The internal reference clock is welded to a 25M crystal oscillator by default and connected to the REF1 pin of AD9518; The external reference clock is converted into a differential through a transformer and connected to the CLK+- pin.



2.3 The Description of FMC Interface

The FMC interface of the FL9613 module is a standard LPC. The following only lists the signal definitions of the power supply and AD chip interfaces on the FMC interface, and the GND signals are not listed. For details, users can refer to the schematic diagram.

Pin Number	Signal Name	Description
C35	+12V	12V power input
C37	+12V	12V power input
D32	+3.3V	3.3V power input
G7	AD1_DCO-	Data clock output of AD1 channel LVDS-N.
G6	AD1_DCO+	Data clock output AD1 channel LVDS- P
H8	AD1_D0-	AD1 channel LVDS data 0 output - N
H7	AD1_D0+	AD1 channel LVDS data 0 output - P
C11	AD1_D1-	AD1 channel LVDS data 1 output - N
C10	AD1_D1+	AD1 channel LVDS data 1 output - P
D12	AD1_D2-	AD1 channel LVDS data 2 output - N
D11	AD1_D2+	AD1 channel LVDS data 2 output - P
H11	AD1_D3-	AD1 channel LVDS data 3 output - N
H10	AD1_D3+	AD1 channel LVDS data 3 output - P
C15	AD1_D4-	AD1 channel LVDS data 4 output - N
C14	AD1_D4+	AD1 channel LVDS data 4 output - P
G13	AD1_D5-	AD1 channel LVDS data 5 output - N
G12	AD1_D5+	AD1 channel LVDS data 5 output - P
H14	AD1_D6-	AD1 channel LVDS data 6 output - N
H13	AD1_D6+	AD1 channel LVDS data 6 output - P

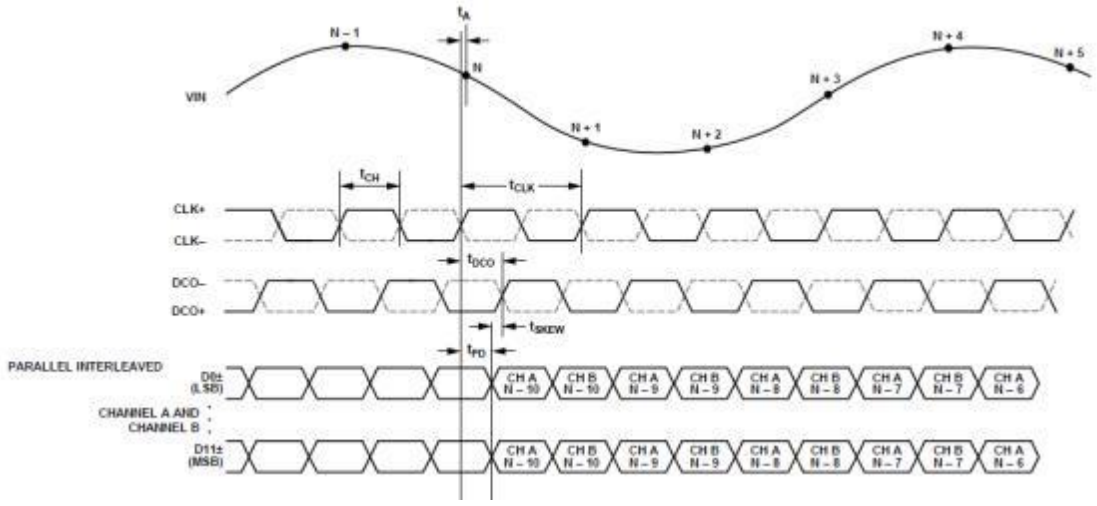
D15	AD1_D7-	AD1 channel LVDS data 7 output-N.
D14	AD1_D7+	AD1 channel LVDS data 7 output-P.
G16	AD1_D8-	AD1 channel LVDS data 8 output-N.
G15	AD1_D8+	AD1 channel LVDS data 8 output-P.
H17	AD1_D9-	AD1 channel LVDS data 9 output-N.
H16	AD1_D9+	AD1 channel LVDS data 9 output-P.
D18	AD1_D10-	AD1 channel LVDS data 10 output-N.
D17	AD1_D10+	AD1 channel LVDS data 10 output-P.
C19	AD1_D11-	AD1 channel LVDS data 11 output-N.
C18	AD1_D11+	AD1 channel LVDS data 11 output-P.
D9	AD1_OR-	AD1 channel input range exceeds indication - N
D8	AD1_OR+	AD1 channel input range exceeds indication - P
G9	AD1_SPI_CS	SPI communication chip selection signal for AD1 chip
G3	AD1_SPI_SCLK	SPI communication clock signal of AD1 chip
G10	AD1_SPI_SDIO	SPI communication data signal of AD1 chip
C23	AD2_DCO-	AD2 channel LVDS data clock output -N.
C22	AD2_DCO+	AD2 channel LVDS data clock output -P.
G22	AD2_D0-	AD2 channel LVDS data 0 output -N.
G21	AD2_D0+	AD2 channel LVDS data 0 output -P.
H23	AD2_D1-	AD2 channel LVDS data 1 output -N.
H22	AD2_D1+	AD2 channel LVDS data 1 output -P.
C27	AD2_D2-	AD2 channel LVDS data 2 output -N.
C26	AD2_D2+	AD2 channel LVDS data 2 output -P.
G25	AD2_D3-	AD2 channel LVDS data 3 output -N.
G24	AD2_D3+	AD2 channel LVDS data 3 output -P.
H26	AD2_D4-	AD2 channel LVDS data 4 output -N.
H25	AD2_D4+	AD2 channel LVDS data 4 output -P.
D27	AD2_D5-	AD2 channel LVDS data 5 output -N.
D26	AD2_D5+	AD2 channel LVDS data 5 output -P.
G28	AD2_D6-	AD2 channel LVDS data 6 output -N.
G27	AD2_D6+	AD2 channel LVDS data 6 output -P.
H29	AD2_D7-	AD2 channel LVDS data 7 output -N.
H28	AD2_D7+	AD2 channel LVDS data 7 output -P.
G31	AD2_D8-	AD2 channel LVDS data 8 output -N.
G30	AD2_D8+	AD2 channel LVDS data 8 output -P.
H32	AD2_D9-	AD2 channel LVDS data 9 output -N.
H31	AD2_D9+	AD2 channel LVDS data 9 output -P.
G34	AD2_D10-	AD2 channel LVDS data 10 output -N.
G33	AD2_D10+	AD2 channel LVDS data 10 output -P.
H35	AD2_D11-	AD2 channel LVDS data 11 output -N.
H34	AD2_D11+	AD2 channel LVDS data 11 output -P.
D21	AD2_OR-	AD2 channel input range exceeds indication-N
D20	AD2_OR+	AD2 channel input range exceeds indication-P

G18	AD2_SPI_CS	SPI communication chip selection signal for AD2 chip
D24	AD2_SPI_SCLK	SPI communication clock signal of AD2 chip
D23	AD2_SPI_SDIO	SPI communication data signal of AD2 chip
H38	CLK_CS	SPI communication chip selection signal for clock chips
G36	CLK_RESET	Reset signal of clock chip
H37	CLK_SCLK	SPI communication clock signal of clock chip
H19	CLK_SDIO	SPI communication data bidirectional signal of clock chip
G37	CLK_SDO	SPI communication data output signal of clock chip
G19	CLK_SYNC	Synchronization signal of clock chip
H5	FPGA_CLK-	FPGA reference clock input-N
H4	FPGA_CLK+	FPGA reference clock input-P
C34	GA0	EEPROM address bit 0
D35	GA1	EEPROM address bit 1
C30	SCL	I2C clock of EEPROM
C31	SDA	I2C data of EEPROM
H20	AD_SYNC_V	Synchronization signal between ADs
G2	TRIG_IN	Trigger input signal
G39	VADJ	VADJ power input
H40	VADJ	VADJ power input

3. AD sampling timing and design

3.1 FL9613 digital output timing

The digital output configuration of AD9613 dual channel AD is in LVDS output mode, with two channels (A and B) sharing a pair of differential clock signals and 12 pairs of differential data signals. The order of data output is alternating, with one AD output on the rising edge of the clock and the other AD data output on the falling edge of the clock.

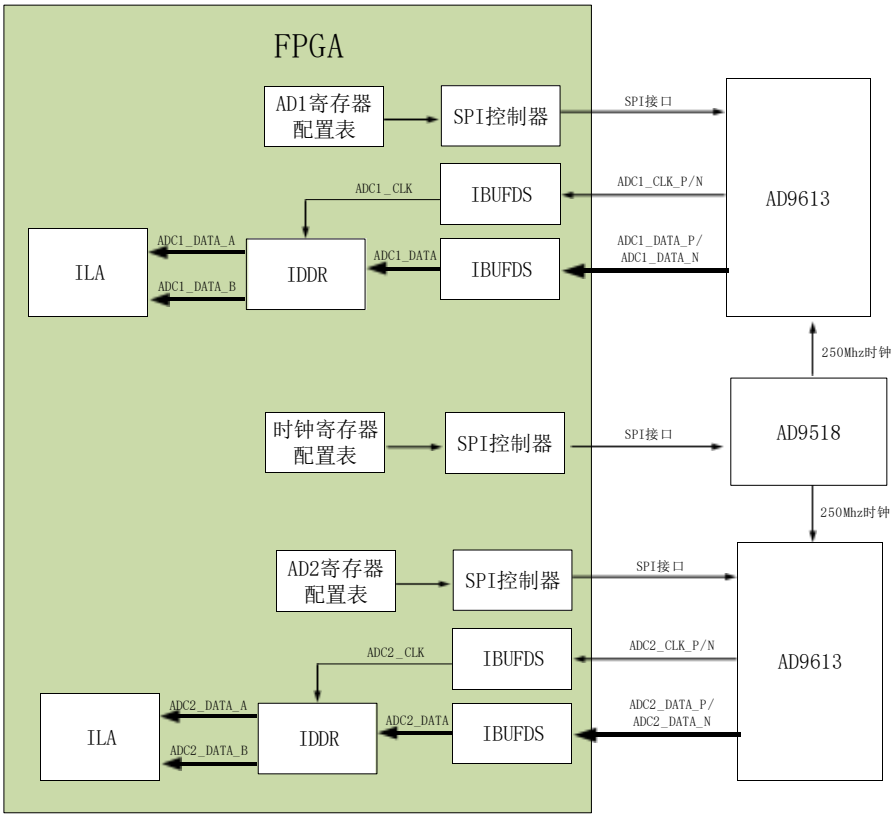


3.2 FL9613 Programming

We provide a routine for AD acquisition and display on the ALINX development board. In this routine, the differential LVDS clock signals and differential LVDS data signals input by two AD9613 are converted into single ended signals through the IBUFDS module, and the 12bit data is then converted into channel A 12bit data and channel B 12bit data through the IDDR module. The 12bit data of channel A and channel B were observed through ILA online debugging.

After powering on, the register of the clock chip AD9518 needs to be configured through the SPI interface to output a differential clock of 250Mhz to the AD9613 chip. Additionally, the registers of AD9613 need to be configured through the SPI interface.

The functional block diagram of FPGA's AD testing is as follows:



Below is a brief functional introduction to the various modules used in FPGA programs:

3.2.1 ad9613_lut_config.v

The AD9613 register configuration table only configures the values of two registers, one is register 0x17 and the other is register 0x FF.

Register 0x17 is used to configure the delay relationship between the output clock and data, which can be adjusted based on actual measurement results.

0x17	DCO output delay (global)	Enable DCO clock delay	Open	Open	DCO clock delay [delay = (3100 ps × register value/31 +100)] 00000 = 100 ps 00001 = 200 ps 00010 = 300 ps ... 11110 = 3100 ps 11111 = 3200 ps	0x00

After configuring register 0x17, it is necessary to write 1 to the lowest bit of register 0xFF to take effect.

Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default Notes/ Comments
0xFF	Transfer	Open	Open	Open	Open	Open	Open	Open	Transfer	0x00	Synchronously transfers data from the master shift register to the slave

For specific register meanings, please refer to the AD9613 chip manual.

3.2.2 ad9518_lut_config.v

AD9518 Register configuration table. There are many registers configured here, please refer to the chip manual for details.

3.2.3 spi_config.v

This module configures registers for AD9613 chip and AD9518 by calling the SPI communication module.

3.3 top.v

The top module not only instantiates the sub modules above, but also implements the following functions.

- ✧ The 50Mhz reference clock required to call PLL IP to generate SPI.
- ✧ Invoking the IBUFDS primitive to convert LVDS differential clock signals and data signals into single ended clock and single ended data.
- ✧ Invoking the IDDR primitive to convert data from dual edge A and B channels into single edge A and B channel data.
- ✧ By calling ILA IP to observe the data of AD1 and AD2, users can modify the interface signals of ILA themselves to observe the signals they want to observe.

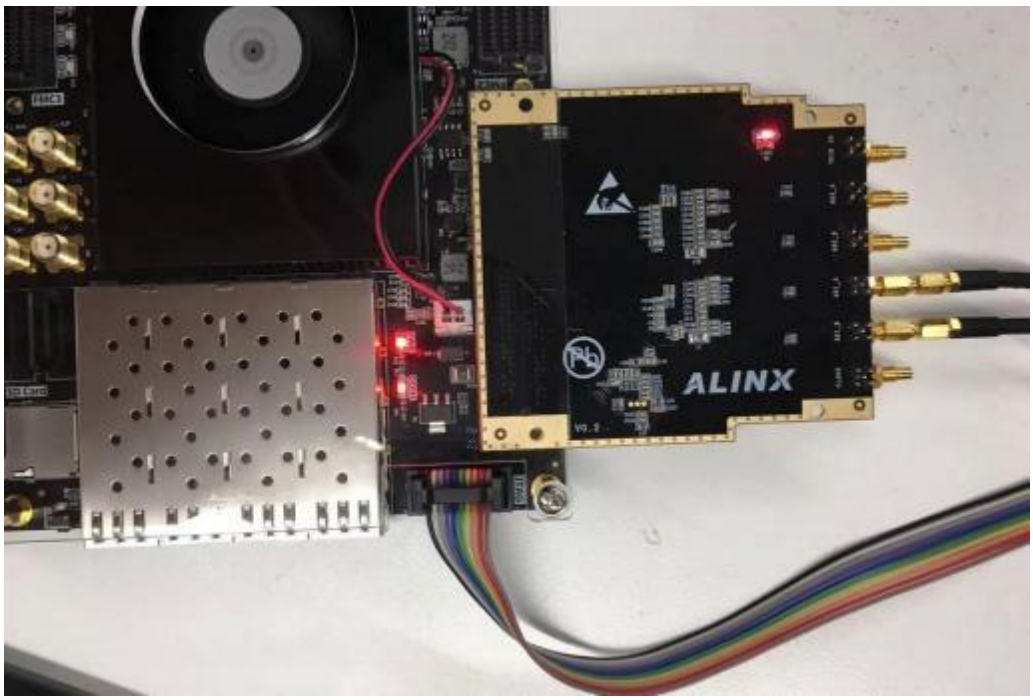
3.4 xdc Constraint File

The XDC constraint file defines the pins for communication between two AD chips and a clock chip.

4. Hardware Connection and Testing

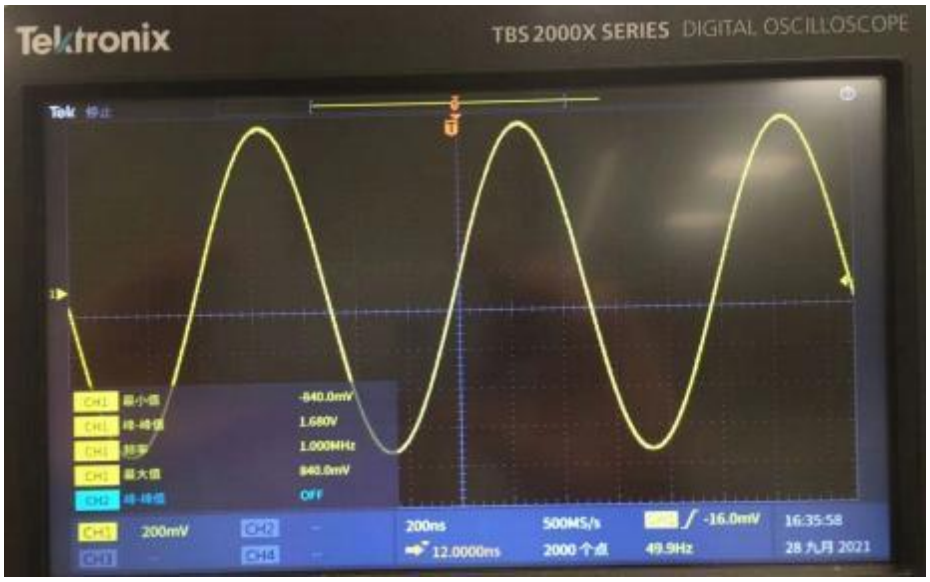
The hardware connection between the FL9613 module and the FPGA development board is very simple. Just plug the FMC interface into the FMC interface of the development board and fix it with screws. We use a signal generator to generate an analog signal and connect it to AD1_ A and AD1_ On the SMC interface of channel B.

The following is the hardware connection diagram for the ALINX AXKU040 development board (FMC1) and FL9613:

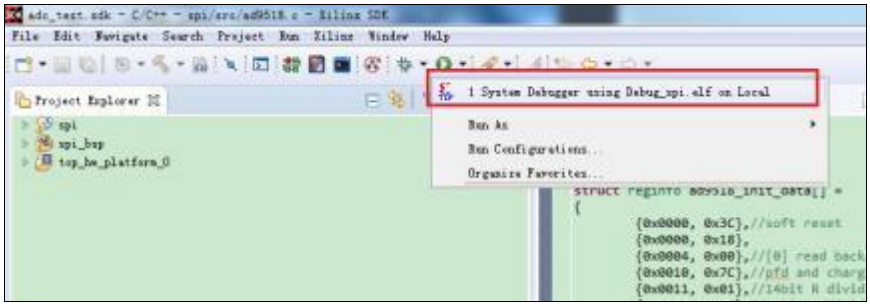


The development board is powered on, and the signal generator generates two positive selection waves, one with a frequency of 1Mhz and the other with a bit 10Mhz. The peak-to-peak value is 3.4V p-p. Because the internal resistance of our signal generator is 50 ohms, and the input impedance of FL9613 is also 50 ohms, the output signal will have partial voltage, so the peak -to-peak value of the input to the AD module is 1.7V p-p.

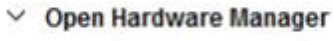
The waveform measured by the signal oscilloscope of AD input is as follows:

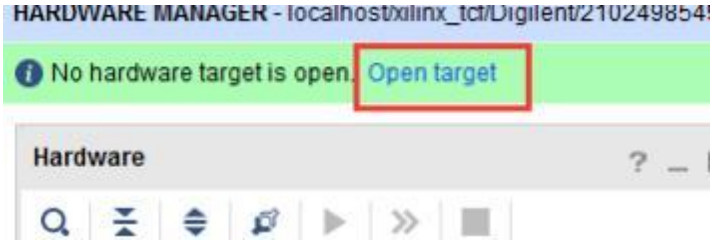


Then download the program from the Vivado software.

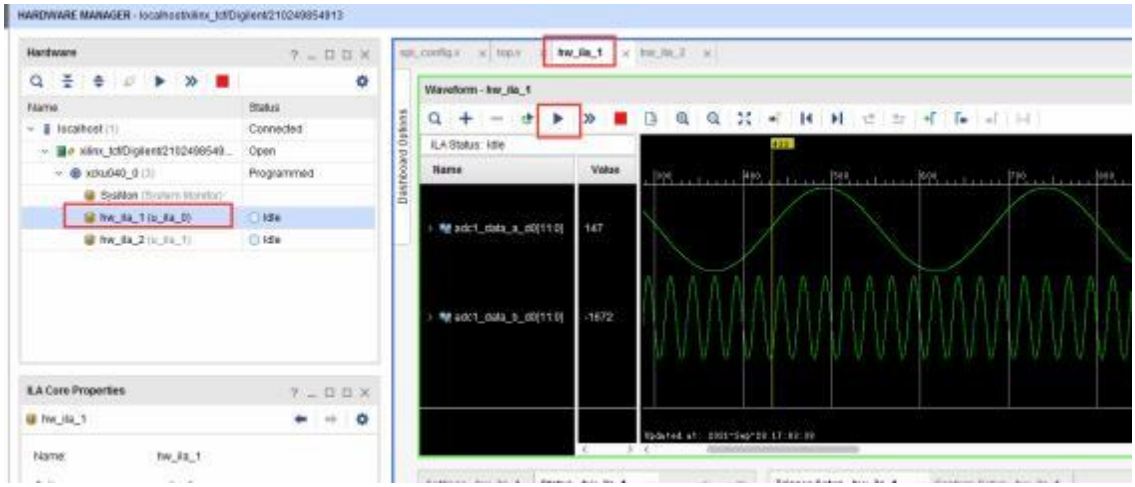


In VIVADO, Open hardware Manager, then Open target.





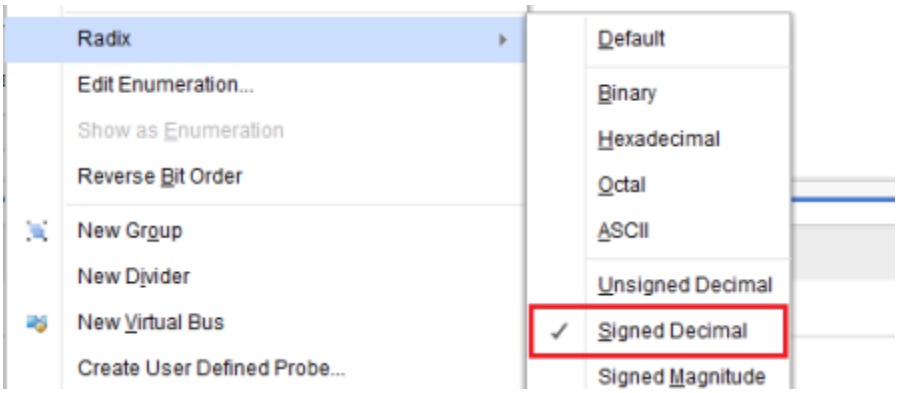
Hw_ Ila_ 1 is the observed data of AD1, click trigger, and you can see the positive selection data of 2 AD channels.



If the waveform display is incorrect, the following items can be checked:

1) Set the waveform display to Analog.

2) The data Radix needs to be set to Signed Decimal.


Radix
Edit Enumeration...
Show as Enumeration
Reverse Bit Order
New Group
New Divider
New Virtual Bus
Create User Defined Probe...
Default
Binary
Hexadecimal
Octal
ASCII
Unsigned Decimal
Signed Decimal
Signed Magnitude