Zynq UltraScale+ Development Board Z7-P User Manual

Table of Contents

Based on XILINX Zynq UltraScale+MPSoCs development platform, our company's development board 2022 (Model: Z7-P) has officially released, and we have prepared this user manual for your quick understanding of this development platform.

This MPSoCs development platform adopts the mode of core board and expansion board, which is convenient for second development and utilization. Its core board uses the solution of ZU7EV, a XILINX Zynq UltraScale+EV chip, and adopts Processing System(PS)+Programmable Logic(PL) technology to integrate quad-core ARM Cortex-A53 and FPGA programmable logic on a single chip. In addition, The PS side of the core board has 4 pieces of 1GB high-speed DDR4 SDRAM chips, 1 piece of 8GB eMMC memory chip, and 2 pieces of 256Mb QSPI FLASH chips; the PL side of the core board has 4 pieces of 1GB DDR4 SDRAM chip.

In the design of carrier board, we provides users with a rich set of peripheral interfaces, for example, 1 FMC HPC, 1 M.2 SSD interface, 1 mini_DP interface, 1 USB3.0 Type-C interface, 1 40-pin expansion port, 2 Gigabit Ethernet interfaces, 2 UART interfaces, 1 PCIEX8 gold finger, 1 TF card interface and so on. It is a "professional grade" ZYNQ development platform because it meets the requirements of high-speed data exchange, data storage, video transmission and processing, deep learning, artificial intelligence and industrial control. Moreover, It provides the possibility of high-speed data transmission and exchange, pre-verification and post-application of data processing. We believe that such a product is ideal for students, engineers and other groups who are engaged in the development of MPSoCs.

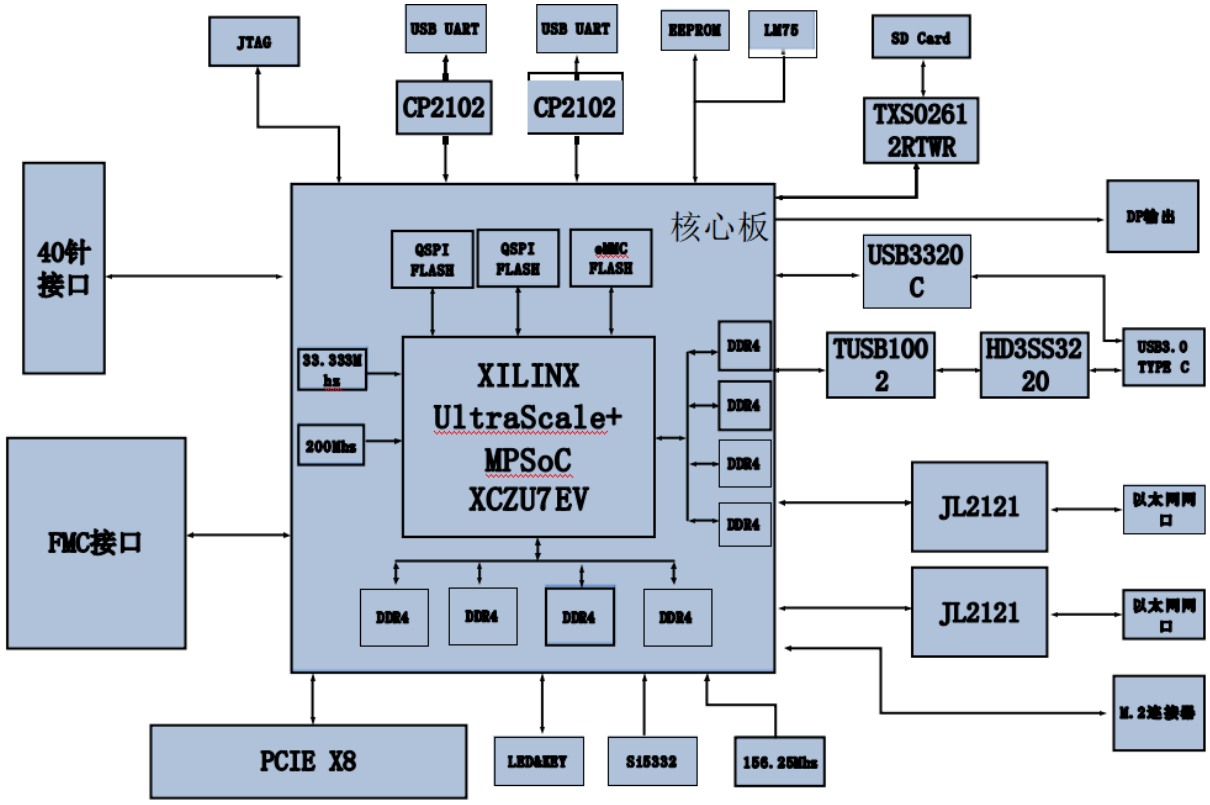

ALINX
FMC

1. FPGA Development Board Introduction

The Z7-P's core board is mainly composed of the minimum system of ZU7EV + 8 DDR4 + eMMC +2 QSPI FLASH. Its main chip adopts Xilinx's Zynq UltraScale+ MPSoCs series' chip, model XCZU7EV—2FFVC1156I. The ZU7EV chip can be divided into a Processor System (PS) and a Programmable Logic (PL). The PS and PL sides have attached four pieces of DDR4 chips respectively, each DDR4 chip's capacity is up to 1G btyes, which enables the ARM system and the FPGA system to process and store data independently. The 8GB eMMC FLASH memory chip and 2 pieces of 256Mb QSPI FLASH chips on the PS side are used to statically store the MPSoCs' operating system, file system and user data.

The Z7-P's carrier board has extended a rich set of peripheral interfaces for the core board, including 1 FMC HPC, 1 M.2 SSD interface, 1 mini_DP interface, 1 USB3.0 interface, 2 Gigabit Ethernet interfaces, 1 FMC HPC interface, 1 40-pin interface, 2 UART interfaces, 1 PCIEX8 gold finger, 1 EEPROM, 1 temperature sensor and some key LEDs.

The following is the structure diagram of the whole development system:



With this diagram, we can see all the interfaces and functions that our development platform contains.

- ZU7EV core board

It is composed of ZU7EV+4GB DDR4 (PS) +4GB DDR4 (PL) +8GB eMMC FLASH + 512Mb QSPI FLASH. It also has 2 crystal oscillator to provide clock, one single-ended 33.3333MHz crystal oscillator is supplied to PS system, the other differential 200MHz crystal oscillator is supplied to the PL logic DDR reference clock.

- PCIe x8 interface

It supports PCI Express 3.0 standard, provides standard PCIex8 high-speed data transmission interface, and single-channel communication rate can up to 8GBaud.

- M.2 interface

One PCIEx1 standard M.2 interface, used to connect the M.2 SSD with a

communication speed up to 6Gbps.

- DP output port

One standard Display Port output display port for displaying video images. The maximum output is 4K@30Hz or 1080P@60Hz.

- USB3.0 interface

One USB3.0 TYPE C interface supports HOST, SLAVE and OTG modes.

- Gigabit Ethernet interface

Two 10/100M/1000M Ethernet RJ45 interfaces, one each for PS and PL, used for Ethernet data exchange with computers or other network devices.

- USB Uart interface

Two Uart to USB interfaces, one each for PS and PL, used for communication with PC for user-friendly debugging. The serial chip adopts the USB-UART chip of Silicon Labs CP2102GM, and the USB interface adopts the MINI USB interface.

- Micro SD card holder

One MicroSD card holder to store operating system images and file systems.

- FMC expansion port

One standard FMC HPC expansion ports that can externally be connected to XILINX's or our various FMC modules (HDMI input/output module, binocular camera module, high-speed AD module, etc.).

- JTAG Debugging port

One 10-pin 2.54mm standard JTAG port used for downloading and debugging FPGA program. Users can debug and download ZU7EV system through XILINX downloader.

- Temperature and humidity sensor

An on-board temperature and humidity sensor chip (LM75) is used to detect the ambient temperature and humidity of the board.

- EEPROM

One piece of EEPROM 24LC04 with IIC interface.

- RTC Real-Time Clock

One built-in RTC real-time clock.

- LED light

Seven LEDs, one is mounted on the core board and another 6 are mounted on the carrier board. Core board contains 1 power indicator, 1 DONE configuration indicator, and 4 user indicators (two are mounted on the side of the board).

- Keys

3 keys in total, one is a reset key, 2 are user keys.

2. ACU7EVB Core Board Introduction

2.1 Introduction

ZYNQ chip of ACU7EVB (core board model, the same below) core board is XCZU7EV-2FFVC1156I of XILINX company's Zynq UltraScale+ MPSoCs EV series.

This core board uses 8 Micron DDR4 chips (MT40A512M16GE), four on PS side and four on PL side, which form a 64-bit data bus bandwidth and a capacity of 4GB. The DDR4 SDRAM can run at a maximum speed of 1200MHz (data rate of 2400Mbps). In addition, the core board is also integrated with two 256MBit QSPI FLASH and 8GB eMMC FLASH chips, which are used to start storage configuration and system files.

In order to connect with the backboard, the four board-to-board connectors of the core board extend the PS-side USB2.0 interface, Gigabit Ethernet interface, SD card interface and other remaining MIO ports; Four pairs of PS MGT high-speed transceiver interfaces; As well as PL-side 16-channels MGT transceiver and almost all I/O ports (HP I/O:134, HD I/O: 46). The line between the XCZU7EV chip and interfaces is processed with equal length and different length, and the size of the core board is only 80*60 (mm), which is very suitable for the secondary development.

ACU7EVB Core Board Top View

2.2 ZYNQ Chip

The development board uses chips (model: XCZU7EV-2FFVC1156I) from Xilinx's Zynq UltraScale+MPSoCs EV series. The ZU7EV chip's PS system integrates four ARM Cortex™-A53 processors with a speed of up to 1.3Ghz and supports level-2 Cache; in addition, ZU7EV also contains two Cortex-R5 processors with a speed of up to 533Mhz.

The ZU7EV chip supports 32-bit or 64-bit DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 memory chips, and has rich high-speed interfaces on the PS side, such as PCIE Gen2, USB3.0, SATA 3.1, and DisplayPort. It also supports USB2.0, Gigabit Ethernet, SD/SDIO, I2C, CAN, UART, GPIO and other interfaces. The PL side contains a wealth of programmable logic unit, DSP and internal RAM.

Figure 2-2-1 shows the Overall Block Diagram of the ZU7EV chip:

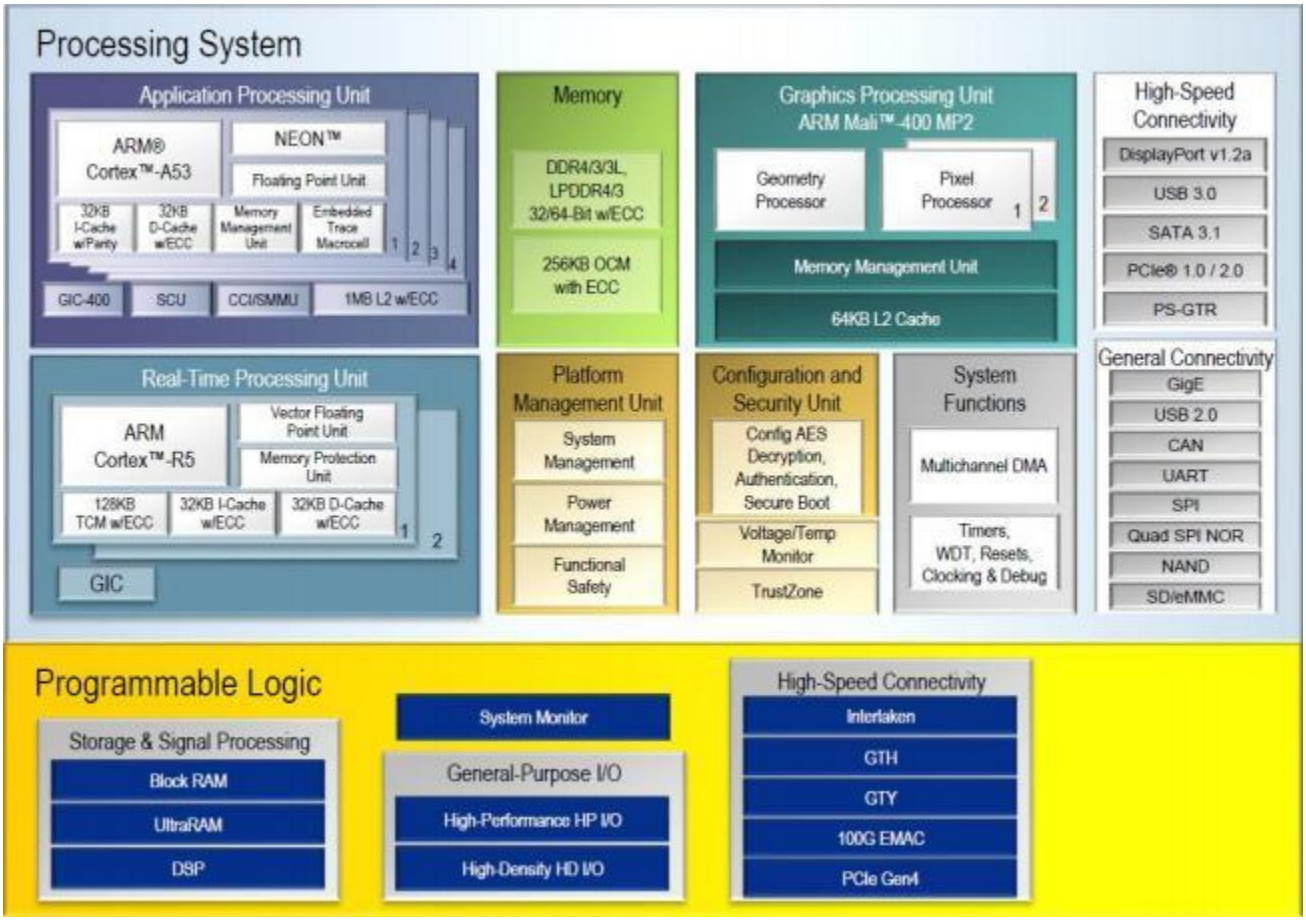


Figure 2-2-1: Overall block diagram of ZYNQ ZU7EV chip

The main parameters of the PS system are as follows:

- ARM quad-core Cortex™-A53 processor with a speed of up to 1.3GHz, each CPU 32KB level-1 instruction and data cache, 1MB level 2 cache, shared by 2 CPUs.
- ARM dual-core Cortex-R5 processor with a speed of up to 533MHz, each CPU 32KB level-1 instruction and data cache, and 128K tightly coupled memory.
- Image video processor Mali-400 MP2 with a speed of up to 677MHz, and 64KB level-2 cache.
- External memory interface: supports 32/64bit DDR4/3/3L, LPDDR4/3 interface.
- Static memory interface: supports NAND, 2xQuad-SPI FLASH.

- High-speed connection interface, supports PCIe Gen2 x 4, 2 x USB3.0, Sata 3.1, Display Port, 4 x Tri-mode Gigabit Ethernet.
- Common connection interfaces: 2 x USB2.0, 2 x SD/SDIO, 2 x UART, 2 x CAN 2.0B, 2 x I2C, 2 x SPI, 4 x 32b GPIO.
- Power management: supports the division of Full/Low/PL/Battery power supplies.
- Encryption algorithm: RSA, AES, and SHA.
- System monitoring: 10-bit 1Mbps AD sampling for temperature and voltage detection.

The main parameters of the PL logic are as follows:

- System Logic Cells: 504K;
- CLB flip-flops: 460.8K;
- CLBLUTs: 230.4K;
- Block RAM: 11Mb;
- Clock Management Units (CMTs): 8;
- DSP Slices: 1728;
- GTH 16.3Gb/s transceivers: 24;

The XCZU7EV-2FFVC1156I chip's speed grade is -2, industrial grade, and is packaged as FFVC1156.

2.3 DDR4 DRAM

The ACU7EVB core board is equipped with eight Micron's 1GB DDR4 chips (model

MT40A512M16LY-062E), among which 4 DDR4 chips are mounted on the PS side to form a 64-bit data bus bandwidth and 4GB capacity, while the other 4 DDR4 chips are mounted on the PL side to form a 64-bit data bus bandwidth and 4GB capacity. The DDR4 SDRAM on the PS side can run at a maximum speed of 1200MHz (data rate of 2400Mbps) and 4 pieces of DDR4 memory systems are directly connected to the memory interface of BANK504 on the PS side. And DDR4 SDRAM on the PL side can also run at a maximum speed of 1200MHz (data rate of 2400Mbps) and 4 pieces of DDR4 memory systems are directly connected to the interface of FPGA's BANK66, BANK67 and BANK68.

The specific configuration of DDR4 SDRAM is shown in Table 2-3-1.

Position	Bit Number	Chip Model	Capacity	Factory
PS	U4,U5,U6,U7	MT40A512M16LY-062E	512M x 16bit	Micron
PL	U17,U19,U45,U46	MT40A512M16LY-062E	512M x 16bit	Micron

Table 2-3-1: DDR4 SDRAM Configuration

The hardware design of DDR4 requires strict consideration of signal integrity, so we have fully considered the matching resistance/terminal resistance, trace impedance control, and trace length control when designing circuit and PCB to ensure high-speed and stable operation of DDR4.

Figure 2-3-1 shows the hardware connection of DDR4 on the PS side:

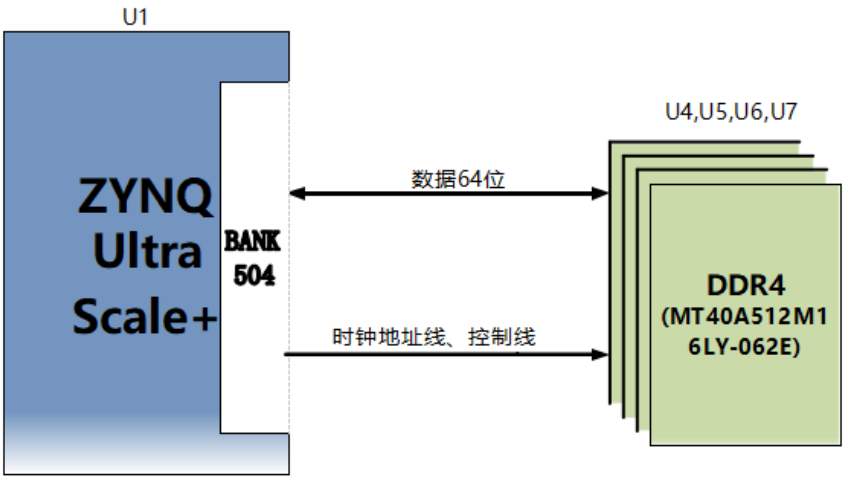


Figure 2-3-1: DDR4 DRAM schematic diagram

Figure 2-3-2 shows the hardware connection of DDR4 DRAM on the PL Side:

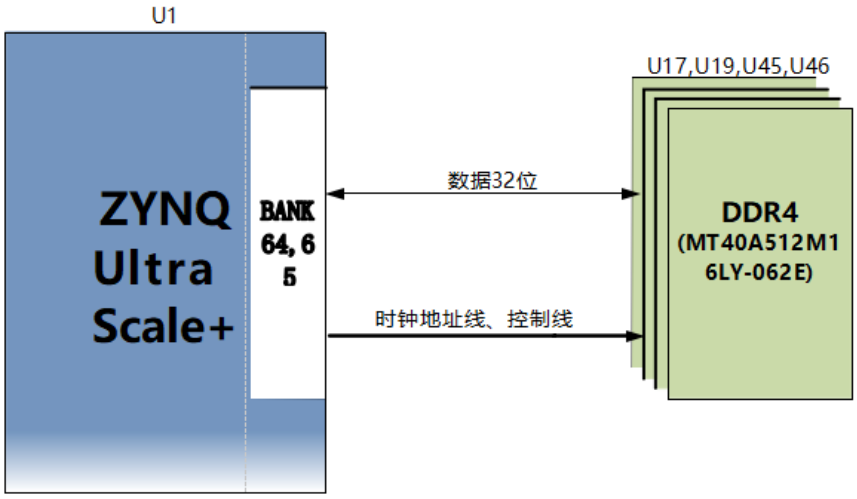


Figure 2-3-2: DDR4 DRAM schematic diagram

PS Side DDR4 SDRAM pin assignment:

Signal Name	Pin Name	Pin Number
PS_DDR4_DQS0_N	PS_DDR_DQS_N0_504	AN27
PS_DDR4_DQS0_P	PS_DDR_DQS_P0_504	AN26
PS_DDR4_DQS1_N	PS_DDR_DQS_N1_504	AP30
PS_DDR4_DQS1_P	PS_DDR_DQS_P1_504	AN29
PS_DDR4_DQS2_N	PS_DDR_DQS_N2_504	AJ26
PS_DDR4_DQS2_P	PS_DDR_DQS_P2_504	AH26

PS_DDR4_DQS3_N	PS_DDR_DQS_N3_504	AK29
PS_DDR4_DQS3_P	PS_DDR_DQS_P3_504	AK28
PS_DDR4_DQS4_N	PS_DDR_DQS_N4_504	AD31
PS_DDR4_DQS4_P	PS_DDR_DQS_P4_504	AD30
PS_DDR4_DQS5_N	PS_DDR_DQS_N5_504	Y28
PS_DDR4_DQS5_P	PS_DDR_DQS_P5_504	Y27
PS_DDR4_DQS6_N	PS_DDR_DQS_N6_504	AB34
PS_DDR4_DQS6_P	PS_DDR_DQS_P6_504	AB33
PS_DDR4_DQS7_N	PS_DDR_DQS_N7_504	W32
PS_DDR4_DQS7_P	PS_DDR_DQS_P7_504	W31
PS_DDR4_DQ0	PS_DDR_DQ0_504	AP27
PS_DDR4_DQ1	PS_DDR_DQ1_504	AP25
PS_DDR4_DQ2	PS_DDR_DQ2_504	AP26
PS_DDR4_DQ3	PS_DDR_DQ3_504	AM26
PS_DDR4_DQ4	PS_DDR_DQ4_504	AP24
PS_DDR4_DQ5	PS_DDR_DQ5_504	AL25
PS_DDR4_DQ6	PS_DDR_DQ6_504	AM25
PS_DDR4_DQ7	PS_DDR_DQ7_504	AM24
PS_DDR4_DQ8	PS_DDR_DQ8_504	AM28
PS_DDR4_DQ9	PS_DDR_DQ9_504	AN28
PS_DDR4_DQ10	PS_DDR_DQ10_504	AP29
PS_DDR4_DQ11	PS_DDR_DQ11_504	AP28
PS_DDR4_DQ12	PS_DDR_DQ12_504	AM31
PS_DDR4_DQ13	PS_DDR_DQ13_504	AP31
PS_DDR4_DQ14	PS_DDR_DQ14_504	AN31
PS_DDR4_DQ15	PS_DDR_DQ15_504	AM30
PS_DDR4_DQ16	PS_DDR_DQ16_504	AF25
PS_DDR4_DQ17	PS_DDR_DQ17_504	AG25
PS_DDR4_DQ18	PS_DDR_DQ18_504	AG26
PS_DDR4_DQ19	PS_DDR_DQ19_504	AJ25
PS_DDR4_DQ20	PS_DDR_DQ20_504	AG24

PS_DDR4_DQ21	PS_DDR_DQ21_504	AK25
PS_DDR4_DQ22	PS_DDR_DQ22_504	AJ24
PS_DDR4_DQ23	PS_DDR_DQ23_504	AK24
PS_DDR4_DQ24	PS_DDR_DQ24_504	AH28
PS_DDR4_DQ25	PS_DDR_DQ25_504	AH27
PS_DDR4_DQ26	PS_DDR_DQ26_504	AJ27
PS_DDR4_DQ27	PS_DDR_DQ27_504	AK27
PS_DDR4_DQ28	PS_DDR_DQ28_504	AL26
PS_DDR4_DQ29	PS_DDR_DQ29_504	AL27
PS_DDR4_DQ30	PS_DDR_DQ30_504	AH29
PS_DDR4_DQ31	PS_DDR_DQ31_504	AL28
PS_DDR4_DQ32	PS_DDR_DQ32_504	AB29
PS_DDR4_DQ33	PS_DDR_DQ33_504	AB30
PS_DDR4_DQ34	PS_DDR_DQ34_504	AC29
PS_DDR4_DQ35	PS_DDR_DQ35_504	AD32
PS_DDR4_DQ36	PS_DDR_DQ36_504	AC31
PS_DDR4_DQ37	PS_DDR_DQ37_504	AE30
PS_DDR4_DQ38	PS_DDR_DQ38_504	AC28
PS_DDR4_DQ39	PS_DDR_DQ39_504	AE29
PS_DDR4_DQ40	PS_DDR_DQ40_504	AC27
PS_DDR4_DQ41	PS_DDR_DQ41_504	AA27
PS_DDR4_DQ42	PS_DDR_DQ42_504	AA28
PS_DDR4_DQ43	PS_DDR_DQ43_504	AB28
PS_DDR4_DQ44	PS_DDR_DQ44_504	W27
PS_DDR4_DQ45	PS_DDR_DQ45_504	W29
PS_DDR4_DQ46	PS_DDR_DQ46_504	W28
PS_DDR4_DQ47	PS_DDR_DQ47_504	V27
PS_DDR4_DQ48	PS_DDR_DQ48_504	AA32
PS_DDR4_DQ49	PS_DDR_DQ49_504	AA33
PS_DDR4_DQ50	PS_DDR_DQ50_504	AA34
PS_DDR4_DQ51	PS_DDR_DQ51_504	AE34
PS_DDR4_DQ52	PS_DDR_DQ52_504	AD34

PS_DDR4_DQ53	PS_DDR_DQ53_504	AB31
PS_DDR4_DQ54	PS_DDR_DQ54_504	AC34
PS_DDR4_DQ55	PS_DDR_DQ55_504	AC33
PS_DDR4_DQ56	PS_DDR_DQ56_504	AA30
PS_DDR4_DQ57	PS_DDR_DQ57_504	Y30
PS_DDR4_DQ58	PS_DDR_DQ58_504	AA31
PS_DDR4_DQ59	PS_DDR_DQ59_504	W30
PS_DDR4_DQ60	PS_DDR_DQ60_504	Y33
PS_DDR4_DQ61	PS_DDR_DQ61_504	W33
PS_DDR4_DQ62	PS_DDR_DQ62_504	W34
PS_DDR4_DQ63	PS_DDR_DQ63_504	Y34
PS_DDR4_DM0	PS_DDR_DM0_504	AN24
PS_DDR4_DM1	PS_DDR_DM1_504	AM29
PS_DDR4_DM2	PS_DDR_DM2_504	AH24
PS_DDR4_DM3	PS_DDR_DM3_504	AJ29
PS_DDR4_DM4	PS_DDR_DM4_504	AD29
PS_DDR4_DM5	PS_DDR_DM5_504	Y29
PS_DDR4_DM6	PS_DDR_DM6_504	AC32
PS_DDR4_DM7	PS_DDR_DM7_504	Y32
PS_DDR4_A0	PS_DDR_A0_504	AN34
PS_DDR4_A1	PS_DDR_A1_504	AM34
PS_DDR4_A2	PS_DDR_A2_504	AM33
PS_DDR4_A3	PS_DDR_A3_504	AL34
PS_DDR4_A4	PS_DDR_A4_504	AL33
PS_DDR4_A5	PS_DDR_A5_504	AK33
PS_DDR4_A6	PS_DDR_A6_504	AK30
PS_DDR4_A7	PS_DDR_A7_504	AJ30
PS_DDR4_A8	PS_DDR_A8_504	AJ31
PS_DDR4_A9	PS_DDR_A9_504	AH31
PS_DDR4_A10	PS_DDR_A10_504	AG31
PS_DDR4_A11	PS_DDR_A11_504	AF31

PS_DDR4_A12	PS_DDR_A12_504	AG30
PS_DDR4_A13	PS_DDR_A13_504	AF30
PS_DDR4_ODT0	PS_DDR_ODT0_504	AP32
PS_DDR4_PARITY	PS_DDR_PARITY_504	AA26
PS_DDR4_RAS_B	PS_DDR_A16_504	AF28
PS_DDR4_RESET_B	PS_DDR_RAM_RST_N_504	AD26
PS_DDR4_WE_B	PS_DDR_A14_504	AG29
PS_DDR4_ACT_B	PS_DDR_ACT_N_504	AE25
PS_DDR4_ALERT_B	PS_DDR_ALERT_N_504	AB26
PS_DDR4_BA0	PS_DDR_BA0_504	AE27
PS_DDR4_BA1	PS_DDR_BA1_504	AE28
PS_DDR4_BG0	PS_DDR_BG0_504	AD27
PS_DDR4_CAS_B	PS_DDR_A15_504	AG28
PS_DDR4_CKE0	PS_DDR_CKE0_504	AN33
PS_DDR4_CS0_B	PS_DDR_CS_N0_504	AP33
PS_DDR4_CLK0_N	PS_DDR_CK_N0_504	AN32
PS_DDR4_CLK0_P	PS_DDR_CK0_504	AL31

PL Side DDR4 SDRAM pin assignment:

Signal Name	Pin Name	Pin Number
PL_DDR4_DQS0_N	IO_L10N_T1U_N7_QBC_AD4N_67	F13
PL_DDR4_DQS0_P	IO_L10P_T1U_N6_QBC_AD4P_67	G14
PL_DDR4_DQS1_N	IO_L4N_T0U_N7_DBC_AD7N_67	B13
PL_DDR4_DQS1_P	IO_L4P_T0U_N6_DBC_AD7P_67	B14
PL_DDR4_DQS2_N	IO_L16N_T2U_N7_QBC_AD3N_67	H17
PL_DDR4_DQS2_P	IO_L16P_T2U_N6_QBC_AD3P_67	H18
PL_DDR4_DQS3_N	IO_L22N_T3U_N7_DBC_AD0N_67	K15
PL_DDR4_DQS3_P	IO_L22P_T3U_N6_DBC_AD0P_67	L15
PL_DDR4_DQS4_N	IO_L16N_T2U_N7_QBC_AD3N_68	D10
PL_DDR4_DQS4_P	IO_L16P_T2U_N6_QBC_AD3P_68	D11

PL_DDR4_DQS5_N	IO_L22N_T3U_N7_DBC_AD0N_68	A10
PL_DDR4_DQS5_P	IO_L22P_T3U_N6_DBC_AD0P_68	B10
PL_DDR4_DQS6_N	IO_L10N_T1U_N7_QBC_AD4N_68	D9
PL_DDR4_DQS6_P	IO_L10P_T1U_N6_QBC_AD4P_68	E9
PL_DDR4_DQS7_N	IO_L4N_T0U_N7_DBC_AD7N_68	J11
PL_DDR4_DQS7_P	IO_L4P_T0U_N6_DBC_AD7P_68	K12
PL_DDR4_DQ0	IO_L9N_T1L_N5_AD12N_67	E17
PL_DDR4_DQ1	IO_L11P_T1U_N8_GC_67	D15
PL_DDR4_DQ2	IO_L8P_T1L_N2_AD5P_67	D17
PL_DDR4_DQ3	IO_L12N_T1U_N11_GC_67	E14
PL_DDR4_DQ4	IO_L9P_T1L_N4_AD12P_67	E18
PL_DDR4_DQ5	IO_L11N_T1U_N9_GC_67	D14
PL_DDR4_DQ6	IO_L12P_T1U_N10_GC_67	E15
PL_DDR4_DQ7	IO_L8N_T1L_N3_AD5N_67	C17
PL_DDR4_DQ8	IO_L2P_T0L_N2_67	B16
PL_DDR4_DQ9	IO_L6P_T0U_N10_AD6P_67	C13
PL_DDR4_DQ10	IO_L3P_T0L_N4_AD15P_67	A15
PL_DDR4_DQ11	IO_L5P_T0U_N8_AD14P_67	A13
PL_DDR4_DQ12	IO_L2N_T0L_N3_67	B15
PL_DDR4_DQ13	IO_L5N_T0U_N9_AD14N_67	A12
PL_DDR4_DQ14	IO_L3N_T0L_N5_AD15N_67	A14
PL_DDR4_DQ15	IO_L6N_T0U_N11_AD6N_67	C12
PL_DDR4_DQ16	IO_L15P_T2L_N4_AD11P_67	H19
PL_DDR4_DQ17	IO_L18P_T2U_N10_AD2P_67	H16
PL_DDR4_DQ18	IO_L17P_T2U_N8_AD10P_67	G18
PL_DDR4_DQ19	IO_L18N_T2U_N11_AD2N_67	G16
PL_DDR4_DQ20	IO_L15N_T2L_N5_AD11N_67	G19
PL_DDR4_DQ21	IO_L14N_T2L_N3_GC_67	F15
PL_DDR4_DQ22	IO_L17N_T2U_N9_AD10N_67	F18
PL_DDR4_DQ23	IO_L14P_T2L_N2_GC_67	G15
PL_DDR4_DQ24	IO_L24N_T3U_N11_67	L16

PL_DDR4_DQ25	IO_L21N_T3L_N5_AD8N_67	J17
PL_DDR4_DQ26	IO_L23P_T3U_N8_67	K19
PL_DDR4_DQ27	IO_L21P_T3L_N4_AD8P_67	K17
PL_DDR4_DQ28	IO_L24P_T3U_N10_67	L17
PL_DDR4_DQ29	IO_L20P_T3L_N2_AD1P_67	J16
PL_DDR4_DQ30	IO_L23N_T3U_N9_67	K18
PL_DDR4_DQ31	IO_L20N_T3L_N3_AD1N_67	J15
PL_DDR4_DQ32	IO_L18N_T2U_N11_AD2N_68	C11
PL_DDR4_DQ33	IO_L17P_T2U_N8_AD10P_68	F12
PL_DDR4_DQ34	IO_L17N_T2U_N9_AD10N_68	E12
PL_DDR4_DQ35	IO_L14P_T2L_N2_GC_68	F11
PL_DDR4_DQ36	IO_L18P_T2U_N10_AD2P_68	D12
PL_DDR4_DQ37	IO_L15N_T2L_N5_AD11N_68	H12
PL_DDR4_DQ38	IO_L15P_T2L_N4_AD11P_68	H13
PL_DDR4_DQ39	IO_L14N_T2L_N3_GC_68	E10
PL_DDR4_DQ40	IO_L20N_T3L_N3_AD1N_68	B8
PL_DDR4_DQ41	IO_L21N_T3L_N5_AD8N_68	A6
PL_DDR4_DQ42	IO_L20P_T3L_N2_AD1P_68	B9
PL_DDR4_DQ43	IO_L23N_T3U_N9_68	A7
PL_DDR4_DQ44	IO_L24P_T3U_N10_68	B11
PL_DDR4_DQ45	IO_L21P_T3L_N4_AD8P_68	B6
PL_DDR4_DQ46	IO_L24N_T3U_N11_68	A11
PL_DDR4_DQ47	IO_L23P_T3U_N8_68	A8
PL_DDR4_DQ48	IO_L12P_T1U_N10_GC_68	G10
PL_DDR4_DQ49	IO_L9P_T1L_N4_AD12P_68	F8
PL_DDR4_DQ50	IO_L8N_T1L_N3_AD5N_68	C8
PL_DDR4_DQ51	IO_L9N_T1L_N5_AD12N_68	E8
PL_DDR4_DQ52	IO_L12N_T1U_N11_GC_68	F10
PL_DDR4_DQ53	IO_L11P_T1U_N8_GC_68	H9
PL_DDR4_DQ54	IO_L8P_T1L_N2_AD5P_68	C9
PL_DDR4_DQ55	IO_L11N_T1U_N9_GC_68	G9
PL_DDR4_DQ56	IO_L5N_T0U_N9_AD14N_68	J14

PL_DDR4_DQ57	IO_L6N_T0U_N11_AD6N_68	K13
PL_DDR4_DQ58	IO_L5P_T0U_N8_AD14P_68	K14
PL_DDR4_DQ59	IO_L2P_T0L_N2_68	K10
PL_DDR4_DQ60	IO_L6P_T0U_N10_AD6P_68	L14
PL_DDR4_DQ61	IO_L3P_T0L_N4_AD15P_68	L12
PL_DDR4_DQ62	IO_L2N_T0L_N3_68	J10
PL_DDR4_DQ63	IO_L3N_T0L_N5_AD15N_68	L11
PL_DDR4_DM0	IO_L7P_T1L_N0_QBC_AD13P_67	D16
PL_DDR4_DM1	IO_L1P_T0L_N0_DBC_67	A17
PL_DDR4_DM2	IO_L13P_T2L_N0_GC_QBC_67	F17
PL_DDR4_DM3	IO_L19P_T3L_N0_DBC_AD9P_67	L20
PL_DDR4_DM4	IO_L13P_T2L_N0_GC_QBC_68	H11
PL_DDR4_DM5	IO_L19P_T3L_N0_DBC_AD9P_68	C7
PL_DDR4_DM6	IO_L7P_T1L_N0_QBC_AD13P_68	F7
PL_DDR4_DM7	IO_L1P_T0L_N0_DBC_68	M13
PL_DDR4_A0	IO_L10P_T1U_N6_QBC_AD4P_66	AK8
PL_DDR4_A1	IO_L6P_T0U_N10_AD6P_66	AM9
PL_DDR4_A2	IO_L10N_T1U_N7_QBC_AD4N_66	AL8
PL_DDR4_A3	IO_L5N_T0U_N9_AD14N_66	AM10
PL_DDR4_A4	IO_L11N_T1U_N9_GC_66	AK10
PL_DDR4_A5	IO_L3N_T0L_N5_AD15N_66	AP11
PL_DDR4_A6	IO_L14N_T2L_N3_GC_66	AJ11
PL_DDR4_A7	IO_L4P_T0U_N6_DBC_AD7P_66	AN9
PL_DDR4_A8	IO_L17N_T2U_N9_AD10N_66	AG10
PL_DDR4_A9	IO_L6N_T0U_N11_AD6N_66	AM8
PL_DDR4_A10	IO_L11P_T1U_N8_GC_66	AJ10
PL_DDR4_A11	IO_L5P_T0U_N8_AD14P_66	AM11
PL_DDR4_A12	IO_L9N_T1L_N5_AD12N_66	AL12
PL_DDR4_A13	IO_L4N_T0U_N7_DBC_AD7N_66	AN8
PL_DDR4_ODT	IO_L16P_T2U_N6_QBC_AD3P_66	AG9
PL_DDR4_RAS_B	IO_L8P_T1L_N2_AD5P_66	AL11

PL_DDR4_RST	IO_L14P_T2L_N2_GC_66	AH11
PL_DDR4_WE_B	IO_L15N_T2L_N5_AD11N_66	AH13
PL_DDR4_ACT_B	IO_L16N_T2U_N7_QBC_AD3N_66	AH9
PL_DDR4_BA0	IO_L7N_T1L_N1_QBC_AD13N_66	AL13
PL_DDR4_BA1	IO_L3P_T0L_N4_AD15P_66	AN11
PL_DDR4_BG0	IO_L7P_T1L_N0_QBC_AD13P_66	AK13
PL_DDR4_CAS_B	IO_L8N_T1L_N3_AD5N_66	AL10
PL_DDR4_CKE	IO_L15P_T2L_N4_AD11P_66	AG13
PL_DDR4_CS_B	IO_L9P_T1L_N4_AD12P_66	AK12
PL_DDR4_CLK_N	IO_L13N_T2L_N1_GC_QBC_66	AJ12
PL_DDR4_CLK_P	IO_L13P_T2L_N0_GC_QBC_66	AH12

2.4 QSPI Flash

The ACU7EVB core board is equipped with two 256MBit Quad-SPI FLASH chips to form an 8-bit bandwidth data bus, the FLASH model is MT25QU256ABA1EW9, which uses the 1.8V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, it can be used as a boot device for the system to store the boot images of the system. These images mainly include FPGA bit files, ARM application code, and other user data files. The specific models and related parameters of QSPI FLASH are shown in Table 2-4-1.

Position	Model	Capacity	Factory
U2,U3	MT25QU256ABA1EW9	256M bit	Micron

Table 2-4-1: Model and parameter of QSPI FLASH

QSPI FLASH is connected to the GPIO port of the BANK500 in the PS side of the ZYNQ chip. In the system design, functions of these PS-side GPIO ports need to be configured as QSPI FLASH ports. Figure 2-4-1 shows the QSPI Flash in the schematic diagram.

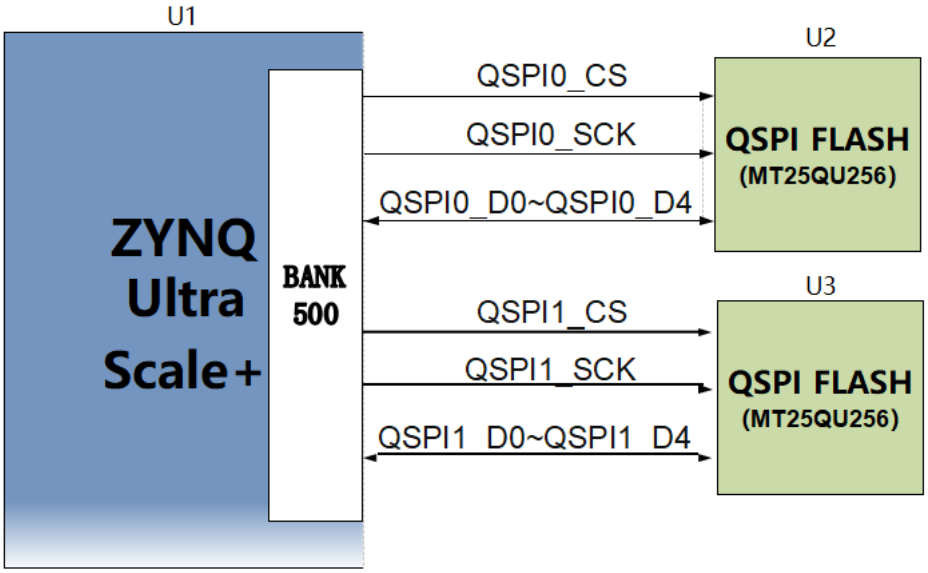


Figure 2-4-1: Connection diagram of QSPI Flash

Configuration chip pin assignments:

Signal Name	Pin Name	Pin Number
MIO0_QSPI0_SCLK	PS_MIO0_500	A24
MIO1_QSPI0_IO1	PS_MIO1_500	C24
MIO2_QSPI0_IO2	PS_MIO2_500	B24
MIO3_QSPI0_IO3	PS_MIO3_500	E25
MIO4_QSPI0_IO0	PS_MIO4_500	A25
MIO5_QSPI0_SS_B	PS_MIO5_500	D25
MIO10_QSPI1_IO2	PS_MIO10_500	F26
MIO11_QSPI1_IO3	PS_MIO11_500	B26
MIO12_QSPI1_SCLK	PS_MIO12_500	C27
MIO7_QSPI1_SS_B	PS_MIO7_500	B25
MIO8_QSPI1_IO0	PS_MIO8_500	D26
MIO9_QSPI1_IO1	PS_MIO9_500	C26

2.5 eMMC Flash

The ACU7EVB core board is equipped with a large-capacity 8GB eMMC FLASH chip (model: MTFC32GAPALBH-IT), which supports the HS-MMC interface under the JEDEC e-MMC V5.0 standard, and the level supports 1.8V or 3.3V. The data width of eMMC FLASH and ZYNQ connection is 8bit. Due to the large-capacity and non-volatile characteristics of eMMC FLASH, it can be used as a large-capacity storage device in the ZYNQ system, such as storing ARM applications, system files and other user data files The specific models and related parameters of eMMC FLASH are shown in Table 2-5-1.

Position	Model	Capacity	Factory
U8	MTFC8GAKAJCN-4M	8G Byte	Micron

Table 2-5-1: Model and parameters of eMMC Flash

The eMMC FLASH is connected to the GPIO port of the PS-side BANK500 of the ZYNQ UltraScale+. In the system design, it is necessary to configure the GPIO port function of the PS side as an EMMC interface. Figure 2-5-1 shows the part of eMMC Flash in the schematic diagram.

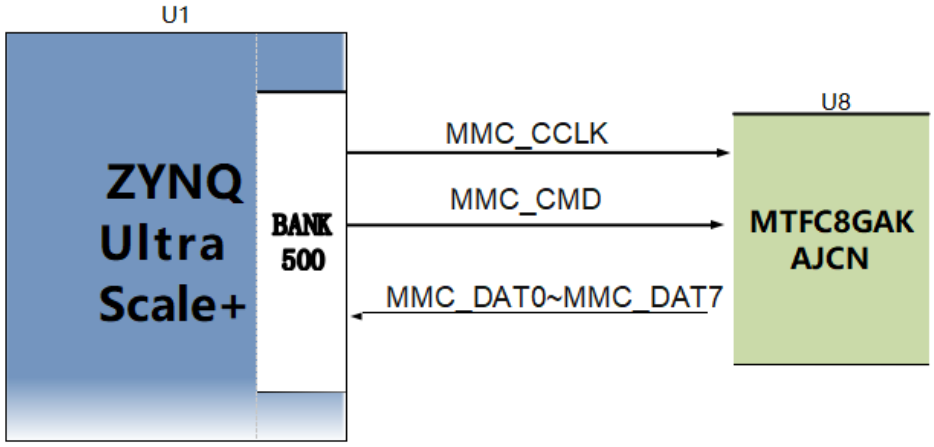


Figure 2-5-1: eMMC Flash connection diagram

Configuration Chip pin assignment:

Signal Name	Pin Name	Pin Number
MMC_CCLK	PS_MIO22_500	F28
MMC_CMD	PS_MIO21_500	C28
MMC_DAT0	PS_MIO13_500	D27
MMC_DAT1	PS_MIO14_500	A27
MMC_DAT2	PS_MIO15_500	E27
MMC_DAT3	PS_MIO16_500	A28
MMC_DAT4	PS_MIO17_500	C29
MMC_DAT5	PS_MIO18_500	F27
MMC_DAT6	PS_MIO19_500	B28
MMC_DAT7	PS_MIO20_500	E29
MMC_RSTN	PS_MIO23_500	B29

2.6 Clock Configuration

The core board provides reference clock and RTC real-time clock for PS system and PL logic respectively, so that PS system and PL logic can work independently. Figure 2-6-1 the schematic diagram of the clock circuit design:

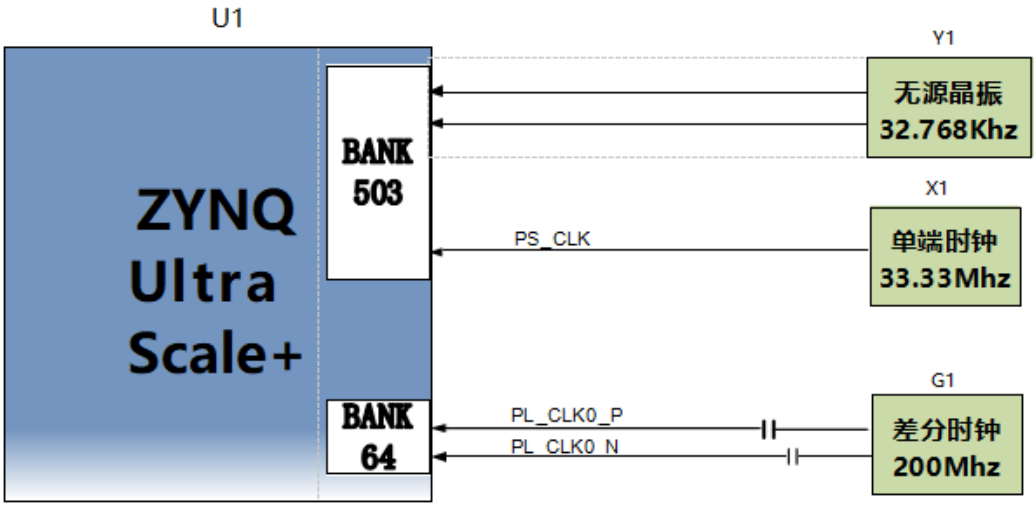


Figure 2-6-1: Core Board Clock Source

PS System RTC Real-Time Clock

The passive crystal Y1 on the core board provides a 32.768KHz real-time clock source for the PS system. The crystal is connected to the pins of PS_PADI_503 and PS_PADO_503 of the BANK503 of the ZYNQ chip. Figure 2-6-2 shows the schematic diagram.

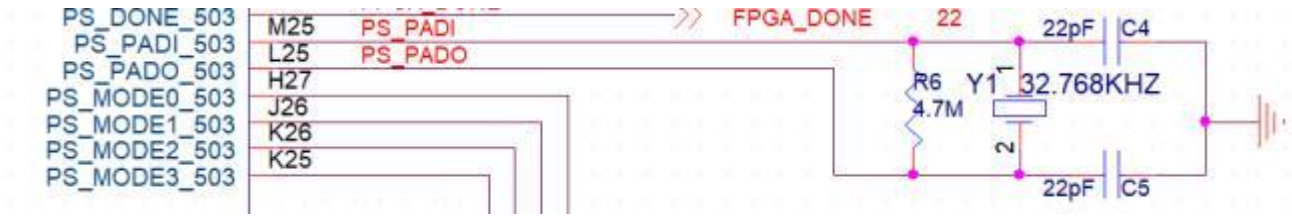


Figure 2-6-2: The passive crystal of RTC

Clock pin assignment:

Signal Name	Pin
PS_PADI_503	M25
PS_PADO_503	L25

PS system clock source:

The X1 crystal oscillator on the core board provides 33.333MHz clock input for the

PS system. The input of the clock is connected to the pin of the PS_REF_CLK_503 of the BANK503 of the ZYNQ chip. Figure 2-6-3 shows the schematic diagram.

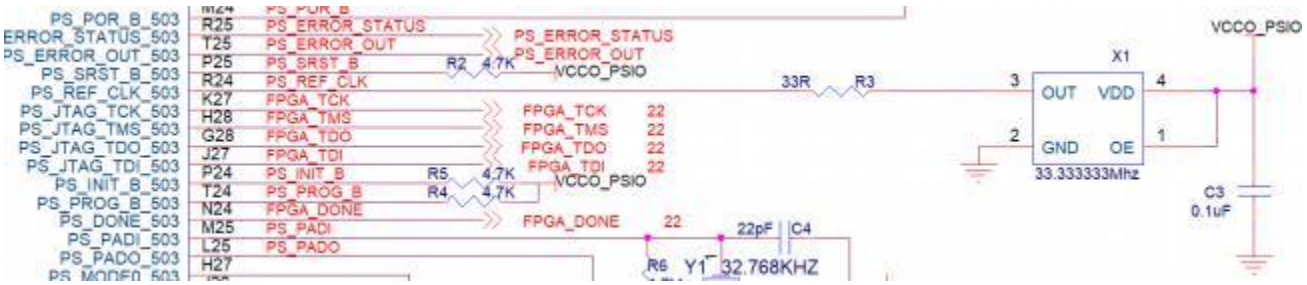


Figure 2-6-3: Active crystal oscillator in the PS

Clock pin assignment:

Signal Name	Pin
PS_REF_CLK	R24

PL system clock source:

A differential 200MHz PL system clock source is provided on the board for the reference clock of the DDR4 controller. The crystal output is connected to PL BANK64's Global clock (MRCC), which can be used to drive DDR4 controllers and user logic circuits within the FPGA. Figure 2-6-4 shows the schematic diagram of the clock source.

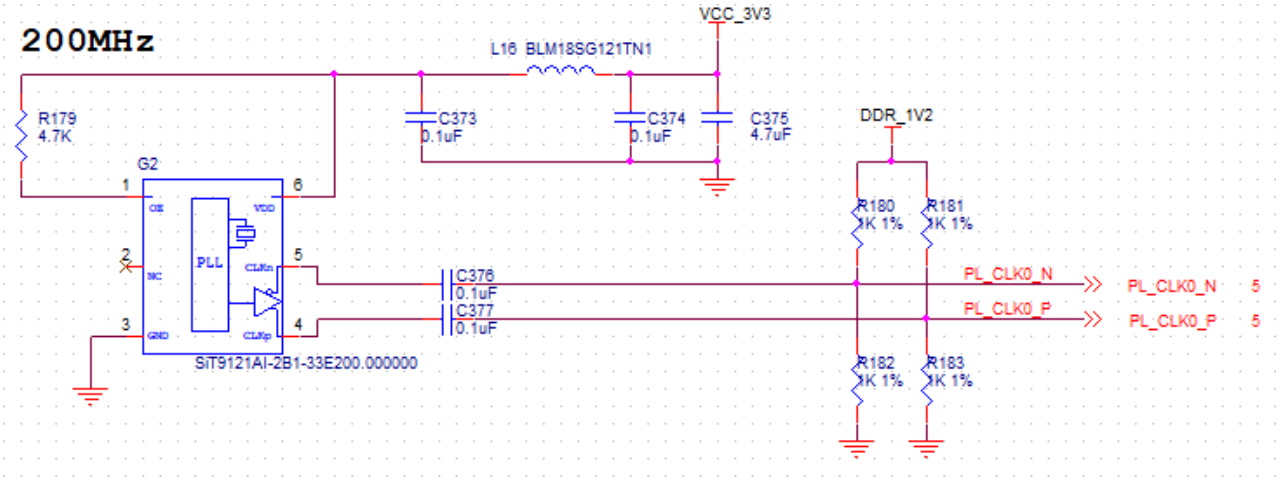


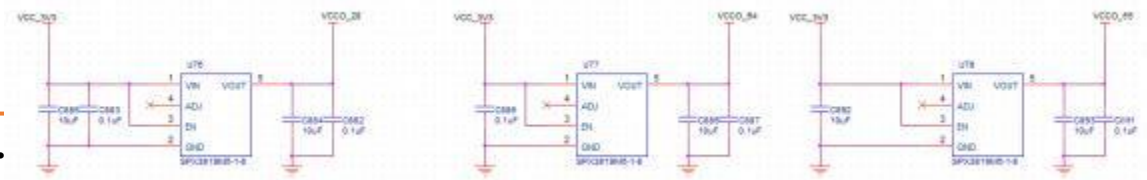
Figure 2-6-4: PL system clock source

PL Clock pin assignment:

Signal Name	Pin
PL_CLK0_P	AJ9
PL_CLK0_N	AK5

2.7 Power Supply

The power supply voltage of the ACU7EVB core board is +12V, and the core board is powered by connecting to the carrier board. On the core board, two MYMGM1R824ELA5RP power chips are connected in parallel to achieve 50A current to provide XCZU7EV with core power supply of 0.85V. The power supply of BANK28, BANK64 and BANK65 is generated by LDO chips, all of which are 1.8V by default. Users can replace the LDO to change the level of the IO (Note that the power supply of these BANKs cannot be higher than 1.8V).



In addition, a PMIC chip TPS6508640 is used on the board to generate all other power supplies required by XCZU7EV chip. Please refer to the power supply chip manual to learn the power design of TPS6508640. Figure 2-7-1 shows the design diagram of TPS6508640:

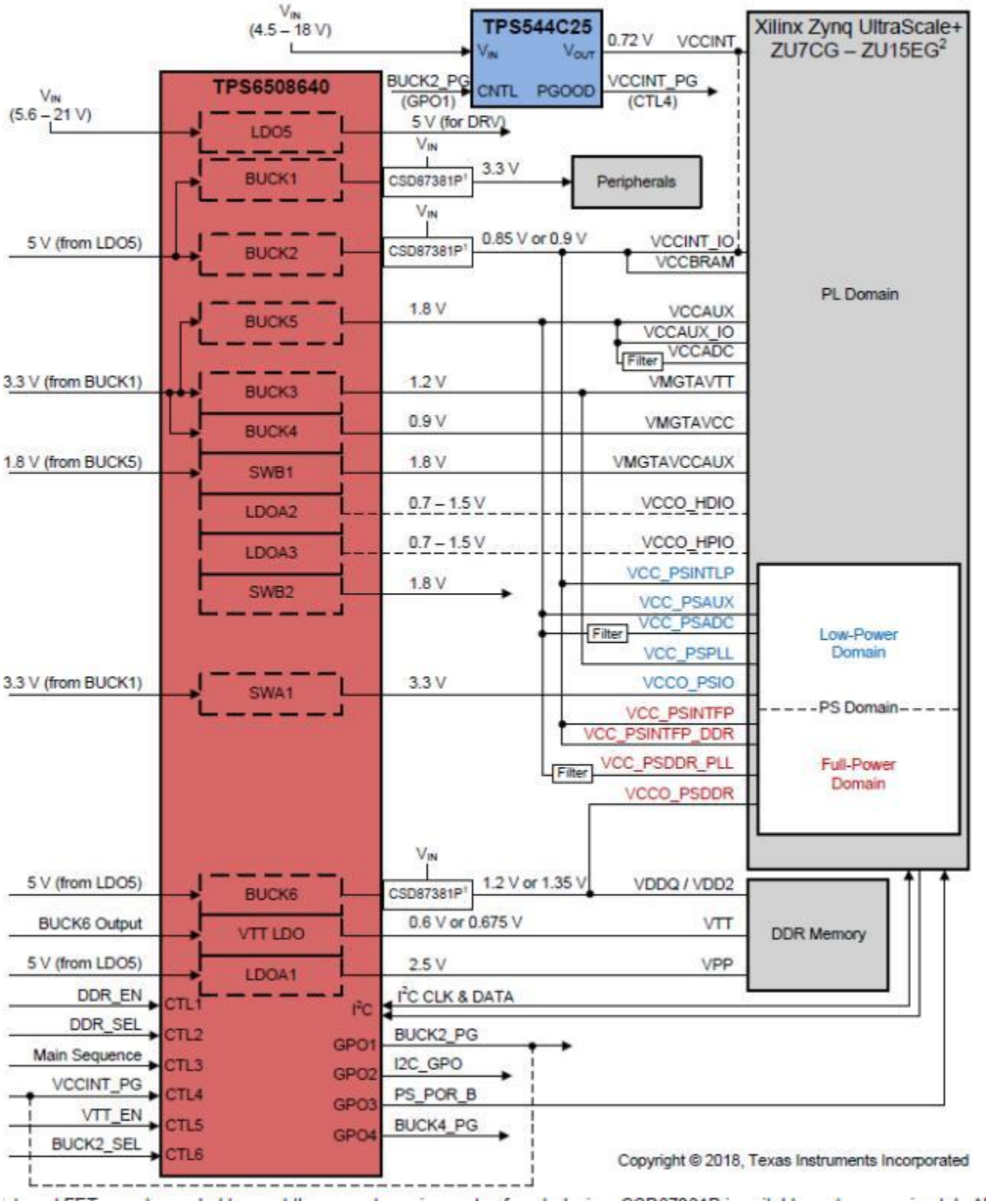
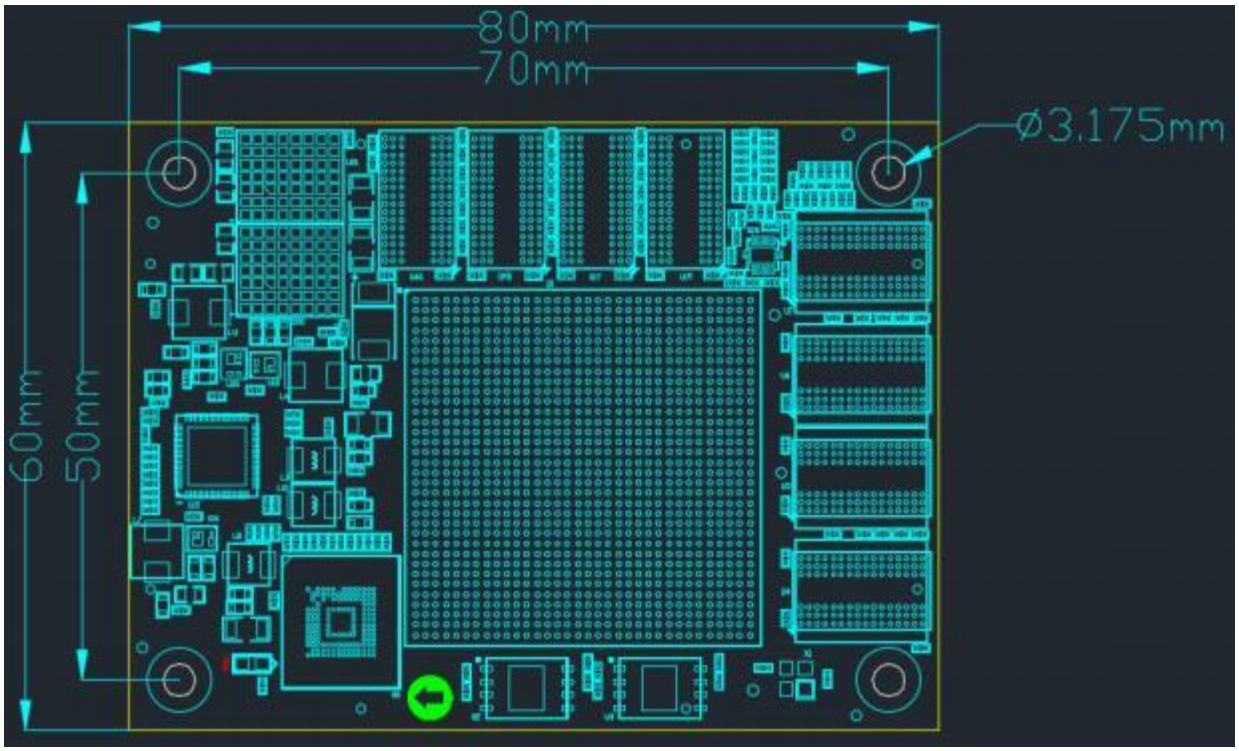


Figure 2-7-1: The design diagram of TPS6508640

2.8 Structure Diagram



Top View

2.9 Board-to-Board Connectors Pin Assignment

The core board is extended to a total of four high-speed expansion ports, using four 120Pin board-to-board connectors (J29~J32) to connect to the carrier board. The connectors use Panasonic AXK5A2137YG, and the connector model of corresponding carrier board is AXK6A2337YG.

J29 Connector

J29 connects +12V power supply, IO of BANK28,BANK87,BANK88 and part of MIO; level standard of BANK87 and BANK88 is 3.3V, level standard of BANK28 is 1.8V. The level of PS MIO is 1.8V standard.

J29 Pin	Signal Name	Pin Number	J29 Pin	Signal Name	Pin Number

1	+12V		2	+12V	
3	+12V		4	+12V	
5	+12V		6	+12V	
7	+12V		8	+12V	
9	+12V		10	+12V	
11	+12V		12	+12V	
13	GND		14	GND	
15	B88_L2_N	B1	16	B88_L1_N	D1
17	B88_L2_P	C1	18	B88_L1_P	E1
19	GND		20	GND	
21	B88_L5_N	C2	22	B88_L4_N	E2
23	B88_L5_P	D2	24	B88_L4_P	E3
25	B88_L8_N	D4	26	B88_L3_N	A2
27	B88_L8_P	E4	28	B88_L3_P	A3
29	GND		30	GND	
31	B88_L7_N	B4	32	B88_L6_N	B3
33	B88_L7_P	C4	34	B88_L6_P	C3
35	B88_L9_N	F4	36	B88_L10_N	A5
37	B88_L9_P	F5	38	B88_L10_P	B5
39	GND		40	GND	
41	B88_L11_N	D5	42	B88_L12_N	E5
43	B88_L11_P	D6	44	B88_L12_P	F6
45	B87_L9_N	J6	46	B87_L10_N	G6
47	B87_L9_P	J7	48	B87_L10_P	H6
49	GND		50	GND	
51	B87_L11_N	G7	52	B87_L3_N	M12
53	B87_L11_P	H7	54	B87_L3_P	N13

55	B87_L5_N	M8	56	B87_L12_N	G8
57	B87_L5_P	M9	58	B87_L12_P	H8
59	GND		60	GND	
61	B87_L8_N	J9	62	B87_L7_N	K8
63	B87_L8_P	K9	64	B87_L7_P	L8
65	B87_L2_N	N8	66	B87_L6_N	L10
67	B87_L2_P	N9	68	B87_L6_P	M10
69	GND		70	GND	
71	B87_L4_N	M11	72	B28_L7_N	D19
73	B87_L4_P	N11	74	B28_L7_P	E19
75	B28_L20_N	C19	76	B28_L9_N	D21
77	B28_L20_P	C18	78	B28_L9_P	D20
79	GND		80	GND	
81	B28_L19_N	A19	82	B28_L10_N	F20
83	B28_L19_P	A18	84	B28_L10_P	G20
85	B28_L21_N	A21	86	B28_L22_N	B19
87	B28_L21_P	A20	88	B28_L22_P	B18
89	GND		90	GND	
91	B28_L24_N	B21	92	B28_L15_N	C22
93	B28_L24_P	B20	94	B28_L15_P	C21
95	B28_L23_N	A23	96	B28_L17_N	C23
97	B28_L23_P	A22	98	B28_L17_P	D22
99	GND		100	GND	
101	PS_MIO43	E30	102	-	-
103	PS_MIO26	A29	104	PS_MIO32	B31
105	PS_MIO27	A30	106	PS_MIO35	C31
107	PS_MIO31	B30	108	PS_MIO36	C32

109	PS_MIO40	D31	110	PS_MIO37	C33
111	PS_MIO44	E32	112	PS_MIO29	A32
113	PS_MIO39	D30	114	PS_MIO30	A33
115	PS_MIO33	B33	116	PS_MIO34	B34
117	PS_MIO41	D32	118	PS_MIO42	D34
119	PS_MIO28	A31	120	PS_MIO38	C34

J30 Connector

The J30 connects to the transceiver signal of the BANK505 MGT, part of the PS MIO and the BANK28. The level standard of BANK28 is 1.8V. The level of PS MIO is 1.8V standard.

J30 Pin	Signal Name	Pin Number	J30 Pin	Signal Name	Pin Number
1	B28_L16_P	E24	2	SD_D2	F31
3	B28_L16_N	D24	4	SD_D3	F32
5	GND		6	GND	
7	B28_L11_N	E22	8	SD_CMD	F33
9	B28_L11_P	F22	10	SD_D0	E34
11	B28_L13_P	F23	12	SD_D1	F30
13	B28_L13_N	E23	14	SD_CLK	F34
15	GND		16	GND	
17	B28_L12_N	F21	18	SD_CD	E33
19	B28_L12_P	G21	20		
21	B28_L3_P	J21	22	USB_STP	H31
23	B28_L3_N	J22	24	USB_DIR	G30
25	GND		26	GND	

27	B28_L8_P	H21	28	USB_CLK	G29
29	B28_L8_N	H22	30	USB_NXT	G33
31			32	USB_DATA0	G34
33			34	USB_DATA1	H29
35	GND		36	GND	
37	B28_L18_N	G26	38	USB_DATA2	G31
39	B28_L18_P	G25	40	USB_DATA3	H32
41	B28_L14_N	G24	42	USB_DATA4	H33
43	B28_L14_P	G23	44	USB_DATA5	H34
45	GND		46	GND	
47			48	USB_DATA6	J29
49			50	USB_DATA7	J30
51			52	PHY1_TXD0	J32
53			54	PHY1_TXD1	J34
55	GND		56	GND	
57			58	PHY1_TXD2	K28
59			60	PHY1_TXD3	K29
61	PS_POR_B	M24	62	PHY1_TXCK	J31
63	FPGA_DONE	N24	64	PHY1_TXCTL	K30
65	GND		66	GND	
67	PS_MODE3	K25	68	PHY1_RXD3	L29
69	PS_MODE2	K26	70	PHY1_RXD2	K34
71	PS_MODE1	J26	72	PHY1_RXD1	K33
73	PS_MODE0	H27	74	PHY1_RXD0	K32
75	GND		76	GND	
77	FPGA_TCK	K27	78	PHY1_RXCTL	L30
79	FPGA_TDI	J27	80	PHY1_RXCK	K31

81	FPGA_TMS	H28	82	PHY1_MDC	L33
83	FPGA_TDO	G28	84	PHY1_MDIO	L34
85	GND		86	GND	
87	505_RX3_N	N34	88	505_TX3_N	N30
89	505_RX3_P	N33	90	505_TX3_P	N29
91	GND		92	GND	
93	505_RX2_N	R34	94	505_TX2_N	P32
95	505_RX2_P	R33	96	505_TX2_P	P31
97	GND		98	GND	
99	505_RX1_N	T32	100	505_TX1_N	R30
101	505_RX1_P	T31	102	505_TX1_P	R29
103	GND		104	GND	
105	505_RX0_N	U34	106	505_TX0_N	U30
107	505_RX0_P	U33	108	505_TX0_P	U29
109	GND		110	GND	
111	505_CLK0_N	T28	112	505_CLK1_N	P28
113	505_CLK0_P	T27	114	505_CLK1_P	P27
115	GND		116	GND	
117	505_CLK2_N	M28	118	505_CLK3_N	M32
119	505_CLK2_P	M27	120	505_CLK3_P	M31

J31 Connector

J31 connects to the IO of BANK64 and BANK65. The level standard of BANK64 and BANK65 is +1.8V.

J31 Pin	Signal Name	Pin Number	J31 Pin	Signal Name	Pin Number
1	POWER_SW		2	VBAT_IN	Y23

3	B65_L24_N	AA20	4	B65_L2_N	AN19
5	B65_L24_P	AA19	6	B65_L2_P	AM19
7	B65_L13_N	AH23	8	B65_L18_N	AE24
9	B65_L13_P	AH22	10	B65_L18_P	AE23
11	GND		12	GND	
13	B65_L8_N	AL23	14	B65_L16_N	AG23
15	B65_L8_P	AL22	16	B65_L16_P	AF23
17	B65_L12_N	AJ22	18	B65_L3_N	AP22
19	B65_L12_P	AJ21	20	B65_L3_P	AP21
21	GND		22	GND	
23	B65_L5_N	AP23	24	B65_L7_N	AL21
25	B65_L5_P	AN22	26	B65_L7_P	AL20
27	B65_L10_N	AK23	28	B65_L21_N	AE20
29	B65_L10_P	AK22	30	B65_L21_P	AD20
31	GND		32	GND	
33	B65_L14_N	AH21	34	B65_L6_N	AN23
35	B65_L14_P	AG21	36	B65_L6_P	AM23
37	B65_L19_N	AE19	38	B65_L17_N	AF22
39	B65_L19_P	AE18	40	B65_L17_P	AF21
41	GND		42	GND	
43	B65_L15_N	AG20	44	B65_L4_N	AN21
45	B65_L15_P	AG19	46	B65_L4_P	AM21
47	B65_L20_N	AC19	48	B65_L11_N	AK20
49	B65_L20_P	AB19	50	B65_L11_P	AJ20
51	GND		52	GND	
53	B65_L23_N	AD19	54	B65_L1_N	AP20
55	B65_L23_P	AC18	56	B65_L1_P	AP19

57	B65_L22_N	AB18	58	B65_L9_N	AK19
59	B65_L22_P	AA18	60	B65_L9_P	AJ19
61	GND		62	GND	
63	B64_L1_P	AP18	64	B64_L9_P	AK18
65	B64_L1_N	AP17	66	B64_L9_N	AL18
67	B64_L6_P	AN17	68	B64_L14_P	AF18
69	B64_L6_N	AN16	70	B64_L14_N	AG18
71	GND		72	GND	
73	B64_L5_P	AP16	74	B64_L11_P	AJ17
75	B64_L5_N	AP15	76	B64_L11_N	AK17
77	B64_L3_P	AM18	78	B64_L4_P	AM14
79	B64_L3_N	AN18	80	B64_L4_N	AN14
81	GND		82	GND	
83	B64_L24_P	AD17	84	B64_L2_P	AN13
85	B64_L24_N	AD16	86	B64_L2_N	AP13
87	B64_L21_P	AB16	88	B64_L8_P	AL16
89	B64_L21_N	AB15	90	B64_L8_N	AL15
91	GND		92	GND	
93	B64_L7_P	AM16	94	B64_L12_P	AJ16
95	B64_L7_N	AM15	96	B64_L12_N	AJ15
97	B64_L10_P	AK15	98	B64_L16_P	AH14
99	B64_L10_N	AK14	100	B64_L16_N	AJ14
101	GND		102	GND	
103	B64_L20_P	AC17	104	B64_L15_P	AE17
105	B64_L20_N	AC16	106	B64_L15_N	AF17
107	B64_L18_P	AG15	108	B64_L17_P	AF16
109	B64_L18_N	AG14	110	B64_L17_N	AF15

111	GND		112	GND	
113	B64_L22_P	AA16	114	B64_L19_P	AD15
115	B64_L22_N	AA15	116	B64_L19_N	AE15
117	B64_L13_P	AH18	118	B64_L23_P	AA14
119	B64_L13_N	AH17	120	B64_L23_N	AB14

J32 Connector Pin Assignment

J32 connects to the transceiver signals of BANK223, BANK224, BANK225, BANK226.

J32 Pin	Signal Name	Pin Number	J32 Pin	Signal Name	Pin Number
1	223_RX0_P	AP4	2	223_TX0_P	AN6
3	223_RX0_N	AP3	4	223_TX0_N	AN5
5	GND		6	GND	
7	223_RX1_P	AN2	8	223_TX1_P	AM4
9	223_RX1_N	AN1	10	223_TX1_N	AM3
11	GND		12	GND	
13	223_RX2_P	AL2	14	223_TX2_P	AL6
15	223_RX2_N	AL1	16	223_TX2_N	AL5
17	GND		18	GND	
19	223_RX3_P	AK4	20	223_TX3_P	AJ6
21	223_RX3_N	AK3	22	223_TX3_N	AJ5
23	GND		24	GND	
25	223_CLK1_P	AC10	26	223_CLK0_P	AD8
27	223_CLK1_N	AC9	28	223_CLK0_N	AD7
29	GND		30	GND	
31	224_RX0_P	AJ2	32	224_TX0_P	AH4
33	224_RX0_N	AJ1	34	224_TX0_N	AH3

35	GND		36	GND	
37	224_RX1_P	AG2	38	224_TX1_P	AG6
39	224_RX1_N	AG1	40	224_TX1_N	AG5
41	GND		42	GND	
43	224_RX2_P	AF4	44	224_TX2_P	AE6
45	224_RX2_N	AF3	46	224_TX2_N	AE5
47	GND		48	GND	
49	224_RX3_P	AE2	50	224_TX3_P	AD4
51	224_RX3_N	AE1	52	224_TX3_N	AD3
53	GND		54	GND	
55	224_CLK1_P	AA10	56	224_CLK0_P	AB8
57	224_CLK1_N	AA9	58	224_CLK0_N	AB7
59	GND		60	GND	
61	225_CLK1_P	W10	62	225_CLK0_P	Y8
63	225_CLK1_N	W9	64	225_CLK0_N	Y7
65	GND		66	GND	
67	225_RX1_P	AB4	68	225_RX0_P	AC2
69	225_RX1_N	AB3	70	225_RX0_N	AC1
71	GND		72	GND	
73	225_TX1_P	AA6	74	225_TX0_P	AC6
75	225_TX1_N	AA5	76	225_TX0_N	AC5
77	GND		78	GND	
79	225_RX2_P	AA2	80	225_RX3_P	W2
81	225_RX2_N	AA1	82	225_RX3_N	W1
83	GND		84	GND	
85	225_TX2_P	Y4	86	225_TX3_P	W6
87	225_TX2_N	Y3	88	225_TX3_N	W5

89	GND		90	GND	
91	226_CLK0_P	V8	92	226_CLK1_P	U10
93	226_CLK0_N	V7	94	226_CLK1_N	U9
95	GND		96	GND	
97	226_RX3_P	P4	98	226_TX3_P	N6
99	226_RX3_N	P3	100	226_TX3_N	N5
101	GND		102	GND	
103	226_RX2_P	R2	104	226_TX2_P	R6
105	226_RX2_N	R1	106	226_TX2_N	R5
107	GND		108	GND	
109	226_RX1_P	U2	110	226_TX1_P	T4
111	226_RX1_N	U1	112	226_TX1_N	T3
113	GND		114	GND	
115	226_RX0_P	V4	116	226_TX0_P	U6
117	226_RX0_N	V3	118	226_TX0_N	U5
119	GND		120	GND	

3. Expansion Board

3.1 Introduction

Through the previous function introduction, we can understand the functions of the expansion board:

- ✧ PCIe x8 interface
- ✧ 1 M.2 interface
- ✧ 1 DP output interface
- ✧ 1 USB3.0 Type-C interface
- ✧ 2 Gigabit Ethernet interfaces
- ✧ 2 USB Uart interfaces
- ✧ 1 Micro SD card holder
- ✧ 1 FMC expansion port
- ✧ 1 40-pin expansion port
- ✧ JTAG debugging interface
- ✧ 1 Temperature sensor
- ✧ 1 EEPROM
- ✧ 2 User LED lights
- ✧ 2 User keys

3.2 PCIE x8 Interface

The Z7-P expansion board is equipped with a PCIe3.0x8 interface, and 8 pairs of transceivers are connected to the golden finger of PCIEx8, which can realize the data

communication of PCIEex8, PCIEex4, PCIex2 and PCIex1.

The transceiver of PCIe interface is directly connected to the GTH transceivers of FPGA BANK223 and BANK224. The 8-channel TX signals and RX signals are connected to the FPGA transceiver in the mode of differential signal, and the single-channel communication rate can be up to 8Gbps bandwidth.

The design diagram of the PCIe interface of the development board is shown in Figure 3-2-1, where the TX transmission signal is connected in AC coupling mode.

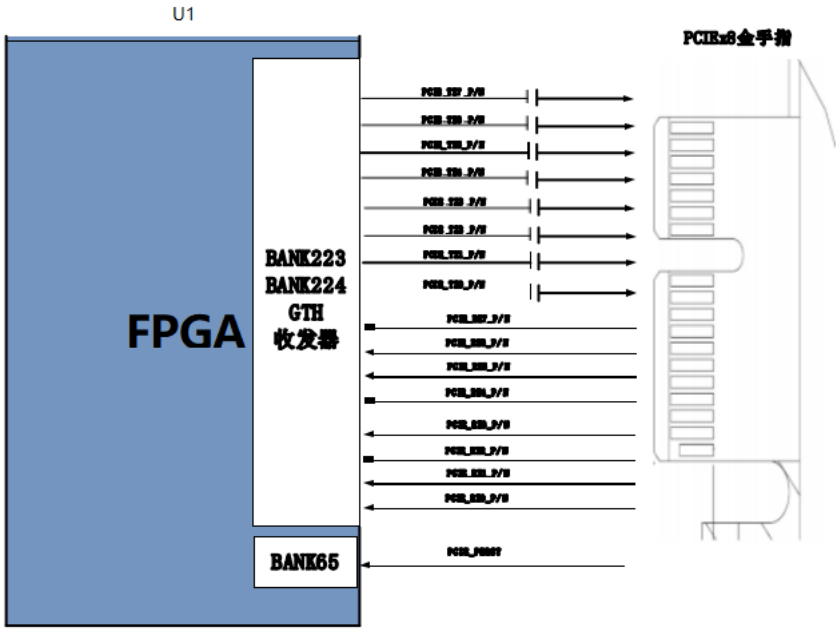


Figure 3-2-1: Design diagram of the PCIe slot

FPGA Pin assignment of the PCIe x8 interface is as follows:

Signal Name	FPGA Pin Name	Pin Number	Remarks
PCIE_RX0_N	223_RX0_N	AP3	PCIE channel 0 data reception, Negative
PCIE_RX0_P	223_RX0_P	AP4	PCIE channel 0 data reception, Positive
PCIE_RX1_N	223_RX1_N	AN1	PCIE channel 1 data reception, Negative

PCIE_RX1_P	223_RX1_P	AN2	PCIE channel 1 data reception, Positive
PCIE_RX2_N	223_RX2_N	AL1	PCIE channel 2 data reception, Negative
PCIE_RX2_P	223_RX2_P	AL2	PCIE channel 2 data reception, Positive
PCIE_RX3_N	223_RX3_N	AK3	PCIE channel 3 data reception, Negative
PCIE_RX3_P	223_RX3_P	AK4	PCIE channel 3 data reception, Positive
PCIE_RX4_N	224_RX0_N	AJ1	PCIE channel 4 data reception, Negative
PCIE_RX4_P	224_RX0_P	AJ2	PCIE channel 4 data reception, Positive
PCIE_RX5_N	224_RX1_N	AG1	PCIE channel 5 data reception, Negative
PCIE_RX5_P	224_RX1_P	AG2	PCIE channel 5 data reception, Positive
PCIE_RX6_N	224_RX2_N	AF3	PCIE channel 6 data reception, Negative
PCIE_RX6_P	224_RX2_P	AF4	PCIE channel 6 data reception, Positive
PCIE_RX7_N	224_RX3_N	AE1	PCIE channel 7 data reception, Negative
PCIE_RX7_P	224_RX3_P	AE2	PCIE channel 7 data reception, Positive
PCIE_TX0_N	223_TX0_N	AN5	PCIE channel 0 data transmission, Negative
PCIE_TX0_P	223_TX0_P	AN6	PCIE channel 0 data transmission, Positive
PCIE_TX1_N	223_TX1_N	AM3	PCIE channel 1 data transmission, Negative
PCIE_TX1_P	223_TX1_P	AM4	PCIE channel 1 data transmission, Positive
PCIE_TX2_N	223_TX2_N	AL5	PCIE channel 2 data transmission, Negative
PCIE_TX2_P	223_TX2_P	AL6	PCIE channel 2 data transmission, Positive
PCIE_TX3_N	223_TX3_N	AJ5	PCIE channel 3 data transmission, Negative
PCIE_TX3_P	223_TX3_P	AJ6	PCIE channel 3 data transmission, Positive

PCIE_TX4_N	224_TX0_N	AH3	PCIE channel 4 data transmission, Negative
PCIE_TX4_P	224_TX0_P	AH4	PCIE channel 4 data transmission, Positive
PCIE_TX5_N	224_TX1_N	AG5	PCIE channel 5 data transmission, Negative
PCIE_TX5_P	224_TX1_P	AG6	PCIE channel 5 data transmission, Positive
PCIE_TX6_N	224_TX2_N	AE5	PCIE channel 6 data transmission, Negative
PCIE_TX6_P	224_TX2_P	AE6	PCIE channel 6 data transmission, Positive
PCIE_TX7_N	224_TX3_N	AD3	PCIE channel 7 data transmission, Negative
PCIE_TX7_P	224_TX3_P	AD4	PCIE channel 7 data transmission, Positive
PCIE_CLK_N	223_CLK0_N	AD7	PCIE channel reference clock, Negative
PCIE_CLK_P	223_CLK0_P	AD8	PCIE channel reference clock, Positive
PCIE_RSTN	B65_L24_N	AA20	Reset signal of the PCIE card

3.3 M.2 Interface

The Z7-P development board is equipped with a PCIE x1 standard M.2 interface for connecting M.2 SSD with communication speeds of up to 6Gbps. The M.2 interface uses the M key slot and supports only PCI-E, but not SATA. You need to select a PCIE-type SSD when selecting an SSD.

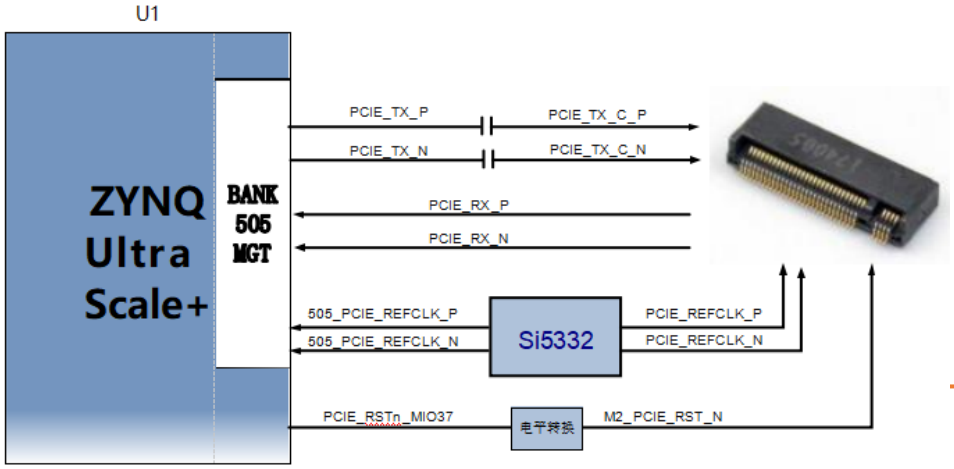


Figure 3-3-1: Design diagram of M.2 Interface

ZYNQ Pin assignment of the M.2 interface is as follows:

Signal Name	Pin Name	Pin Number	Remarks
PCIE_TX_N	505_TX0_N	U30	PCIE data transmission, Negative
PCIE_TX_P	505_TX0_P	U29	PCIE data transmission, Positive
PCIE_RX_N	505_RX0_N	U34	PCIE data reception, Negative
PCIE_RX_P	505_RX0_P	U33	PCIE data reception, Positive
505_PCIE_REFCLK_N	505_CLK0_N	T28	PCIE reference clock, Negative
505_PCIE_REFCLK_P	505_CLK0_P	T27	PCIE reference clock, Positive
PCIE_RSTN_MIO37	PS_MIO37	C33	PCIE reset signal

3.4 DP Display Port

The Z7-P development board has one mini DisplayPort output display port for displaying video images. The port supports VESA DisplayPort V1.2a output standard, supports a maximum output of 4K x 2K@30Fps, supports video formats include Y-only, YCbCr444, YCbCr422, YCbCr420 and RGB. Each color supports 6, 8, 10, or 12 bits.

The DisplayPort data transmission channel is output directly with ZU7EV's BANK505 PS MGT driver, and the LANE2 and LANE3 TX signals of the MGT are connected to the DP connector in differential signal mode. The DisplayPort auxiliary channel is connected to the MIO pin of the PS. Figure 3-4-1 shows the design diagram of DP output port:

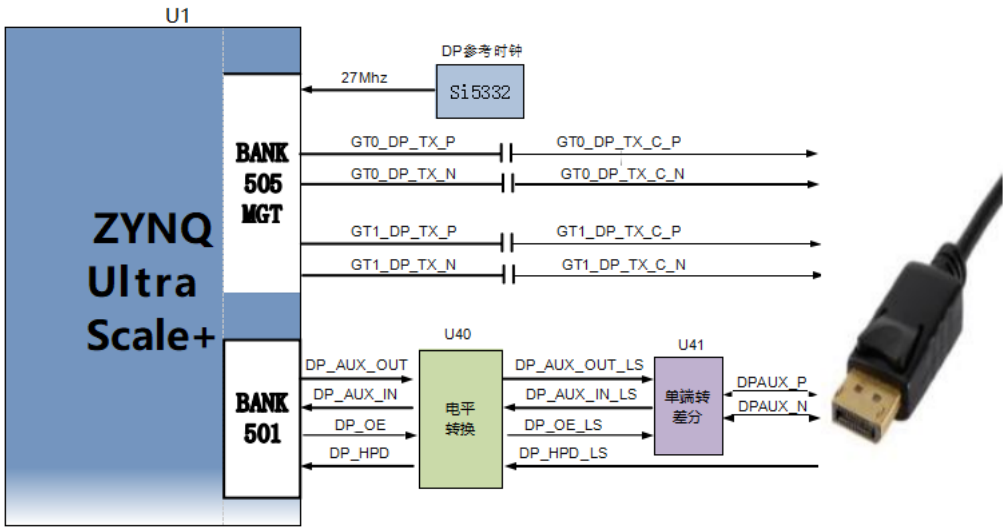


Figure 3-4-1: The design diagram of DP output port

ZYNQ pin assignment of DisplayPort port:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Remarks
GT0_DP_TX_N	505_TX3_N	N30	DP data, Low-level transmission, Negative
GT0_DP_TX_P	505_TX3_P	N29	DP data, Low-level transmission, Positive
GT1_DP_TX_N	505_TX2_N	P32	DP data, High-level transmission, Negative
GT1_DP_TX_P	505_TX2_P	P31	DP data, High-level transmission, Positive
505_DP_CLKN	505_CLK2_N	M28	DP reference clock, Negative
505_DP_CLKP	505_CLK2_P	M27	DP reference clock, Positive
DP_AUX_OUT_MIO27	PS_MIO27	A30	DP auxiliary data output
DP_AUX_IN_MIO30	PS_MIO30	A33	DP auxiliary data input

DP_OE_MIO29	PS_MIO29	A32	DP auxiliary data output enable
DP_HPD_MIO28	PS_MIO28	A31	DP insertion signal detection

3.5 USB3.0 Interface

The Z7-P expansion board has one USB3.0 TYPE C interface, supports HOST, SLAVE, OTG mode, and delivers data in a transmission speed of up to 5.0Gb/s. USB3.0 is connected through the PIPE3 interface, and USB2.0 is connected to the external USB3320C chip through the ULPI interface to achieve high-speed data communication of USB3.0 and USB2.0.

Figure 3-5-1 shows the schematic diagram of USB3.0 connection:

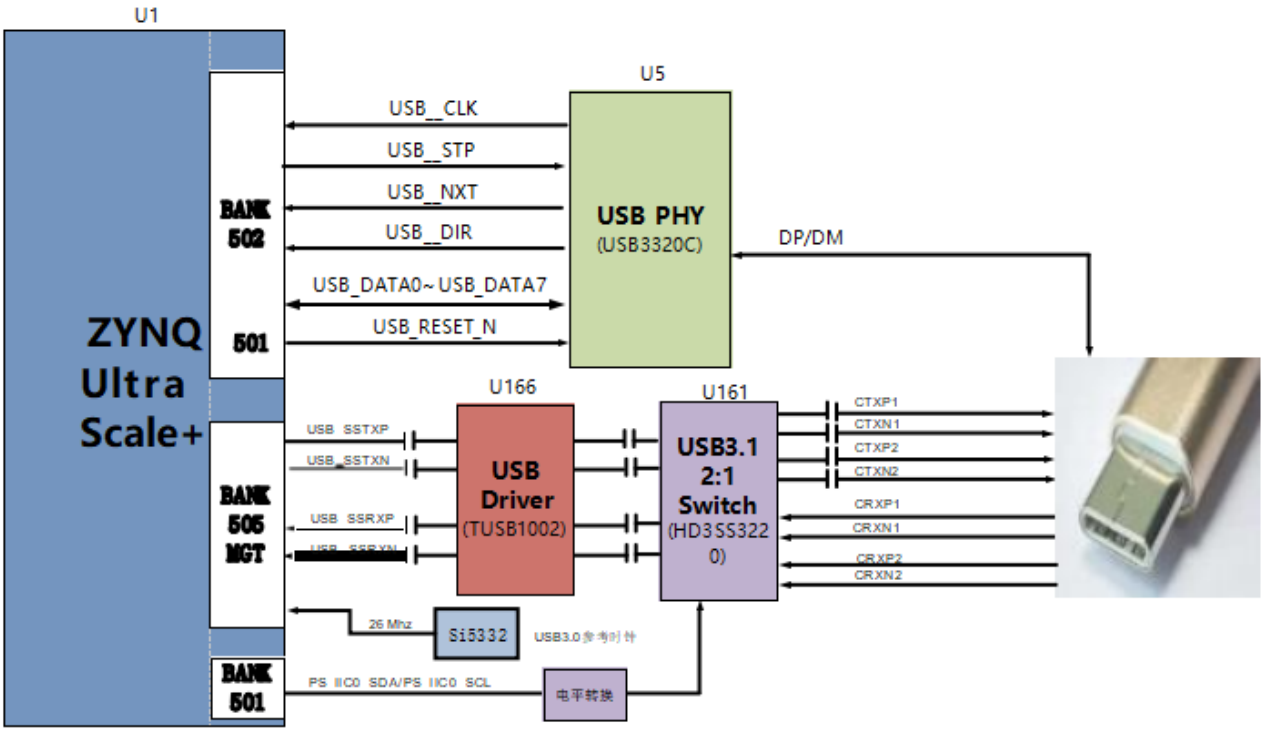


Figure 3-5-1: The schematic diagram of USB3.0 interface

Pin Assignment of USB interface:

Signal Name	Pin Name	Pin Number	Remarks

USB_SSTXN	505_TX1_N	R30	USB3.0 data transmission, Positive
USB_SSTXP	505_TX1_P	R29	USB3.0 data transmission, Negative
USB_SSRXN	505_RX1_N	T32	USB3.0 data reception, Positive
USB_SSRXP	505_RX1_P	T31	USB3.0 data reception, Negative
USB_DATA0	PS_MIO56	G34	USB2.0 data Bit0
USB_DATA1	PS_MIO57	H29	USB2.0 data Bit1
USB_DATA2	PS_MIO54	G31	USB2.0 data Bit2
USB_DATA3	PS_MIO59	H32	USB2.0 data Bit3
USB_DATA4	PS_MIO60	H33	USB2.0 data Bit4
USB_DATA5	PS_MIO61	H34	USB2.0 data Bit5
USB_DATA6	PS_MIO62	J29	USB2.0 data Bit6
USB_DATA7	PS_MIO63	J30	USB2.0 data Bit7
USB_STP	PS_MIO58	H31	USB2.0 stop signal
USB_DIR	PS_MIO53	G30	USB2.0 data direction signal
USB_CLK	PS_MIO52	G29	USB2.0 clock signal
USB_NXT	PS_MIO55	G33	USB2.0 next data signal
USB_RESET_N	PS_MIO32	B31	USB2.0 reset signal
PS_IIC0_SCL	PS_MIO34	B34	I2C clock signal
PS_IIC0_SDA	PS_MIO35	C31	I2C data signal

3.6 Gigabit Ethernet Interface

The Z7-P expansion board has two Gigabit Ethernet interfaces, one of which is connected to the PS side and the other one is connected to the PL side. Ethernet chip adopts industrial Ethernet GPHY chip (JL2121-N040I) from JLSemi to provide users with network communication services. The Ethernet PHY chip on the PS side is connected to the GPIO interface of the BANK502 on the PS on ZYNQ, while it on the PL side is connected to the IO of the BANK35. The JL2121 chip supports 10/100/1000 Mbps network transmission rate and communicates with the MAC layer of the Zynq7000 system through the RGMII interface. JL2121D supports MDI/MDX self-adaptive, various speed self-adaptive and Master/Slave self-adaptive, supports MDIO bus for PHY register management.

When the JL2121 is powered on, it detects some specific IO level states to determine its own working mode. Table 3-6-1 shows the default settings of the GPHY chip after it is powered on.

Configuration Pin	Description	Configuration Value
RXD3_ADR0 RXC_ADR1 RXCTL_ADR2	PHY address in MDIO/MDC mode	The PHY address is 011
RXD1_TXDLY	TX clock 2ns delay	Delay
RXD0_RXDLY	RX clock 2ns delay	Delay

Table 3-6-1: Default settings of the PHY chip

When the network is connected to Gigabit Ethernet, PHY chip JL2121 will transmit

data with ZYNQ through the RGMII bus with a transmission clock of 125Mhz. Data is sampled on the rising edge and falling edge of the clock.

When the network is connected to 100 Gigabit Ethernet, PHY chip JL2121 will transmit data with ZYNQ through the RGMII bus with a transmission clock of 25Mhz. Data is sampled on the rising edge and falling edge of the clock.

Figure 3-6-1 shows the connection between ZYNQ and Ethernet PHY chip.

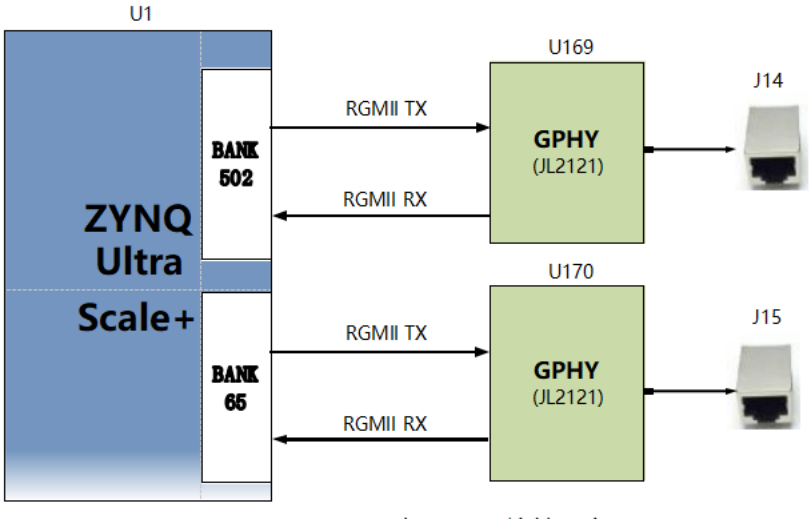


Figure 3-6-1: Connection between ZYNQ and GPHY

PS Gigabit Ethernet pin assignment is as follows:

Signal Name	Pin Name	Pin Number	Remarks
PHY1_TXCK	PHY1_TXCK	J31	Ethernet 1 RGMII transmission clock
PHY1_TXD0	PHY1_TXD0	J32	Ethernet 1 transmission data bit 0
PHY1_TXD1	PHY1_TXD1	J34	Ethernet 1 transmission data bit 1
PHY1_TXD2	PHY1_TXD2	K28	Ethernet 1 transmission data bit 2
PHY1_TXD3	PHY1_TXD3	K29	Ethernet 1 transmission data bit 3

PHY1_TXCTL	PHY1_TXCTL	K30	Ethernet 1 transmission enable signal
PHY1_RXCK	PHY1_RXCK	K31	Ethernet 1 RGMII reception clock
PHY1_RXD0	PHY1_RXD0	K32	Ethernet 1 reception data Bit 0
PHY1_RXD1	PHY1_RXD1	K33	Ethernet 1 reception data Bit 1
PHY1_RXD2	PHY1_RXD2	K34	Ethernet 1 reception data Bit 2
PHY1_RXD3	PHY1_RXD3	L29	Ethernet 1 reception data Bit 3
PHY1_RXCTL	PHY1_RXCTL	L30	Ethernet 1 reception data valid signals
PHY1_MDC	PHY1_MDC	L33	Ethernet 1 MDIO manage clock
PHY1_MDIO	PHY1_MDIO	L34	Ethernet 1 MDIO manage data

PL Gigabit Ethernet pin assignment is as follows:

Signal Name	Pin Name	Pin Number	Remarks
PHY2_TXCK	B65_L3_N	AP22	Ethernet 2 RGMII transmission clock
PHY2_TXD0	B65_L6_P	AM23	Ethernet 2 transmission data bit 0
PHY2_TXD1	B65_L6_N	AN23	Ethernet 2 transmission data bit 1
PHY2_TXD2	B65_L13_N	AH23	Ethernet 2 transmission data bit 2
PHY2_TXD3	B65_L3_P	AP21	Ethernet 2 transmission data bit 3
PHY2_TXCTL	B65_L16_P	AF23	Ethernet 2 transmit the enable signal

PHY2_RXCK	B65_L13_P	AH22	Ethernet 2 RMII reception clock
PHY2_RXD0	B65_L2_P	AM19	Ethernet 2 reception data Bit 0
PHY2_RXD1	B65_L18_N	AE24	Ethernet 2 reception data Bit 1
PHY2_RXD2	B65_L18_P	AE23	Ethernet 2 reception data Bit 2
PHY2_RXD3	B65_L24_P	AA19	Ethernet 2 reception data Bit 3
PHY2_RXCTL	B65_L2_N	AN19	Ethernet 2 reception data valid signals
PHY2_MDC	B64_L6_N	AN16	Ethernet 2 MDIO manage clock
PHY2_MDIO	B64_L6_P	AN17	Ethernet 2 MDIO manage data
PHY2_RESET	B65_L16_N	AG23	Ethernet 2 reset signal

3.7 USB Uart Interface

The Z7-P expansion board is equipped with two Uart to USB interfaces., one of them is connected to the PS side and the other one is connected to the PL side. The conversion chip adopts USB-UAR chip of Silicon Labs CP2102, and the USB interface adopts the MINI USB interface, which can be connected to the USB interface of the PC with a USB cable for serial data communication. Figure 3-7-1 shows the schematic diagram of USB Uart circuit design:

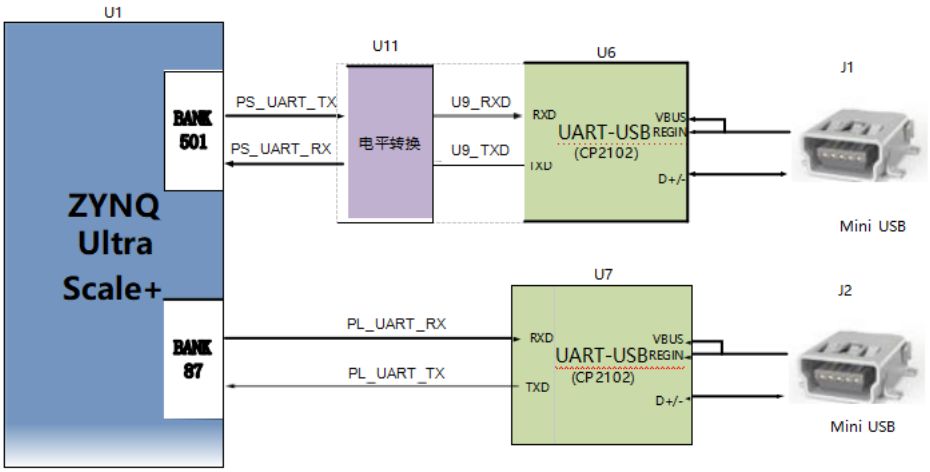


Figure 3-7-1: Schematic diagram of USB-to-Serial port

ZYNQ pin assignment of USB-to-serial port:

Signal Name	Pin Name	Pin Number	Remarks
PS_UART_RX	PS_MIO42	D34	PS Uart1 data input
PS_UART_TX	PS_MIO43	E30	PS Uart1 data output
PL_UART_RX	B87_L2_N	N8	PL Uart data input
PL_UART_TX	B87_L2_P	N9	PL Uart data output

3.8 Micro SD Card Holder

The expansion board contains a Micro SD card interface to provide users access to the SD card memory for storing the ZU7EV chip's BOOT program, Linux operating system kernel, file system, and other user data files.

The SDIO signal is connected to the IO signal of the PS BANK501 of ZU7EV, and we connect BANK501 and SD card through the TXS02612 level converter because the VCCIO of BANK501 has been set to 1.8V, but the data level of the SD card is 3.3V. Figure 3-8-1 shows the schematic diagram of the ZU7EV PS and SD card connector.

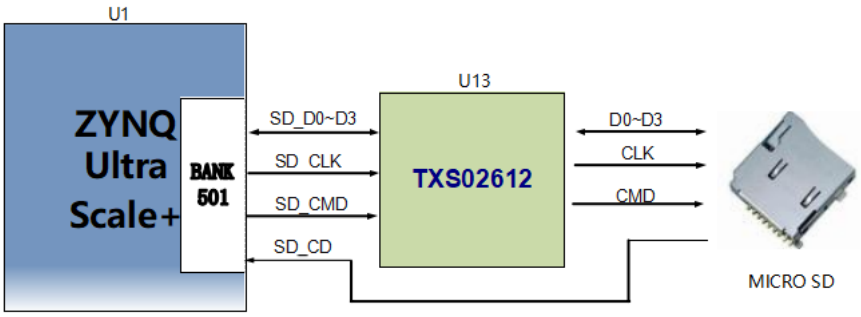


Figure 3-8-1: Schematic diagram of the SD card connection

SD card slot pin assignment:

Signal Name	Pin Name	Pin Number	Remarks
SD_CLK	SD_CLK	F34	SD clock signal
SD_CD	SD_CD	E33	SD command signal
SD_D0	SD_D0	E34	SD data Data0
SD_D1	SD_D1	F30	SD data Data1
SD_D2	SD_D2	F31	SD data Data2
SD_D3	SD_D3	F32	SD Data Data3
SD_CMD	SD_CMD	F33	SD card detection signal

3.9 FMC Connector

Z7-P expansion board is equipped with a standard FMC HPC expansion port, can be externally connected to XILINX' s or ALINX' s various FMC modules (HDMI input/output module, binocular camera module, high-speed AD module, etc.). The FMC expansion port package contains 36 pairs of differential IO signals and 2 pairs of GTX transceiver signals.

The 59 pairs of differential signals of the FMC expansion port are connected to the IO of the BANK28, BANK64, BANK65 of the ZYNQ Ultrascale+ chip with 1.8V level standard, and the differential signals support LVDS data communication. 8 pairs of GTX transceiver signals are connected to BANK225 and BANK226.

Figure 3-9-1 shows the schematic diagram of ZYNQ Ultrascale+ and FMC connectors.

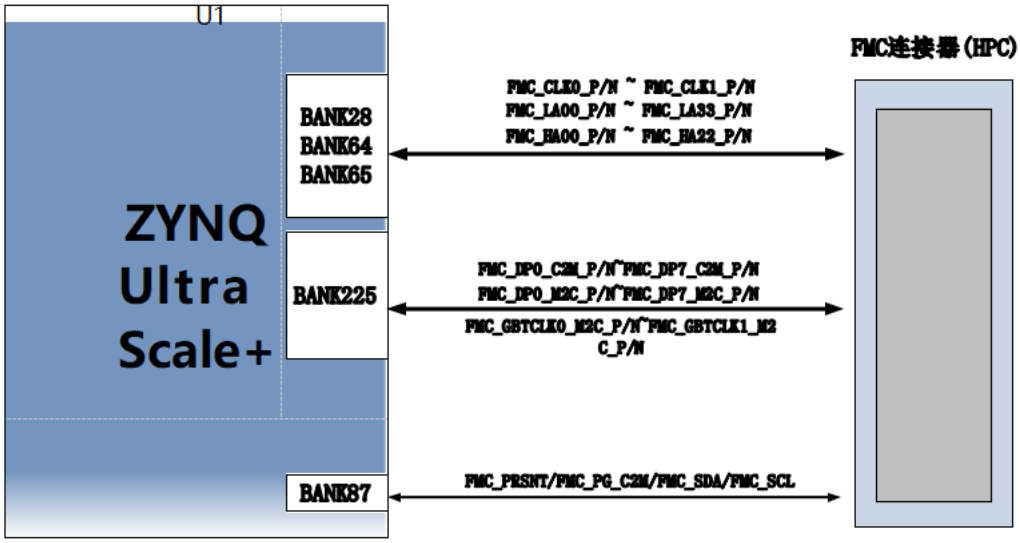


Figure 3-9-1: Connection diagram of FMC connector

Pin assignments of FMC connector is as follows:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Remarks
FMC_DP0_C2M_N	225_TX1_N	AA5	FMC transceiver data transmission 0, Negative
FMC_DP0_C2M_P	225_TX1_P	AA6	FMC transceiver data transmission 0, Positive
FMC_DP1_C2M_N	225_TX2_N	Y3	FMC transceiver data transmission 1,

			Negative
FMC_DP1_C2M_P	225_TX2_P	Y4	FMC transceiver data transmission 1, Positive
FMC_DP2_C2M_N	225_TX0_N	AC5	FMC transceiver data transmission 2, Negative
FMC_DP2_C2M_P	225_TX0_P	AC6	FMC transceiver data transmission 2, Positive
FMC_DP3_C2M_N	225_TX3_N	W5	FMC transceiver data transmission 3, Negative
FMC_DP3_C2M_P	225_TX3_P	W6	FMC transceiver data transmission 3, Positive
FMC_DP4_C2M_N	226_TX2_N	R5	FMC transceiver data transmission 4, Negative
FMC_DP4_C2M_P	226_TX2_P	R6	FMC transceiver data transmission 4, Positive
FMC_DP5_C2M_N	226_TX3_N	N5	FMC transceiver data transmission 5, Negative
FMC_DP5_C2M_P	226_TX3_P	N6	FMC transceiver data transmission 5, Positive
FMC_DP6_C2M_N	226_TX0_N	U5	FMC transceiver data transmission 6, Negative

FMC_DP6_C2M_P	226_TX0_P	U6	FMC transceiver data transmission 6, Positive
FMC_DP7_C2M_N	226_TX1_N	T3	FMC transceiver data transmission 7, Negative
FMC_DP7_C2M_P	226_TX1_P	T4	FMC transceiver data transmission 7, Positive
FMC_DP0_M2C_N	225_RX1_N	AB3	FMC transceiver data reception 0, Negative
FMC_DP0_M2C_P	225_RX1_P	AB4	FMC transceiver data reception 0, Positive
FMC_DP1_M2C_N	225_RX2_N	AA1	FMC transceiver data reception 1, Negative
FMC_DP1_M2C_P	225_RX2_P	AA2	FMC transceiver data reception 1, Positive
FMC_DP2_M2C_N	225_RX0_N	AC1	FMC transceiver data reception 2, Negative
FMC_DP2_M2C_P	225_RX0_P	AC2	FMC transceiver data reception 2, Positive
FMC_DP3_M2C_N	225_RX3_N	W1	FMC transceiver data reception 3, Negative
FMC_DP3_M2C_P	225_RX3_P	W2	FMC transceiver data reception 3,

			Positive
FMC_DP4_M2C_N	226_RX2_N	R1	FMC transceiver data reception 4, Negative
FMC_DP4_M2C_P	226_RX2_P	R2	FMC transceiver data reception 4, Positive
FMC_DP5_M2C_N	226_RX3_N	P3	FMC transceiver data reception 5, Negative
FMC_DP5_M2C_P	226_RX3_P	P4	FMC transceiver data reception 5, Positive
FMC_DP6_M2C_N	226_RX0_N	V3	FMC transceiver data reception 6, Negative
FMC_DP6_M2C_P	226_RX0_P	V4	FMC transceiver data reception 6, Positive
FMC_DP7_M2C_N	226_RX1_N	U1	FMC transceiver data reception 7, Negative
FMC_DP7_M2C_P	226_RX1_P	U2	FMC transceiver data reception 7, Positive
FMC_GBTCLK0_M2C_N	225_CLK0_N	Y7	FMC transceiver reference clock input 0, Negative
FMC_GBTCLK0_M2C_P	225_CLK0_P	Y8	FMC transceiver reference clock input 0, Positive

FMC_GBTCLK1_M2C_N	226_CLK0_N	V7	FMC transceiver reference clock input 1, Negative
FMC_GBTCLK1_M2C_P	226_CLK0_P	V8	FMC transceiver reference clock input 1, Positive
FMC_CLK0_N	B64_L11_N	AK17	FMC refers to the 1st-channel reference clock, Negative
FMC_CLK0_P	B64_L11_P	AJ17	FMC refers to the 1st-channel reference clock, Positive
FMC_CLK1_N	B64_L12_N	AJ15	FMC refers to the 2nd-channel reference clock, Negative
FMC_CLK1_P	B64_L12_P	AJ16	FMC refers to the 2nd-channel reference clock, Positive
FMC_LA00_CC_N	B65_L12_N	AJ22	FMC refers to 0th-channel data (clock), Negative
FMC_LA00_CC_P	B65_L12_P	AJ21	FMC refers to 0th-channel data (clock), Positive
FMC_LA01_CC_N	B65_L14_N	AH21	FMC refers to the 1st-channel data (clock), Negative
FMC_LA01_CC_P	B65_L14_P	AG21	FMC refers to the 1st-channel data (clock), Positive
FMC_LA02_N	B65_L5_N	AP23	FMC refers to the 2nd-channel data,

			Negative
FMC_LA02_P	B65_L5_P	AN22	FMC refers to the 2nd-channel data, Positive
FMC_LA03_N	B65_L17_N	AF22	FMC refers to the 3rd-channel data, Negative
FMC_LA03_P	B65_L17_P	AF21	FMC refers to the 3rd-channel data, Positive
FMC_LA04_N	B65_L4_N	AN21	FMC refers to the 4th-channel data, Negative
FMC_LA04_P	B65_L4_P	AM21	FMC refers to the 4th-channel data, Positive
FMC_LA05_N	B65_L15_N	AG20	FMC refers to the 5th-channel data, Negative
FMC_LA05_P	B65_L15_P	AG19	FMC refers to the 5th-channel data, Positive
FMC_LA06_N	B65_L8_N	AL23	FMC refers to the 6th-channel data, Negative
FMC_LA06_P	B65_L8_P	AL22	FMC refers to the 6th-channel data, Positive
FMC_LA07_N	B65_L9_N	AK19	FMC refers to the 7th-channel data, Negative

FMC_LA07_P	B65_L9_P	AJ19	FMC refers to the 7th-channel data, Positive
FMC_LA08_N	B65_L11_N	AK20	FMC refers to the 8th-channel data, Negative
FMC_LA08_P	B65_L11_P	AJ20	FMC refers to the 8th-channel data, Positive
FMC_LA09_N	B65_L10_N	AK23	FMC refers to the 9th-channel data, Negative
FMC_LA09_P	B65_L10_P	AK22	FMC refers to the 9th-channel data, Positive
FMC_LA10_N	B65_L1_N	AP20	FMC refers to the 10th-channel data, Negative
FMC_LA10_P	B65_L1_P	AP19	FMC refers to the 10th-channel data, Positive
FMC_LA11_N	B65_L20_N	AC19	FMC refers to the 11th-channel data, Negative
FMC_LA11_P	B65_L20_P	AB19	FMC refers to the 11th-channel data, Positive
FMC_LA12_N	B65_L7_N	AL21	FMC refers to the 12th-channel data, Negative
FMC_LA12_P	B65_L7_P	AL20	FMC refers to the 12th-channel data,

			Positive
FMC_LA13_N	B65_L21_N	AE20	FMC refers to the 13th-channel data, Negative
FMC_LA13_P	B65_L21_P	AD20	FMC refers to the 13th-channel data, Positive
FMC_LA14_N	B65_L19_N	AE19	FMC refers to the 14th-channel data, Negative
FMC_LA14_P	B65_L19_P	AE18	FMC refers to the 14th-channel data, Positive
FMC_LA15_N	B65_L22_N	AB18	FMC refers to the 15th-channel data, Negative
FMC_LA15_P	B65_L22_P	AA18	FMC refers to the 15th-channel data, Positive
FMC_LA16_N	B65_L23_N	AD19	FMC refers to the 16th-channel data, Negative
FMC_LA16_P	B65_L23_P	AC18	FMC refers to the 16th-channel data, Positive
FMC_LA17_CC_N	B64_L14_N	AG18	FMC refers to the 17th-channel data (clock), Negative
FMC_LA17_CC_P	B64_L14_P	AF18	FMC refers to the 17th-channel data (clock), Positive

FMC_LA18_CC_N	B64_L13_N	AH17	FMC refers to the 18th-channel data (clock), Negative
FMC_LA18_CC_P	B64_L13_P	AH18	FMC refers to the 18th-channel data (clock), Positive
FMC_LA19_N	B64_L7_N	AM15	FMC refers to the 19th-channel data, Negative
FMC_LA19_P	B64_L7_P	AM16	FMC refers to the 19th-channel data, Positive
FMC_LA20_N	B64_L15_N	AF17	FMC refers to the 20th-channel data, Negative
FMC_LA20_P	B64_L15_P	AE17	FMC refers to the 20th-channel data, Positive
FMC_LA21_N	B64_L5_N	AP15	FMC refers to the 21th-channel data, Negative
FMC_LA21_P	B64_L5_P	AP16	FMC refers to the 21th-channel data, Positive
FMC_LA22_N	B64_L4_N	AN14	FMC refers to the 22th-channel data, Negative
FMC_LA22_P	B64_L4_P	AM14	FMC refers to the 22th-channel data, Positive
FMC_LA23_N	B64_L3_N	AN18	FMC refers to the 23th-channel data,

			Negative
FMC_LA23_P	B64_L3_P	AM18	FMC refers to the 23th-channel data, Positive
FMC_LA24_N	B64_L16_N	AJ14	FMC refers to the 24th-channel data, Negative
FMC_LA24_P	B64_L16_P	AH14	FMC refers to the 24th-channel data, Positive
FMC_LA25_N	B64_L10_N	AK14	FMC refers to the 25th-channel data, Negative
FMC_LA25_P	B64_L10_P	AK15	FMC refers to the 25th-channel data, Positive
FMC_LA26_N	B64_L1_N	AP17	FMC refers to the 26th-channel data, Negative
FMC_LA26_P	B64_L1_P	AP18	FMC refers to the 26th-channel data, Positive
FMC_LA27_N	B64_L2_N	AP13	FMC refers to the 27th-channel data, Negative
FMC_LA27_P	B64_L2_P	AN13	FMC refers to the 27th-channel data, Positive
FMC_LA28_N	B64_L17_N	AF15	FMC refers to the 28th-channel data, Negative

FMC_LA28_P	B64_L17_P	AF16	FMC refers to the 28th-channel data, Positive
FMC_LA29_N	B64_L19_N	AE15	FMC refers to the 29th-channel data, Negative
FMC_LA29_P	B64_L19_P	AD15	FMC refers to the 29th-channel data, Positive
FMC_LA30_N	B64_L22_N	AA15	FMC refers to the 30th-channel data, Negative
FMC_LA30_P	B64_L22_P	AA16	FMC refers to the 30th-channel data, Positive
FMC_LA31_N	B64_L20_N	AC16	FMC refers to the 31th-channel data, Negative
FMC_LA31_P	B64_L20_P	AC17	FMC refers to the 31th-channel data, Positive
FMC_LA32_N	B64_L21_N	AB15	FMC refers to the 32th-channel data, Negative
FMC_LA32_P	B64_L21_P	AB16	FMC refers to the 32th-channel data, Positive
FMC_LA33_N	B64_L23_N	AB14	FMC refers to the 33th-channel data, Negative
FMC_LA33_P	B64_L23_P	AA14	FMC refers to the 33th-channel data,

			Positive
FMC_PRSNT	B87_L4_P	N11	FMC module existence signal
FMC_PG_C2M	B87_L8_P	K9	FMC Power Good signal
FMC_SCL	B87_L6_P	M10	FMC I2C communication clock
FMC_SDA	B87_L6_N	L10	FMC I2C communication data

3.10 40-Pin Expansion Port

There is a 40-pin expansion port J16 with 2.54mm standard pitch on the Z7-P expansion board, which is used to connect each module of ALINX or the external circuit designed by the user. 34 signals of the expansion port are connected to the IO of BANK87 and BANK88, and the level is 3.3V standard. Figure 3-10-1 shows the circuit diagram of the 40-pin expansion port.

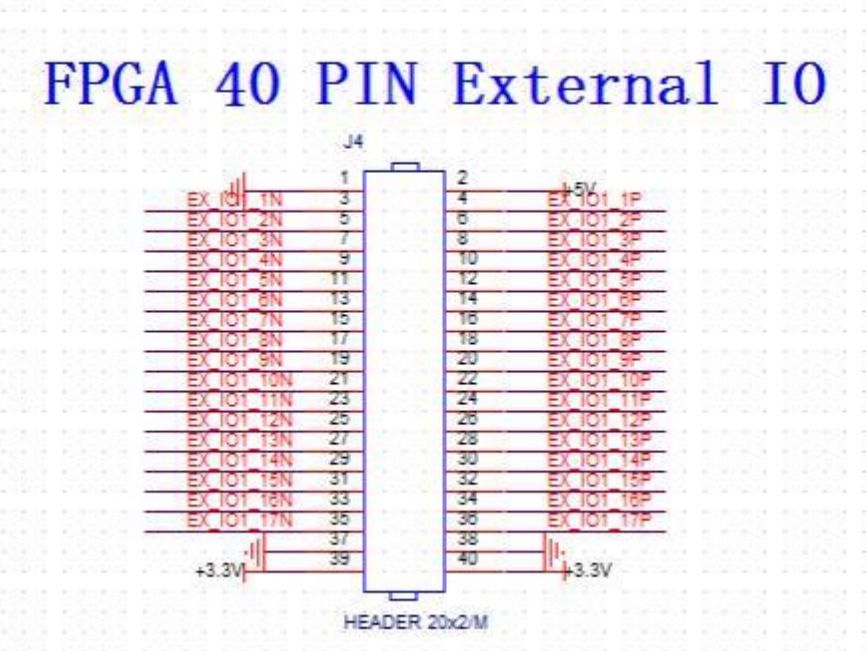


Figure 3-10-1: Schematic diagram of 40-pin expansion port J4

40-pin expansion port pin assignment is as follows:

Connector Pin	Signal Name	ZYNQ Pin Name	ZYNQ Pin Number
3	IO1_1N	B88_L4_N	E2
4	IO1_1P	B88_L4_P	E3
5	IO1_2N	B88_L1_N	D1
6	IO1_2P	B88_L1_P	E1
7	IO1_3N	B88_L5_N	C2
8	IO1_3P	B88_L5_P	D2
9	IO1_4N	B87_L11_N	G7
10	IO1_4P	B87_L11_P	H7
11	IO1_5N	B88_L11_N	D5
12	IO1_5P	B88_L11_P	D6
13	IO1_6N	B88_L9_N	F4
14	IO1_6P	B88_L9_P	F5
15	IO1_7N	B88_L8_N	D4
16	IO1_7P	B88_L8_P	E4
17	IO1_8N	B87_L9_N	J6
18	IO1_8P	B87_L9_P	J7
19	IO1_9N	B88_L7_N	B4
20	IO1_9P	B88_L7_P	C4
21	IO1_10N	B88_L2_N	B1
22	IO1_10P	B88_L2_P	C1
23	IO1_11N	B88_L3_N	A2
24	IO1_11P	B88_L3_P	A3
25	IO1_12N	B88_L6_N	B3
26	IO1_12P	B88_L6_P	C3

27	IO1_13N	B88_L10_N	A5
28	IO1_13P	B88_L10_P	B5
29	IO1_14N	B88_L12_N	E5
30	IO1_14P	B88_L12_P	F6
31	IO1_15N	B87_L10_N	G6
32	IO1_15P	B87_L10_P	H6
33	IO1_16N	B87_L12_N	G8
34	IO1_16P	B87_L12_P	H8
35	IO1_17N	B87_L3_N	M12
36	IO1_17P	B87_L3_P	N13

3.11 JTAG Debugging Interface

A JTAG interface is reserved on the Z7-P expansion board for downloading ZYNQ UltraScale+ programs or curing programs to FLASH. In order to avoid damage to the ZYNQ UltraScale+ chip due to live plugging, we add a diode to protect the JTAG signal to ensure that the signal voltage is within the range accepted by the FPGA. Figure 3-11-1 shows the schematic diagram of JTAG.

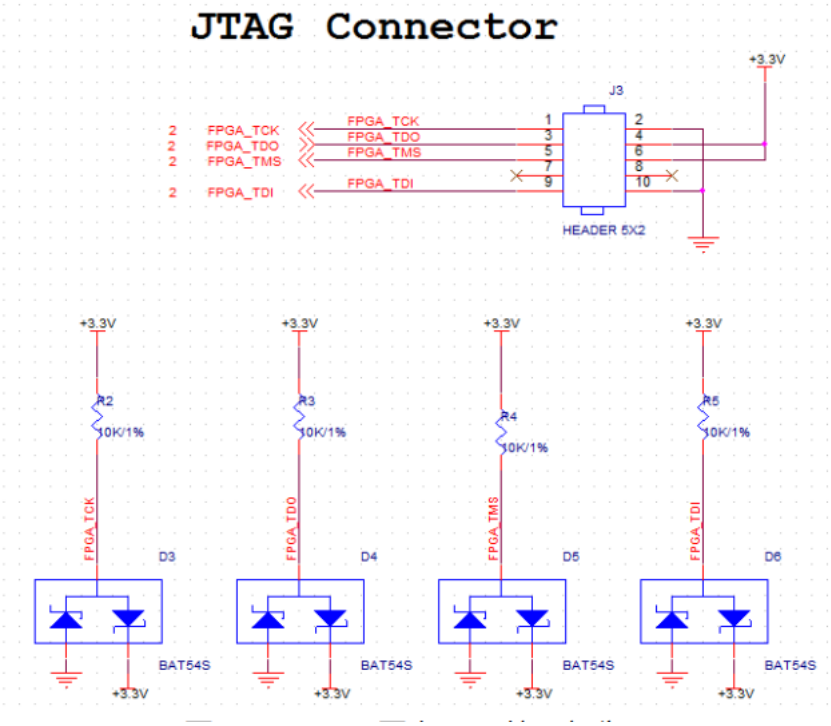


Figure 3-11-1: JTAG in the schematic diagram

3.12 EEPROM and Temperature Sensor

The Z7-P development board carries an EEPROM (model: 24LC04, capacity: 4Kbit (2*256*8bit)), and is connected to the PS side through the IIC bus for communication. The board also includes a high-precision, low-power consumption, digital temperature sensor chip called ON Semiconductor's LM75, which has a temperature accuracy of 0.5 degrees. The EEPROM and temperature sensor are mounted to the Bank501 MIO of ZYNQ UltraScale+ via the I2C bus. FIG. 3-12-1 shows the schematic diagram of EEPROM and temperature sensor.

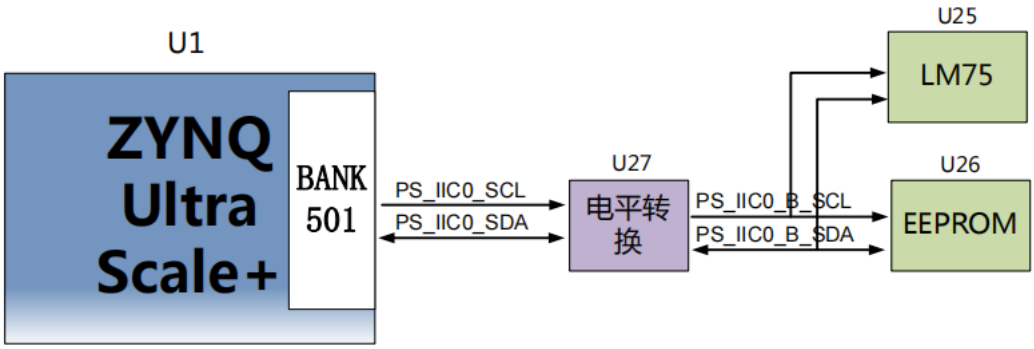


Figure 3-12-1: The schematic diagram of EEPROM and temperature sensor

EEPROM communication pin assignment is as follows:

Signal Name	Pin Name	Pin Number	Remarks
PS_IIC0_SCL	PS_MIO34	B34	I2C clock signal
PS_IIC0_SDA	PS_MIO35	C31	I2C data signal

3.13 LED Light

The Z7-P expansion board has 4 LEDs, including 1 power indicator, 1 DONE indicator, 1 PS control indicator, 1 PL control indicator. Users can control the on and off through the program. Figure 3-13-1 the schematic diagram of the hardware connection of the user's LED light:

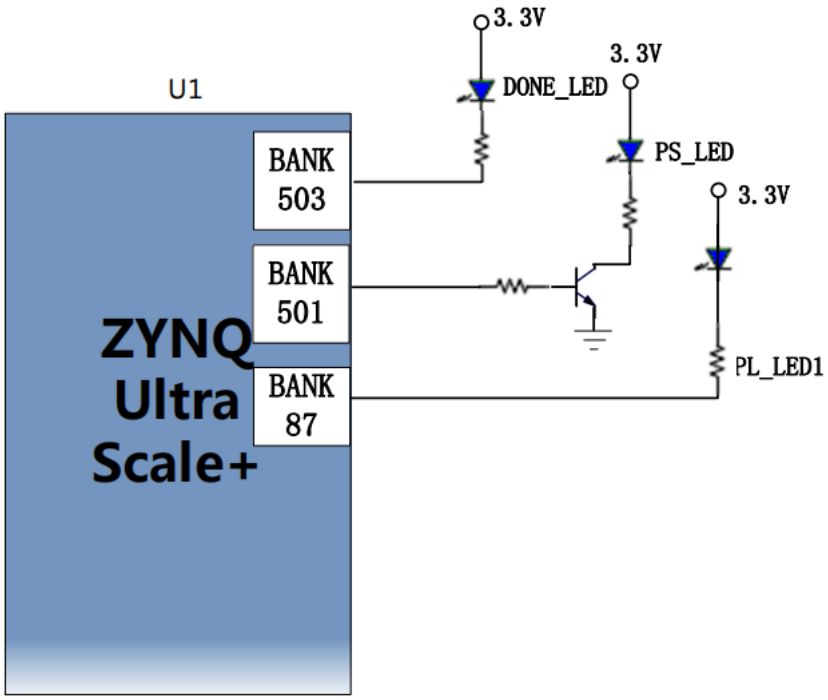


Figure 3-13-1: Hardware connection diagram of the user's LED light

User LED Light pin assignment:

Signal Name	Pin Name	Pin Number	Remarks
PS_LED	PS_MIO44	E32	User PS LED light
PL_LED	B87_L5_P	M9	User PL LED light

3.14 Key

The Z7-P expansion board has one RESET key and two user keys. The reset signal is inputted by connecting to the reset chip on the core board, then users can use this reset key to reset the ZYNQ system. One of the user keys is connected to the MIO of PS, and the other one is connected to the IO of PL. Both the reset key and user keys are active at low levels. Figure 3-14-1 shows the connection diagram of user keys:

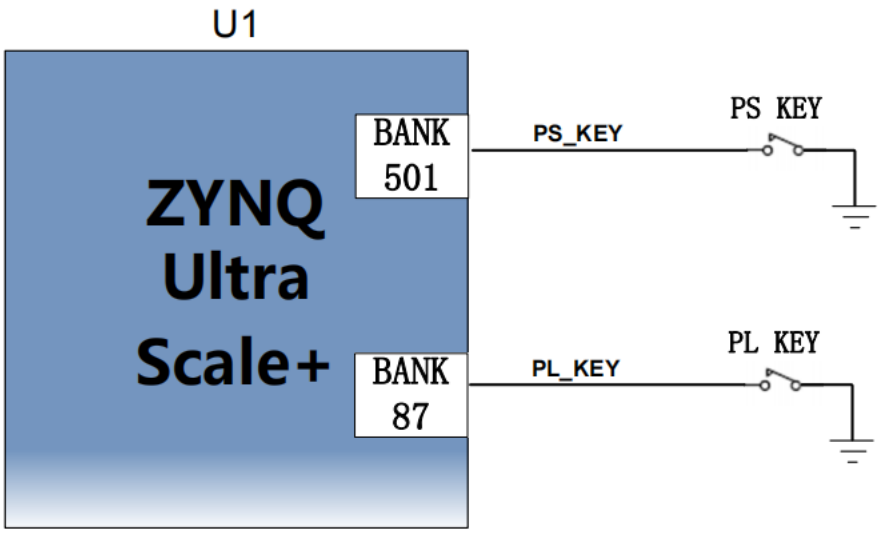


Figure 3-14-1: The connection diagram of user keys

Keys' pin assignment:

Signal Name	Pin Name	Pin Number	Remarks
PS_KEY	PS_MIO40	D31	PS key input
PL_KEY	B87_L8_N	J9	PL key input

3.15 Dip Switch Configuration

There is a 4-bit dip switch SW1 on the development board to configure the startup mode of the ZYNQ system. The Z7-P system development platform supports four kinds of startup modes: JTAG debugging mode, QSPI FLASH, EMMC and SD2.0 card startup mode. After the ZU7EV chip is powered on, it checks the (PS_MODE0~3) level to determine which startup mode to use. Users can select different startup modes by using dip switch SW1 on the expansion board. Table 3-15-1 shows the startup mode configuration of SW1.

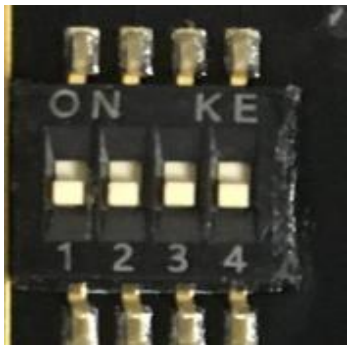
SW1	Dip Position (1, 2, 3, 4)	MODE[3:0]	Startup Mode
	ON，ON，ON，ON	0000	PS JTAG
	ON，ON，OFF ,ON	0010	QSPI FLASH
	ON，OFF，ON，OFF	0101	SD Card
	ONOFF，OFF，ON	0110	EMMC

Table 3-15-1: Startup mode configuration of SW1

3.16 Power Supply

The power input voltage of the Z7-P development board is 12V DC. The Z7-P development board can be powered by DC JACK or PCIE. On the carrier board, 1-channel DC/DC power chip ETA8156 and 3-channel DC/DC power chip ETA1471 are used to convert +5V, +3.3V, +1.8V, FMC_VADJ. Figure 3-16-1 shows design diagram of the power supply:

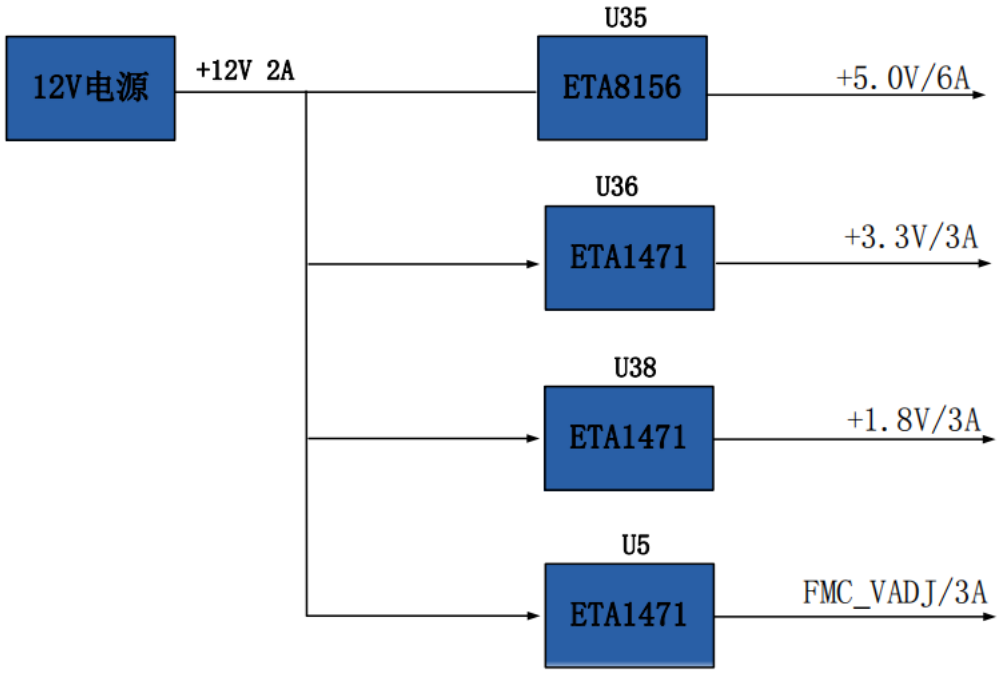


Figure 3-16-1: Schematic diagram of the power interface part

The functions of each power distribution are shown in the following table:

Power Supply	Function
+5.0V	USB power supply
+1.8V	Ethernet, USB2.0
+3.3V	Ethernet, USB2.0, M.2, SD, DP, CAN, RS485
FMC_VADJ	FMC

3.17 Fan

Because ZU7EV generates a lot of heat when it works properly, we added a cooling fin and fan to the chip on the board to prevent the chip from overheating. The control of the fan is controlled by ZYNQ chip, the control PIN is connected to the IO of BANK87 (PIN M8), if the IO level output is low, the MOSFET tube will on and the fan will work, or if the IO level output is high, the fan will stop working.

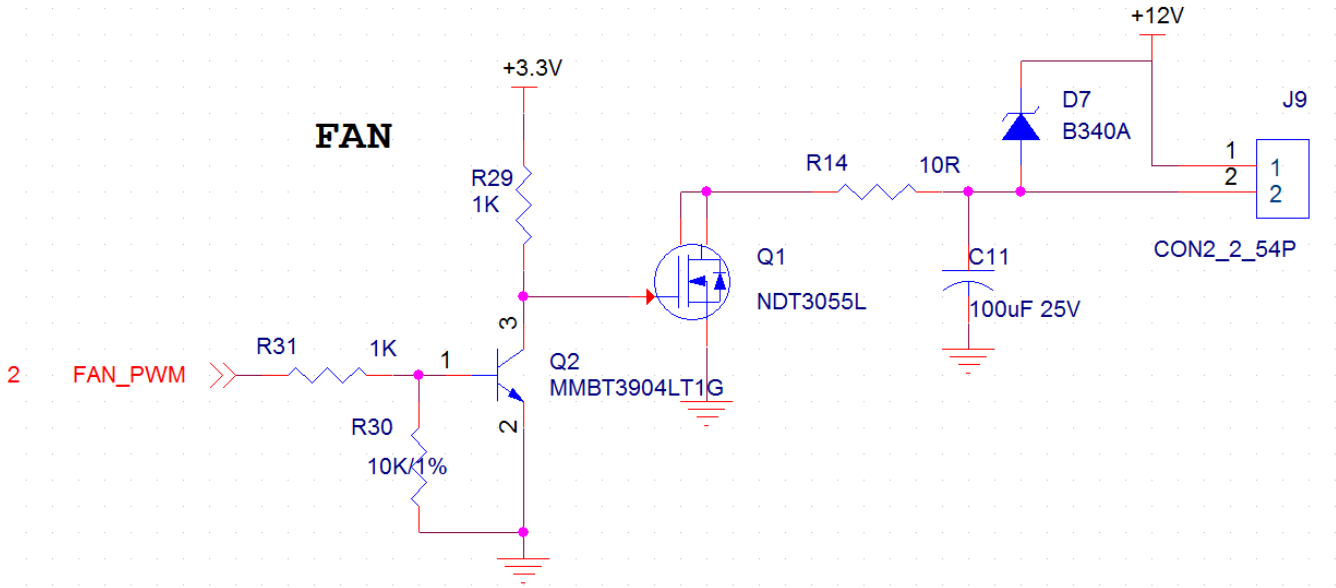


Figure 3-17-1: The design of fan on the development board

The fan has been fixed on the development board with screws before delivery. The power supply of the fan is connected to the socket of the J9. The red one is positive and the black one is negative.

3.18 Structure and Dimension

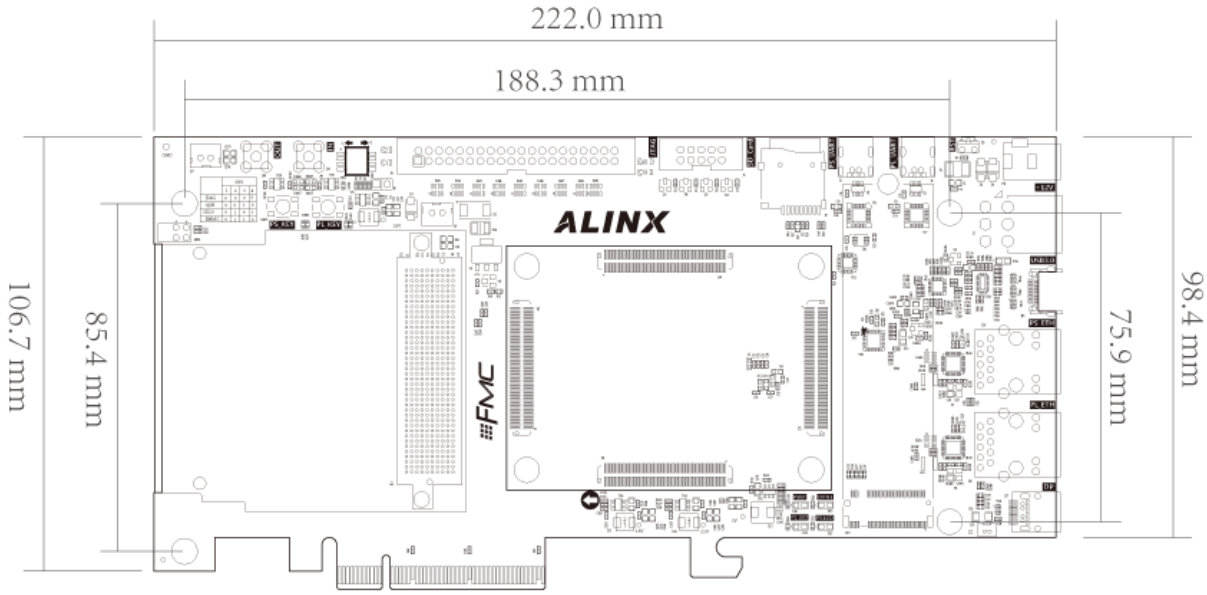


Figure 3-18-1: Top View