An9920 3-Pin Switch-Mode LED Lamp Driver

Features

- Constant output current: 100mA
- Universal 85-264VAC operation
- Fixed off-time buck converter
- Internal 475 V power MOSFET

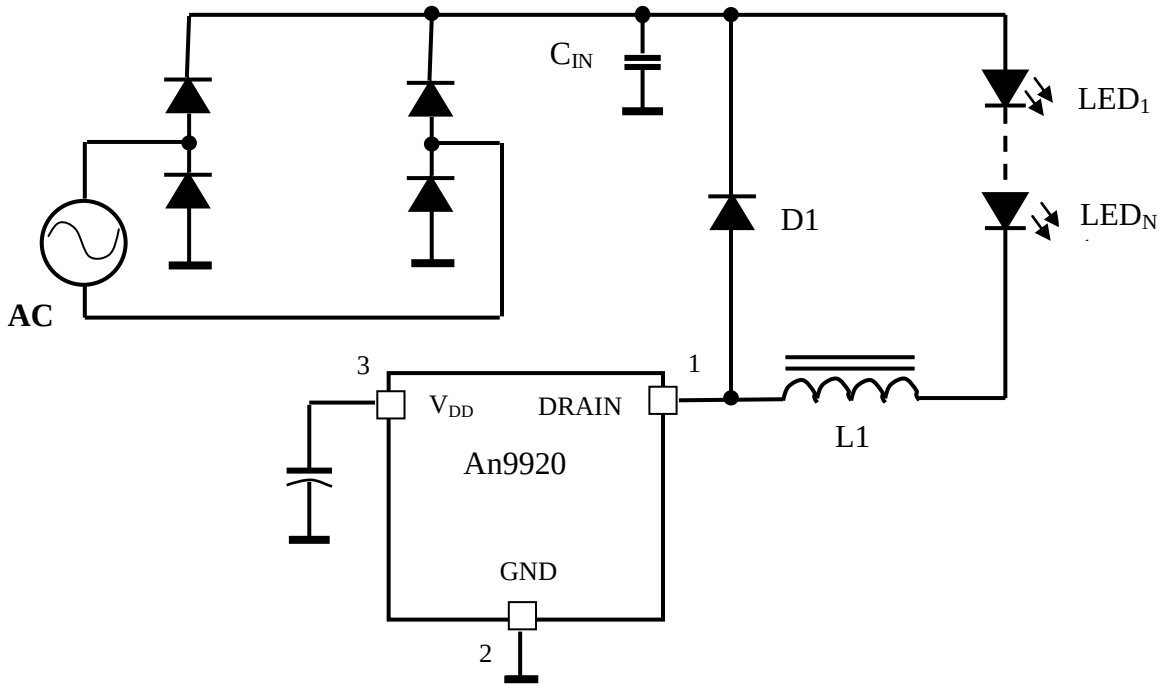
Applications

- Decorative lighting
- Low power lighting fixtures

General Description

The An9920 is a pulse width modulated (PWM) high efficiency LED driver control IC. It allows efficient operation of LED strings from voltage sources ranging up to 400VDC. The An9920 includes an internal high voltage switching MOSFET controlled with fixed off-time (T_{OFF}) of approximately 10.5µs. The LED string is driven at constant current, thus providing constant light output and enhanced reliability. The output current is internally fixed at 100mA for An9920. The peak current control scheme provides good regulation of the output current throughout the universal AC line voltage range of 85 to 264VAC or DC input voltage of 20 to 400V and is inherently protected from input under-voltage condition.

Typical Application Circuit



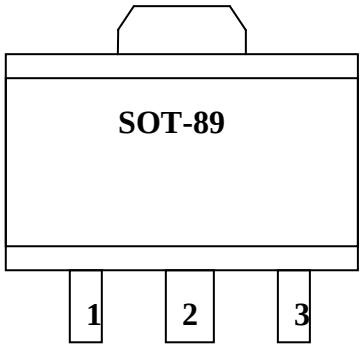
Absolute Maximum Ratings

Parameter	Value
Supply voltage, V_{DD}	-0.3 to +10V
Supply current, I_{DD}	+5mA
Operating ambient temperature range	-40 ºC to +85 ºC
Operating junction temperature range	-40 ºC to +125 ºC
Storage temperature range	-65 ºC to +150 ºC
Power dissipation @ 25 ºC, SOT-89	1600mW (Mounted on FR4 board, 25mm x 25mm x 1.57mm)

Stresses beyond those listed under ''Absolute Maximum Ratings'' may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Also limited by package power dissipation limit, whichever is lower.

Pin Configurations



DRAIN GND VDD

Top View

Electrical Characteristics

(*Specifications are at T_A = 25°C and V_{DRAIN}=50V, unless otherwise noted)*

Symbol	Description	Min.	Typ.	Max.	Units	Conditions
Regulator (V_{DD})						
V_{DD}	V_{DD} regulator output	-	7.8	-	V	---
V_{DRAIN}	V_{DRAIN} supply voltage	20	-	-	V	---
V_{UVLO}	V_{DD} undervoltage threshold	5.0	-	-	V	---
ΔV_{UVLO}	V_{DD} undervoltage lockout hysteresis	-	200	-	mV	---
I_{DD}	Operating supply current	-	220	400	µA	$V_{DD(EXT)}$ = 8.5V, V_{DRAIN} = 40V
Output (DRAIN)						
V_{BR}	Breakdown voltage *	475	-	-	V	---
R_{ON}	On-resistance	-	-	100	Ω	I_{DRAIN} = 100mA
C_{DRAIN}	Output capacitance #	-	1.0	5.0	pF	V_{DRAIN} = 400V
I_{SAT}	MOSFET saturation current #	150	210	-	mA	---
Current Sense Comparator						
I_{TH}	Threshold average current *	98	115	126	mA	---
T_{BLANK}	Leading edge blanking delay * #	200	300	400	ns	---
$T_{ON(MIN)}$	Minimum on-time	-	-	1300	ns	---
OFF-Time Generator						
T_{OFF}		8	10.5	13	µs	---

Note:

***-** Denotes the specifications which apply over the full operating ambient temperature range of - 40 ºC < T_A < + 85 ºC.

- Denotes guaranteed by design.

Functional Description

Input Voltage Regulator

The An9920 is a PWM peak current controller for controlling a buck converter topology in continuous conduction mode (CCM). The output current is internally preset at 100mA.

When the input voltage of 20 to 400V appears at the DRAIN pin, the internal high-voltage linear regulator seeks to maintain a constant voltage 7.8VDC at the V_{DD} pin. Until this voltage exceeds the internally programmed under-voltage threshold, the output switching MOSFET is non-conductive. When the threshold is exceeded, the MOSFET turns on. The input current begins to flow into the DRAIN pin. Hysteresis is provided in the under-voltage comparator to prevent oscillation.

When the input current exceeds the internal preset level, a current sense comparator resets an RS flip-flop, and the MOSFET turns off. At the same time, a one-shot circuit is activated that determines the duration of the off-state (10.5µs typ.). As soon as this time is over, the flip-flop sets again. The new switching cycle begins.
A "blanking" delay of 300ns is provided that prevent false triggering of the current sense comparator due to the leading edge spike caused by circuit parasitics.

Application Information

The An9920 is a low-cost off-line buck converter IC specifically designed for driving multi-LED strings. It can be operated from either universal AC line range of 85 to 264VAC, or 20 to 400 VDC, and drives up to tens of high brightness LEDs. All LEDs can be run in series, and the An9920 regulates at constant current, yielding uniform illumination. The An9920 is compatible with triac dimmers. The output current is internally fixed at 100mA. This part is available in space saving TO-92 and SOT-89 package.

Selecting L1 and D1

There is a certain trade-off to be considered between optimal sizing of the output inductor L1 and the tolerated output current ripple. The required value of L1 is inversely proportional to the ripple current ΔI_O in it.

$$\mathbf{L1 = (V_O \cdot T_{OFF}) / \Delta I_O} \qquad \mathbf{(1)}$$

where V_O is the forward voltage of the LED string. T_{OFF} is the off-time of the An9920.The output current in the LED string (I_O) is calculated then as:

$$\mathbf{I_O = I_{TH} - (\Delta I_O / 2)} \qquad \mathbf{(2)}$$

where I_{TH} is the current sense comparator threshold. The ripple current introduces a peak-to-average error in the output current setting that needs to be accounted for. Due to the constant off-time control technique used in the An9920, the ripple current is independent of the input AC or DC line voltage variation. Therefore, the output current will remain unaffected by the varying input voltage.

Adding a filter capacitor across the LED string can reduce the output current ripple even further, thus permitting a reduce value of L1. However, one must keep in mind that the peak-to-average current error is affected by the variation of T_{OFF}. Therefore, the initial output current accuracy might be sacrificed at large ripple current in L1.

Another important aspect of designing an LED driver with the An9920 is related to certain parasitic elements of the circuit, including distributed coil capacitance of L1, junction capacitance and reverse recovery of the rectifier diode D1, capacitance of the printed circuit board traces C_{PCB} and output capacitance C_{DRAIN} of the controller itself. These parasitic elements affect the efficiency of the switching converter and could potentially cause false triggering of the current sense comparator if not properly managed. Minimizing these parasitics is essential for efficient and reliable operation of the An9920.

Coil capacitance of inductors is typically provided in the manufacture′s data books either directly or in terms of the self-resonant frequency (SRF).

$$\mathbf{SRF = 1 / [2\pi \cdot \sqrt{(L \cdot C_L)}]}$$

where L is the inductance value, and C_L is the coil capacitance. Charging and discharging this capacitance every switching cycle causes high-current spikes in the LED string. Therefore, connecting a small capacitor C_O (~10nF) is recommended to bypass these spikes.

Using an ultra-fast rectifier diode for D1 is recommended to achieve high efficiency and reduce the risk of false triggering of the current sense comparator. Using diodes with shorter reverse recovery time t_{rr} and lower junction capacitance C_J achieves better performance. The reverse voltage rating V_R of the diode must be greater than the maximum input voltage of the LED lamp.

The total parasitic capacitance present at the DRAIN pin of the An9920 can be calculated as:

$$\mathbf{C_P = C_{DRAIN} + C_{PCB} + C_L + C_J} \qquad \mathbf{(3)}$$

When the switching MOSFET turns on, the capacitance C_P is discharged into the DRAIN pin of the IC. The discharge current is limited to about 210mA typically. However, it may become lower at increased junction temperature. The duration of the leading edge current spike can be estimated as:

$$T_{SPIKE} = [(V_{IN} \cdot C_P) / (I_{SAT})] + t_{rr} \quad (4)$$

In order to avoid false triggering of the current sense comparator, C_P must be minimized in accordance with the following expression:

$$C_P < I_{SAT} \cdot (T_{BLANK(MIN)} - t_{rr}) / V_{IN(MAX)} \quad (5)$$

where $T_{BLANK(MIN)}$ is the minimum blanking time of 200ns, and $V_{IN(MAX)}$ is the maximum instantaneous input voltage. .

Estimating Power Loss

Discharging the parasitic capacitance CP into the DRAIN pin of the An9920 is responsible for the bulk of the switching power loss. It can be estimated using the following equation:

$$P_{SWITCH} = [(V_{IN}^2 \cdot C_P / 2) + V_{IN} \cdot I_{SAT} \cdot t_{rr}] \cdot F_S \quad (6)$$

where F_S is the switching frequency, I_{SAT} is the saturated DRAIN current of the An9920. The switching loss is the greatest at the maximum input voltage. The switching frequency is given by the following:

$$F_S = (V_{IN} - \eta^{-1} \cdot V_O) / V_{IN} \cdot T_{OFF} \quad (7)$$

where η is the efficiency of the power converter.

When the An9920 LED driver is powered from the full-wave rectified AC input, the switching power loss can be estimated as:

$$P_{SWIYCH} \approx [1 / (2 \cdot T_{OFF})] \cdot (V_{AC} \cdot {}_P + 2 \cdot I_{SAT} \cdot t_{rr}) \cdot (V_{AC} - \eta^{-1} \cdot V_O) \quad (8)$$

V_{AC} is the input AC line voltage.

The switching power loss associated with turn-off transitions of the DRAIN pin can be disregarded. Due to the large amount of parasitic capacitance connected to this switching node, the turn-off transition occurs essentially at zero- voltage. Conduction power loss in the An9920 can be calculated as:

$$P_{COND} = (D \cdot I_O^2 \cdot R_{ON}) + [I_{DD} \cdot V_{IN} \cdot (1 - D)] \quad (9)$$

where $D = V_O / (\eta \cdot V_{IN})$ is the duty ratio, R_{ON} is the on-resistance, IDD is the internal linear regulator current.

When the LED driver is powered from the full-wave rectified AC line input, the exact equation for calculating the conduction loss is more cumbersome. However, it can be estimated using the following equation:

$$P_{COND} = (K_C \cdot I_O^2 \cdot R_{ON}) + (K_D \cdot I_{DD} \cdot V_{AC}) \quad (10)$$

where V_{AC} is the input AC line voltage. The coefficients K_C and K_D can be determined from the minimum duty ratio of the An9920.

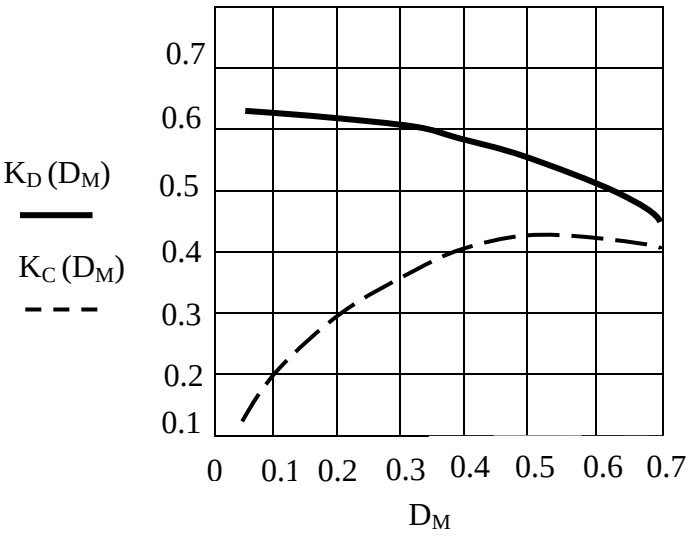


Fig.1. Conduction Loss Coefficients K_C and K_D

EMI Filter

As with all off-line converters, selecting an input filter is critical to obtaining good EMI. A switching side capacitor, albeit of small value, is necessary in order to ensure low impedance to the high frequency switching current of the converter. As a rule of thumb, this capacitor should be approximately 0.1 - 0.2µF/W of LED output power. A recommended input filter is shown in Figure 2 for the following design example.

Design Example

Let us design an An9920 LED lamp driver meeting the following specification:

Input: Universal AC, 85-135VAC

Output Current: 100mA

Load: String of 24 LED (Power TOPLED OSRAM® V_F = 2.5V max. each)

Step 1. Calculation L1.

The output voltage V_O =24 x V_F =60V (max.). Use equation (1) assuming a 30% peak-to-peak ripple.

$L1 = (60V \cdot 10.5\mu s) / (0.3 \cdot 100mA) = 21mH$

Select L1 = 22mH, I = 150mA. Typical SRF = 270KHz. Calculate the coil capacitance.

$C_L = 1 / [L1 \cdot (2\pi \cdot SRF)^2] = 1 / [22mH \cdot (2\pi \cdot 270KHz)^2] \approx 15pF$

Step 2. Selecting D1.

Select D1 MUR160 with $V_R = 600V$, trr ≈ 50ns and $C_J \approx 8pF$ (V_F>50V).

Step 3. Calculating total parasitic capacitance using (3).

$C_P = 5pF + 5pF + 15pF + 8pF = 33pF$

Step 4. Calculating the leading edge spike duration using (4), (5).

$T_{SPIKE} = (135V \cdot \sqrt{2} \cdot 33pF) / 150mA + 50ns \approx 92ns < T_{BLANK(MIN)}=200ns$

Step 5. Estimating power dissipation in An9920 at 135VAC using (8) and (10).

Let us assume that the overall efficiency η = 0.7.

Switching Power Loss

$P_{SWITCH} = (135V \cdot 33pF + 2 \cdot 150mA \cdot 50ns) \cdot (135V - 60V/0.7) / (2 \cdot 10.5\mu s) \approx 46mW$

Minimum Duty Ratio

$D_M = 60V / (0.7 \cdot 135V \cdot \sqrt{2}) \approx 0.45$

Conduction Power Loss

$P_{COND} = 0.42 \cdot (100mA)^2 \cdot 100\Omega + 0.57 \cdot 200\mu A \cdot 135V \approx 435mW$

Total Power Dissipation in An9920:

$P_{TOTAL} = 46mW + 435mW = 481mW$

Step 6. Selecting input capacitor C_{IN}

Output Power = 60V · 100mA = 6W

Select $C_{IN} = 0.68\mu F$, 250V

Figure 2. Universal 85 - 135VAC LED Lamp Driver

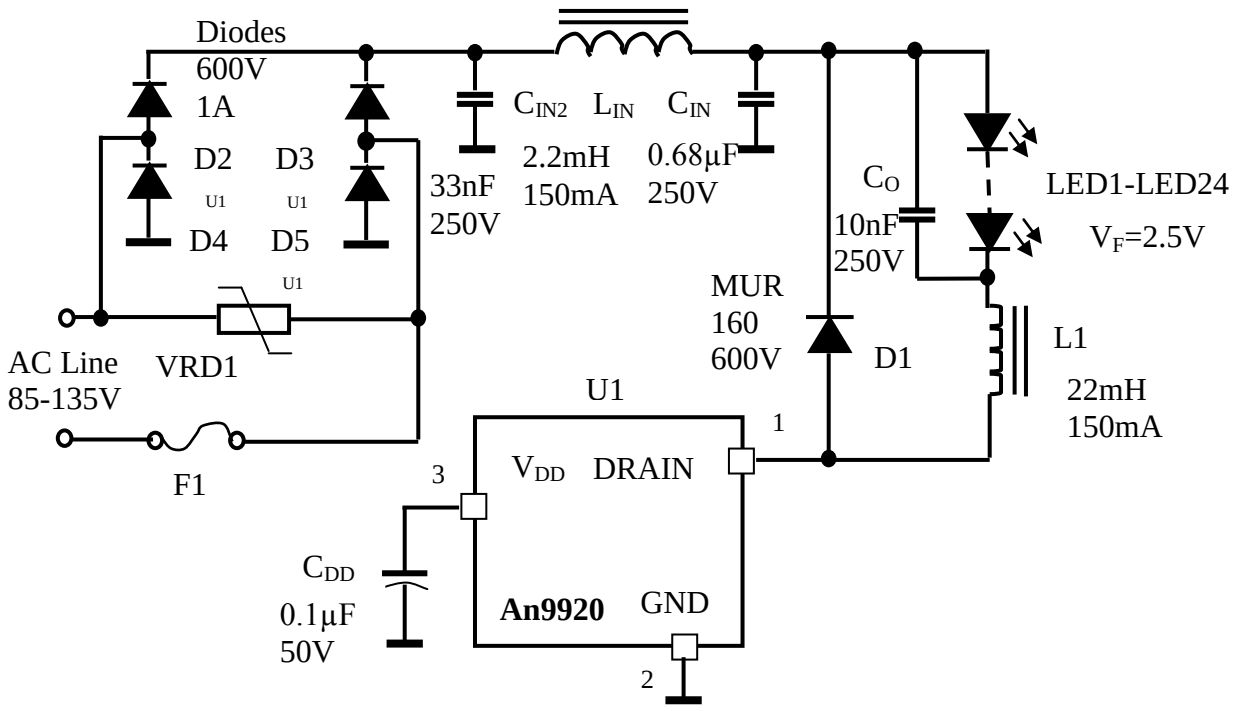


Figure 3. Typical Efficiency

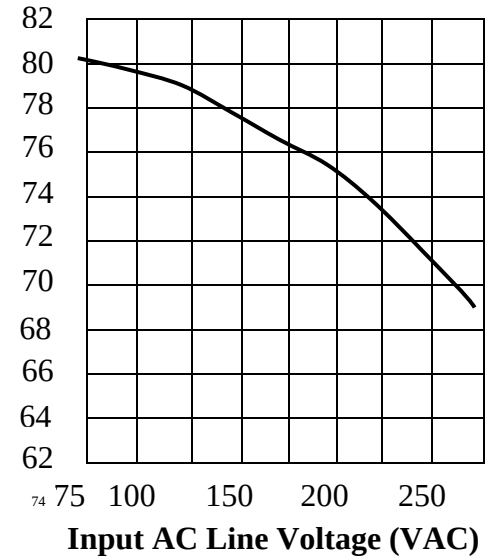


Figure 4. Switch-On-Off Transition. Ch1: V_{DRAIN}, Ch3: I_{DRAIN}

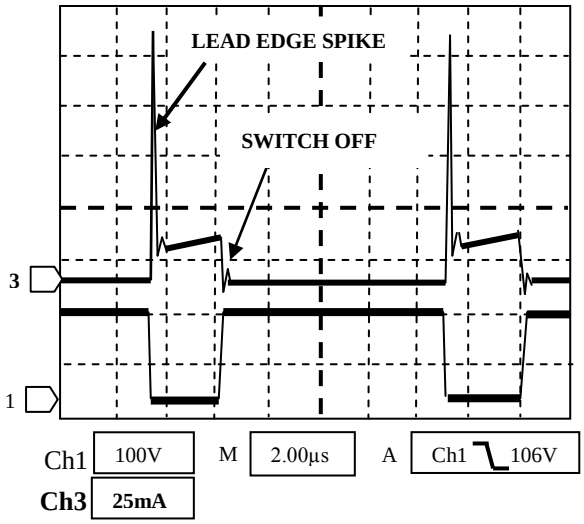


Figure 5. Lead Edge Spike Ch1: V_{DRAIN}, Ch3: I_{DRAIN}

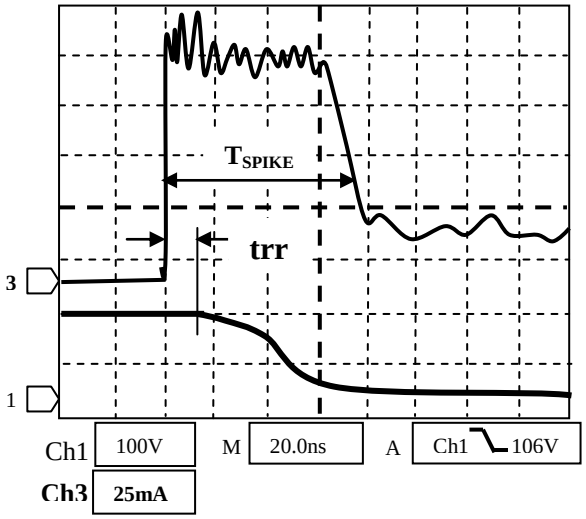
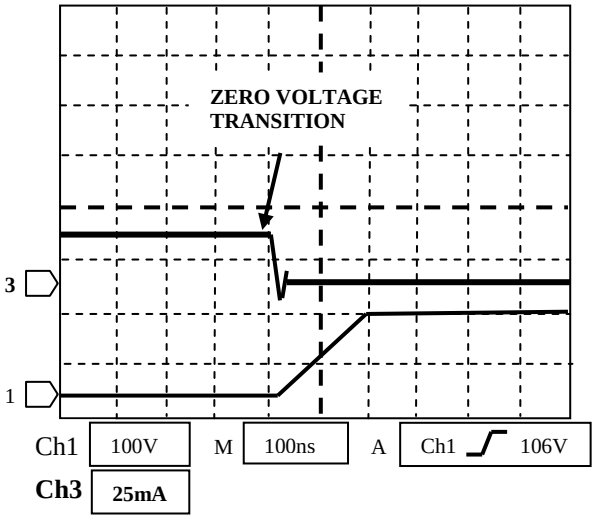
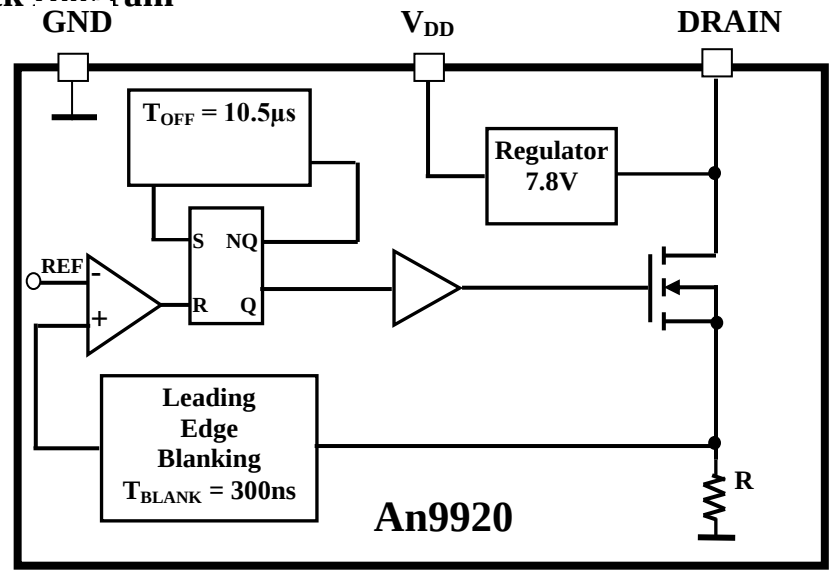


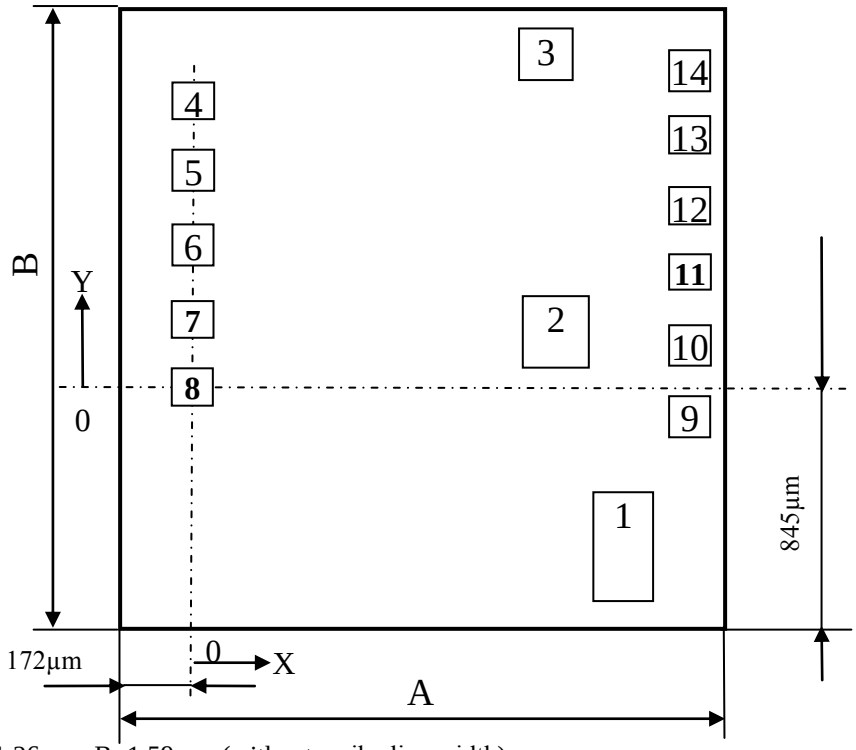
Figure 6. Switch-Off Transition. Ch1: V_{DRAIN}, Ch3: I_{DRAIN}



Functional Block Diagram



Pad Diagram



1. Chip size: A=1.26mm, B=1.59mm (without scribe line width).
2. Scribe line width: X=80µm, Y=80µm
3. Pad size: Pad 1: 101µm x 202µm
   Pad 2: 125µm x 165µm
   Pad 3: 100µm x 100µm
   Pad 4÷Pad 14: 90µm x 90µm
4. Substrate to GND.
5. Wafer thickness: 460 µm

Pad Description and Location

№ Pad	Symbol	Description	X (мкм)	Y (мкм)
1	DRAIN	Switching MOSFET Drain Output and Linear Regulator Input	883	-554
2	GND	Common Connection for all Circuits	712	130
3	V_{DD}	Power Supply Pin for Internal Control Circuit. Bypass this pin with a 0.1µF low impedance capacitor	692	638
4	V_{REF}	Reference Voltage Output, Test Pad	0	520
5	GND1	Ground Input for V_{REF} trimming, Test Pad	0	390
6	F0	V_{REF} Trimming Least Significant Input, Test Pad	0	260
7	F1	V_{REF} Trimming Middle Significant Input, Test pad	0	130
8	F2	V_{REF} Trimming Most Significant Input, Test Pad	0	0
9	S	Switching MOSFET Source Output, Test Pad	983	-21
10	F5	I_{TH} Trimming Most Significant Input, Test Pad	983	109
11	F4	I_{TH} Trimming Middle Significant Input, Test Pad	983	239
12	F6	I_{TH} Trimming Common Input, Test Pad	983	369
13	F3	I_{TH} Trimming Least Significant Input, Test Pad	983	499
14	G	Gate Input, Test Pad	983	629

An9920 Layout Considerations

See Figure 7 for a recommended circuit board layout for the An9920.

Single Point Grounding

Use a single point ground connection from the input filter capacitor to the area of copper connected to the GND pin.

Bypass Capacitor (C_{DD})

The V_{DD} pin bypass capacitor C_{DD} should be located as near as possible to the V_{DD} and GND pins.

Switching Loop Areas

The area of the switching loop connecting the input filter capacitor C_{IN}, the diode D1 and the An9920 together should be kept as small as possible.
The switching loop area connecting the output filter capacitor C_O, the inductor L1 and the diode D1 together should be kept as small as possible.

Thermal Considerations vs. Radiated EMI

The cooper area where GND pin is connected acts not only as a single point ground, but also as a heat sink.
This area should be maximized for good heat sinking, especially when An9920 (SOT-89 package), is used.
The same applies to the cathode of the free-wheeling diode D1. Both nodes are quiet and therefore, will not cause radiated RF emission. The switching node copper area connected to the DRAIN pin of the An9920, the anode of D1 and the inductor L1 needs to be minimized. A large switching node area can increase high frequency radiated EMI.

Input Filter Layout Considerations

The input circuit of the EMI filter must not be placed in the direct proximity to the inductor L1 in order to avoid magnetic coupling of its leakage fields. This consideration is especially important when unshielded construction of L1 is used. When an axial input EMI filter inductor L_{IN} is selected, it must be positioned orthogonal with respect to L1. The loop area formed by C_{IN2}, L_{IN}, and C_{IN} should be minimized. The input lead wires must be twisted together.

Figure7. Recommended circuit board layout with the An9920 (SOT-89 package)