

AN0022

Getting started guide for AT32F415 series

Introduction

This user manual provides information on how to use AT32F415 MCU for project development in a quickly manner.

Applicable products :

Part number	AT32F415xx
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1 Development environment

MCU resources download address:

■ Visit Artery website: <u>http://www.arterytek.com</u>

1.1 Set up AT32 development environment

1.1.1 Debug tools

At present, AT32F415 evaluation board is equipped with AT-Link/J-Link. The following picture is for AT-START-F415 (right) with AT-Link-EZ (left).



Figure 1. AT-Link

1.1.2 Programming tools and software

AT programming tools and software: AT_Link, ICP/ISP. Third-party programming tools:

- Xuanwei: <u>https://xuanweikeji.taobao.com</u>
- Maxwiz: <u>www.maxwiz.com.cn</u>
- ZLG: <u>http://tools.zlg.cn/tools</u>
- Amo:http://www.amomcu.cn



1.1.3 AT32 KEIL and IAR development environment

For Keil compiling system, it is recommended to use Keil 4.74, 5.13 or above.
 When using AT-Link in Keil environment, select "CMSIS-DAP debugger "in "Debug".

	Figure	2. Keil D)ebug	option		
Device Target Output Listing Vser	C/C++ A	sm Linker	Debug	Vtilities		
C Use Simulator with restrictions	Settings	⊙ <u>U</u> se: CMSI	S-DAP Del	bugger	•	Settings
Limit Speed to Real-Time						

In "Utilities", first untick the box "Use Debug Driver" and then tick it again.

 Figure 3. Keil Utilities option

 Device Target Output Listing User
 C/C++
 Asm
 Linker
 Debug
 Vtilities

 Configure Rash Menu Command
 Image: Configure Rash Menu Command
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 Image: Configure Rash Menu Command

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 Image: Configure Rash Menu Command
 Image: Configure Rash Menu Command

 Image: Configure Rash Menu C

② For IAR compiling system, it is recommended to use IAR 7.0, IAR 6.1 or above.
 When using AT-Link-EZ in IAR environment, select "CMSIS-DAP" in "Debugger".

Figure 4. Select CMSIS_DAP in the IAR_Debugger

Kuntime Checking C/C++ Compiler Assembler	Setup	Download	Images	Extra Options	Multicore	Plugins	
Output Converter Custom Build Build Actions	<u>D</u> river CMSI	s dap	~	<u> R</u> un to main			
Debugger Simulator	- S <u>e</u> tu	p macros					

③ BSP and PACK

For detailed operation on BSP and PACK, please refer to *BSP and Pack application note* available in the BSP folder.



2 Enhanced functions of AT32F415

2.1 Prefetch buffer

Thanks to the prefetch buffer, faster CPU execution is possible as the CPU fetches one word at a time with the next word readily available in the prefetch buffer. The prefetch controller decides whether to access the Flash memory according to the available space in the prefetch buffer. The Prefetch controller starts a read operation when there is at least one free space.

Different latency should be set for different SYSCLK by setting the bit2~0 in the FLASH_ACR register.

LATENCY: Latency

These bits represent the ratio of the SYSCLK period to the Flash access time.

000: Zero wait state, if 0 <SYSCLK≤ 32 MHz

001: One wait state, if 32 <SYSCLK≤ 64 MHz

010: TWO wait states, if 64 <SYSCLK≤ 96 MHz

011: Three wait states, if 96 <SYSCLK≤ 128 MHz

100: Four wait states, if 128 <SYSCLK≤ 150 MHz

The following bond font is added in the system frequency configuration function of AT. For others, find the same location to do the same settings.

```
static void SetSysClockTo72M(void)
    ...
    ...
   if (HSEStatus == (uint32_t)0x01)
    #if defined (AT32F415xx)
    /* Enable Prefetch Buffer */
   FLASH->ACR /= FLASH_ACR_PRFTBE;
                                                              //Enable the prefetch buffer
   /* Flash 1 wait state */
  FLASH->ACR &= (uint32_t)((uint32_t)~FLASH_ACR_LATENCY);
FLASH->ACR |= (uint32_t)FLASH_ACR_LATENCY_2;
                                                           //Two wait states
#endif
...
•••
}
• • •
• • •
}
```

Note: The prefetch buffer must be kept on when using a prescaler different from 1 on the AHB clock.



2.2 PLL clock settings

There are two ways to configure the PLL of AT32F415 series: RCC_CFG and RCC_PLL. Use the RCC_PLL configuration to configure more PLL clock frequency with the formula: PLL output clock= PLL reference input clock x PLL_NS / (PLL_MS x PLL_FR).

PLL reference input clock: set to the same parameters as the actual HSE or HSI by PLL_FREF PLL_NS: 31~500 PLL_MS: 1~15 PLL_FR: set by PLL_FR

The following bond font is added in the AT library system frequency configuration function, such as void SetSysClockTo150M (void), HSE=8 MHz.

Note: When using RCC_PLL, 500MHz <= PLL reference input clock x PLL_NS/PLL_MS <= 1000MHz must be met.



2.3 PLL auto step-by-step frequency switching function

When the PLL embedded in the AT32F415 series is greater than 108 MHz, the auto step-by-step frequency switching function should be operated. The following bond font is added in the system frequency configuration function of AT library, such as void SetSysClockTo150M (void). For others, find the same location to do the same settings.

```
static void SetSysClockTo150M(void)
{
  if (HSEStatus == (uint32_t)0x01)
  {
...
    /* Wait till PLL is ready */
    while((RCC->CTRL & RCC_CTRL_PLLSTBL) == 0)
    }
#if defined (AT32F413xx) || defined (AT32F415xx)
    RCC_StepModeCmd(ENABLE);
                                       // enable the auto step-by-step frequency switching function
#endif
    /* Select PLL as system clock source */
    RCC->CFG &= (uint32_t)((uint32_t)~(RCC_CFG_SYSCLKSEL));
    RCC->CFG |= (uint32_t)RCC_CFG_SYSCLKSEL_PLL;
    /* Wait till PLL is used as system clock source */
    while ((RCC->CFG & (uint32_t)RCC_CFG_SYSCLKSTS) != RCC_CFG_SYSCLKSTS_PLL)
    {
#if defined (AT32F413xx) || defined (AT32F415xx)
    RCC_StepModeCmd(DISABLE);
                                     //disable the auto step-by-step frequency switching function
#endif
  }
}
```

Note: If the auto step-by-step frequency switching feature is enabled, it must be disabled after the clock is switched, and enable and disable must be paired.



2.4 Encryption (Read protection)

2.4.1 Read protection

Read protection, commonly referred to as "encryption", acts on the entire Flash storage area. Once the read protection is set in the Flash, the embedded Flash storage area can only be read through the normal execution of the program instead of JTAG or SWD. When the read protection is disabled using ISP/ICP tool, the chip will erase the Flash.

ISP/ICP tool can be used to enable/disable read protection as follows:

ICP tool

Read protection: "Target"---"read protection"---"enable protection"

Artery ICP Pr	rogrammer_V2.	4.00				_		\times	
File J-Link	settings AT	-Link settings	Target	Language	Help	_			
Disconnect	Part Numbe	r: AT32F415F		ss erase se main flash		17	ΓE	7	
AT-Link v	AT-Link-EZ AT-Link SN:	FW Vers EFDC4151010		se sectors		1.	特		
	SPIM	FLACIL DA		tion Bytes		Ħ	17	/]	
		FLASH_DA	Rea	d protection	•		Enable	common	read protection
	Type GD25Q1	27C 16M	sLib	o status			Enable	advance	d read protection
Memory read	-		Sys	tem memory	AP mode	_	Disable		
Address 0x	0800000	Read size Ox	Dov	wnLoad			Read		
File info			Flas	sh CRC					
	name ect_L0.hex	File siz 9480	Deb	bug	0,00001000-00	- 01757,		dd lete	

Figure 5. ICP enable read protection

Disable read protection: "Target"----"read protection"----"disable read protection"

Figure 6. ICP disable read protection

	ogrammer_V2.4.00 settings AT-Link	settings	Target	Language	Help			×	
Disconnect	Part Number: A		Ma	ss erase se main flash		12	FER	γ	
T-Link v	AT-Link-EZ AT-Link SN: EF	FW Vers DC4151010		se sectors			特		
	SPIM	FLASH_DA		tion Bytes	•	.			read protection
	Type GD25Q127C	16M	sLib	o status		-			read protection
Memory read	-		Sys	tem memory	AP mode		Disable		
Address 0x	08000000 Rea	ad size Ox	Dov	wnLoad			Read		
File info			Flas	sh CRC					
No. File r	ame ct L0.hex	File siz 9480		bug	8,00001000-000	01757	Ad 08 Dele	_	



Artery ISP Programmer tool

Read protection: "*enable/disable protection*"---"*enable---read protection*"---"*Next*"---" Yes", and the program is encrypted.

Figure 7. ISP enable read protection

Erase	● All ○ Selec	tion	🔿 Edit Opti	ion Byt
Downlo	ad to device		🔿 Disable s	5Lib
sLib	Status: DISABLE	Start page		
Remai	ning usage times: 256	DATA start pa	ge	
Passw	ord Ox	End page		
No.	File Name	File Size	111 p (p)	
0pt	optio rimize te us	u sure to enable the rea	Address Range(0x)	Delet
Opt Wri Addr	optio timize	u sure to enable the rea	ad protection?	Delet
Opt Wri Addr App End	optio imize ite us. ess O: oly Option Bytes	u sure to enable the rea	nd protection?	Delet wnload ram
Opt Wri Addr App End	optio timize te us ess Or ply Option Bytes able Read Protection aft	u sure to enable the rea	nd protection?	Delet wnload ram

Disable read protection: "*enable/disable protection*"---"*disable-read protection*"---"*Next*"— "Yes", and then the Flash can be unencrypted.

	SP Programmer_V1.5.30		-	
	, <u>1715</u>	<mark>マ</mark> Y 雅	特力	
O Erase O Downlo	 All Selecti ad to device 	on	○ Edit O ○ Disabl	ption Byte: e sLib
Renai	Status: DISABLE ning usage times: 256 ord Ox	Start page DATA start p End page	ago	
No.	File Name	File Size	Address Range(Ox)	Add
E_{T}	The flash memory	will be mass erased	and all contents will b	be a
Er A		will be mass erased to disable the read	and all contents will b protection? Yes No	be in the second se
A.		to disable the read	protection?	
A Enc	lost ,Are you sure	to disable the read	protection?	De la
Upload Firmwaa Flash	I lost Are you sure able Read Protection after from device re CEC Page fill [] CEC Start page page0—	to disable the read	Protection? Yes No nd page page0-0x800	

Figure 8. ISP disable read protection



Artery ISP Multi-Port Programmer

Read protection: "*enable/disable protection*"---"*enable-read protection*"---click on "Begin", and then the program is encrypted.

	-	D. ISP Multi-	Port P	rograr	nmer ena	ble read pi	rot ×
			ESA	雅			
guage 	English Port name	<pre>Port type: UART Device AT32F403AVGT7_1024K</pre>	~ Progress		Refresh	(F5)	
					Begin(F2)		>
	load files						
No.	File name			File size	Address range(Ox)	Add	
ption	bytes file:					Open Edit	
pera	tion Downlo	ad Settings UART Set	tings SPIM	Settings			٦
() Ma	ss erase	O Page erase		🔘 Download	APP 🔘 Downlo	ad option bytes file	
() Fi	rmware CRC		protection	ENABLE	Read Protection	×	
_	sable sLib able password	0x	⊖ Flash C	AC Start page End page	2	~ ~	
Proje	ct file setting						
Proje	t info:			Open proje	ct Save project	🗌 Project mode	

Disable read protection: "*enable/disable protection*"--- "*disable-read protection*"—click on "*Begin*", then the Flash is unencrypted. The read protection cannot be disabled by the erase operation.

Artery ISP Multi-Port					
	Programmer_ V1.4.00				- 🗆 🗙
	ا۲۲ ا	ESA.	雅特	寺力	
anguage: English	∨ Port type: UART	\sim		Refresh(F5)	🖌 Select all
No. Port name	Device	Progress		Status	
1 COM10	AT32F403AVGT7_1024K				
<					>
				Begin(F2)	Cancel(Esc)
Download files					
No. File name		Fi	le size	Address range(Ox)	Add
					Delete
Option bytes file:				Op	en Edit
Option bytes file:				0p	en. Edit
	ad Settings UART Se	ttings SPIM Set	tings	0p	en Edit
Operation Downloa	-	-	-		
Operation Downlos	O Page eraze		tings Download A	PP O Download o	en Edit
Operation Downloa	-		-		
Operation Downlos	O Page eraze	e protection DI	Download A SABLE	PP O Download o	
Operation Downlos	O Page eraze	e protection III O Flash CRC	Download A	PP O Download o	
Operation Downlow Mass erase Firmware CRC Disable sLib	O Page eraze	e protection III O Flash CRC	Download A SABLE Start page	PP O Download o	

Figure 10. ISP Multi-Port Programmer disable read protection



2.4.2 Write protection

Write protection acts on the whole Flash storage area or some pages. Once the write protection is set in the Flash, the embedded Flash storage area cannot be written in any way. ISP/ICP tools can be used to enable/disable the write protection.

① Artery ICP Programmer tool

Enable write protection: click "*Target*"---"*Write protection option byte*"----Select the pages to be protected----"*Apply to device*"

File J-Link	settings AT-Li	ink settings	Targ	et Li	angua	ge H	lelp				
Disconnect	Part Number:	AT32F415	RCT7-	7 F	lashSi	ze: 25	6KB		17	E	7Y
	Option Bytes	Photo Annalia									
T-Link	Option Bytes										
	Read protectio	n option byt	es								
	RDP A5	Disable		~							
Memory re	User option by	tes									
Address 0x	USER FF	WDG SW	nRs	T_STOP	M ni	RST_STC	BY				
File info	Write protection	n option byt	es								
No. File	Name	Start addres	s End	addres	s Si	ze		w	^		WRP0 F9
	page0	0x8000000	0x8	0007FF	0	(800(2K)		N			
	page1	0x8000800	0x8	OOOFFF	0	/800(2K)		N			WRP1 FF
	page2	0x8001000		0017FF		(800(2K)		Y			WRP2 FF
	✓ page3	0x8001800 0x8002000		001FFF 0027FF		(800(2K) (800(2K)		Y V			WRP3 FF
	i page4 i page5	0x8002000		0027FF		(800(2K)		v v			
Flash info	- anané	0-9002000		002755		-000/10/			~		Select all
_	Data option by	tes									
	Date	0	1	2	3	4	5	6	7	^	Clear
	Data 07 (0x)	FF	FF	FF	FF	FF	FF	FF	FF		cicui
	Data 815 (0x) FF	FF	FF	FF	FF	FF	FF	FF	11	
	Data 1623 (0	x) FF	FF	FF	FF	FF	FF	FF	FF		Load file
	Data 2431 (0	x) FF	FF	FF	FF	FF	FF	FF	FF		Save to file
10:29:26 : AT-											
10:29:27 : Part											
10:29:27 : Part 10:29:27 : Tarç											

Figure 11. ICP pgrammer enable read protection

Disable write protection: click "*Target*"---"*Write protection option byte*"----Select the pages to be canceled ---"*Apply to device*". The write protection cannot be disabled by the erase operation.

ile J-Link	settings AT-	Link settin	gs Tai	rget Li	inguage	н н	elp					
isconnect	Part Numbe	r: AT32F4		7-7 F	lashSizo	e: 256	КВ	;	17	ΓΞ	7 Y	L
-Link	Ø Option Bytes											
-LINK												
	Read protect	ion option	oytes									
	RDP A5	Disable		~								
lemory re	User option	ovtes										
lemory re												
ddress 0x	USER FF	WDG_S	N 🗹 nF	RST_STOP	✓ nRS	T_STD	ЗY					
ile info	Write protect	ion ontion	hutes									
No. File	Name	Start add		nd addres					•			
	Dage0	0x80000		nd addres x80007FF		, 00(2K)		W			WRP0	FF
	paget	0x80008		x8000FFF		00(2K)		N			WRP1	FF
	page2	0x80010		x80017FF		00(2K)		N			WRP2	FF
	page3	0x80018	0 0	x8001FFF	0x8	00(2K)		N			WRP3	FF
-	page4	0x80020	0 0	x80027FF	0x8	00(2K)		N			WKP5	
ash info	page5	0x80028		x8002FFF		00(2K)		N			Select	tall
	0.0006	0-90020	× •		00	00(3)/3	_	N1			_	
_	Data option	bytes										
	Date) 1	2	3	4	5	6	7	^	Clea	ar 🛛
	Data 07 (0:			FF	FF	FF	FF	FF	FF	-01		
	Data 815 (F FF	FF	FF	FF	FF	FF	FF			
	Data 1623			FF	FF	FF	FF	FF	FF		Load t	file
	Data 2431	(0x) F	F FF	FF	FF	FF	FF	FF	FF	~	Save to	file
:29:26 : AT-												
:29:27 : Part												
:29:27 : Tarç												
						_						

Figure 12. ICP pgrammer disable read protection



2 Artery ISP Programmer tool

Enable write protection: check "*Enable/Disable protection*"---Select "*Enable*"--- "*Write protection*"----Select the pages to be protected---Click "*OK*"---Click "*Next*"---"Yes".

Name						
AT GAIL G	Start address	End address	Size	R	w	^
Page0	0x08000000	0x080007FF	0x800 (2K)	N	N	
Page1	0x08000800	0x08000FFF	0x800 (2K)	N	N	
🗸 Page2	0x08001000	0x080017FF	0x800(2K)	N	N	
🗸 Page3	0x08001800	0x08001FFF	0x800(2K)	N	N	
🗸 Page4	0x08002000	0x080027FF	0x800(2K)	N	N	
🗸 Page5	0x08002800	0x08002FFF	0x800(2K)	N	N	
Page6	0x08003000	0x080037FF	0x800 (2K)	N	N	
Page7	0x08003800	0x08003FFF	0x800(2K)	N	N	
Page8	0x08004000	0x080047FF	0x800 (2K)	N	N	
Page9	0x08004800	0x08004FFF	0x800(2K)	N	N	
Page10	0x08005000	0x080057FF	0x800 (2K)	N	N	
Page11	0x08005800	0x08005FFF	0x800 (2K)	N	N	
Page12	0x08006000	0x080067FF	0x800 (2K)	N	N	
Page13	0x08006800	0x08006FFF	0x800(2K)	N	N	
Page14	0x08007000	0x080077FF	0x800(2K)	N	N	
Page15	0x08007800	0x08007FFF	0x800(2K)	N	N	
Page16	0x08008000	0x080087FF	0x800(2K)	N	N	
Page17	0x08008800	0x08008FFF	0x800(2K)	N	N	
Page18	0x08009000	0x080097FF	0x800(2K)	N	N	~
4 -					>	

Figure 13. ISP pgrammer enable read protection

Disable write protection: check "*Enable/Disable protection*"---select "*Disable*"--- "*Write protection*"---Click "*Next*"---" Yes". The write protection cannot be disabled by the erase operation.

雅特力 ۲I ○ Erase O Edit Option Bytes O Download to device 🔘 Disable sLib Start page DATA start pag End page File Name File Size Address Range(Ox) No. 1 LED, hex 4208 08000000-0800106F Confirm < > you sure to disable the write protection? r download uzer program Op Wr Addr step 0x 0000001 是(Y) 否(N) Enable Read Protection after Download Common read protection \sim ○ Upload from device 🔘 Firmware CRC Page fill FF ○ Flash CRC Start page page0-0x8000000 ∨ End page page0-0x8000000 ∨ ● Enable/Disable protection DISABLE ∨ Write Protection **~** Back Next Cancel Close

Figure 14. ISP programmer disable read protection



③ Artery ISP Multi-Port Programmer tool

Enable write protection: check "*Enable/Disable protection*"---select "*Enable*"---- "*Write protection*"----select the pages to be protected---click "*OK*"---click "*Begin*"---click "Yes".

Memory Ma					<u>が</u> 建1 ×	
viemory ivia	ipping				~	Status
ame	Start address	End address	Size	R	w ^	- Status
Page0	0x8000000	0x80007FF	0x800(2K)	-	-	
Parel	0x8000800	0x8000FFF	0x800(2K)	-	-	
Page2	0x8001000	0x80017FF	0x800 (2K)	-	-	
Page3	0x8001800	0x8001FFF	0x800(2K)	-	-	
Page4	0x8002000	0x80027FF	0x800(2K)	-	-	
Page5	0x8002800	0x8002FFF	0x800(2K)	-	-	
Page6	0x8003000	0x80037FF	0x800(2K)	-	-	
Page7	0x8003800	0x8003FFF	0x800(2K)	-	-	Begin(F2) Cancel(Esc)
Page8	0x8004000	0x80047FF	0x800(2K)	-	-	
Page9	0x8004800	0x8004FFF	0x800(2K)	-	-	
Page10	0x8005000	0x80057FF	0x800(2K)	-	-	ddress range(Ox) Add
Page11	0x8005800	0x8005FFF	0x800(2K)	_	-	ddress range(Ux) Add
Page12	0x8006000 0x8006800	0x80067FF 0x8006FFF	0x800(2K) 0x800(2K)	_		Delete
Page13 Page14	0x8006800	0x8006FFF	0x800(2K)	_		Derere
] Fage14 Page15	0x8007800	0x80077FF	0x800(2K)			
Page16	0x8008000	0x80087FF	0x800(2K)			
Page17	0x8008800	0x8008FFF	0x800(2K)	_	_	Open Edit
Page18	0x8009000	0x80097FF	0x800(2K)	_	_	
lingero	0x000000	0.0000111	ONOGO (LIA)		>	
						1
🗌 Select al	1		01	K	Cancel	O Download option bytes file
	⊖ Firmware CRC	🖲 Enabl	e/Disable protec	tion EN	ABLE	
	🔿 Disable sLib		() F1	ash CRC		
					Start page	• • • • • • • • • • • • • • • • • • •
	Disable password	0x			End page	

Figure 15. ISP Multi-Port programmer enable read protection

Disable write protection: check "*Enable/Disable protection*"---select "*Disable*"--- "*Write protection*"---Click "*Begin*"---Yes. The write protection cannot be disabled by the erase operation.

Figure 16. ISP Multi-Port programmer disable read protection

guage: English	V Port type: US		作 た ま fresh(F5 Refresh(F5) 🔽 Select all
o. VID	Device	Progress	Status	
1 AT32	AT32F415RCT7-7_25	6K		
Confirm		×		-
			Begin(F2)	Cancel(Esc)
Downly 🧿 👝				
	re you sure to disable th	he write protection?		
No.	re you sure to disable th	he write protection?	ze Address range(Ox)	bbA
		=	ze Address range(Ox)	Add
	re you sure to disable th 是(Y)		ze Address range(Ox)	
		=		
No.	是(Y)	ii: 百八四百百百百百百百百百百百百百百百百百百百百百百百百百百百百百百百百百百百	01	Delete
No.	是(Y)	=	01	Delete
No.	是(Y)	部 图(N) Settings SPIM Settings		Delete
No. potion bytes file:	是(Y) Dad Settings UART ○ Page erase	部 图(N) Settings SPIM Settings	Load AFP O Download	Delete
No. Potion bytes file: Operation Downle O Mass erase	是(Y) Dad Settings UART ○ Page erase	· · · · · · · · · · · · · · · · · · ·	Load APP O Download	Delete



Overview

At present, more and more microcontroller applications need to use complex algorithms and middleware solutions, therefore, how to protect the core algorithms and intellectual property codes (IP-Code) developed by software solutions providers has become a very important subject in the microcontroller applications.

In response to this important demand, AT32F415 series provide the security library function (sLib) to prevent important IP-Code from being modified or read by end-user programs to achieve protection.

• Application principle

Supports the use of password to protect the specified program area (security library) in the

main Flash. The IDH can store the core algorithm into this security library to implement protection, with the remaining blank area for end customers to conduct secondary development.

The security library is divided into instruction security library (sLib_Code) and data security

library (sLib_Data), and part or the whole security library can be selected to store instructions, but the whole security library is not supported to store data.

■ The program code in the sLib_Code can only be fetched by the MCU through the I-Code bus

(can only be executed), and cannot be read through the D-Code bus (including ISP/ICP debug mode and programs started from internal RAM). All the values read are 0xFF when accessing to sLib_Code by reading data.

- The data in the sLib_Data can only be read through D-Code, but not written.
- The program code and data in the security data cannot be erase until a correct password is

entered. If attempt to write to or erase the security library in the event of a wrong password, the WRPRTFLR bit of the FLASH_STS register will issue a warning by setting "1".

■ The program code and data in the security library would not be erased when the end user

performs the whole chip erase on the main Flash memory.

■ When the protection function of security library is activated, it can be disabled by writing the

previously set password in the sLib_PSW register. When the protection function of security library is disabled, the erase operation will be performed on the whole Flash memory (including the contents in the security library). Therefore, even if the password set by IDH is leaked, the program code will not be disclosed.

• How to operate security library

Please refer to AT32F415 sLib Application note for further details.

2.5 Set the system memory as an extended main memory

By default, the system memory is used as BOOT mode to store the original factory-cured startup code. However, new functions have been added in the AT32F415 products, where the system memory can also be selected as the extended area (AP mode) of the main memory to store user-defined codes.

Note: the system memory AP mode can only be set once and is irreversible. After setting, the original system memory BOOT mode cannot be restored.

During product development, Artery ICP Programmer is used to set the system memory as an extended main memory, with the following procedures:

- Connect J-Link or AT-Link simulator to AT-START-F415 board and power on.
- Turn on the ICP programmer, and select J-Link or AT-Link to connect.
- In menu bar: click "Device operation"---select "system memory AP mode".

₩ Artery ICP Programmer_V2.4.00		I	– 🗆 X
File J-Link settings AT-Link settings	Target	Language Help	
Disconnect Part Number: AT32F415F		s erase e main flash	
AT-Link FW Version AT-Link SN: 4CDB4151010	Erac	e sectors	進特力
SPIM FLASH_DA Type GD25Q127C 16M	Rea	ion Bytes d protection status	/PA12 pins) /PB11 pins)
Memory read settings	Syst	tem memory AP mode	
Address 0x 08000000 Read size 0x	Dov	vnLoad	Read
File info	Flas	h CRC	
No. File name	Deb	ug	x) Add Delete

Figure 17. System memory AP mode

• To prevent incorrect operation, you need to manually enter the encryption key 0xA35F6D24. Then, a success or failure message will appear in the "Flash info" window.

Figure 18. Flash information window

Flash info	File info	Flash CRC	File CRC verify	DownLoad
13:49:41 - 01	peration canceled			^
13:52:07 : En	abling AP mode			^
13:52:30 : En	able AP mode successfully!			
				~
urrent Time	: 2020/8/21 13:52:42	All Rights reserved by A	Artery Technology C	o.Ltd



In mass production, the Artery ICP Programmer is used to set the system memory as an extended main memory as follows:

- Connect AT-Link (the AT-Link EZ in the picture above does not support offline programming, so choose non-EZ version of AT-Link) simulator to the AT-START-F415 board and power on.
- Activate the ICP programmer, and select AT-Link to connect.
- In menu bar: AT-Link settings----click "Offline project configuration" to generate offline projects.
- The following are the steps that generate offline project:
- 1. Click "create a new project"
- 2. Enter the project name in the "Project name"
- 3. Select the MCU part number in the "Supported MCU"
- 4. Add .hex files
- 5. Select SWD in the "Download communication interface"
- 6. Check the "System memory AP mode" and enter the encryption key
- 7. Click the "Save project files or "Save the project to AT-Link"

Other options are set depending on the actual needs.

Figure 19. How to generate offline project

₩ AT-Link Setting	-
AT-Link settings AT-Link offline config settings	AT-Link offline download status
Offline project	✓ Delete Creat
Project name test1	Device AT32F415 V AT32F415RCT7-7 V
No. File name File siz 1 LED.hex 4208	e Address range(0x) Storage loca Add 08000000-0800106F Delete
<	>
Erase option Erase the pages of file size(Igno	ore blank pages) 🗸
Download times	Download interface SWD \checkmark
Encryption transmit Verify	Reset and run
Write option bytes	
Common read protection	✓ System memory AP mode Key:(0x) A35F6D24 (0xA35F6D24)
Software serial number(SN) SPIM settings	sLib settings
☐ Write software serial number	
Write address in flash: 0x 08010000	
Initial SN: 0x 00000001	
Increase step: 0x 00000001	
	Load parameters Save parameters
Open project Save project file	Save project to AT-Link Close



Figure 20. How to save offline project

AT-Link project file sett	ings	_		×
✓ Only used at the sp	ecified AT-Link			
AT-Link SN:	4CDB415101C0C1290)4971C02		
Only used once at	the same AT-Link			
	C	Ж	Cancel	

• In step 7, if the operation "Save the project to AT-Link" is successful, in the offline download status monitoring window, select the project name in the "Select offline download item", and click "Save and activate", you can start programming.

-Link settings AT-Link of	fline config settings	AT-Link offli	ne download status	
elect offline download it	em:		Download interface:	SWD
test1	✓ Save and activ	ate	ISP uart baud rate:	115200
			ISP boot mode:	AutoMatic
activated project:	test1			
otal downloads: Unlim				
otal downloads: Unlim Downloaded times: 0		Successful d	ownloads: 0	
		Successful d	ownloads: 0	
		Successful d	ownloads: 0	
		Successful d	ownloads: 0	
		Successful d		download
		Successful d	Start	
		Successful d	Start Start butto	n free download
		Successful d	Start Start butto	

Od Activista offlin

For demo on using the user program in the system memory, please refer to BSP under the location:

AT32F4xx_StdPeriph_Lib_V1.x.x\Utilities\AT32F415_SysMem_AP_Demo.

For ICP user manual, please refer to:

ICP_Programming_Tool_Vx.x.x\Document\UM_ICP_Programmer.

For AT-Link user manual, please refer to:

AT-Link_Vx.x.x\User Manual\AT-Link_User_Manual_SC.



3 How to distinguish AT and other ICs

① Read the Cortex-M series CPU ID to distinguish M0, M3 and M4 core.

i = *(uint32_t *)0xE000ED00;//read PID
if((i & 0xc241) == 0xc241)
 printf("This chip is Cortex-M4.\r\n");
else
 printf("This chip is Other Device.\r\n");

2 Read PID and UID to distinguish

```
/* Obtain the base address of AT32 MCU PID/UID*/
      #define DEVICE_ID_ADDR1 0x1FFFF7F3
       #define DEVICE_ID_ADDR2 0xE0042000
  /* To store ID */
           uint8_t ID[5] = \{0\};
  /* AT32 mcu type table */
  const uint64_t AT32_MCU_ID_TABLE[] =
                                                                                                                                                               /* 415 mcu */
{
           0x000000570030240, //AT32F415RCT7
                                                                                                                                                     256KB
                                                                                                                                                                                    LQFP64
           0x0000005700301C1, //AT32F415RBT7
                                                                                                                                                      128KB
                                                                                                                                                                                    LQFP64
    };
  /* Get PID/UID */
ID[0] = *(int*)DEVICE_ID_ADDR1;
ID[1] = *(int*)(DEVICE_ID_ADDR2+3);
ID[2] = *(int*)(DEVICE_ID_ADDR2+2);
ID[3] = *(int*)(DEVICE_ID_ADDR2+1);
ID[4] = *(int*)(DEVICE_ID_ADDR2+0);
/* 组合 PID/UID */
  AT_device_id =
       ((uint64\_t)ID[0]<<32)|((uint64\_t)ID[1]<<24)|((uint64\_t)ID[2]<<16)|((uint64\_t)ID[3]<<8)|((uint64\_t)ID[4]<<0)|(uint64\_t)ID[4]<<0)|(uint64\_t)ID[4]<<0)|(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<
       ;
/* Judge AT32 MCU */
for(i=0;i<sizeof(AT32_MCU_ID_TABLE)/sizeof(AT32_MCU_ID_TABLE[0]);i++)
{
       if(AT_device_id == AT32_MCU_ID_TABLE[i])
                 printf("This chip is AT32F4xx.\r\n");
               else
                     printf("This chip is Other Device.\r\n");
    }
```



4 FAQs during download and compiling

4.1 Error occurred during the downloading

4.1.1 Error: Flash Download failed – "Cortex-M4"

An error pops up during KEIL emulation or download:

Figure 22. Flash Download failed - "Cortex- 4"

Timing	μVision	17 (Am.)	23
while (
}			
L		Error: Flash Download failed - *	Cortex-M4"
日/**			
* @bri			
* @par			
* @ret			确定
L */			明定
void Tim			

Several possible reasons are as follows:

A. The read protection is enabled: you need to disable MCU read protection before download;

B. Select a wrong Flash file algorithm: you need to add a correct Flash file algorithm at Flash Down location.

C. Select wrong Boot0 and Boot1: Boot0 and Boot1 pin level should be set to Boot0=0 and Boot1=0 respectively so that MCU starts from the main Flash memory;

D. J-Link driver version is too old: it is recommended to use a version above 6.20C;

E. JTAG/SWD PIN is disabled, please refer to the section "4.1.3 AT32 resume download.



4.1.2 ISP serial interface gets stuck during download

When the ISP serial interface is used to download, it occasionally gets stuck, causing the PC not to release the serial port.

Solutions:

- Power supply is not stable;
- Use a better USB-to-serial interface tool, such as CH340 chip.

4.1.3 AT32 resume download

When using AT32F415, users may not be able to download the program after the following operations:

■ After the JTAG/SWD PIN is disabled, the program cannot be downloaded and the JTAG/SWD device cannot be found.

■ After entering Standby mode, the program cannot be downloaded and JTAG/SWD device cannot be found.

Here we provide the solutions in KEIL and IAR environment:

Solution 1: switch boot mode

Switch the boot mode to Boot[1:0]=01b to boot in the system memory, and use ISP tool to resume download.

Solution 2: ICP tool and AT-Link-EZ

AT-Link-EZ is specially designed for AT32, so ICP and AT-Link-EZ can use resume download.



5 Revision history

Date	Revision	Changes
2019.08.23	1.00	Initial release
2019.11.22	101	Added 2.5 section for system memory description and updated AT32 resume download.

Table 1. Document revision history

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