

AN0022

Getting started guide for AT32F415 series

# Introduction

This user manual provides information on how to use AT32F415 MCU for project development in a quickly manner.

Applicable products :

Part number	AT32F415xx



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# 1 Development environment

MCU resources download address:

■ Visit Artery website: <u>http://www.arterytek.com</u>

# 1.1 Set up AT32 development environment

### 1.1.1 Debug tools

At present, AT32F415 evaluation board is equipped with AT-Link/J-Link. The following picture is for AT-START-F415 (right) with AT-Link-EZ (left).



Figure 1. AT-Link

# 1.1.2 Programming tools and software

AT programming tools and software: AT\_Link, ICP/ISP. Third-party programming tools:

- Xuanwei: <u>https://xuanweikeji.taobao.com</u>
- Maxwiz: <u>www.maxwiz.com.cn</u>
- ZLG: <u>http://tools.zlg.cn/tools</u>
- Amo:http://www.amomcu.cn



### 1.1.3 AT32 KEIL and IAR development environment

For Keil compiling system, it is recommended to use Keil 4.74, 5.13 or above.
 When using AT-Link in Keil environment, select "CMSIS-DAP debugger "in "Debug".

	Figure	2. Keil D	)ebug	option			
Device   Target   Output   Listing   User	C/C++   A	sm Linker	Debug	Vtilities			
C Use Simulator with restrictions	Settings	€ <u>U</u> se: CMS	IS-DAP Del	bugger	•	Settings	
Limit Speed to Real-Time							l

In "Utilities", first untick the box "Use Debug Driver" and then tick it again.

 Device Target Output Listing User
 C/C++
 Asm
 Linker
 Debug
 Vtilities

 Configure Rash Menu Command
 Image: Compare the second second

② For IAR compiling system, it is recommended to use IAR 7.0, IAR 6.1 or above.
 When using AT-Link-EZ in IAR environment, select "CMSIS-DAP" in "Debugger".

Figure 4. Select CMSIS\_DAP in the IAR\_Debugger

C/C++ Compiler	Setup	Download	Images	Extra Options	Multicore	Plugins	
Output Converter Custom Build Build Actions	Driver CMSI	S DAP	~	<u> R</u> un to main			
Debugger Simulator	- S <u>e</u> tu	p macros					

③ BSP and PACK

For detailed operation on BSP and PACK, please refer to *BSP and Pack application note* available in the BSP folder.



# 2 Enhanced functions of AT32F415

# 2.1 Prefetch buffer

Thanks to the prefetch buffer, faster CPU execution is possible as the CPU fetches one word at a time with the next word readily available in the prefetch buffer. The prefetch controller decides whether to access the Flash memory according to the available space in the prefetch buffer. The Prefetch controller starts a read operation when there is at least one free space.

Different latency should be set for different SYSCLK by setting the bit2~0 in the FLASH\_ACR register.

LATENCY: Latency

These bits represent the ratio of the SYSCLK period to the Flash access time.

000: Zero wait state, if 0 <SYSCLK≤ 32 MHz

001: One wait state, if 32 <SYSCLK≤ 64 MHz

010: TWO wait states, if 64 <SYSCLK≤ 96 MHz

011: Three wait states, if 96 <SYSCLK≤ 128 MHz

100: Four wait states, if 128 <SYSCLK≤ 150 MHz

The following bond font is added in the system frequency configuration function of AT. For others, find the same location to do the same settings.

```
static void SetSysClockTo72M(void)
    ...
    ...
   if (HSEStatus == (uint32_t)0x01)
    #if defined (AT32F415xx)
    /* Enable Prefetch Buffer */
   FLASH->ACR /= FLASH_ACR_PRFTBE;
                                                              //Enable the prefetch buffer
   /* Flash 1 wait state */
  FLASH->ACR &= (uint32_t)((uint32_t)~FLASH_ACR_LATENCY);
FLASH->ACR |= (uint32_t)FLASH_ACR_LATENCY_2;
                                                           //Two wait states
#endif
...
•••
}
• • •
• • •
}
```

Note: The prefetch buffer must be kept on when using a prescaler different from 1 on the AHB clock.



# 2.2 PLL clock settings

There are two ways to configure the PLL of AT32F415 series: RCC\_CFG and RCC\_PLL. Use the RCC\_PLL configuration to configure more PLL clock frequency with the formula: PLL output clock= PLL reference input clock x PLL\_NS / (PLL\_MS x PLL\_FR).

PLL reference input clock: set to the same parameters as the actual HSE or HSI by PLL\_FREF PLL\_NS: 31~500 PLL\_MS: 1~15 PLL\_FR: set by PLL\_FR

The following bond font is added in the AT library system frequency configuration function, such as void SetSysClockTo150M (void), HSE=8 MHz.

*Note:* When using RCC\_PLL, 500MHz <= PLL reference input clock x PLL\_NS/PLL\_MS <= 1000MHz must be met.



# 2.3 PLL auto step-by-step frequency switching function

When the PLL embedded in the AT32F415 series is greater than 108 MHz, the auto step-by-step frequency switching function should be operated. The following bond font is added in the system frequency configuration function of AT library, such as void SetSysClockTo150M (void). For others, find the same location to do the same settings.

```
static void SetSysClockTo150M(void)
{
  if (HSEStatus == (uint32_t)0x01)
  {
...
    /* Wait till PLL is ready */
    while((RCC->CTRL & RCC_CTRL_PLLSTBL) == 0)
    }
#if defined (AT32F413xx) || defined (AT32F415xx)
    RCC_StepModeCmd(ENABLE);
                                       // enable the auto step-by-step frequency switching function
#endif
    /* Select PLL as system clock source */
    RCC->CFG &= (uint32_t)((uint32_t)~(RCC_CFG_SYSCLKSEL));
    RCC->CFG |= (uint32_t)RCC_CFG_SYSCLKSEL_PLL;
    /* Wait till PLL is used as system clock source */
    while ((RCC->CFG & (uint32_t)RCC_CFG_SYSCLKSTS) != RCC_CFG_SYSCLKSTS_PLL)
    {
#if defined (AT32F413xx) || defined (AT32F415xx)
    RCC_StepModeCmd(DISABLE);
                                     //disable the auto step-by-step frequency switching function
#endif
  }
}
```

Note: If the auto step-by-step frequency switching feature is enabled, it must be disabled after the clock is switched, and enable and disable must be paired.



# 2.4 Encryption (Read protection)

### 2.4.1 Read protection

Read protection, commonly referred to as "encryption", acts on the entire Flash storage area. Once the read protection is set in the Flash, the embedded Flash storage area can only be read through the normal execution of the program instead of JTAG or SWD. When the read protection is disabled using ISP/ICP tool, the chip will erase the Flash.

ISP/ICP tool can be used to enable/disable read protection as follows:

### ICP tool

Read protection: "Target"---"read protection"---"enable protection"

4	C Artery	/ ICP Program	nmer_V2	.4.00						_		×			
	File	J-Link settin	gs AT	-Link setti	ings	Target	Language	Help							
	Discourse	Part	Numbe	er: AT32	F415F	Ma	ss erase		1	2	Ξ.	$\sim$			
	AT-Lin	AT-	Link-EZ Link SN:	FW EFDC41	V Vers 15101(	Eras	se main flash se sectors		H H	: 4	- ` ;;	、 カ			
		s	РΙΜ	FLA	SH_DA	Opt	tion Bytes		_ [		• <u> </u>				
		Туре	GD25Q	127C	16N	Red	iu protection			En	able ci	ommon	read	protecti	ion
	Memo	ory read sett	nas			sLib	o status		_	Die	able a	uvance	ureau	i protect	lion
			-	Deed at	- 0	Sys	tem memory	AP mode	-						
	Addre	ss 0x 08000	000	Kead siz	ze Ux	Dov	wnLoad			F	Read				
	File in	fo				Flas	sh CRC								
	No. 1	File name Project_L0.	hex	1	File siz 9480	Deb	bug	10,0001000-0	0000017	57,08	Ad Dele	d ete			
L															

Figure 5. ICP enable read protection

Disable read protection: "Target"----"read protection"----"disable read protection"

Figure 6. ICP disable read protection

₩ Artery ICP Programmer_V2.4.00		– 🗆 X
File J-Link settings AT-Link settings	Target Language Help	
Disconnect AT-Link V Part Number: AT32F415F AT-Link-EZ FW Vers AT-Link SN: EFDC4151010	Mass erase Erase main flash Erase sectors Option Bytes	17FE7Y 催特力
SPIM FLASH_DA Type GD25Q127C 16M	Read protection	Enable common read protection
Memory read settings	System memory AP mode	Disable
Address 0x 08000000 Read size 0x	DownLoad	Read
File info	Flash CRC	
No.         File name         File siz           1         Project_L0.hex         9480	Debug	ol1757,08 Delete



Artery ISP Programmer tool

Read protection: "*enable/disable protection*"---"*enable---read protection*"---"*Next*"---" Yes", and the program is encrypted.

Figure 7. ISP enable read protection

Erase	● All ○ Selec	tion	🔿 Edit Opti	ion Byt
Downlo	ad to device		🔿 Disable s	5Lib
sLib	Status: DISABLE	Start page		
Remai	ning usage times: 256	DATA start pa	ge	
Passw	ord Ox	End page		
No.	File Name	<b>z</b> 11. c1	111 p (p)	
Erase Opt	optio rimize te us	u sure to enable the rea	Address Range(UX)	Delet wnload ram
Erase Opt Wri Addr App End	Optio optio inire ite us ess O obly Option Bytes able Read Protection aft	u sure to enable the rea	Address Range(Ux)	Delet: wnload ram 0000001
Erase Opt Wri Addr App End	Confirm optio imize ite us ess O oly Option Bytes hble Read Protection aft from device	u sure to enable the rea Yes	Address Range(Ux) Address Range	Delet wnload ram 0000001
Erase Opt Wri Addr End pload	optio inize ite us ess 0 obly Option Bytes able Read Protection aft from device re CRC Page fill	rile Size	Address Range(Ux) Address Range	Delet wnload ram 0000001

Disable read protection: "*enable/disable protection*"---"*disable-read protection*"---"*Next*"— "Yes", and then the Flash can be unencrypted.

	SP Programmer_V1.5.30		-	
	, <u>1715</u>	<mark>マ</mark> Y 雅	特力	
) Erase Downlo	<ul> <li>All</li> <li>Selecti</li> <li>ad to device</li> </ul>	on	○ Edit O ○ Disabl	ption Byte: e sLib
sLib Remai Passw	Status: DISABLE ning usage times: 256 ord Ox	Start page DATA start p End page	ago	
No.	File Name	File Size	Address Range(Ox)	Add
Ex	The flash memory	will be mass erased	and all contents will b	be a
Er A	The flash memory lost ,Are you sure	will be mass erased to disable the read	and all contents will b protection? Yes No	be in the second se
Er A	The flash memory lost ,Are you sure	will be mass erased to disable the read	and all contents will b protection? Yes No	
Er A Dupload	The flash memory lost Are you sure     balk Read Protection after     from device     rec EC     Page fill	vill be mass erased to disable the read	and all contents will b protection? Yes No	De la
Er A Upload Firmwan Flash	The flash memory lost Are you sure ble Read Protection after from device     re CBC Page fill     CEC Start page page0— (Disable protection IDIS)	vill be mass erased to disable the read p	and all contents will b protection? Yes No nd page page0—02600 testion V	

Figure 8. ISP disable read protection



Artery ISP Multi-Port Programmer

Read protection: "*enable/disable protection*"---"*enable-read protection*"---click on "Begin", and then the program is encrypted.

F	Figure 9	. ISP Multi-	Port P	rograr	nmer ena	able re	ad pi	ot ×
	, ioi maia ron	<u>ا</u> ۲۲.	<b>2</b> 7	雅	特力			~
, 1	e: English Port name COM10	Port type: UART Device AT32F403AVGT7_1024K	~ Progress		Refre: Status	sh(F5)	Select all	
								>
owi	nload files				Begin(F	2) Can	icel(Esc)	
No.	File name			File size	Address range(Ox	)	Add Delete	
tior	bytes file:					Open	Edit	
per	ation Downlo	ad Settings UART Set	tings SPIM	Settings				7
() M	ass erase	O Page erase		🔿 Download	APP 🔿 Down	load option by	ytes file	
) f	irmware CRC	● Enable/Disable	protection	ENABLE	Read Protection	n	<b>~</b>	
O D	isable sLib	0x	⊖ Flash C	RC Start page End page	2	× ×		
Proje	ct file setting							
Proje	ct info:			Open proje	ct Save projec	t Pro	ject mode	

Disable read protection: "*enable/disable protection*"--- "*disable-read protection*"—click on "*Begin*", then the Flash is unencrypted. The read protection cannot be disabled by the erase operation.

Artery ISP Multi-Port					
	Programmer_ V1.4.00				- 🗆 🗙
	ا۲۲ ا	ESA.	雅特	寺力	
anguage: English	✓ Port type: UART	$\sim$		Refresh(F5)	🖌 Select all
No. Port name	Device	Progress		Status	
1 COM10	AT32F403AVGT7_1024K				
<					>
				Begin(F2)	Cancel(Esc)
Download files					
No. File name		Fi	le size	Address range(Ox)	Add
					Delete
Option bytes file:				Op	en Edit
Option bytes file:				0p	en Edit
Option bytes file:	ad Settings UART Se	ttings SPIM Set	tings	0p	en Edit
Option bytes file:	ad Settings UART Se	ttings SPIM Set	tings		en Edit
Option bytes file: Operation Downlos Mass erase	ad Settings UART Se	ttings SPIM Set	tings Download A	Op PP O Download o	en Edit
Option bytes file: Operation Downlos Mazz eraze O Firmware CRC	ad Settings UART Se O Page erase I Enable/Disabl	ttings SPIM Set	tings Download A SABLE	PP Download of Read Protection	n Edit
Option bytes file: Operation Downlow Mass erase O Firmware CRC O Disable sLib	ad Settings UART Se O Page erase The Baable/Disabl	e protection DI	tings Download A SABLE	PP Download of Read Protection	en Edit
Option bytes file: Operation Downlos Mass erase O Firmware CBC O Disable sLib Disable password	ad Settings UART Se O Page erase Table/Disable	e protection DI O Flash CRC	tings Download A SABLE Start page End page	FF O Download of	en Edit
Operation Downlos Operation Downlos Office erase O Fireware CRC O Bisable sLib Disable passed Project file setting	ad Settings UART Se	e protection M O Flesh CRC	tings Download A SABLE Start page End page	FF O Dornload c	en Edit

### Figure 10. ISP Multi-Port Programmer disable read protection



## 2.4.2 Write protection

Write protection acts on the whole Flash storage area or some pages. Once the write protection is set in the Flash, the embedded Flash storage area cannot be written in any way. ISP/ICP tools can be used to enable/disable the write protection.

### ① Artery ICP Programmer tool

Enable write protection: click "*Target*"---"*Write protection option byte*"----Select the pages to be protected----"*Apply to device*"

File J-Link	settings AT-Li	ink settings	Targ	et Li	angua	ge ⊦	lelp				
Disconnect	Part Number:	AT32F415	RCT7-	7 F	lashSi	ze: 25	6KB		17	E	7Y
	AT LINK	Photo Annalia									
T-Link	Option Bytes										
	Read protectio	n option byt									
	RDP A5	Disable		~							
Memory re	User option by	tes									
Address 0x	USER FF	wdg_sw	nRs	T_STOP	⊠ n	RST_STC	BY				
File info	Write protectio	n option byt	95								
No. File	Name	Start addres	s End	addres	s Si	ze		w	^		WDD0 F0
	page0	0x8000000	0x8	0007FF	0:	(800(2K)		N			10 19
	page1	0x8000800	0x8	000FFF	0:	<800(2K)		N			WRP1 FF
	page2	0x8001000	0x8	0017FF	0:	<800(2K)		Y			WRP2 FF
	i page3	0x8001800	0x8	001FFF	0:	<800(2K)		Y V			WRP3 FF
	Dages	0x8002800	0x8	002766	0	(800(2K)		v			
Flash info		0-9002000	<u>~-</u>	002755	~			**	~		Select all
	Data option by	tes									
	Date	0	1	2	3	4	5	6	7	^	Clear
	Data 07 (0x)	FF	FF	FF	FF	FF	FF	FF	FF		
	Data 815 (0x	) FF	FF	FF	FF	FF	FF	FF	FF		
	Data 1623 (0	x) FF	FF	FF	FF	FF	FF	FF	FF		Load file
	Data 2431 (0	x) FF	FF	FF	FF	FF	FF	FF	FF		Save to file
10:29:26 : AT-											
10:29:27 · Part											
10:29:27 : Tarç											

## Figure 11. ICP pgrammer enable read protection

Disable write protection: click "*Target*"---"*Write protection option byte*"----Select the pages to be canceled ---"*Apply to device*". The write protection cannot be disabled by the erase operation.

le J-Li	nk settings 🛛 A	T-Link settir	ngs T	Farget	Lar	nguage	H H	elp					
isconnec	Part Numb	er: AT32F	415RC	T7-7	Fla	shSizo	: 256	КВ	<b>,</b>	17	ΓΞ	<b>Z</b> Y	r
. the la	57 Option Byt	es			-								
-LINK													
	Read prote	ction option	bytes										
	RDP AS	Disable			$\sim$								
	Urer optio	buter											
iemory r	• •••• • • •												
ddress 0	USER FF	WDG_S	sw 🖂	nRST_S	STOP	nRS n	T_STDE	8¥					
ilo info													
	write prote	ction option	bytes					_					
INO. FI	e Name	Start ad	ldress	End a	ddress	Size			w	^		WRP0	FF
	page0	0x80000	000	0x800	07FF	0x8	00(2K)		N	- 1		WRP1	FF
	page1	0x80008	300	0x800	OFFF	0x8	00(2K)		N				
	page2	0x80010	300	0x800	1666	0x8	DO(2K)		N			WKP2	
_	page3	0x80020	000	0x800	27FF	0x8	00(2K)		N			WRP3	FF
	page5	0x80028	300	0x800	2FFF	0x8	00(2K)		N				
ash info		000020	200	0000	2765	0.0	00(20)		NI .	~		Selec	rt all
_	Data option	n bytes											
	Date		0	1	2	3	4	5	6	7	^	Cle	ar
	Data 07	(0x)	FF F	FF	FF	FF	FF	FF	FF	FF			
	Data 81	i (0x)	FF F	F	FF	FF	FF	FF	FF	FF			
	Data 16	!3 (0x)	FF F	FF	FF	FF	FF	FF	FF	FF		Load	file
	Data 24	1 (0x)	FF F	F	FF	FF	FF	FF	FF	FF	~	Save t	o file
29:26 : AT	-												
20-27 · Da													
:29:27 : Pa	2												
				1									

### Figure 12. ICP pgrammer disable read protection



2 Artery ISP Programmer tool

Enable write protection: check "*Enable/Disable protection*"---Select "*Enable*"--- "*Write protection*"----Select the pages to be protected---Click "*OK*"---Click "*Next*"---"Yes".

Nume         Start address         End address         Size         R         W           Page0         0x0000000         0x0000077F         0x0000280         N         N           Page1         0x0000000         0x0000077F         0x0000280         N         N           Page2         0x0000000         0x0000017FF         0x0000280         N         N           Page3         0x000001000         0x000017FF         0x0000280         N         N           Page4         0x0000000         0x000017FF         0x0000280         N         N           Page4         0x000002000         0x000027FF         0x0000280         N         N           Page5         0x00002800         0x000027FF         0x0000280         N         N           Page5         0x00002800         0x000027FF         0x0000280         N         N           Page6         0x0000000         0x000027FF         0x0000280         N         N           Page7         0x0000000         0x000007FF         0x0000280         N         N           Page10         0x00000000         0x00007FF         0x0000280         N         N           Page12         0x00000000         0x00007FF	Memory Ma	pping					>
P sge0         0x60000000         0x000007FF         0x600(2E)         N         N           P sge1         0x60000000         0x00000FFF         0x600(2E)         N         N           P sge2         0x60000000         0x00000FFF         0x600(2E)         N         N           P sge3         0x60001800         0x00001FFF         0x600(2E)         N         N           P sge4         0x60001800         0x00001FFF         0x600(2E)         N         N           P sge4         0x6000000         0x00002FFF         0x600(2E)         N         N           P sge4         0x60002000         0x00002FFF         0x600(2E)         N         N           P sge5         0x60002000         0x00002FFF         0x600(2E)         N         N           P sge6         0x60004000         0x00002FFF         0x600(2E)         N         N           P sge6         0x60004000         0x00007FF         0x600(2E)         N         N           P sge6         0x60006000         0x00007FF         0x600(2E)         N         N           P sge10         0x60006000         0x00007FF         0x600(2E)         N         N           P sge14         0x60007000         0x00	Name	Start address	End address	Size	R	W	^
Paral         0x0000000         0x00000FFF         0x0000(2K)         N         N           Paral         0x00001000         0x000017FF         0x0000(2K)         N         N           Paral         0x00001000         0x000017FF         0x0000(2K)         N         N           Paral         0x00001000         0x000027FF         0x000(2K)         N         N           Paral         0x00000000         0x000027FF         0x000(2K)         N         N           Paral         0x0000000         0x000037FF         0x000(2K)         N         N           Paral         0x00003000         0x000037FF         0x000(2K)         N         N           Paral         0x00003000         0x000037FF         0x000(2K)         N         N           Paral         0x00003000         0x000037FF         0x000(2K)         N         N           Paral         0x00004000         0x00007FF         0x000(2K)         N         N           Paral         0x00005800         0x00005FFF         0x000(2K)         N         N           Paral         0x0000000         0x00007FF         0x000(2K)         N         N           Paral         0x00000000         0x00007FF	Page0	0x0800000	0x080007FF	0x800 (2K)	N	N	
P sec2         0x08001000         0x080017FF         0x800(2E)         N         N           P sec3         0x08001800         0x080017FF         0x800(2E)         N         N           P sec4         0x08001800         0x080017FF         0x800(2E)         N         N           P sec4         0x0800200         0x080027FF         0x800(2E)         N         N           P sec4         0x08002000         0x080027FF         0x800(2E)         N         N           P sec4         0x08002000         0x080037FF         0x800(2E)         N         N           P sec4         0x0800300         0x080037FF         0x800(2E)         N         N           P sec4         0x08000000         0x080047FF         0x800(2E)         N         N           P sec4         0x08000500         0x080047FF         0x800(2E)         N         N           P sec10         0x08000500         0x080067FF         0x800(2E)         N         N           P sec12         0x08000600         0x080067FF         0x800(2E)         N         N           P sec14         0x080007000         0x080077FF         0x800(2E)         N         N           P sec16         0x0800000	Page1	0x08000800	0x08000FFF	0x800(2K)	N	N	
P sgc3         0:00001800         0:00001FFF         0:8000(2E)         N         N           P sgc4         0:00000200         0:00002FFF         0:8000(2E)         N         N           P sgc5         0:00002000         0:000027FF         0:8000(2E)         N         N           P sgc5         0:00002000         0:000027FF         0:8000(2E)         N         N           P sgc6         0:00002000         0:000037FF         0:8000(2E)         N         N           P sgc7         0:0800020FF         0:8000(2E)         N         N           P sgc8         0:080004000         0:000047FF         0:8000(2E)         N         N           P sgc9         0:080004000         0:00007FF         0:8000(2E)         N         N           P sgc10         0:080005000         0:00005FFF         0:8000(2E)         N         N           P sgc11         0:080005000         0:00005FFF         0:8000(2E)         N         N           P sgc13         0:000005000         0:00000FFF         0:8000(2E)         N         N           P sgc14         0:00000700         0:00006FFF         0:8000(2E)         N         N           P sgc16         0:00000000         0:000006	✓ Page2	0x08001000	0x080017FF	0x800(2K)	N	N	
P see4         0x00002707         0x00002777         0x000027777         0x00002777         0x0000277	✓ Page3	0x08001800	0x08001FFF	0x800(2K)	N	N	
▼ Page5         0x80002200         0x80002277F         0x8000(2K)         N         N           Page5         0x80002200         0x8000277F         0x800(2K)         N         N           Page7         0x80003800         0x080037F         0x800(2K)         N         N           Page7         0x80004000         0x080037F         0x800(2K)         N         N           Page8         0x80004000         0x080047F         0x800(2K)         N         N           Page9         0x8000500         0x080047F         0x800(2K)         N         N           Page9         0x8000500         0x080057F         0x800(2K)         N         N           Page10         0x8000500         0x080057F         0x800(2K)         N         N           Page12         0x8000600         0x080057F         0x800(2K)         N         N           Page14         0x80007000         0x080077F         0x800(2K)         N         N           Page14         0x80007800         0x080077F         0x800(2K)         N         N           Page17         0x8000800         0x080087FF         0x800(2K)         N         N           Page17         0x8000800         0x080087FF	✓ Page4	0x08002000	0x080027FF	0x800(2K)	N	N	
Figs         One0003000         0x000377F         Ox0000(2E)         N         N           Page7         0x0003000         0x0000377F         0x000(2E)         N         N           Page8         0x00003000         0x0000377F         0x000(2E)         N         N           Page8         0x00004000         0x0000477F         0x000(2E)         N         N           Page9         0x00004000         0x0000477F         0x000(2E)         N         N           Page10         0x00005000         0x0000577F         0x000(2E)         N         N           Page11         0x00005000         0x0000577F         0x800(2E)         N         N           Page12         0x00006000         0x0000577F         0x800(2E)         N         N           Page13         0x0000000         0x0000577F         0x800(2E)         N         N           Page14         0x0000000         0x0000777F         0x800(2E)         N         N           Page16         0x0000000         0x000077F         0x800(2E)         N         N           Page16         0x00008000         0x0000877F         0x800(2E)         N         N           Page16         0x00008000         0x0000877F <td>🗹 Page5</td> <td>0x08002800</td> <td>0x08002FFF</td> <td>0x800(2K)</td> <td>N</td> <td>N</td> <td></td>	🗹 Page5	0x08002800	0x08002FFF	0x800(2K)	N	N	
Pser7         Ox60003800         00000387FF         Ox6000(2K)         N         N           Pser8         0x00004800         0x000047FF         0x000(2K)         N         N           Pser9         0x00004800         0x000047FF         0x000(2K)         N         N           Pser9         0x00004800         0x00007FF         0x000(2K)         N         N           Pser9         0x0000500         0x00007FF         0x000(2K)         N         N           Pser9         0x000000         0x00007FF         0x000(2K)         N         N           Pser9         0x0000000         0x00007FF         0x000(2K)         N         N           Pser9         0x000000         0x00007FF         0x000(2K)         N         N           Pser9         0x0000000         0x00007FF         0x000(2K)         N         N           Pser9         0x00007000         0x00007FF         0x000(2K)         N         N           Pser9         0x00007000         0x00007FF         0x000(2K)         N         N           Pser9         0x00007000         0x00007FF         0x000(2K)         N         N           Pser9         0x0000000         0x000007FF         0x0	Page6	0x08003000	0x080037FF	0x800(2K)	N	N	
Psgs8         0x08004000         0x0800477F         0x800(2K)         N         N           Psgs9         0x08004800         0x0800477F         0x800(2K)         N         N           Psgs9         0x08004800         0x0800477F         0x800(2K)         N         N           Psgs10         0x08005800         0x0800577F         0x800(2K)         N         N           Psgs11         0x08005800         0x0800577F         0x800(2K)         N         N           Psgs13         0x08006800         0x0800777F         0x800(2K)         N         N           Psgs13         0x0800700         0x0800777F         0x800(2K)         N         N           Psgs14         0x0800700         0x0800777F         0x800(2K)         N         N           Psgs16         0x0800800         0x080077FF         0x800(2K)         N         N           Psgs17         0x0800800         0x080067FF         0x800(2K)         N         N           Psgs18         0x0800800         0x080067FF         0x800(2K)         N         N           Psgs18         0x0800800         0x080067FF         0x800(2K)         N         N	Page7	0x08003800	0x08003FFF	0x800(2K)	N	N	
P scol         0x08004800         0x0800487F         0x800(2K)         N         N           P scol         0x0800500         0x080057F         0x800(2K)         N         N           P scol         0x08000500         0x080007FF         0x800(2K)         N         N           P scol         0x08000700         0x080077FF         0x800(2K)         N         N           P scol         0x08000700         0x080077FF         0x800(2K)         N         N           P scol         0x0800077FF         0x800(2K)         N         N         N           P scol         0x0800800         0x080087FF         0x800(2K)         N         N           P scol         0x0800800         0x080087FF         0x800(2K)         N         N           P scol         0x0800800         0x080087FF         0x800(2K)         N         N           P scol         0x0800800         0x080087FF	Page8	0x08004000	0x080047FF	0x800(2K)	N	N	
Page10         0x08005000         0x0800577F         0x800(2K)         N         N           Page11         0x08005800         0x0800577F         0x800(2K)         N         N           Page12         0x08006800         0x0800577F         0x800(2K)         N         N           Page12         0x08006800         0x0800577F         0x800(2K)         N         N           Page13         0x08006800         0x0800577F         0x800(2K)         N         N           Page14         0x08007000         0x080077FF         0x800(2K)         N         N           Page15         0x08007000         0x080077FF         0x800(2K)         N         N           Page16         0x08008000         0x080087FF         0x800(2K)         N         N           Page17         0x08008000         0x080087FF         0x800(2K)         N         N           Page18         0x08009000         0x080097FF         0x800(2K)         N         N           Page18         0x08009000         0x080097FF         0x800(2K)         N         N	Page9	0x08004800	0x08004FFF	0x800(2K)	N	N	
Psec11         Occ60005800         0x08005FFF         Dx800(2K)         N         N           Psec12         0x08006000         0x080067FF         0x800(2K)         N         N           Psec13         0x08006000         0x080067FF         0x800(2K)         N         N           Psec13         0x0800600         0x08007FF         0x800(2K)         N         N           Psec14         0x0800700         0x08007FFF         0x800(2K)         N         N           Psec15         0x08000         0x08007FFF         0x800(2K)         N         N           Psec16         0x0800800         0x080087FF         0x800(2K)         N         N           Psec16         0x0800800         0x080087FF         0x800(2K)         N         N           Psec17         0x0800800         0x08009FFF         0x800(2K)         N         N            0x08009000         0x08009FFF         0x800(2K)         N         N	Page10	0x08005000	0x080057FF	0x800(2K)	N	N	
Psec12         0x00006000         0x0000677F         0x0000677F         0x0000677F         0x0000677F         0x0000677F         0x00007000         0x000077FF         0x00007000         0x000077FF         0x00007000         0x000077FF         0x00007000         0x000077FF         0x00007200         0x000077FF         0x00007200         0x000077FF         0x00007200         0x000007FF         0x00007200         0x000007FF         0x000002000         0x0000007FF         0x000002000         0x0000007FF         0x000002000         0x0000007FF         0x000002000         0x000007FF         0x000002000         0x00000000000000000000000000000000000	Page11	0x08005800	0x08005FFF	0x800(2K)	N	N	
Page13         Ox60006800         Ox600687FF         Ox6000(2K)         N         N           Page14         Ox60007000         Ox600077FF         Ox600(2K)         N         N           Page15         Ox60007000         Ox600077FF         Ox600(2K)         N         N           Page15         Ox6000000         Ox600077FF         Ox600(2K)         N         N           Page16         Ox6000000         Ox600087FF         Ox600(2K)         N         N           Page17         Ox60008800         Ox600087FF         Ox600(2K)         N         N           Page18         Ox60000000         Ox600087FF         Ox600(2K)         N         N           Page18         Ox60000000         Ox600097FF         Ox600(2K)         N         N           C	Page12	0x08006000	0x080067FF	0x800(2K)	N	N	
Psge14         0x0000700         0x000777F         0x0007020         N         N           Psge15         0x0000700         0x000077FF         0x00000200         N         N           Psge16         0x0000000         0x00007FF         0x0000200         N         N           Psge16         0x0000000         0x000087FF         0x0000200         N         N           Psge10         0x0000000         0x000007FF         0x00002000         N         N           Psge10         0x00000000         0x000097FF         0x00002000         N         N             0x0000000         0x000097FF         0x000020000000000000000000000000000000	Page13	0x08006800	0x08006FFF	0x800(2K)	N	N	
Page15         0x80007800         0x800787FF         0x8000(2K)         N         N           Page16         0x80008000         0x080087FF         0x8000(2K)         N         N           Page16         0x8000800         0x080080FFF         0x8000(2K)         N         N           Page18         0x080009000         0x0800097FF         0x800(2K)         N         N           Page18         0x08009000         0x080097FF         0x800(2K)         N         N           <	Page14	0x08007000	0x080077FF	0x800(2K)	N	N	
Page16         0x00000000         0x0000677F         0x0000 (2K)         N         N           Page17         0x00008000         0x000067FF         0x0000 (2K)         N         N           Page18         0x0000000         0x000007FF         0x0000 (2K)         N         N           Page18         0x00000000         0x0000000FFF         0x0000(2K)         N         N              >         >         >         >	Page15	0x08007800	0x08007FFF	0x800(2K)	N	N	
Page17         0x08008800         0x08008FFF         0x800 (2K)         N         N           Page18         0x08009000         0x080097FF         0x800 (2K)         N         N         V           <	Page16	0x08008000	0x080087FF	0x800(2K)	N	N	
P age18         0x06009000         0x060097FF         0x800 (2K)         N         N         √           <	Page17	0x08008800	0x08008FFF	0x800(2K)	N	N	
< > >	Page18	0x08009000	0x080097FF	0x800(2K)	N	N	~
	<					)	•

Figure 13. ISP pgrammer enable read protection

Disable write protection: check "*Enable/Disable protection*"---select "*Disable*"--- "*Write protection*"---Click "*Next*"---" Yes". The write protection cannot be disabled by the erase operation.

#### 雅特力 ۲I ○ Erase O Edit Option Bytes O Download to device 🔘 Disable sLib Start page DATA start pag End page File Name File Size Address Range(Ox) No. 1 LED, hex 4208 08000000-0800106F Confirm < > you sure to disable the write protection? r download uzer program Op Wr Addr step 0x 0000001 是(Y) 否(N) ..... Enable Read Protection after Download Common read protection $\sim$ ○ Upload from device ..... 🔘 Firmware CRC Page fill FF ○ Flash CRC Start page page0-0x8000000 ∨ End page page0-0x8000000 ∨ ● Enable/Disable protection DISABLE ∨ Write Protection **~** Back Next Cancel Close

### Figure 14. ISP programmer disable read protection



③ Artery ISP Multi-Port Programmer tool

Enable write protection: check "*Enable/Disable protection*"---select "*Enable*"---- "*Write protection*"----select the pages to be protected---click "*OK*"---click "*Begin*"---click "Yes".

Memory Ma	pping				;	X Refresh(F5) Select all
ame	Start address	End address	Size	R	w ^	A Status
Page0	0x8000000	0x80007FF	0x800(2K)	_		
Pagel	0x8000800	0x8000FFF	0x800(2K)	-	-	
Page2	0x8001000	0x80017FF	0x800(2K)	-		
Page3	0x8001800	0x8001FFF	0x800(2K)	-	-	
Page4	0x8002000	0x80027FF	0x800(2K)	-	-	
Page5	0x8002800	0x8002FFF	0x800(2K)	-	-	
l'age6	0x8003000	0x80037FF	0x800(2K)	-	-	
] Page7	0x8003800	0x8003FFF	0x800(2K)	-	-	Begin(F2) Cancel(Esc)
Page8	0x8004000	0x80047FF	0x800(2K)	-	-	begin(i'L)
Page9	0x8004800	0x8004FFF	0x800(2K)	-	-	
Page10	0x8005000	0x80057FF	0x800(2K)	-	-	
Page11	0x8005800	0x8005FFF	0x800(2K)	-	-	ddress range(Ox) Add
Page12	0x8006000	0x80067FF	0x800(2K)	-	-	
Page13	0x8006800	0x8006FFF	0x800(2K)	-	-	Delete
Page14	0x8007000	0x80077FF	0x800(2K)	-	-	
] Page15	0x8007800	0x8007FFF	0x800(2K)	-	-	
] Page16	0x8008000	0x80087FF	0x800(2K)	-	-	Onen Edit
Page17	0x8008800	0x8008FFF	0x800(2K)	-	-	
Page18	0x8009000	0x80097FF	0x800(2K)	-	— v	/
					>	
🗌 Select al	1		01	κ	Cancel	O Download option bytes file
	○ Firmware CRC	🖲 Enabl	e/Disable protec	tion EN	ABLE	✓ Write Protection ✓
	🔿 Disable sLib		() <b>F</b> ]	ash CBC 🗆		
	O DIMOIT MID		O FI	ash UKC	Start pag	e v
					Start pag	se v

Figure 15. ISP Multi-Port programmer enable read protection

Disable write protection: check "*Enable/Disable protection*"---select "*Disable*"--- "*Write protection*"---Click "*Begin*"---Yes. The write protection cannot be disabled by the erase operation.

Figure 16. ISP Multi-Port programmer disable read protection

mage English	Part time:		Befresh(F	5) Select all
o. VID	Device	Progress	Status	
1 AT32	AT32F415RCT7-7_2	256K		
Confirm		×	_	
			Begin(F2)	Cancel(Esc)
Downly 🛃	Are you sure to disable	the write protection?		
No.	Are you sure to disable	the write protection?	ize Address range(Ox)	Add
No.	Are you sure to disable	the write protection?	ize Address range(Ox)	Add
No.	Are you sure to disable 是(Y)	the write protection?	ize Address range(Ox)	Add
No.	Are you sure to disable 是(Y)	the write protection?	ize Address range(0x)	Add Delete Dpen Edit
No.	Are you sure to disable 是(Y)	the write protection?	ize Address range(Ox)	Add Delete Open Edit
Downline     Image: Comparison of the second s	Are you sure to disable 문(Y) load Settings UAR	the write protection?	ize Address range(Ox)	Add Delete Dpen Edit
Downli     ?       No.     .       Dotion bytes file:       Operation     Down       O Mass erase	Are you sure to disable हि(۲) load Settings UAR Page eras	the write protection? ) 플(N) (T Settings SPIM Setting	ize Address range(Ox)	Add Delete Open Edit
No. No. No. No. No. No. No. No.	Are you sure to disable हिएग load Settings UAR Page er as () Enable/Di	the write protection?	ize Address range(Ox) s aload AFP Download E V Write Protection	Add Delete Dpen Edit
No. No. No. Deperation Down Mass erase Firmware CRC O Disable sLib	Ioad Settings UAR Page eras Enable/Di	the write protection?          If Settings       SPIM Setting         Settings       SPIM Setting         sable protection       DISABL         Plash CRC       Flash CRC	ize Address range(Ox) s aload APP O Download E V Write Protection	Add Delete Dpen Edit



### Overview

At present, more and more microcontroller applications need to use complex algorithms and middleware solutions, therefore, how to protect the core algorithms and intellectual property codes (IP-Code) developed by software solutions providers has become a very important subject in the microcontroller applications.

In response to this important demand, AT32F415 series provide the security library function (sLib) to prevent important IP-Code from being modified or read by end-user programs to achieve protection.

# • Application principle

Supports the use of password to protect the specified program area (security library) in the

main Flash. The IDH can store the core algorithm into this security library to implement protection, with the remaining blank area for end customers to conduct secondary development.

The security library is divided into instruction security library (sLib\_Code) and data security

library (sLib\_Data), and part or the whole security library can be selected to store instructions, but the whole security library is not supported to store data.

■ The program code in the sLib\_Code can only be fetched by the MCU through the I-Code bus

(can only be executed), and cannot be read through the D-Code bus (including ISP/ICP debug mode and programs started from internal RAM). All the values read are 0xFF when accessing to sLib\_Code by reading data.

- The data in the sLib\_Data can only be read through D-Code, but not written.
- The program code and data in the security data cannot be erase until a correct password is

entered. If attempt to write to or erase the security library in the event of a wrong password, the WRPRTFLR bit of the FLASH\_STS register will issue a warning by setting "1".

■ The program code and data in the security library would not be erased when the end user

performs the whole chip erase on the main Flash memory.

■ When the protection function of security library is activated, it can be disabled by writing the

previously set password in the sLib\_PSW register. When the protection function of security library is disabled, the erase operation will be performed on the whole Flash memory (including the contents in the security library). Therefore, even if the password set by IDH is leaked, the program code will not be disclosed.

### • How to operate security library

Please refer to AT32F415 sLib Application note for further details.

# 2.5 Set the system memory as an extended main memory

By default, the system memory is used as BOOT mode to store the original factory-cured startup code. However, new functions have been added in the AT32F415 products, where the system memory can also be selected as the extended area (AP mode) of the main memory to store user-defined codes.

Note: the system memory AP mode can only be set once and is irreversible. After setting, the original system memory BOOT mode cannot be restored.

During product development, Artery ICP Programmer is used to set the system memory as an extended main memory, with the following procedures:

- Connect J-Link or AT-Link simulator to AT-START-F415 board and power on.
- Turn on the ICP programmer, and select J-Link or AT-Link to connect.
- In menu bar: click "Device operation"---select "system memory AP mode".

₩ Artery ICP Programmer_V2.4.00		I	– 🗆 X
File J-Link settings AT-Link settings	Target	Language Help	
Disconnect Part Number: AT32F415F	Mas	is erase	12L=2A
AT-Link FW Version AT-Link SN: 4CDB4151010	Eras	e sectors	作
SPIM FLASH_DA	Opt Read sLib	ion Bytes d protection status	(PA12 pins) (PB11 pins)
Memory read settings	Syst	tem memory AP mode	
Address 0x 08000000 Read size 0x	Dov	vnLoad	Read
File info	Flas	h CRC	
No. File name	Deb	ug	x) Add Delete

Figure 17. System memory AP mode

• To prevent incorrect operation, you need to manually enter the encryption key 0xA35F6D24. Then, a success or failure message will appear in the "Flash info" window.

Figure 18. Flash information window

Flash info File info	Flash CRC File CRC verify Dow	InLoad
13:49:41 : Operation canceled		^
13:52:07 Enabling AP mode 13:52:30 Enable AP mode successfully!		
		~
Current Time: 2020/8/21 13:52:42	All Rights reserved by Artery Technology Co.Ltd	



In mass production, the Artery ICP Programmer is used to set the system memory as an extended main memory as follows:

- Connect AT-Link (the AT-Link EZ in the picture above does not support offline programming, so choose non-EZ version of AT-Link) simulator to the AT-START-F415 board and power on.
- Activate the ICP programmer, and select AT-Link to connect.
- In menu bar: AT-Link settings----click "Offline project configuration" to generate offline projects.
- The following are the steps that generate offline project:
- 1. Click "create a new project"
- 2. Enter the project name in the "Project name"
- 3. Select the MCU part number in the "Supported MCU"
- 4. Add .hex files
- 5. Select SWD in the "Download communication interface"
- 6. Check the "System memory AP mode" and enter the encryption key
- 7. Click the "Save project files or "Save the project to AT-Link"

Other options are set depending on the actual needs.

### Figure 19. How to generate offline project

₩ AT-Link Setting	-
AT-Link settings AT-Link offline config settings AT	-Link offline download status
Offline project	✓ Delete Creat
Project name test1	Device AT32F415 V AT32F415RCT7-7 V
No. File name File size 1 LED.hex 4208	Address range(0x) Storage loca Add 08000000-0800106F Delete
<	>
Erase option Erase the pages of file size(Ignor	e blank pages) 🗸
Download times	Download interface SWD $\checkmark$
Encryption transmit     Verify	Reset and run
Write option bytes	
□ Enable RDP after download Common read protection ∨	System memory AP mode Key:(0x) A35F6D24 (0xA35F6D24)
Software serial number(SN) SPIM settings	sLib settings
☐ Write software serial number	
Write address in flash: 0x 08010000	
Initial SN: 0x 0000001	
Increase step: 0x 00000001	
	Load parameters Save parameters
Open project Save project file	Save project to AT-Link Close



### Figure 20. How to save offline project

AT-Link project file sett	ings	_		×
✓ Only used at the sp	ecified AT-Link			
AT-Link SN:	4CDB415101C0C1290	)4971C02		
Only used once at	the same AT-Link			
	C	Ж	Cancel	

• In step 7, if the operation "Save the project to AT-Link" is successful, in the offline download status monitoring window, select the project name in the "Select offline download item", and click "Save and activate", you can start programming.

Line secange /// Line entite coming secange	nk offline download status
elect offline download item:	Download interface: SWD
test1 v Save and activate	ISP uart baud rate: 115200
	ISP boot mode: AutoMatic
ctivated project: test1	
otal downloads: Unlimited	
Downloaded times: 0 Succes	sful downloads: 0
Downloaded times: 0 Succes	sful downloads: 0
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For demo on using the user program in the system memory, please refer to BSP under the location:

AT32F4xx\_StdPeriph\_Lib\_V1.x.x\Utilities\AT32F415\_SysMem\_AP\_Demo.

For ICP user manual, please refer to:

ICP\_Programming\_Tool\_Vx.x.x\Document\UM\_ICP\_Programmer.

For AT-Link user manual, please refer to:

AT-Link\_Vx.x.x\User Manual\AT-Link\_User\_Manual\_SC.



# 3 How to distinguish AT and other ICs

① Read the Cortex-M series CPU ID to distinguish M0, M3 and M4 core.

i = \*(uint32\_t \*)0xE000ED00;//read PID
if((i & 0xc241) == 0xc241)
 printf("This chip is Cortex-M4.\r\n");
else
 printf("This chip is Other Device.\r\n");

### 2 Read PID and UID to distinguish

```
/* Obtain the base address of AT32 MCU PID/UID*/
      #define DEVICE_ID_ADDR1 0x1FFFF7F3
       #define DEVICE_ID_ADDR2 0xE0042000
  /* To store ID */
           uint8_t ID[5] = \{0\};
  /* AT32 mcu type table */
  const uint64_t AT32_MCU_ID_TABLE[] =
                                                                                                                                                               /* 415 mcu */
{
           0x000000570030240, //AT32F415RCT7
                                                                                                                                                     256KB
                                                                                                                                                                                    LQFP64
           0x0000005700301C1, //AT32F415RBT7
                                                                                                                                                      128KB
                                                                                                                                                                                    LQFP64
    };
  /* Get PID/UID */
ID[0] = *(int*)DEVICE_ID_ADDR1;
ID[1] = *(int*)(DEVICE_ID_ADDR2+3);
ID[2] = *(int*)(DEVICE_ID_ADDR2+2);
ID[3] = *(int*)(DEVICE_ID_ADDR2+1);
ID[4] = *(int*)(DEVICE_ID_ADDR2+0);
/* 组合 PID/UID */
  AT_device_id =
       ((uint64\_t)ID[0]<<32)|((uint64\_t)ID[1]<<24)|((uint64\_t)ID[2]<<16)|((uint64\_t)ID[3]<<8)|((uint64\_t)ID[4]<<0)|(uint64\_t)ID[4]<<0)|(uint64\_t)ID[4]<<0)|(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<<0||(uint64\_t)ID[4]<
       ;
/* Judge AT32 MCU */
for(i=0;i<sizeof(AT32_MCU_ID_TABLE)/sizeof(AT32_MCU_ID_TABLE[0]);i++)
{
       if(AT_device_id == AT32_MCU_ID_TABLE[i])
                 printf("This chip is AT32F4xx.\r\n");
               else
                     printf("This chip is Other Device.\r\n");
    }
```



# 4 FAQs during download and compiling

# 4.1 Error occurred during the downloading

## 4.1.1 Error: Flash Download failed – "Cortex-M4"

An error pops up during KEIL emulation or download:

# Figure 22. Flash Download failed - "Cortex- 4"

Timing	Vision	17 (Am.)	23
while (			
}			
L		Error: Flash Download failed - *	Cortex-M4"
戶/**			
* @bri			
* @par			
* @ret			THAT
L */			明定
woid Tim			

Several possible reasons are as follows:

A. The read protection is enabled: you need to disable MCU read protection before download;

B. Select a wrong Flash file algorithm: you need to add a correct Flash file algorithm at Flash Down location.

C. Select wrong Boot0 and Boot1: Boot0 and Boot1 pin level should be set to Boot0=0 and Boot1=0 respectively so that MCU starts from the main Flash memory;

D. J-Link driver version is too old: it is recommended to use a version above 6.20C;

E. JTAG/SWD PIN is disabled, please refer to the section "4.1.3 AT32 resume download.



## 4.1.2 ISP serial interface gets stuck during download

When the ISP serial interface is used to download, it occasionally gets stuck, causing the PC not to release the serial port.

Solutions:

- Power supply is not stable;
- Use a better USB-to-serial interface tool, such as CH340 chip.

### 4.1.3 AT32 resume download

When using AT32F415, users may not be able to download the program after the following operations:

■ After the JTAG/SWD PIN is disabled, the program cannot be downloaded and the JTAG/SWD device cannot be found.

■ After entering Standby mode, the program cannot be downloaded and JTAG/SWD device cannot be found.

Here we provide the solutions in KEIL and IAR environment:

Solution 1: switch boot mode

Switch the boot mode to Boot[1:0]=01b to boot in the system memory, and use ISP tool to resume download.

Solution 2: ICP tool and AT-Link-EZ

AT-Link-EZ is specially designed for AT32, so ICP and AT-Link-EZ can use resume download.



# 5 Revision history

Date	Revision	Changes
2019.08.23	1.00	Initial release
2010 11 22	1 01	Added 2.5 section for system memory description and updated AT32 resume
2019.11.22	101	download.

### Table 1. Document revision history

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