1. Features

- **Low-voltage and Standard-voltage Operation**
  - **1.8 (V_{CC} = 1.8V to 5.5V)**
- **Internally Organized 2048 x 8 (16K)**
- **Two-wire Serial Interface**
- **Schmitt Trigger, Filtered Inputs for Noise Suppression**
- **Bidirectional Data Transfer Protocol**
- **1 MHz (5V, 2.5V), 400 kHz (1.8V) Compatibility**
- **Write Protect Pin for Hardware Data Protection**
- **16-byte Page (16K) Write Modes**
- **Partial Page Writes Allowed**
- **Self-timed Write Cycle (5 ms max)**
- **High-reliability**
  - **Endurance: 1 Million Write Cycles**
  - **Data Retention: 100 Years**
- **8-lead PDIP, 8-lead JEDEC SOIC, 8-lead Ultra-Thin Mini-MAP (MLP 2x3), 5-lead SOT23, 8-lead Ultra Lead Frame Land Grid Array (ULA), 8-lead TSSOP and 8-ball dBGA2 Packages**
- **Lead-free/Halogen-free**
- **Die Sales: Wafer Form, Tape and Reel, and Bumped Wafers**

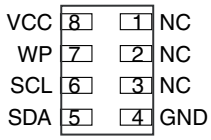
2. Description

The AT24C16B provides 16384 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 2048 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The AT24C16B is available in space-saving 8-lead PDIP, 8-lead JEDEC SOIC, 8-lead Ultra Thin Mini-MAP (MLP 2x3), 5-lead SOT23, 8-lead Ultra Lead Frame Land Grid Array (ULA), 8-lead TSSOP, and 8-ball dBGA2 packages and is accessed via a Two-wire serial interface. In addition, the AT24C16B is available in 1.8V (1.8V to 5.5V) version.

Table 2-1. Pin Configuration

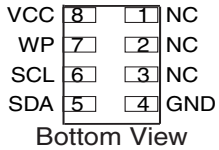
Pin Name	Function
NC	No Connect
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
GND	Ground
VCC	Power Supply

8-lead Ultra Lead Frame Land Grid Array (ULA)



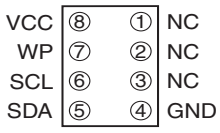
Bottom View

8-lead Ultra Thin Mini-MAP (MLP 2x3)



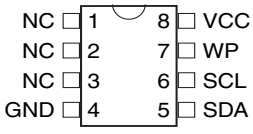
Bottom View

8-ball dBGA2

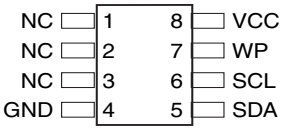


Bottom View

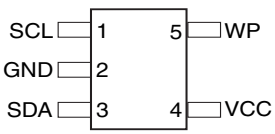
8-lead TSSOP



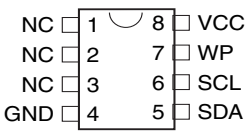
8-lead SOIC



5-lead SOT23



8-lead PDIP



Two-wire Serial EEPROM

16K (2048 x 8)

AT24C16B

Not Recommeded for New Design. Replaced by AT24C16C.

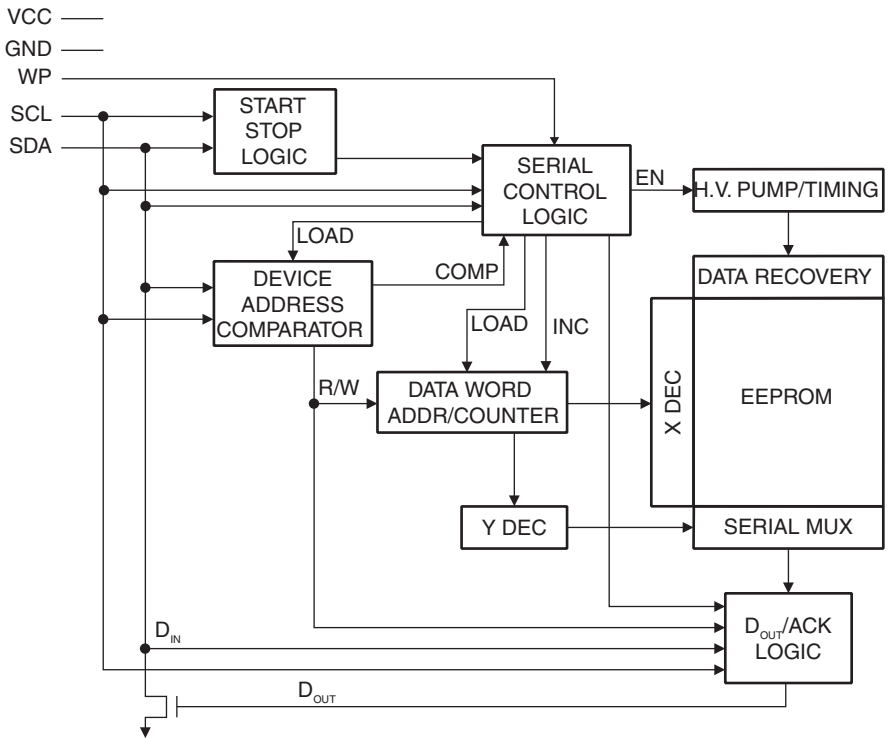
5175E–SEEPR–3/09

Absolute Maximum Ratings

Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on Any Pin with Respect to Ground	–1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 2-1. Block Diagram



3. Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

DEVICE/PAGE ADDRESSES: The AT24C16B does not use the device address pins, which limits the number of devices on a single bus to one.

WRITE PROTECT (WP): The AT24C16B has a write protect pin that provides hardware data protection. The write protect pin allows normal read/write operations when connected to ground (GND). When the write protect pin is connected to V_{CC}, the write protection feature is enabled and operates as shown in Table 3-1.

Table 3-1. Write Protect

WP Pin Status	Part of the Array Protected
	24C16B
At V_{CC}	Full (16K) Array
At GND	Normal Read/Write Operations

4. Memory Organization

AT24C16B, 16K SERIAL EEPROM: Internally organized with 128 pages of 16 bytes each, the 16K requires an 11-bit data word address for random word addressing.

Table 4-1. Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +1.8V

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

Table 4-2. DC Characteristics

Applicable over recommended operating range from: T_{AI} = –40°C to +85°C, V_{CC} = +1.8V to +5.5V (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1}	Supply Voltage			1.8		5.5	V
I_{CC1}	Supply Current	V_{CC} = 5.0V	READ at 400 kHz		1.0	2.0	mA
I_{CC2}	Supply Current	V_{CC} = 5.0V	WRITE at 400 kHz		2.0	3.0	mA
I_{SB1}	Standby Current (1.8V option)	V_{CC} = 1.8V	V_{IN} = V_{CC} or V_{SS}			1.0	µA
		V_{CC} = 5.5V				6.0	
I_{LI}	Input Leakage Current V_{CC} = 5.0V	V_{IN} = V_{CC} or V_{SS}			0.10	3.0	µA
I_{LO}	Output Leakage Current V_{CC} = 5.0V	V_{OUT} = V_{CC} or V_{SS}			0.05	3.0	µA
V_{IL}	Input Low Level[1]			–0.6		V_{CC} x 0.3	V
V_{IH}	Input High Level[1]			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL1}	Output Low Level	V_{CC} = 1.8V	I_{OL} = 0.15 mA			0.2	V
V_{OL2}	Output Low Level	V_{CC} = 3.0V	I_{OL} = 2.1 mA			0.4	V

Notes: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

Table 4-3. AC Characteristics (Industrial Temperature)

Applicable over recommended operating range from T_{AI} = –40°C to +85°C, V_{CC} = +1.8V to +5.5V, CL = 100 pF (unless otherwise noted). Test conditions are listed in Note 2.

Symbol	Parameter	1.8-volt		2.5, 5.0-volt		Units
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		400		1000	kHz
t_{LOW}	Clock Pulse Width Low	1.3		0.4		µs
t_{HIGH}	Clock Pulse Width High	0.6		0.4		µs
t_{AA}	Clock Low to Data Out Valid	0.05	0.9	0.05	0.55	µs
t_{BUF}	Time the bus must be free before a new transmission can start(1)	1.3		0.5		µs
$t_{HD.STA}$	Start Hold Time	0.6		0.25		µs
$t_{SU.STA}$	Start Set-up Time	0.6		0.25		µs
$t_{HD.DAT}$	Data In Hold Time	0		0		µs
$t_{SU.DAT}$	Data In Set-up Time	100		100		ns
t_R	Inputs Rise Time(1)		0.3		0.3	µs
t_F	Inputs Fall Time(1)		300		100	ns
$t_{SU.STO}$	Stop Set-up Time	0.6		0.25		µs
t_{DH}	Data Out Hold Time	50		50		ns
t_{WR}	Write Cycle Time		5		5	ms
Endurance(1)	25°C, Page Mode, 3.3V	1,000,000				Write Cycles

Notes: 1. This parameter is characterized and is not 100% tested.

2. AC measurement conditions:
   R_L (connects to V_{CC}): 1.3 kΩ (2.5V, 5.0V), 10 kΩ (1.8V)
   Input pulse voltages: 0.3 V_{CC} to 0.7 V_{CC}
   Input rise and fall times: ≤ 50 ns
   Input and output timing reference voltages: 0.5 V_{CC}

5. Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see Figure 7-2 on page 8). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see Figure 7-3 on page 8).

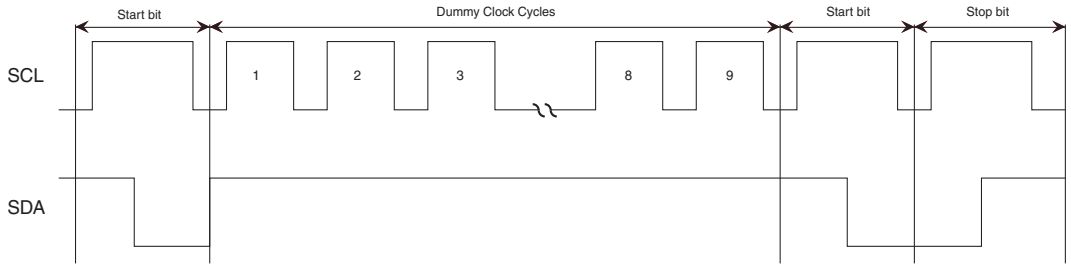
STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (see Figure 7-3 on page 8).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

STANDBY MODE: The AT24C16B features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations.

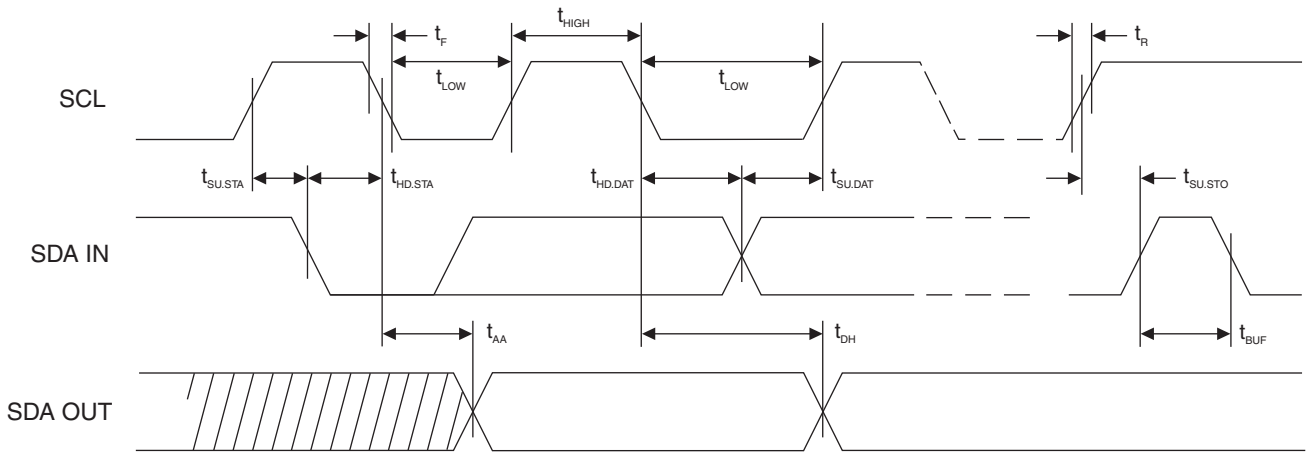
2-WIRE SOFTWARE RESET: After an interruption in protocol, power loss or system reset, any 2-wire part can be protocol reset by following these steps:

1. Create a start bit condition.
2. Clock 9 cycles.
3. Create another start bit followed by stop bit condition as shown below.



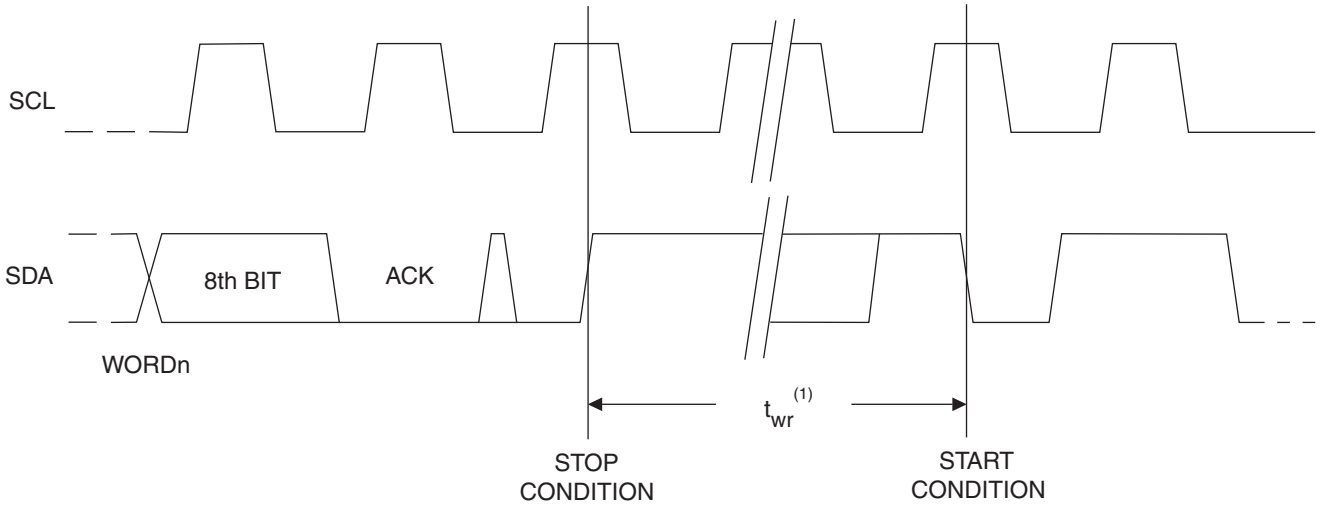
6. Bus Timing

Figure 6-1. SCL: Serial Clock, SDA: Serial Data I/O®



7. Write Cycle Timing

Figure 7-1. SCL: Serial Clock, SDA: Serial Data I/O



Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

Figure 7-2. Data Validity

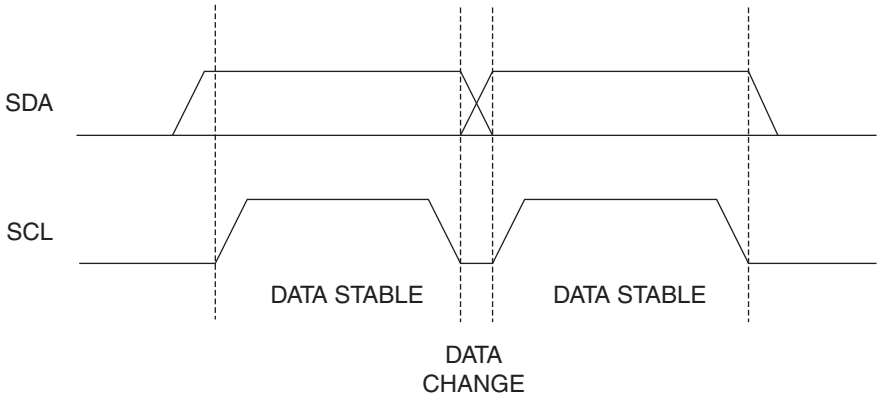


Figure 7-3. Start and Stop Definition

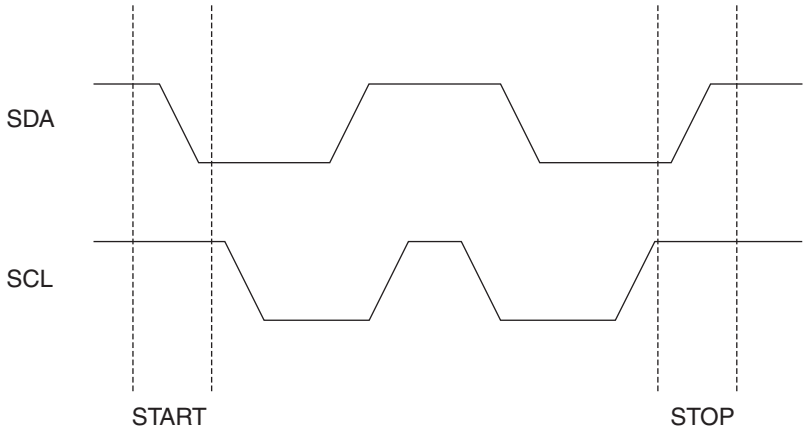
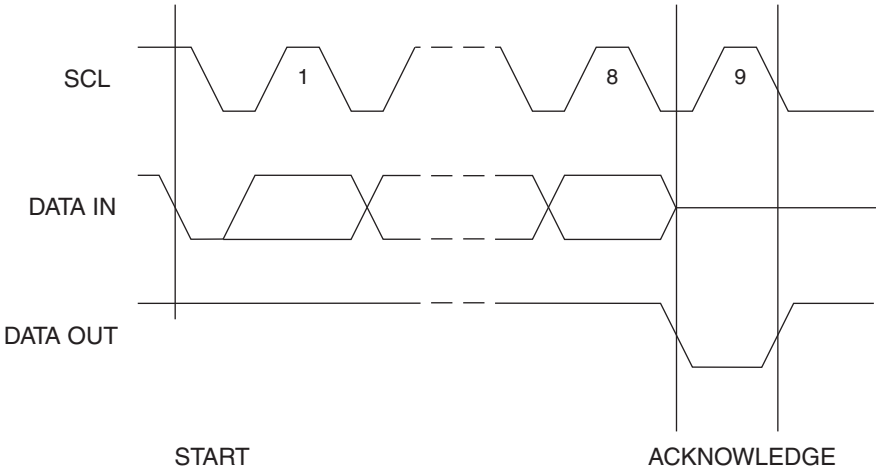


Figure 7-4. Output Acknowledge



8. Device Addressing

The 16K EEPROM device requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (refer to Figure 10-1).

The device address word consists of a mandatory one, zero sequence for the first four most significant bits as shown. This is common to all the EEPROM devices.

The next 3 bits used for memory page addressing and are the most significant bits of the data word address which follows.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the chip will return to a standby state.

9. Write Operations

BYTE WRITE: A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see Figure 10-2 on page 11).

PAGE WRITE: The 16K EEPROM is capable of an 16-byte page write.

A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to fifteen data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see Figure 10-3 on page 11).

The data word address lower three bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than sixteen data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue.

10. Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (see Figure 10-4 on page 11).

RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (see Figure 10-5 on page 12).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (see Figure 10-6 on page 12).

Figure 10-1. Device Address

Figure 10-2. Byte Write

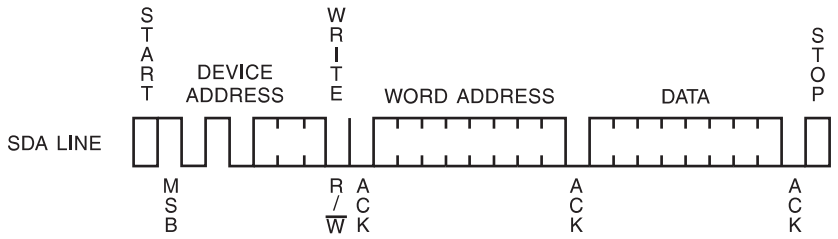


Figure 10-3. Page Write

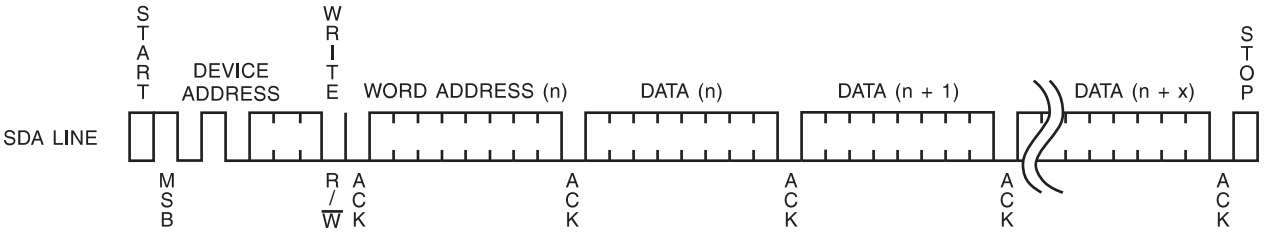


Figure 10-4. Current Address Read

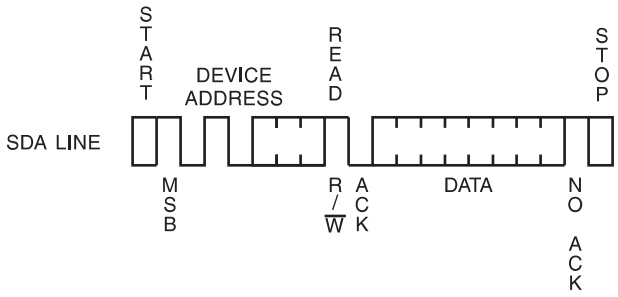


Figure 10-5. Random Read

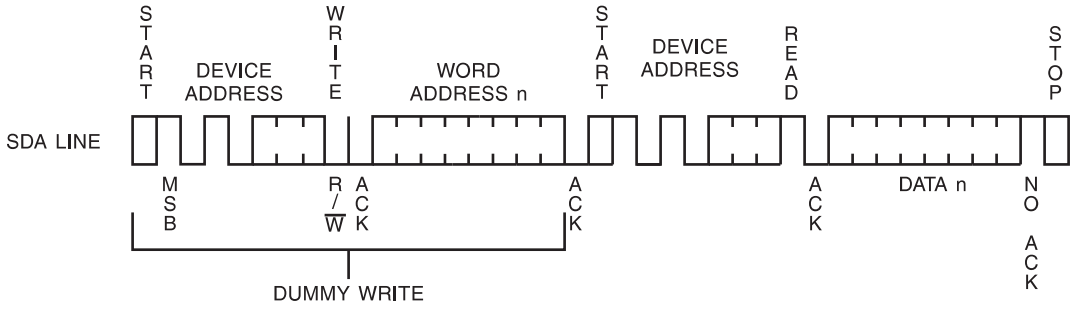
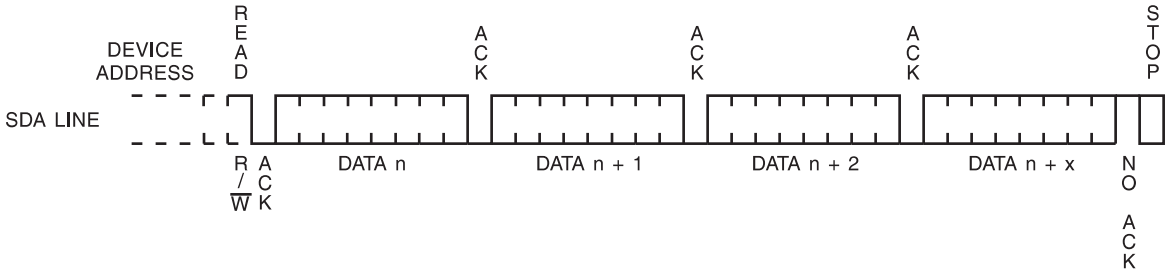


Figure 10-6. Sequential Read



AT24C16B Ordering Information

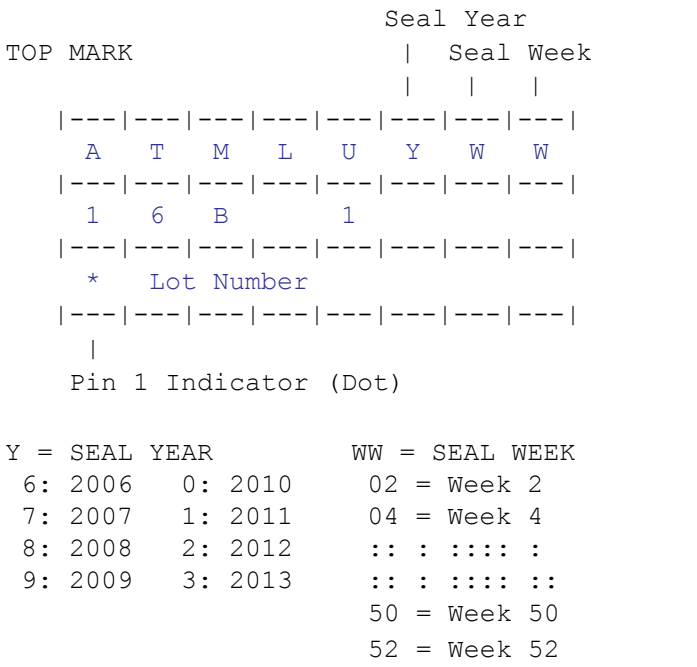
Ordering Codes	Voltage	Package	Operating Range
AT24C16B-PU (Bulk Form Only)	1.8	8P3	Lead-Free/Halogen-Free Industrial Temperature (-40°C to 85°C)
AT24C16BN-SH-B(1) (NiPdAu Lead Finish)	1.8	8S1	
AT24C16BN-SH-T(2) (NiPdAu Lead Finish)	1.8	8S1	
AT24C16B-TH-B(1) (NiPdAu Lead Finish)	1.8	8A2	
AT24C16B-TH-T(2) (NiPdAu Lead Finish)	1.8	8A2	
AT24C16BY6-YH-T(2) (NiPdAu Lead Finish)	1.8	8Y6	
AT24C16BD3-DH-T(2) (NiPdAu Lead Finish)	1.8	8D3	
AT24C16BTSU-T(2)	1.8	5TS1	
AT24C16BU3-UU-T(2)	1.8	8U3-1	
AT24C16B-W-11(3)	1.8	Die Sales	Industrial Temperature (-40°C to 85°C)

Notes: 1. "-B" denotes bulk.
2. "-T" denotes tape and reel. SOIC = 4K per reel. TSSOP, Ultra Thin Mini MAP, SOT23, dBGA2 = 5K per reel.
3. Available in tape and reel, and wafer form; order as SL788 for inkless wafer form. Bumped die available upon request. Please contact Serial Interface Marketing.

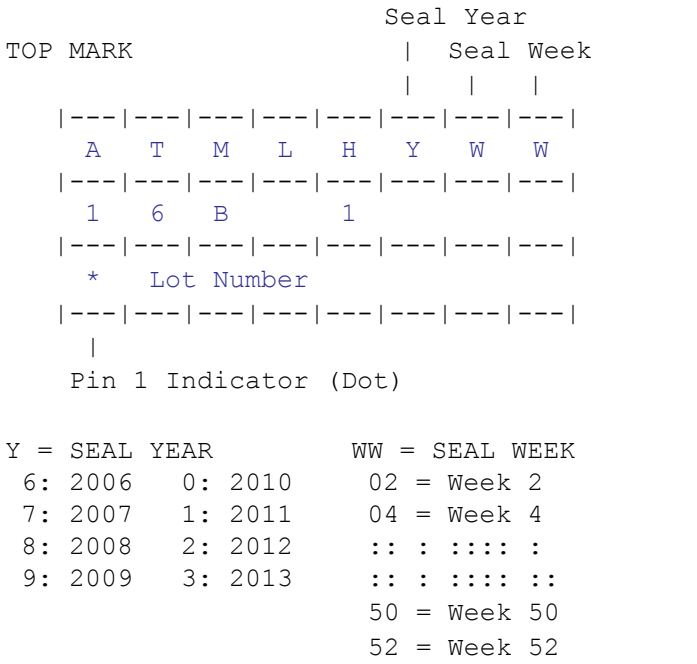
Package Type	
8P3	8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8A2	8-lead, 4.4 mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)
8Y6	8-lead, 2.0 mm x 3.00 mm Body, 0.50 mm Pitch, Ultra Thin Mini-MAP, Dual No Lead Package (DFN), (MLP 2x3 mm)
5TS1	5-lead, 2.90 mm x 1.60 mm Body, Plastic Thin Shrink Small Outline Package (SOT23)
8U3-1	8-ball, die Ball Grid Array Package (dBGA2)
8D3	8-lead, 1.80 mm x 2.20 mm Body, Ultra Lead Frame Land Grid Array (ULA)
Options	
–1.8	Low-voltage (1.8V to 5.5V)

11. Part Marking

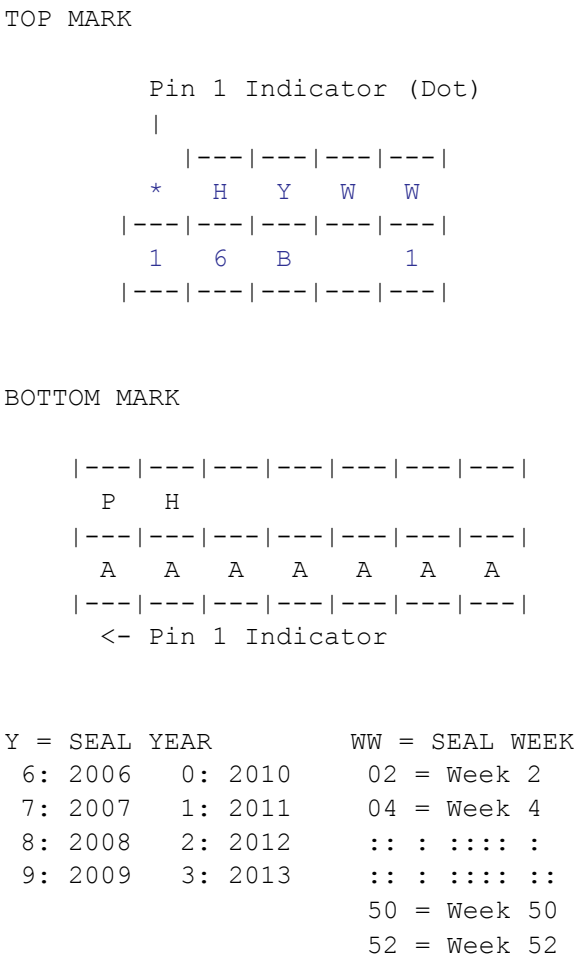
11.1 8-PDIP



11.2 8-SOIC


Seal Year
TOP MARK
Seal Week
A T M L H Y W W
1 6 B 1
* Lot Number
Pin 1 Indicator (Dot)
Y = SEAL YEAR
6: 2006
7: 2007
8: 2008
9: 2009
0: 2010
1: 2011
2: 2012
3: 2013
WW = SEAL WEEK
02 = Week 2
04 = Week 4
50 = Week 50
52 = Week 52
Lot Number to Use ALL Characters in Marking
BOTTOM MARK
No Bottom Mark

11.3 8-TSSOP


TOP MARK
Pin 1 Indicator (Dot)
* H Y W W
1 6 B 1
BOTTOM MARK
P H
A A A A A A A
<- Pin 1 Indicator
Y = SEAL YEAR
6: 2006
7: 2007
8: 2008
9: 2009
0: 2010
1: 2011
2: 2012
3: 2013
WW = SEAL WEEK
02 = Week 2
04 = Week 4
50 = Week 50
52 = Week 52

11.4 8-Ultra Thin Mini-Map

```
TOP MARK
            |---|---|---|
              1   6   B
            |---|---|---|
              H   1
            |---|---|---|
              Y   X   X
            |---|---|---|
              *
              |
    Pin 1 Indicator (Dot)

Y = YEAR OF ASSEMBLY

XX = ATMEL LOT NUMBER TO COORESPOND WITH
NSEB TRACE CODE LOG BOOK.
(e.g. XX = AA, AB, AC,...AX, AY, AZ)

Y = SEAL YEAR
 6: 2006   0: 2010
 7: 2007   1: 2011
 8: 2008   2: 2012
 9: 2009   3: 2013
```

11.5 8-ULA

```
TOP MARK
            |---|---|---|
              1   6   B
            |---|---|---|
              Y   X   X
            |---|---|---|
              *
              |
              Pin 1 Indicator (Dot)

  Y = BUILD YEAR
2006  = 6       2008  = 8
2007  = 7       Etc. . .

  XX = ATMEL LOT NUMBER TO COORESPOND WITH
       NSEB TRACE CODE LOG BOOK.
   (e.g. XX = AA, AB, AC,...AX, AY, AZ)
```

11.6 dBGA2

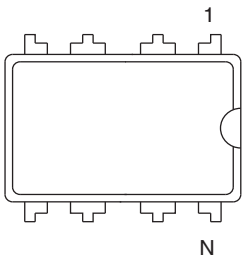
TOP MARK
LINE 1-------> 16BU
LINE 2-------> PYMTC
|<-- Pin 1 This Corner
P = COUNTRY OF ORIGIN
Y = ONE DIGIT YEAR CODE
4: 2004 7: 2007
5: 2005 8: 2008
6: 2006 9: 2009
M = SEAL MONTH (USE ALPHA DESIGNATOR A-L)
A = JANUARY
B = FEBRUARY
" " """""""
J = OCTOBER
K = NOVEMBER
L = DECEMBER
TC = TRACE CODE (ATMEL LOT
NUMBERS TO CORRESPOND
WITH ATK TRACE CODE LOG BOOK)

11.7 SOT23

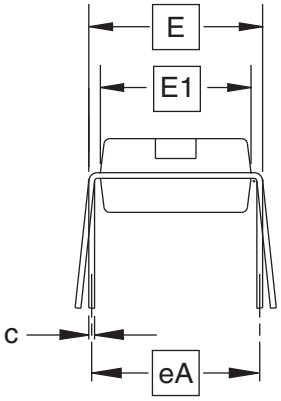
TOP MARK
|---|---|---|---|---|---|
Line 1 ----------> 1 6 B 1 U
|---|---|---|---|---|---|
*
|
XXX = Device
V = Voltage Indicator
U = Material Set
Pin 1 Indicator (Dot)
BOTTOM MARK
|---|---|---|---|
Y M T C
|---|---|---|---|
Y = One Digit Year Code
M = Seal Month
(Use Alpha Designator A-L)
TC = Trace Code

12. Packaging Information

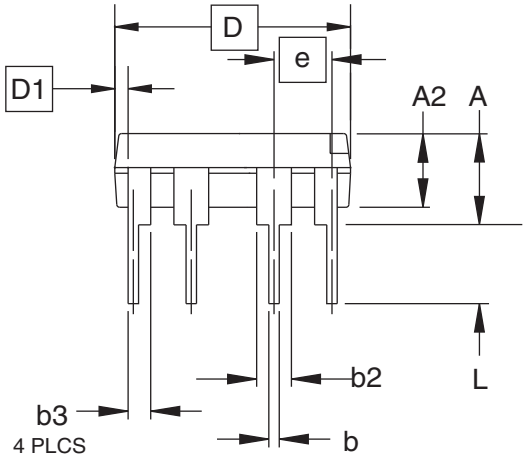
12.1 8P3 – PDIP



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = inches)

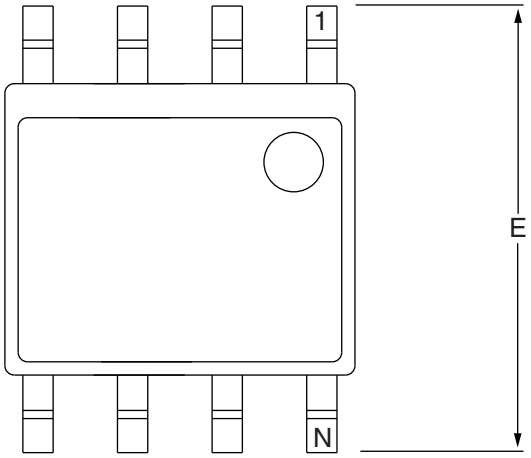
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	0.210	2
A2	0.115	0.130	0.195	
b	0.014	0.018	0.022	5
b2	0.045	0.060	0.070	6
b3	0.030	0.039	0.045	6
c	0.008	0.010	0.014	
D	0.355	0.365	0.400	3
D1	0.005	–	–	3
E	0.300	0.310	0.325	4
E1	0.240	0.250	0.280	3
e	0.100 BSC			
eA	0.300 BSC			4
L	0.115	0.130	0.150	2

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA, for additional information.
2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.010 inch.
4. E and eA measured with the leads constrained to be perpendicular to datum.
5. Pointed or rounded lead tips are preferred to ease insertion.
6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25 mm).

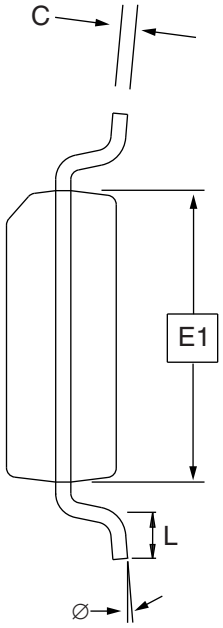
01/09/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**8P3**, 8-lead, 0.300" Wide Body, Plastic Dual In-line Package (PDIP)	8P3	B

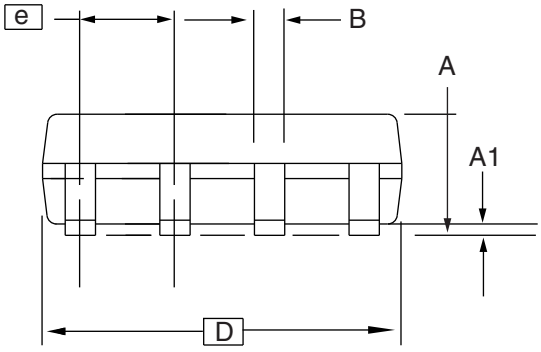
12.2 8S1 – JEDEC SOIC



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

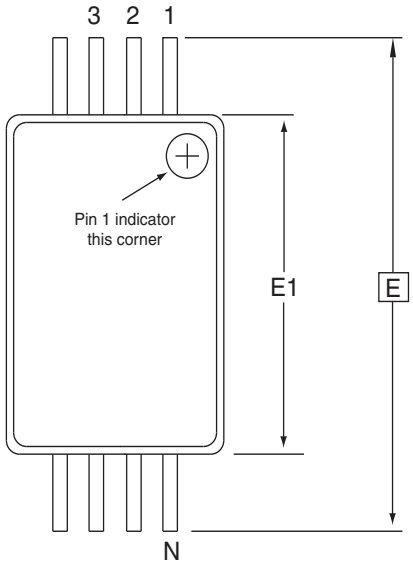
SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.00	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
∅	0°	–	8°	

Note: These drawings are for general information only. Refer to JEDEC Drawing MS-012, Variation AA for proper dimensions, tolerances, datums, etc.

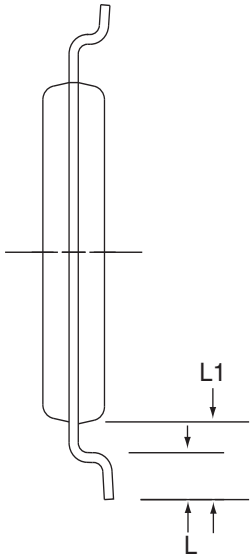
10/7/03

1150 E. Cheyenne Mtn. Blvd. Colorado Springs, CO 80906	**TITLE** **8S1**, 8-lead (0.150" Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	**DRAWING NO.** 8S1	**REV.** B

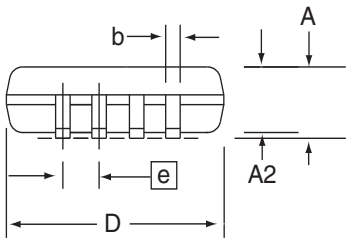
12.3 8A2 – TSSOP



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

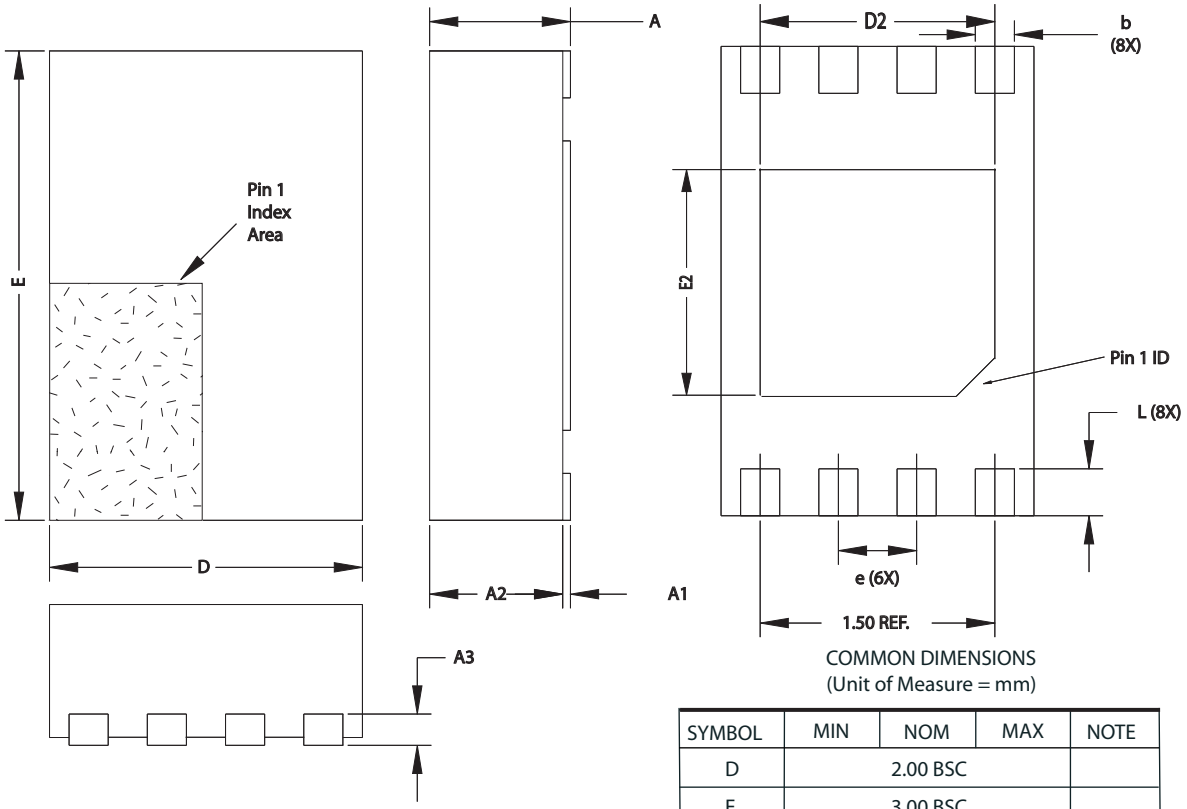
SYMBOL	MIN	NOM	MAX	NOTE
D	2.90	3.00	3.10	2, 5
E		6.40 BSC		
E1	4.30	4.40	4.50	3, 5
A	–	–	1.20	
A2	0.80	1.00	1.05	
b	0.19	–	0.30	4
e		0.65 BSC		
L	0.45	0.60	0.75	
L1		1.00 REF		

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and ad acent lead is 0.07 mm.
5. Dimension D and E1 to be determined at Datum Plane H.

5/30/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**8A2**, 8-lead, 4.4 mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	8A2	B

12.4 8Y6 - Mini Map



COMMON DIMENSIONS
(Unit of Measure = mm)

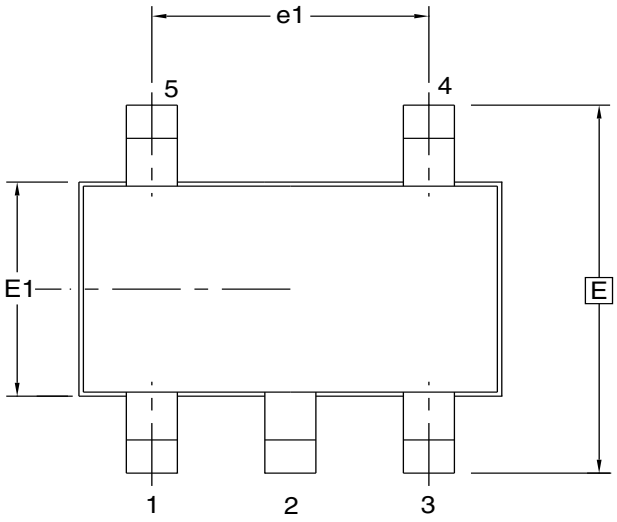
SYMBOL	MIN	NOM	MAX	NOTE
D		2.00 BSC		
E		3.00 BSC		
D2	1.40	1.50	1.60	
E2	-	-	1.40	
A	-	-	0.60	
A1	0.0	0.02	0.05	
A2	-	-	0.55	
A3		0.20 REF		
L	0.20	0.30	0.40	
e		0.50 BSC		
b	0.20	0.25	0.30	2

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-229, for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.
3. Soldering the large thermal pad is optional, but not recommended. No electrical connection is accomplished to the device through this pad, so if soldered it should be tied to ground

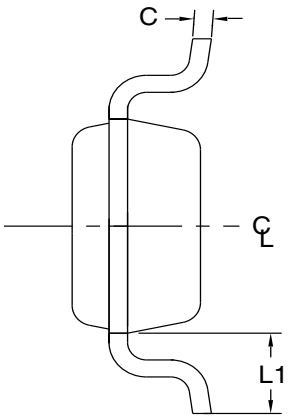
10/16/07

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	8Y6, 8-lead 2.0 x 3.0 mm Body, 0.50 mm Pitch, Utlra Thin Mini-Map, Dual No Lead Package (DFN) ,(MLP 2x3)	8Y6	D

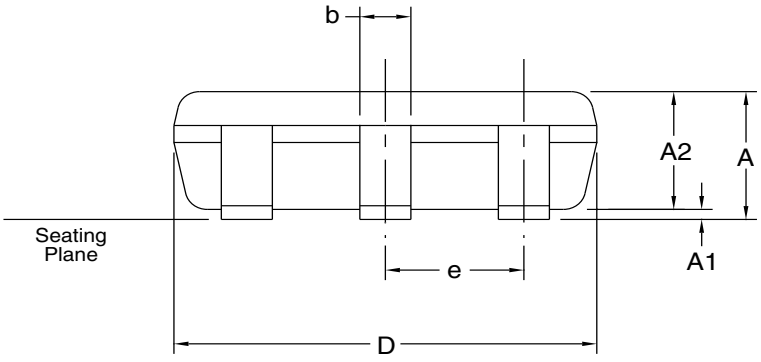
12.5 5TS1 – SOT23



Top View



End View



Side View

NOTES:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-193, Variation AB, for additional information.
2. Dimension D does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.15 mm per side.
3. The package top may be smaller than the package bottom. Dimensions D and E1 are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body.
4. These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.
5. Dimension "b" does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the "b" dimension at maximum material condition. The Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and an adjacent lead shall not be less than 0.07 mm.

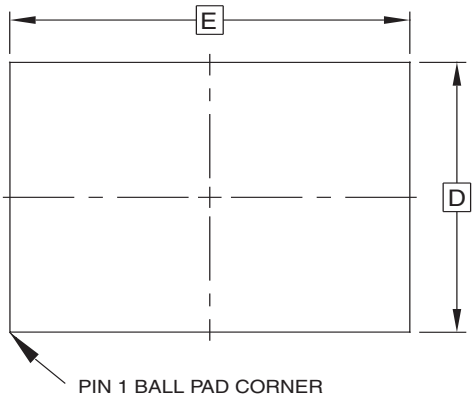
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.10	
A1	0.00	–	0.10	
A2	0.70	0.90	1.00	
c	0.08	–	0.20	4
D		2.90 BSC		2, 3
E		2.80 BSC		2, 3
E1		1.60 BSC		2, 3
L1		0.60 REF		
e		0.95 BSC		
e1		1.90 BSC		
b	0.30	–	0.50	4, 5

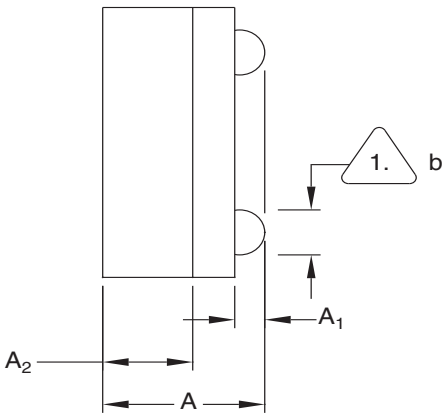
6/25/03

	TITLE	DRAWING NO.	REV.
1150 E. Cheyenne Mtn. Blvd. Colorado Springs, CO 80906	**5TS1,** 5-lead, 1.60 mm Body, Plastic Thin Shrink Small Outline Package (SHRINK SOT)	PO5TS1	A

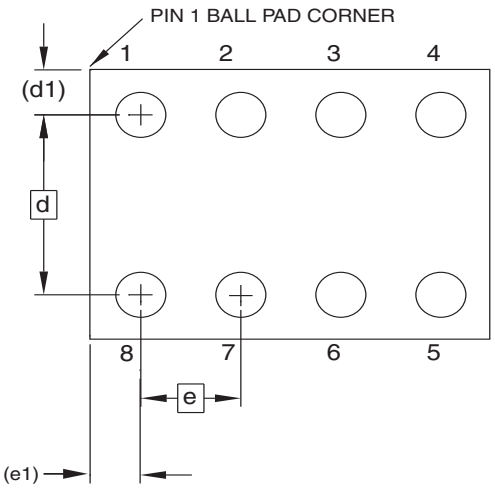
12.6 8U3-1 – dBGA2



Top View



Side View



Bottom View
8 SOLDER BALLS

1. Dimension “b” is measured at the maximum solder ball diameter.

This drawing is for general information only.

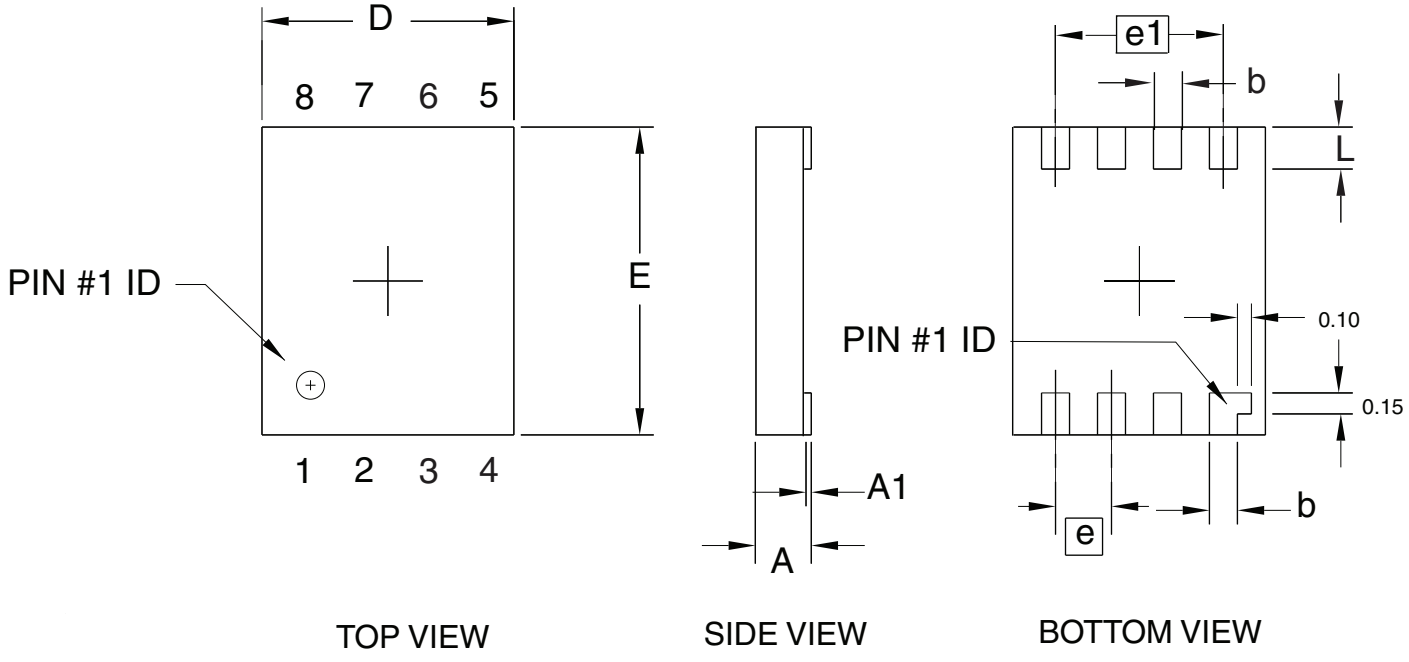
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.71	0.81	0.91	
A1	0.10	0.15	0.20	
A2	0.40	0.45	0.50	
b	0.20	0.25	0.30	
D	1.50 BSC			
E	2.00 BSC			
e	0.50 BSC			
e1	0.25 REF			
d	1.00 BSC			
d1	0.25 REF			

6/24/03

	TITLE	DRAWING NO.	REV.
1150 E. Cheyenne Mtn. Blvd. Colorado Springs, CO 80906	**8U3-1,** 8-ball, 1.50 x 2.00 mm Body, 0.50 mm pitch, Small Die Ball Grid Array Package (dBGA2)	PO8U3-1	A

12.7 8D3 - ULA



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	0.40	
A1	0.00	–	0.05	
D	1.70	1.80	1.90	
E	2.10	2.20	2.30	
b	0.15	0.20	0.25	
e		0.40 TYP		
e1		1.20 REF		
L	0.25	0.30	0.35	

11/15/05

	TITLE	DRAWING NO.	REV.
1150 E. Cheyenne Mtn. Blvd. Colorado Springs, CO 80906	**8D3**, 8-lead (1.80 x 2.20 mm Body) Ultra Leadframe Land Grid Array (ULLGA) D3	8D3	0

13. Revision History

Lit No.	Date	Comment
5175E	7/2012	Not recommended for new design. Use AT24C16C.
5175E	3/2009	Changed the Vcc to 5.5V in the test condition for Isb1
5175D	6/2008	Deleted A0, A1, A2 pin-outs
5175C	11/2007	AT24C16B product with date code 742 or later supports 5Vcc operation Added ULA package information
5175B	4/2007	Removed reference to Waffle Pack Corrected Note 3 on Page 13 Added lines to Ordering Code table
5175A	3/2007	Initial document release

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