Quad 2-Input Multiplexer

1. Description

The 74HC/HCT157 are quad 2-input multiplexers which select 4 bits of data from two sources under the control of a common data select input (S). The enable input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs (1Y to 4Y) are forced LOW regardless of all other input conditions.

Moving the data from two groups of registers to four common output buses is a common use of the 74HC/HCT157. The state of the common data select input (S) determines the particular register from which the data comes. It can also be used as function generator. The device is useful for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common.

The 74HC/HCT157 is logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S.

The logic equations are:

$1Y=\overline{E}\times\left(1I1\times S+1I0\times\overline{S}\right)$

$2Y=\overline{E}\times\left(2I1\times S+2I0\times\overline{S}\right)$

$3Y=\overline{E}\times\left(3I1\times S+3I0\times\overline{S}\right)$

$4Y=\overline{E}\times\left(4I1\times S+4I0\times\overline{S}\right)$

The 74HC/HCT157 is identical to the 74HC/HCT158 but has non-inverting (true) outputs.

2. Features

- Input levels:
  - For 74HC157: CMOS level
  - For 74HCT157: TTL level
- Low-power dissipation
- Non-inverting data path
- Specified from -40℃ to +105℃
- Packaging information:
  DIP16/SOIC16/TSSOP16

3. Ordering Information

Type Number	Package Type	Packing	Notes
74HC157N	DIP-16	Tube	
74HC157N	DIP-16	Tube	
74HC157D	SOIC-16	Tape & Reel	
74HC157D	SOIC-16	Tape & Reel	
74HC157PW	TSSOP-16	Tape & Reel	
74HC157PW	TSSOP-16	Tape & Reel	

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

4. Functional Diagram

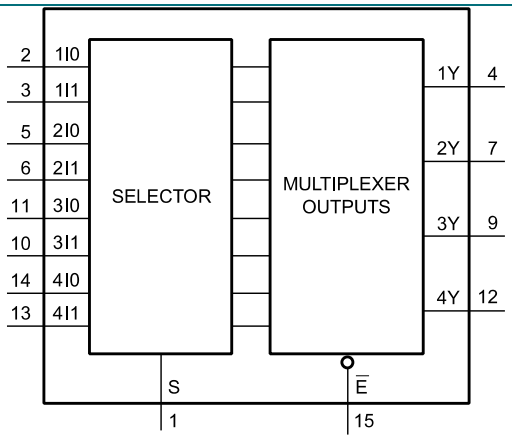


Fig. 1. Logic Symbol

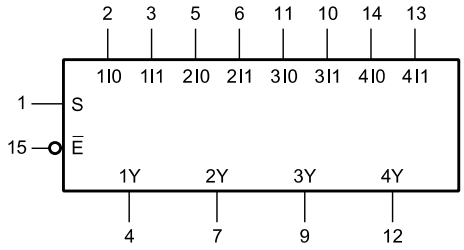


Fig. 2. Logic Symbol

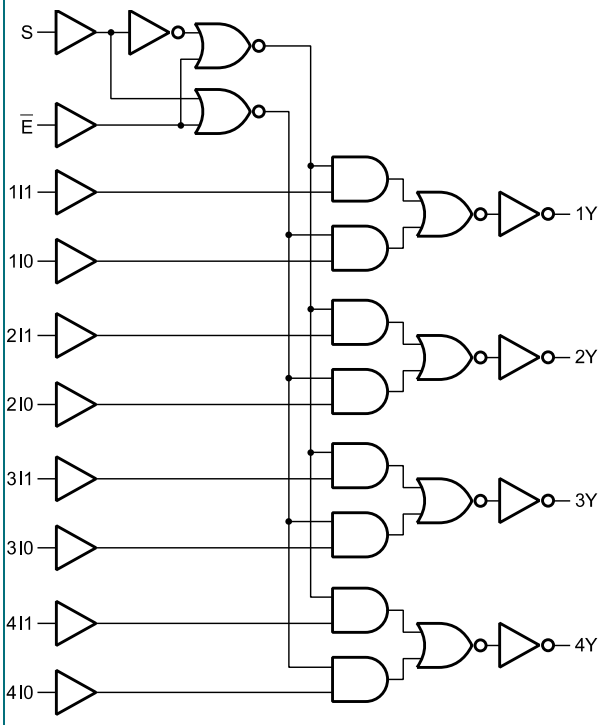


Fig. 3. Logic Diagram

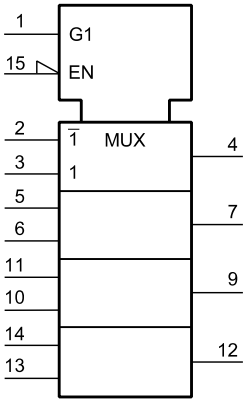
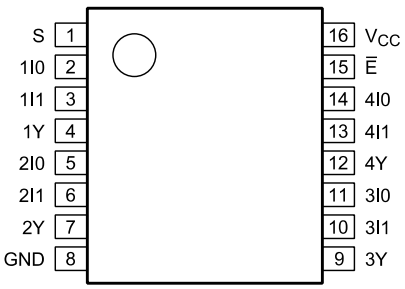


Fig. 4. IEC Logic Symbol



Pin Cinfiguration

Pin Description

Pin No.	Pin Name	Description
1	S	common data select input
2	1I0	data input from source 0
3	1I1	data input from source 1
4	1Y	multiplexer output
5	2I0	data input from source 0
6	2I1	data input from source 1
7	2Y	multiplexer output
8	GND	ground (0V)
9	3Y	multiplexer output
10	3I1	data input from source 1
11	3I0	data input from source 0
12	4Y	multiplexer output
13	4I1	data input from source 1
14	4I0	data input from source 0
15	$\overline{E}$	enable input (active LOW)
16	V_{CC}	supply voltage

Function Table

Input				Output
$\overline{E}$	S	nI0	nI1	nY
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care.

5. Electrical Parameter

Absolute Maximum Ratings

(Voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V_{CC}	-		-0.5	+7.0	V
input clamping current	I_{IK}	$V_I < -0.5V$ or $V_I > V_{CC}+0.5V$		-	±20	mA
output clamping current	I_{OK}	$V_O < -0.5V$ or $V_O > V_{CC}+0.5V$		-	±20	mA
output current	I_O	V_O= -0.5V to (V_{CC}+0.5V)		-	±25	mA
supply current	I_{CC}	-		-	+50	mA
ground current	I_{GND}	-		-50	-	mA
storage temperature	T_{stg}	-		-65	+150	˚C
total power dissipation	P_{tot}	-		-	500	mW
soldering temperature	T_L	10s	DIP	245		˚C
			SOIC	250		˚C

Note:

1 For DIP16 packages: above 70˚C the value of P_{tot} derates linearly with 12mW/K.

2 For SOIC16 packages: above 70˚C the value of P_{tot} derates linearly with 8mW/K.

3 For (T)SSOP16 packages: above 60˚C the value of P_{tot} derates linearly with 5.5mW/K.

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
74HC157						
supply voltage	V_{CC}	-	2.0	5.0	6.0	V
input voltage	V_I	-	0	-	^{V}CC	V
output voltage	V_O	-	0	-	^{V}CC	V
input transition rise and fall rate	Δt/ΔV	V_{CC}=2.0V	-	-	625	ns/V
		V_{CC}=4.5V	-	1.67	139	ns/V
		V_{CC}=6.0V	-	-	83	ns/V
ambient temperature	T_{amb}	-	-40	-	+105	˚C
74HCT157						
supply voltage	V_{CC}	-	4.5	5.0	5.5	V
input voltage	V_I	-	0	-	^{V}CC	V
output voltage	V_O	-	0	-	^{V}CC	V
input transition rise and fall rate	Δt/ΔV	V_{CC}=4.5V	-	1.67	139	ns/V
ambient temperature	T_{amb}	-	-40	-	+105	˚C

6. Electrical Characteristics

DC Characteristics 1

(T_{amb}=25°C, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
74HC157							
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	1.2	-	V
		V_{CC}=4.5V		3.15	2.4	-	V
		V_{CC}=6.0V		4.2	3.2	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	0.8	0.5	V
		V_{CC}=4.5V		-	2.1	1.35	V
		V_{CC}=6.0V		-	2.8	1.8	V
HIGH-level output voltage	V_{OH}	V_I=V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	2.0	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	4.5	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	6.0	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.98	4.32	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.48	5.81	-	V
LOW-level output voltage	V_{OL}	V_I=V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	0	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	0	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	0	0.1	V
			I_O=4.0mA; V_{CC}=4.5V	-	0.15	0.26	V
			I_O=5.2mA; V_{CC}=6.0V	-	0.16	0.26	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±0.1	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	8.0	uA
input capacitance	C_I	-		-	3.5	-	pF
74HCT157							
HIGH-level input voltage	V_{IH}	V_{CC}=4.5V to 5.5V		2.0	1.6	-	V
LOW-level input voltage	V_{IL}	V_{CC}=4.5V to 5.5V		-	1.2	0.8	V
HIGH-level output voltage	V_{OH}	V_I=V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=-20uA	4.4	4.5	-	V
			I_O=-4.0mA	3.98	4.32	-	V
LOW-level output voltage	V_{OL}	V_I=V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=20uA	-	0	0.1	V
			I_O=4.0mA	-	0.15	0.26	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±0.1	uA

supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	8.0	uA
additional supply current	ΔI_{CC}	V_I=V_{CC}-2.1V; other inputs at V_{CC} or GND; I_O=0A; V_{CC}=4.5V to 5.5V	per input pin; nI0, nI1 inputs	-	100	360	uA
			per input pin; $\overline{E}$ input	-	60	216	uA
			per input pin; S input	-	100	360	uA
input capacitance	C_I	-		-	3.5	-	pF

DC Characteristics 2

(T_{amb}=-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
74HC157							
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
HIGH-level output voltage	V_{OH}	V_I=V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.84	-	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.34	-	-	V
LOW-level output voltage	V_{OL}	V_I=V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
			I_O=4.0mA; V_{CC}=4.5V	-	-	0.33	V
			I_O=5.2mA; V_{CC}=6.0V	-	-	0.33	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	80	uA
74HCT157							
HIGH-level input voltage	V_{IH}	V_{CC}=4.5V to 5.5V		2.0	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=4.5V to 5.5V		-	-	0.8	V
HIGH-level output voltage	V_{OH}	V_I=V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=-20uA	4.4	-	-	V
			I_O=-4.0mA	3.84	-	-	V
LOW-level	V_{OL}	V_I=V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=20uA	-	-	0.1	V

output voltage			I_O=4.0mA	-	-	0.33	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±1.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	80	uA
additional supply current	ΔI_{CC}	V_I=V_{CC}-2.1V; other inputs at V_{CC} or GND; I_O=0A; V_{CC}=4.5V to 5.5V	per input pin; nI0, nI1 inputs	-	-	450	uA
			per input pin; $\overline{E}$ input	-	-	270	uA
			per input pin; S input	-	-	450	uA

DC Characteristics 3

(T_{amb}=-40°C to +105°C, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
74HC157							
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
HIGH-level output voltage	V_{OH}	V_I=V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.7	-	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.2	-	-	V
LOW-level output voltage	V_{OL}	V_I=V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
			I_O=4.0mA; V_{CC}=4.5V	-	-	0.4	V
			I_O=5.2mA; V_{CC}=6.0V	-	-	0.4	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	160	uA
74HCT157							
HIGH-level input voltage	V_{IH}	V_{CC}=4.5V to 5.5V		2.0	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=4.5V to 5.5V		-	-	0.8	V
HIGH-level output voltage	V_{OH}	V_I=V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=-20uA	4.4	-	-	V
			I_O=-4.0mA	3.7	-	-	V
LOW-level	V_{OL}	V_I=V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=20uA	-	-	0.1	V

output voltage			I_O=4.0mA	-	-	0.4	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±1.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	160	uA
additional supply current	ΔI_{CC}	V_I=V_{CC}-2.1V; other inputs at V_{CC} or GND; I_O=0A; V_{CC}=4.5V to 5.5V	per input pin; nI0, nI1 inputs	-	-	490	uA
			per input pin; $\overline{E}$ input	-	-	294	uA
			per input pin; S input	-	-	490	uA

AC Characteristics 1

(T_{amb}=25°C, GND =0V, C_L=50pF, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
74HC157							
propagation delay	t_{pd}	nI0, nI1 to nY; see Figure 6[1]	V_{CC}=2.0V	-	36	125	ns
			V_{CC}=4.5V	-	13	25	ns
			V_{CC}=5.0V; C_L=15pF	-	11	-	ns
			V_{CC}=6.0V	-	10	21	ns
		S to nY; see Figure 6[1]	V_{CC}=2.0V	-	41	125	ns
			V_{CC}=4.5V	-	15	25	ns
			V_{CC}=5.0V; C_L=15pF	-	12	-	ns
			V_{CC}=6.0V	-	12	21	ns
		$\overline{E}$ to nY; see Figure 7[1]	V_{CC}=2.0V	-	39	115	ns
			V_{CC}=4.5V	-	14	23	ns
			V_{CC}=5.0V; C_L=15pF	-	11	-	ns
			V_{CC}=6.0V	-	11	20	ns
transition time	t_t	nY; see Figure 6[2]	V_{CC}=2.0V	-	19	75	ns
			V_{CC}=4.5V	-	7	15	ns
			V_{CC}=6.0V	-	6	13	ns
power dissipation capacitance	C_{PD}	C_L=50pF; f=1MHz; V_I=GND to V_{CC}[3]		-	70	-	pF
74HCT157							
propagation delay	t_{pd}	nI0, nI1 to nY; see Figure 6[1]	V_{CC}=4.5V	-	16	27	ns
			V_{CC}=5.0V; C_L=15pF	-	13	-	ns
		S to nY; see Figure 6[1]	V_{CC}=4.5V	-	22	37	ns
			V_{CC}=5.0V; C_L=15pF	-	19	-	ns
		$\overline{E}$ to nY; see Figure 7[1]	V_{CC}=4.5V	-	15	26	ns
			V_{CC}=5.0V; C_L=15pF	-	12	-	ns
transition time	t_t	nY; V_{CC}=4.5V; see Figure 6[2]		-	7	15	ns
power dissipation capacitance	C_{PD}	C_L=50pF; f=1MHz; V_I=GND to V_{CC}-1.5V[3]		-	70	-	pF

Note:

1 t_{pd} is the same as t_{PLH} and t_{PHL}.

2 t_t is the same as t_{THL} and t_{TLH}.

3 C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D=C_{PD}\times V_{CC}^2\times f_i\times N+\sum(C_L\times V_{CC}^2\times f_o)$ where:

f_i=input frequency in MHz;

f_o=output frequency in MHz;

C_L=output load capacitance in pF;

V_{CC}=supply voltage in V;

N=number of inputs switching;

$\sum(C_L\times V_{CC}^2\times f_o)$=sum of outputs.

AC Characteristics 2

(T_{amb}=-40°C to +85°C, GND=0V, C_L=50pF, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
74HC157							
propagation delay	t_{pd}	nI0, nI1 to nY; see Figure 6[1]	V_{CC}=2.0V	-	-	155	ns
			V_{CC}=4.5V	-	-	31	ns
			V_{CC}=6.0V	-	-	26	ns
		S to nY; see Figure 6[1]	V_{CC}=2.0V	-	-	155	ns
			V_{CC}=4.5V	-	-	31	ns
			V_{CC}=6.0V	-	-	26	ns
		$\overline{E}$ to nY; see Figure 7[1]	V_{CC}=2.0V	-	-	145	ns
			V_{CC}=4.5V	-	-	29	ns
			V_{CC}=6.0V	-	-	25	ns
transition time	t_t	nY; see Figure 6[2]	V_{CC}=2.0V	-	-	95	ns
			V_{CC}=4.5V	-	-	19	ns
			V_{CC}=6.0V	-	-	16	ns
74HCT157							
propagation delay	t_{pd}	nI0, nI1 to nY; see Figure 6[1]	V_{CC}=4.5V	-	-	34	ns
		S to nY; see Figure 6[1]	V_{CC}=4.5V	-	-	46	ns
		$\overline{E}$ to nY; see Figure 7[1]	V_{CC}=4.5V	-	-	33	ns
transition time	t_t	nY; V_{CC}=4.5V; see Figure 6[2]		-	-	19	ns

Note:

1 t_{pd} is the same as t_{PLH} and t_{PHL}.

2 t_t is the same as t_{THL} and t_{TLH}.

AC Characteristics 3

(T_{amb}=-40°C to +105°C, GND=0V, C_L=50pF, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
74HC157							
propagation delay	t_{pd}	nI0, nI1 to nY; see Figure 6[1]	V_{CC}=2.0V	-	-	190	ns
			V_{CC}=4.5V	-	-	38	ns
			V_{CC}=6.0V	-	-	32	ns
		S to nY; see Figure 6[1]	V_{CC}=2.0V	-	-	190	ns
			V_{CC}=4.5V	-	-	38	ns
			V_{CC}=6.0V	-	-	32	ns
		— E to nY; see Figure 7[1]	V_{CC}=2.0V	-	-	175	ns
			V_{CC}=4.5V	-	-	35	ns
			V_{CC}=6.0V	-	-	30	ns
transition time	t_t	nY; see Figure 6[2]	V_{CC}=2.0V	-	-	110	ns
			V_{CC}=4.5V	-	-	22	ns
			V_{CC}=6.0V	-	-	19	ns
74HCT157							
propagation delay	t_{pd}	nI0, nI1 to nY; see Figure 6[1]	V_{CC}=4.5V	-	-	41	ns
		S to nY; see Figure 6[1]	V_{CC}=4.5V	-	-	56	ns
		$\overline{E}$ to nY; see Figure 7[1]	V_{CC}=4.5V	-	-	39	ns
transition time	t_t	nY; V_{CC}=4.5V; see Figure 6[2]		-	-	22	ns

Note:

1 t_{pd} is the same as t_{PLH} and t_{PHL}.

2 t_t is the same as t_{THL} and t_{TLH}.

7. Testing Circuit

AC Testing Circuit

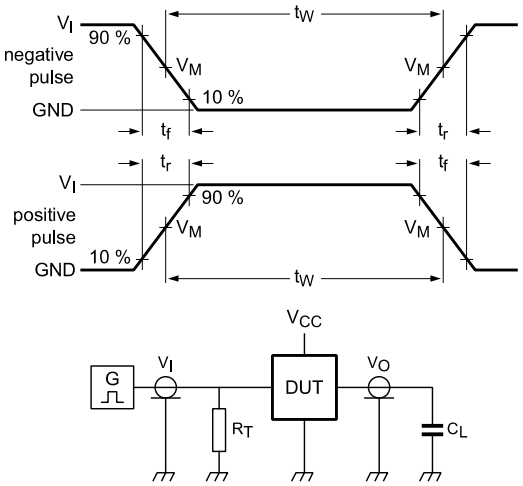


Fig. 5. Test circuit for measuring switching times

Definitions for test circuit:

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.

AC Testing Waveforms

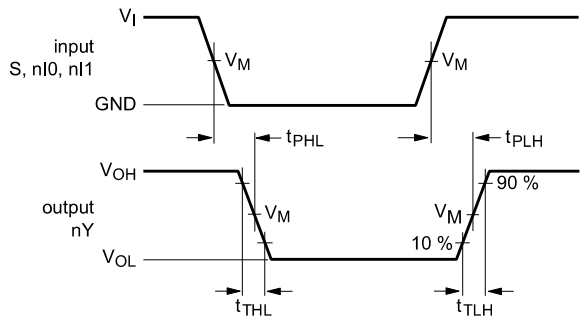


Fig. 6. Propagation delay input (nI0, nI1, S) to output (nYn)

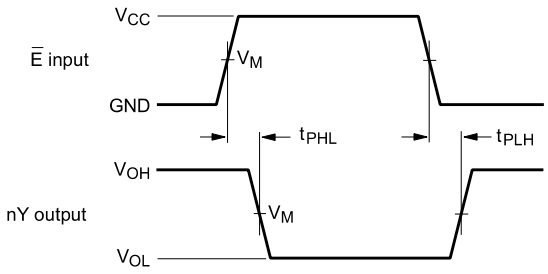


Fig. 7. Propagation delay input ($\overline{E}$) to output (nY)

Measurement Points

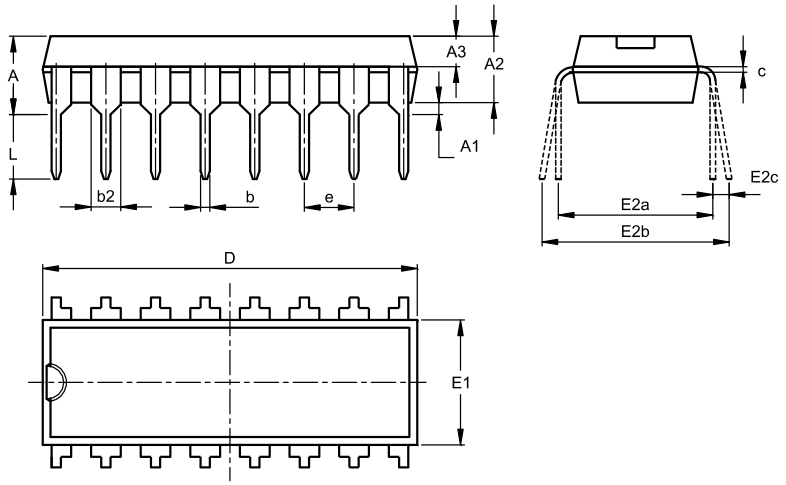
Type	Input	Output
	V_M	V_M
74HC157	0.5×V_{CC}	0.5×V_{CC}
74HCT157	1.3V	1.3V

Test Data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74HC157	V_{CC}	6ns	15pF, 50pF	t_{PHL}, t_{PLH}
74HCT157	3V	6ns	15pF, 50pF	t_{PHL}, t_{PLH}

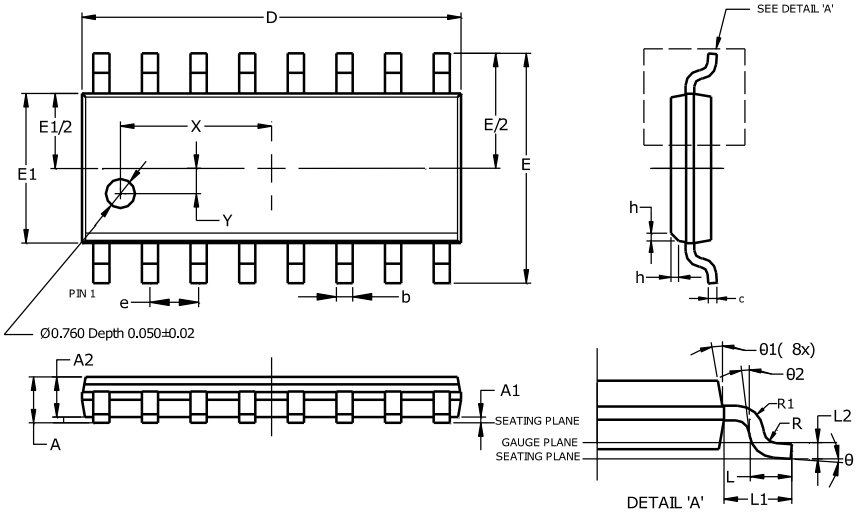
8. Package Outlines

DIP-16



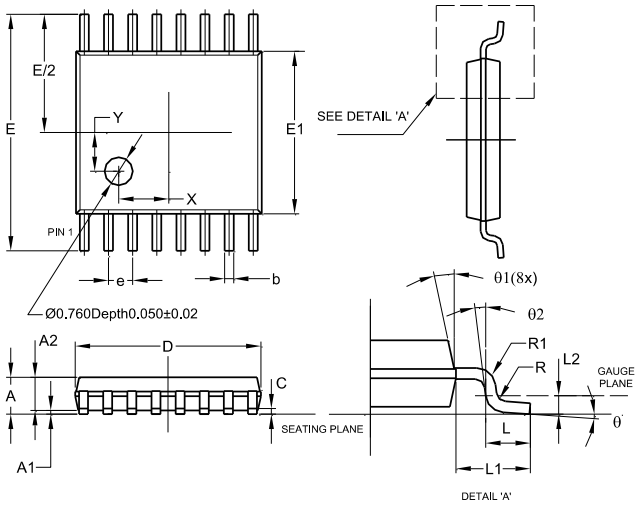
PDIP-16			
Dim	Min	Max	Nom
A	3.60	4.00	3.80
A1	0.51	-	
A2	3.20	3.40	3.30
A3	1.47	1.57	1.52
b	0.44	0.53	–
b2	1.52BSC		
c	0.25	0.31	–
D	18.90	19.30	19.10
E1	6.15	6.55	6.35
E2a	7.62 BSC		
E2b	7.62	9.30	–
E2c	0.00	0.84	–
e	2.54BSC		
L	3.00	–	–
All Dimensions in mm			

SOIC-16



SOIC-16			
Dim	Min	Max	Typ
A	–	1.260	–
A1	0.10	0.23	–
A2	1.02	–	–
b	0.31	0.51	–
c	0.10	0.25	–
D	9.80	10.00	–
E	5.90	6.10	–
E1	3.80	4.00	–
e	1.27 BSC		
h	0.15	0.25	0.20
L	0.40	1.27	–
L1	1.04 REF		
L2	0.25 BSC		
R	0.07	–	–
R1	0.07	–	–
X	3.945 REF		
Y	0.661 REF		
θ	0°	8°	–
θ1	5°	15°	–
θ2	0°	–	–
All Dimensions in mm			

TSSOP-16



TSSOP-16			
Dim	**Min**	**Max**	**Typ**
A	-	1.08	-
A1	0.05	0.15	-
A2	0.80	0.93	-
b	0.19	0.30	-
c	0.09	0.20	-
D	4.90	5.10	-
E	6.40 BSC		
E1	4.30	4.50	-
e	0.65 BSC		
L	0.45	0.75	-
L1	1.00 REF		
L2	0.25 BSC		
R / R1	0.09	-	-
X	-	-	1.350
Y	-	-	1.050
θ	0°	8°	-
θ1	5°	15°	-
θ2	0°	-	-
All Dimensions in mm			

9. Disclaimers

Limited warranty and liability

Information in this document is believed to be accurate and reliable. However, Fulihao does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. It is the customer's responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application.

Suitability for use

Fulihao products are designed for specific applications and should not be used for any purpose (including, without limitation, automotive, aerospace, medical, life-saving applications, or any other application which requires especially high reliability for the prevention of such defect as may directly cause damage to the third party's life, body or property) not expressly set forth in applicable Fulihao product documentation.

Right to make changes

Fulihao reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. Fulihao takes no responsibility for the content in this document if provided by an information source outside of Fulihao. This document supersedes and replaces all information supplied prior to the publication hereof.