74HC165/74HCT165

1. Description

The 74HC/HCT165 is 8-bit serial or parallel-in/serial-out shift registers. The device features a serial data input (DS), eight parallel data inputs (D0 to D7) and two complementary serial outputs (Q7 and $\overline{Q7}$ the parallel load input ($\overline{PL}$) is LOW the data from D0 to D7 is loaded into the shift register — asynchronously. When PL is HIGH data enters the register serially at DS. When the clock enable input ($\overline{CE}$) is LOW data is shifted on the LOW-to-HIGH transitions of the CP input. A HIGH on $\overline{CE}$ will disable the CP input. Inputs are overvoltage tolerant to 15V. This enables the device to be used in HIGH-to-LOW level shifting applications.

2. Features

- Input levels:
  For 74HC165: CMOS level
  For 74HCT165: TTL level
- Asynchronous 8-bit parallel load
- Synchronous serial input
- Specified from -40℃ to +85℃
- Packaging information: DIP16/SOP16/TSSOP16

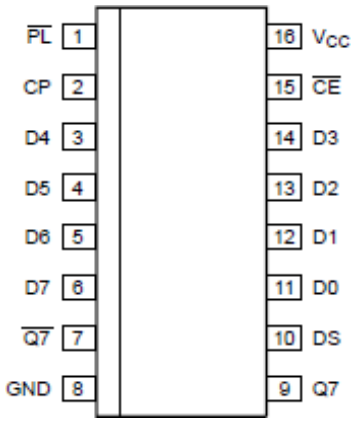
3. Ordering Information

Table 1. Ordering Information

Type Number	Package Type	Packing
74HC165N	DIP-16	Tape & Reel
74HCT165N		Tape & Reel
74HC165D	SOP-16	Tape & Reel
74HCT165D		Tape & Reel
74HC165PW	TSSOP-16	Tape & Reel
74HCT165PW		Tape & Reel

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

4. Pin Configurations



Pin No.	Pin Name	Description
1	$\overline{PL}$	asynchronous parallel load input (active LOW)
2	CP	clock input (LOW-to-HIGH, edge-triggered)
3	D4	parallel data input (also referred to as Dn)
4	D5	parallel data input (also referred to as Dn)
5	D6	parallel data input (also referred to as Dn)
6	D7	parallel data input (also referred to as Dn)
7	$\overline{Q}7$	complementary output from the last stage
8	GND	ground (0V)
9	Q7	serial output from the last stage
10	DS	serial data input
11	D0	parallel data input (also referred to as Dn)
12	D1	parallel data input (also referred to as Dn)
13	D2	parallel data input (also referred to as Dn)
14	D3	parallel data input (also referred to as Dn)
15	$\overline{CE}$	clock enable input (active LOW)
16	V_{CC}	supply voltage

Table 2. Function Table

Operating mode	Input					Qn register		Output	
	$\overline{PL}$	$\overline{CE}$	CP	DS	D0 to D7	Q0	Q1 to Q6	Q7	$\overline{Q}7$
parallel load	L	X	X	X	L	L	L to L	L	H
	L	X	X	X	H	H	H to H	H	L
serial shift	H	L	↑	l	X	L	q0 to q5	q6	$\overline{q}6$
	H	L	↑	h	X	H	q0 to q5	q6	$\overline{q}6$
	H	↑	L	l	X	L	q0 to q5	q6	$\overline{q}6$
	H	↑	L	h	X	H	q0 to q5	q6	$\overline{q}6$
Hold "Do nothing"	H	H	X	X	X	q0	q1 to q6	q7	$\overline{q}7$
	H	X	H	X	X	q0	q1 to q6	q7	$\overline{q}7$

Note:

H=HIGH voltage level;

h=HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition; L=LOW voltage level; ↑=LOW-to-HIGH clock transition;

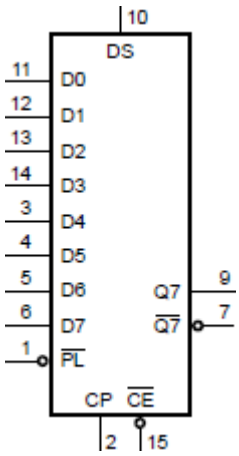
l=LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;

q=state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition; X=don't care;

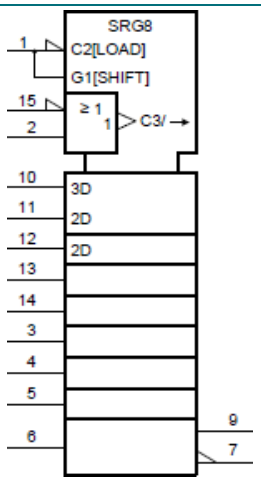
↑=LOW-to-HIGH clock transition.

5. Block Diagram

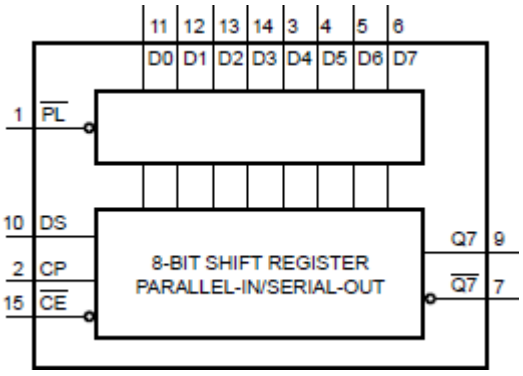
Fig. 1. Block diagram



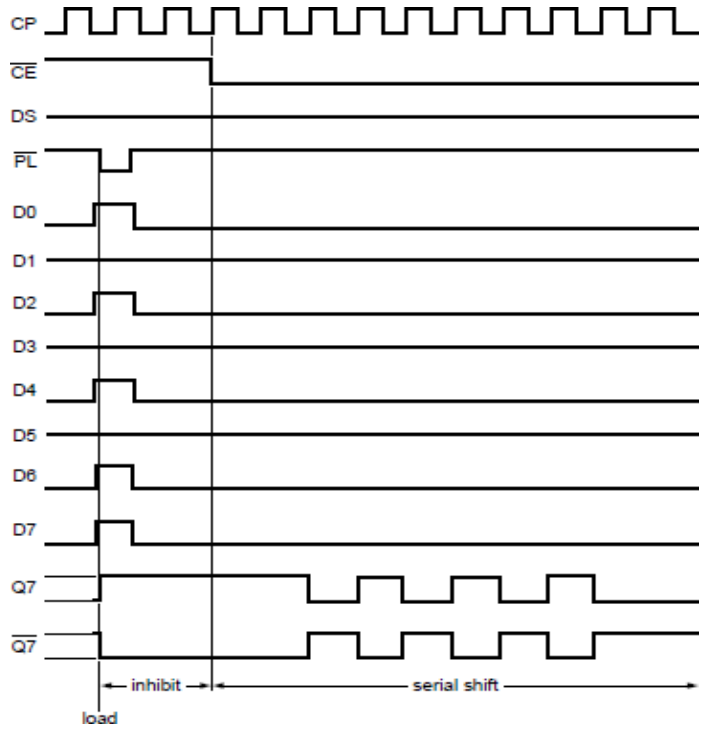
Logic symbol



IEC logic symbol



Functional diagram



Timing diagram

6. Electrical Parameter

Table 3. Absolute Maximum Ratings

(Voltages are referenced to GND(ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
Supply voltage	V_{CC}	-		-0.5	+7	V
Input clamping current	I_{IK}	$V_I < -0.5V$ or $V_I > V_{CC}+0.5V$		-	±20	mA
Output clamping current	I_{OK}	$V_O < -0.5V$ or $V_O > V_{CC}+0.5V$		-	±20	mA
Output current	I_O	$-0.5V < V_O < V_{CC}+0.5V$		-	±25	mA
Supply current	I_{CC}	-		-	50	mA
Ground current	I_{GND}	-		-50	-	mA
Total power dissipation	P_{tot}	-		-	500	mW
Storage temperature	T_{stg}	-		-65	+150	˚C
Soldering temperature	T_L	10s	DIP	245		˚C
			SOP	250		˚C

Note:

[1] For DIP16 packages: above 70˚C the value of P_{tot} derates linearly with 12mW/K.

[2] For SOP16 packages: above 70˚C the value of P_{tot} derates linearly with 8mW/K.

[3] For (T)SSOP16 packages: above 60˚C the value of P_{tot} derates linearly with 5.5mW/K.

Table 4. Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
74HC165						
Supply Voltage	V_{CC}	-	2.0	5.0	6.0	V
Input Voltage	V_I	-	0	-	V_{CC}	V
Output Voltage	V_O	-	0	-	V_{CC}	V
Input Transition Rise and Fall Rate	Δt/ΔV	V_{CC}=2.0V	-	-	625	ns/V
		V_{CC}=4.5V	-	1.67	139	ns/V
		V_{CC}=6.0V	-	-	83	ns/V
Ambient Temperature	T_{amb}	-	-40	-	+85	˚C
74HCT165						
Supply Voltage	V_{CC}	-	4.5	5.0	5.5	V
Input Voltage	V_I	-	0	-	V_{CC}	V
Output Voltage	V_O	-	0	-	V_{CC}	V
Input Transition Rise and Fall Rate	Δt/ΔV	V_{CC}=2.0V	-	-	-	ns/V
		V_{CC}=4.5V	-	1.67	139	ns/V
		V_{CC}=6.0V	-	-	-	ns/V

Ambient Temperature	T_{amb}	-	-40	-	+85	˚C

Table 5. DC Characteristics 1

(T_{amb}=25˚C, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
74HC165							
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	1.2	-	V
		V_{CC}=4.5V		3.15	2.4	-	V
		V_{CC}=6.0V		4.2	3.2	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	0.8	0.5	V
		V_{CC}=4.5V		-	2.1	1.35	V
		V_{CC}=6.0V		-	2.8	1.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	2.0	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	4.5	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	6.0	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.98	4.32	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.48	5.81	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	0	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	0	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	0	0.1	V
			I_O=4.0mA; V_{CC}=4.5V	-	0.15	0.26	V
			I_O=5.2mA; V_{CC}=6.0V	-	0.16	0.26	V
input leakage current	I_I	V_I= V_{CC} or GND; V_{CC}=6.0V		-	-	±0.1	uA
supply current	I_{CC}	V_I= V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	8	uA
input capacitance	C_I	-		-	3.5	-	pF
74HCT165							
HIGH-level input voltage	V_{IH}	V_{CC}=4.5V to 5.5V		2.0	1.6	-	V
LOW-level input voltage	V_{IL}	V_{CC}=4.5V to 5.5V		-	1.2	0.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=-20uA	4.4	4.5	-	V
			I_O=-4.0mA	3.98	4.32	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=4.5V	-	0	0.1	V
			I_O=5.2mA; V_{CC}=6.0V	-	0.16	0.26	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±0.1	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	8.0	uA
additional supply current	ΔI_{CC}	per input pin; V_I=V_{CC}-2.1V;	Dn and DS inputs	-	35	126	uA

		other inputs at V_{CC} or GND; V_{CC}=4.5V to 5.5V	— — CP, CE, and PL inputs	-	65	234	uA
input capacitance	C_I	-		-	3.5	-	pF

Table 6. DC Characteristics 2

(T_{amb}=-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
74HC165							
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	1.2	-	V
		V_{CC}=4.5V		3.15	2.4	-	V
		V_{CC}=6.0V		4.2	3.2	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	0.8	0.5	V
		V_{CC}=4.5V		-	2.1	1.35	V
		V_{CC}=6.0V		-	2.8	1.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	2.0	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	4.5	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	6.0	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.98	4.32	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.48	5.81	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	0	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	0	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	0	0.1	V
			I_O=4.0mA; V_{CC}=4.5V	-	0.15	0.26	V
			I_O=5.2mA; V_{CC}=6.0V	-	0.16	0.26	V
input leakage current	I_I	V_I= V_{CC} or GND; V_{CC}=6.0V		-	-	±0.1	uA
supply current	I_{CC}	V_I= V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	8	uA
input capacitance	C_I	-		-	3.5	-	pF
74HCT165							
HIGH-level input voltage	V_{IH}	V_{CC}=4.5V to 5.5V		2.0	1.6	-	V
LOW-level input voltage	V_{IL}	V_{CC}=4.5V to 5.5V		-	1.2	0.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=-20uA	4.4	4.5	-	V
			I_O=-4.0mA	3.98	4.32	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=4.5V	-	0	0.1	V
			I_O=5.2mA; V_{CC}=6.0V	-	0.16	0.26	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±0.1	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	8.0	uA

additional supply current	ΔI_{CC}	per input pin; $V_I=V_{CC}$-2.1V; other inputs at V_{CC} or GND; V_{CC}=4.5V to 5.5V	Dn and DS inputs	-	35	126	uA
			$\overline{CP}$, $\overline{CE}$, and $\overline{PL}$ inputs	-	65	234	uA
input capacitance	C_I	-		-	3.5	-	pF

Table 7. AC Characteristics 1

(T_{amb}=25°C, GND=0V, CL=50pf, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
74HC165							
propagation delay	t_{pd}	CP, $\overline{CE}$ to Q7, $\overline{Q7}$; see Figure 6	V_{CC}=2.0V	-	52	165	ns
			V_{CC}=4.5V	-	19	33	ns
			V_{CC}=5.0V; C_L=15pF	-	16	-	ns
			V_{CC}=6.0V	-	15	28	ns
		$\overline{PL}$ to Q7, $\overline{Q7}$; see Figure 7	V_{CC}=2.0V	-	50	165	ns
			V_{CC}=4.5V	-	18	33	ns
			V_{CC}=5.0V; C_L=15pF	-	15	-	ns
			V_{CC}=6.0V	-	14	28	ns
		D7 to Q7, $\overline{Q7}$; see Figure 8	V_{CC}=2.0V	-	36	120	ns
			V_{CC}=4.5V	-	13	24	ns
			V_{CC}=5.0V; C_L=15pF	-	11	-	ns
			V_{CC}=6.0V	-	10	20	ns
transition time	t_t	Q7, $\overline{Q7}$ output; see Figure 6	V_{CC}=2.0V	-	19	75	ns
			V_{CC}=4.5V	-	7	15	ns
			V_{CC}=6.0V	-	6	13	ns
pulse width	t_W	CP input HIGH or LOW; see Figure 6	V_{CC}=2.0V	80	17	-	ns
			V_{CC}=4.5V	16	6	-	ns
			V_{CC}=6.0V	14	5	-	ns
		$\overline{PL}$ input LOW; see Figure 7	V_{CC}=2.0V	80	14	-	ns
			V_{CC}=4.5V	16	5	-	ns
			V_{CC}=6.0V	14	4	-	ns
recovery time	t_{rec}	$\overline{PL}$ to CP, $\overline{CE}$; see Figure 7	V_{CC}=2.0V	100	22	-	ns
			V_{CC}=4.5V	20	8	-	ns
			V_{CC}=6.0V	17	6	-	ns
set-up time	t_{su}	DS to CP, $\overline{CE}$; see Figure 9	V_{CC}=2.0V	80	11	-	ns
			V_{CC}=4.5V	16	4	-	ns
			V_{CC}=6.0V	14	3	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$;	V_{CC}=2.0V	80	17	-	ns

		see Figure 9	V_{CC}=4.5V	16	6	-	ns
			V_{CC}=6.0V	14	5	-	ns
		Dn to $\overline{PL}$; see Figure 10	V_{CC}=2.0V	80	22	-	ns
			V_{CC}=4.5V	16	8	-	ns
			V_{CC}=6.0V	14	6	-	ns
hold time	t_h	DS to CP, CE and Dn to $\overline{PL}$; see Figure 9	V_{CC}=2.0V	5	2	-	ns
			V_{CC}=4.5V	5	2	-	ns
			V_{CC}=6.0V	5	2	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$; see Figure 9	V_{CC}=2.0V	5	-17	-	ns
			V_{CC}=4.5V	5	-6	-	ns
			V_{CC}=6.0V	5	-5	-	ns
maximum frequency	f_{max}	CP input; see Figure 6	V_{CC}=2.0V	6	17	-	MHz
			V_{CC}=4.5V	30	51	-	MHz
			V_{CC}=5.0V;C_L=15pF	-	56	-	MHz
			V_{CC}=6.0V	35	61	-	MHz
Power dissipation capacitance	C_{PD}	per package; V_I= GND to V_{CC}	-	35	-	pF	
74HCT165							
propagation delay	t_{pd}	CP, $\overline{CE}$ to Q7, $\overline{Q7}$; see Figure 6	V_{CC}=4.5V	-	17	34	ns
			V_{CC}=5.0V;C_L=15pF	-	14	-	ns
		$\overline{PL}$ to Q7, $\overline{Q7}$; see Figure 7	V_{CC}=4.5V	-	20	40	ns
			V_{CC}=5.0V;C_L=15pF	-	17	-	ns
		$\overline{PL}$ to Q7, $\overline{Q7}$; see Figure 7	V_{CC}=4.5V	-	14	28	ns
			V_{CC}=5.0V;C_L=15pF	-	11	-	ns
transition time	t_t	Q7, $\overline{Q7}$ output; see Figure 6	V_{CC}=4.5V	-	7	15	ns
pulse width	t_W	CP input; see Figure 6	V_{CC}=4.5V	16	6	-	ns
		$\overline{PL}$ input; see Figure 7	V_{CC}=4.5V	20	9	-	ns
recovery time	t_{rec}	$\overline{PL}$ to CP, $\overline{CE}$; see Figure 7	V_{CC}=4.5V	20	8	-	ns
set-up time	t_{su}	DS to CP, $\overline{CE}$; see Figure 9	V_{CC}=4.5V	20	2	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$; see Figure 9	V_{CC}=4.5V	20	7	-	ns
		Dn to $\overline{PL}$; see Figure 10	V_{CC}=4.5V	20	10	-	ns
hold time	t_h	DS to CP, CE and Dn to $\overline{PL}$; see Figure 9	V_{CC}=4.5V	7	-1	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$; see Figure 9	V_{CC}=4.5V	0	-7	-	ns
maximum frequency	f_{max}	CP input; see Figure 6	V_{CC}=4.5V	26	44	-	MHz
			V_{CC}=5.0V;C_L=15pF	-	48	-	MHz
Power dissipation capacitance	C_{PD}	per package; V_I= GND to V_{CC}-1.5V	-	35	-	pF	

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_t is the same as t_{THL} and t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D=(C_{PD}\times V_{CC}^2\times f_i\times N)+\Sigma(C_L\times V_{CC}^2\times f_o)$ where:

fi=input frequency in MHz;

fo=output frequency in MHz;

CL=output load capacitance in pF;

V_{CC}=supply voltage in V;

N=number of inputs switching;

$\Sigma(C_L\times V_{CC}^2\times f_o)$=sum of outputs.

Table 8. AC Characteristics 2

(Tamb=-40°C to +85°C, GND=0V, CL=50pf, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
74HC165							
propagation delay	t_{pd}	CP, $\overline{CE}$ to Q7, $\overline{Q7}$; see Figure 6	V_{CC}=2.0V	-	-	205	ns
			V_{CC}=4.5V	-	-	41	ns
			V_{CC}=6.0V	-	-	35	ns
		$\overline{PL}$ to Q7, $\overline{Q7}$; see Figure 7	V_{CC}=2.0V	-	-	205	ns
			V_{CC}=4.5V	-	-	41	ns
			V_{CC}=6.0V	-	-	35	ns
		D7 to Q7, $\overline{Q7}$; see Figure 8	V_{CC}=2.0V	-	-	150	ns
			V_{CC}=4.5V	-	-	30	ns
			V_{CC}=6.0V	-	-	26	ns
transition time	t_t	Q7, $\overline{Q7}$ output; see Figure 6	V_{CC}=2.0V	-	-	95	ns
			V_{CC}=4.5V	-	-	19	ns
			V_{CC}=6.0V	-	-	16	ns
pulse width	t_W	CP input HIGH or LOW; see Figure 6	V_{CC}=2.0V	100	-	-	ns
			V_{CC}=4.5V	20	-	-	ns
			V_{CC}=6.0V	17	-	-	ns
		$\overline{PL}$ input LOW; see Figure 7	V_{CC}=2.0V	100	-	-	ns
			V_{CC}=4.5V	20	-	-	ns
			V_{CC}=6.0V	17	-	-	ns
recovery time	t_{rec}	$\overline{PL}$ to CP, $\overline{CE}$; see Figure 7	V_{CC}=2.0V	125	-	-	ns
			V_{CC}=4.5V	25	-	-	ns
			V_{CC}=6.0V	21	-	-	ns
set-up time	t_{su}	DS to CP, $\overline{CE}$; see Figure 9	V_{CC}=2.0V	100	-	-	ns
			V_{CC}=4.5V	20	-	-	ns
			V_{CC}=6.0V	17	-	-	ns

		$\overline{CE}$ to CP and CP to $\overline{CE}$; see Figure 9	V_{CC}=2.0V	100	-	-	ns
			V_{CC}=4.5V	20	-	-	ns
			V_{CC}=6.0V	17	-	-	ns
		Dn to $\overline{PL}$; see Figure 10	V_{CC}=2.0V	100	-	-	ns
			V_{CC}=4.5V	20	-	-	ns
			V_{CC}=6.0V	17	-	-	ns
hold time	t_h	DS to CP, CE and Dn to $\overline{PL}$; see Figure 9	V_{CC}=2.0V	5	-	-	ns
			V_{CC}=4.5V	5	-	-	ns
			V_{CC}=6.0V	5	-	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$; see Figure 9	V_{CC}=2.0V	5	-	-	ns
			V_{CC}=4.5V	5	-	-	ns
			V_{CC}=6.0V	5	-	-	ns
maximum frequency	f_{max}	CP input; see Figure 6	V_{CC}=2.0V	5	-	-	MHz
			V_{CC}=4.5V	24	-	-	MHz
			V_{CC}=6.0V	28	-	-	MHz
74HCT165							
propagation delay	t_{pd}	CP, $\overline{CE}$ to Q7, $\overline{Q7}$; see Figure 6	V_{CC}=4.5V	-	-	43	ns
		$\overline{PL}$ to Q7, $\overline{Q7}$; see Figure 7	V_{CC}=4.5V	-	-	50	ns
		$\overline{PL}$ to Q7, $\overline{Q7}$; see Figure 7	V_{CC}=4.5V	-	-	35	ns
transition time	t_t	Q7, $\overline{Q7}$ output; see Figure 6	V_{CC}=4.5V	-	-	19	ns
pulse width	t_w	CP input; see Figure 6	V_{CC}=4.5V	20	-	-	ns
		$\overline{PL}$ input; see Figure 7	V_{CC}=4.5V	25	-	-	ns
recovery time	t_{rec}	$\overline{PL}$ to CP, $\overline{CE}$; see Figure 7	V_{CC}=4.5V	25	-	-	ns
set-up time	t_{su}	$\overline{CE}$ to CP and CP to $\overline{CE}$; see Figure 9	V_{CC}=4.5V	25	-	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$; see Figure 9	V_{CC}=4.5V	25	-	-	ns
		Dn to $\overline{PL}$; see Figure 10	V_{CC}=4.5V	25	-	-	ns
hold time	t_h	DS to CP, CE and Dn to $\overline{PL}$; see Figure 9	V_{CC}=4.5V	9	-	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$; see Figure 9	V_{CC}=4.5V	0	-	-	ns
maximum frequency	f_{max}	CP input; see Figure 6	V_{CC}=4.5V	21	-	-	MHz

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_t is the same as t_{THL} and t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D=(C_{PD}\times V_{CC}^2\times f_i\times N)+\Sigma(C_L\times V_{CC}^2\times f_o)$ where:

fi=input frequency in MHz;

fo=output frequency in MHz;

CL=output load capacitance in pF;

V_{CC}=supply voltage in V;

N=number of inputs switching;

$\Sigma(C_L\times V_{CC}^2\times f_o)$=sum of outputs.

7. Testing Circuit

AC Testing Circuit

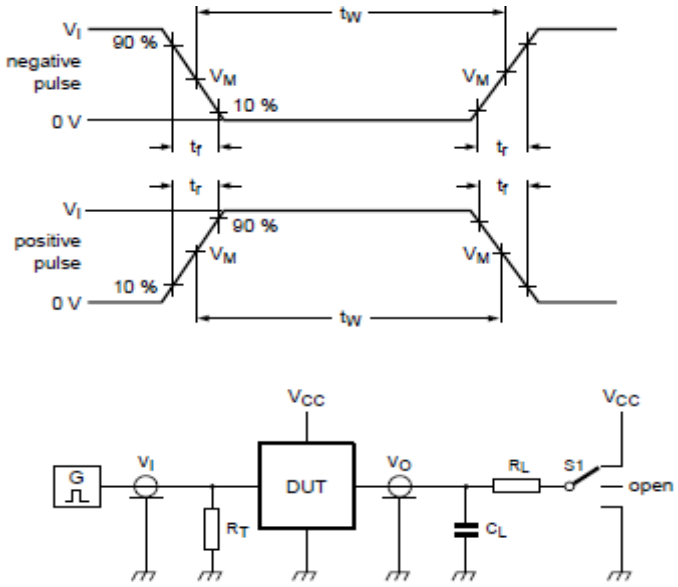


Fig. 2. Test circuit for measuring switching times

Definitions for test circuit:

C_L=load capacitance including jig and probe capacitance.

R_T=termination resistance should be equal to the output impedance Z_o of the pulse generator.

R_L=Load resistance.

S1=Test selection switch.

AC Testing Waveforms

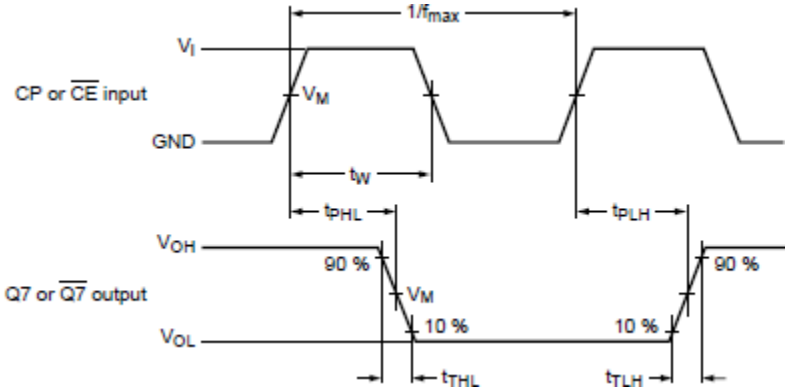


Fig. 3. The clock (CP) or clock enable (CE) to output (Q7 or Q7) propagation delays, the clock pulse width, the maximum clock frequency and the output transition times

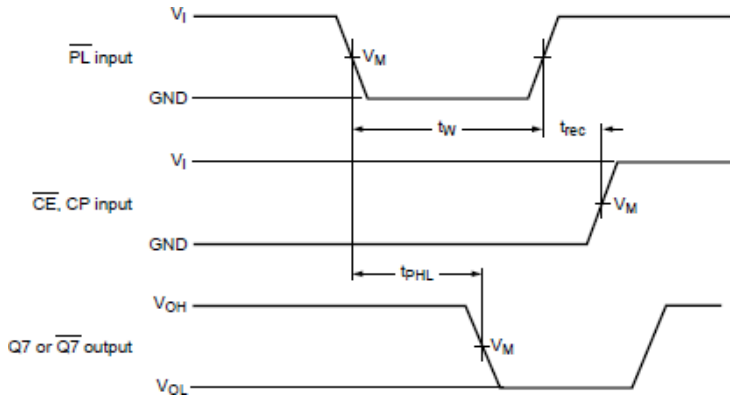


Fig. 4. The parallel load (PL) pulse width, the parallel load to output (Q7 or Q7) propagation delays, the parallel load to clock (CP) and clock enable (CE) recovery time

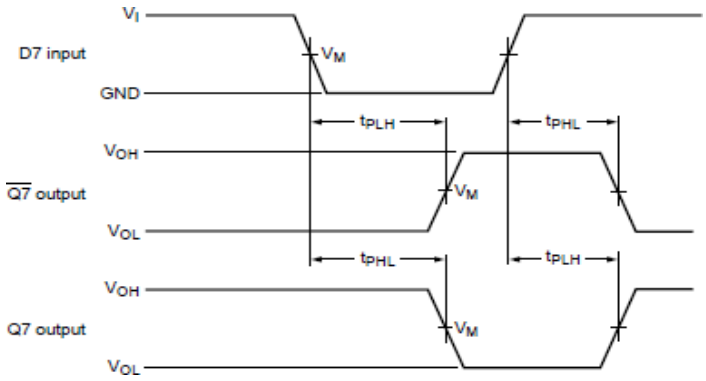
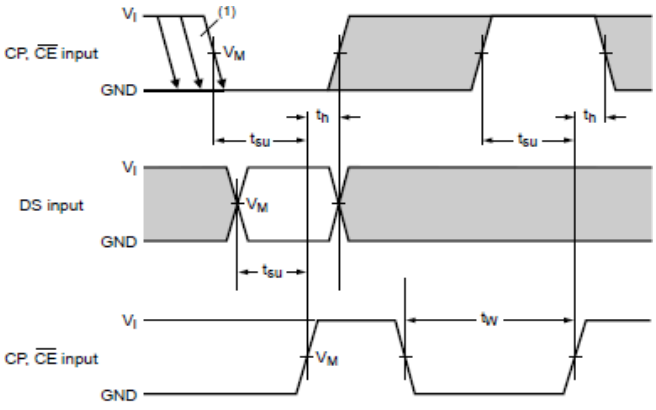


Fig. 5. The data input (D7) to output (Q7 or Q7) propagation delays when PL is LOW



(1) $\overline{CE}$ may change only from HIGH-to-LOW while CP is LOW.

Fig. 6. The set-up and hold times from the serial data input (DS) to the clock (CP) and clock enable (CE) inputs, from the clock enable input (CE) to the clock input (CP) and from the clock input (CP) to the clock enable input (CE)

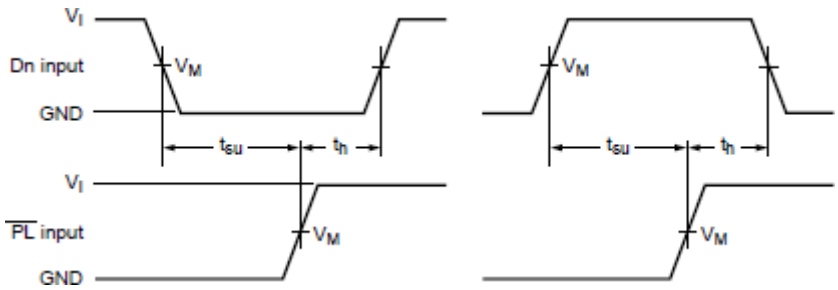


Fig. 7. The set-up and hold times from the data inputs (Dn) to the parallel load input (PL)

Measurement Points

Type	Input		Output
	V_I	V_M	V_M
74HC165	V_{CC}	$0.5\times V_{CC}$	$0.5\times V_{CC}$
74HCT165	3V	1.3V	1.3V

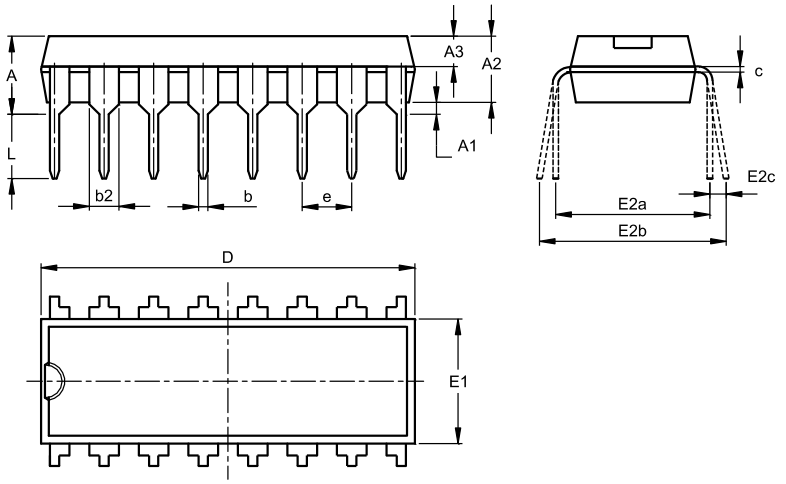
Test Data

Type	Input		Load		S1 position
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
74HC165	^{V}CC	6.0ns	15pF, 50pF	1kΩ	open
74HCT165	3.0V	6.0ns	15pF, 50pF	1kΩ	open

8. Package Information

DIP-16

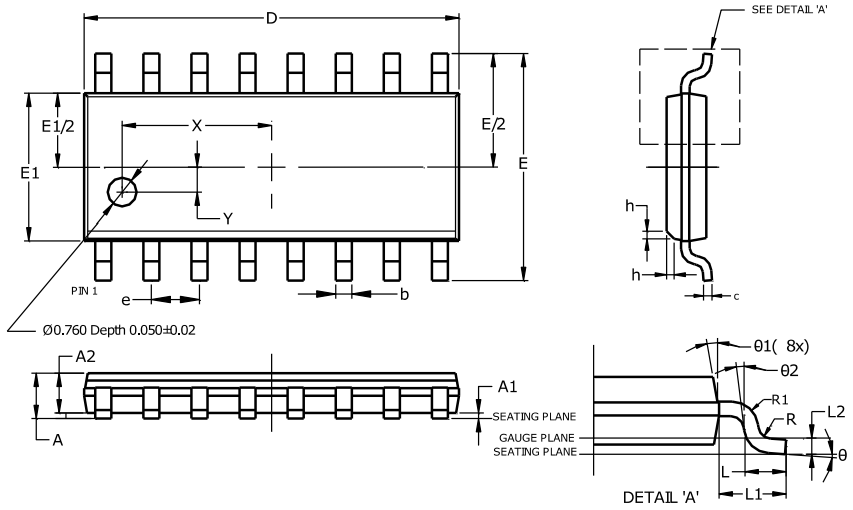
PDIP-16



PDIP-16			
Dim	Min	Max	Nom
A	3.60	4.00	3.80
A1	0.51	-	
A2	3.20	3.40	3.30
A3	1.47	1.57	1.52
b	0.44	0.53	–
b2	1.52BSC		
c	0.25	0.31	–
D	18.90	19.30	19.10
E1	6.15	6.55	6.35
E2a	7.62 BSC		
E2b	7.62	9.30	–
E2c	0.00	0.84	–
e	2.54BSC		
L	3.00	–	–
All Dimensions in mm			

SOP-16

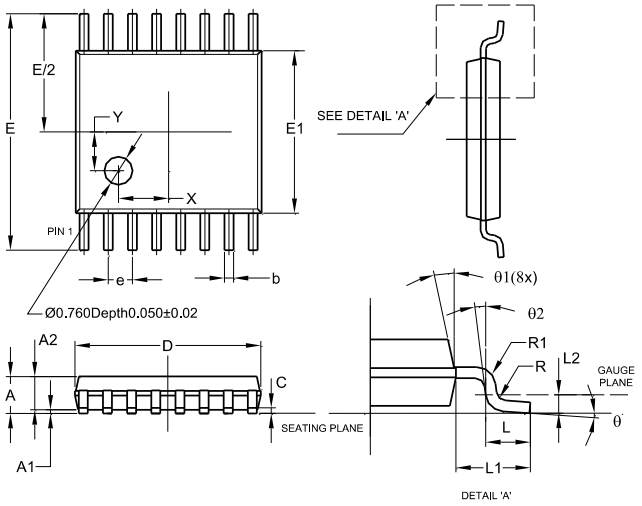
SOP-16



SOP-16			
Dim	Min	Max	Typ
A	--	1.260	--
A1	0.10	0.23	--
A2	1.02	--	--
b	0.31	0.51	--
c	0.10	0.25	--
D	9.80	10.00	--
E	5.90	6.10	--
E1	3.80	4.00	--
e	1.27 BSC		
h	0.15	0.25	0.20
L	0.40	1.27	--
L1	1.04 REF		
L2	0.25 BSC		
R	0.07	--	--
R1	0.07	--	--
X	3.945 REF		
Y	0.661 REF		
θ	0°	8°	--
θ1	5°	15°	--
θ2	0°	--	--
All Dimensions in mm			

TSSOP-16

TSSOP-16



TSSOP-16			
Dim	**Min**	**Max**	**Typ**
A	-	1.08	-
A1	0.05	0.15	-
A2	0.80	0.93	-
b	0.19	0.30	-
c	0.09	0.20	-
D	4.90	5.10	-
E	6.40 BSC		
E1	4.30	4.50	-
e	0.65 BSC		
L	0.45	0.75	-
L1	1.00 REF		
L2	0.25 BSC		
R / R1	0.09	-	-
X	-	-	1.350
Y	-	-	1.050
θ	0°	8°	-
θ1	5°	15°	-
θ2	0°	-	-
All Dimensions in mm			

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