8-bit Serial-in, Serial or Parallel-out Shift Register with Output Latches; 3-state

1. Description

The 74HC/HCT595 is an 8-bit serial-in/serial or parallel-out shift register with a storage register and 3-state outputs. Both the shift and storage register have separate clocks. The device features a serial input (DS) and a serial output (Q7S) to enable cascading and an asynchronous reset $\overline{MR}$ input. A LOW on $\overline{MR}$ will reset the shift register. Data is shifted on the LOW-to-HIGH transitions of the SHCP input. The data in the shift register is transferred to the storage register on a LOW-to-HIGH transition of the STCP input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register. Data in the storage register appears at the output whenever the output enable input ($\overline{OE}$) is LOW. A HIGH on $\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the registers. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features

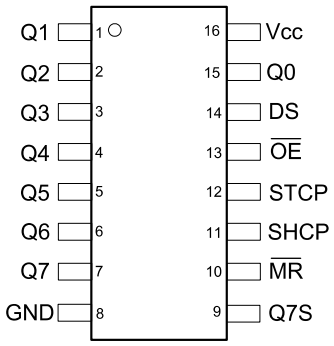
- Input levels:
  - For 74HC595: CMOS level
  - For 74HCT595: TTL level
- 8-bit serial input
- 8-bit serial or parallel output
- Storage register with 3-state outputs
- Shift register with direct clear
- Specified from -40˚C to +125˚C
- Packaging information:
  DIP16/SOIC16/TSSOP16

3. Ordering Information

Type Number	Package Type	Packing	SPQ
74HC595N	DIP-16	Tube	
74HC595D	SOIC-16	Reel	
74HC595PW	TSSOP-16	Reel	
74HCT595N	DIP-16	Tube	
74HCT595D	SOIC-16	Reel	
74HCT595PW	TSSOP-16	Reel	

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

4. Pin Assignments



5. Pin Descriptions

Pin No.	Pin Name	Description
1	Q1	parallel data output
2	Q2	parallel data output
3	Q3	parallel data output
4	Q4	parallel data output
5	Q5	parallel data output
6	Q6	parallel data output
7	Q7	parallel data output
8	GND	ground (0V)
9	Q7S	serial data output
10	$\overline{MR}$	master reset (active LOW)
11	SHCP	shift register clock input
12	STCP	storage register clock input
13	$\overline{OE}$	output enable input (active LOW)
14	DS	serial data input
15	Q0	parallel data output
16	V_{CC}	supply voltage

6. Block Diagram And Pin Description

Block Diagram

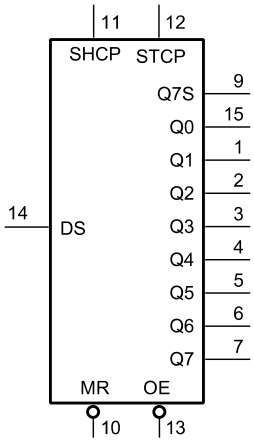


Fig. 1. Logic symbol

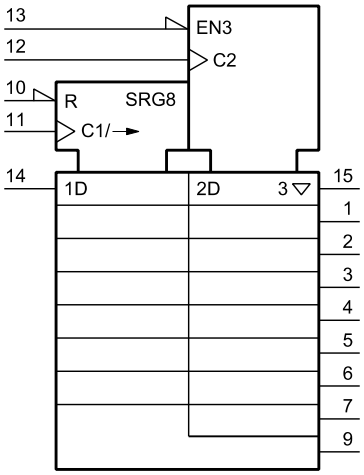


Fig. 2. IEC logic symbol

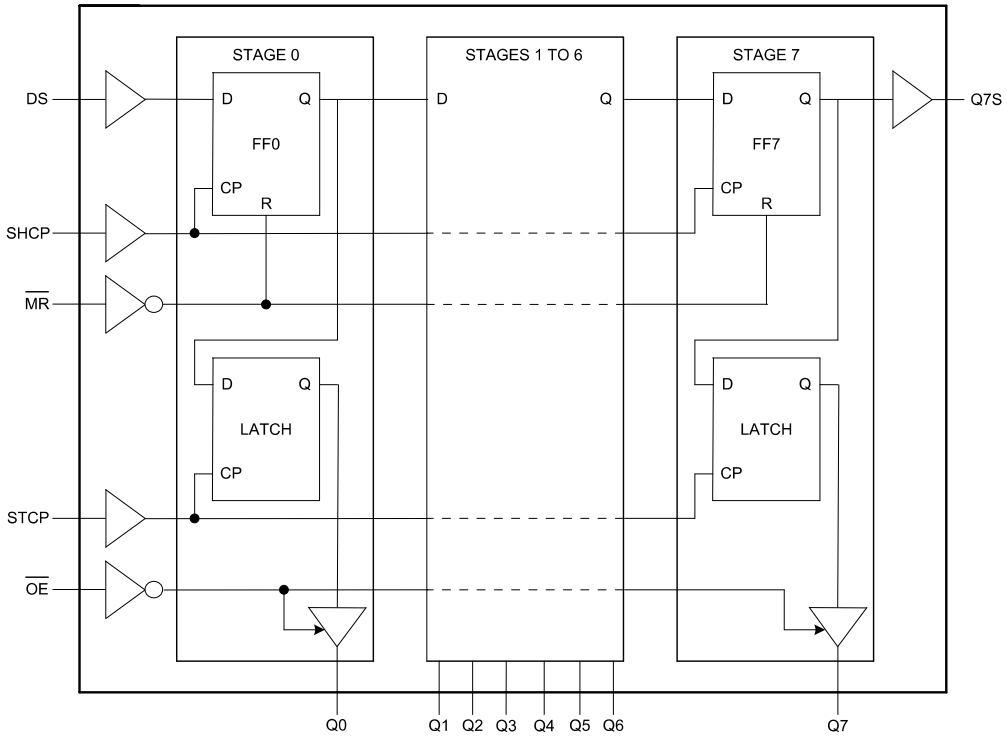


Fig. 3. Logic Diagram

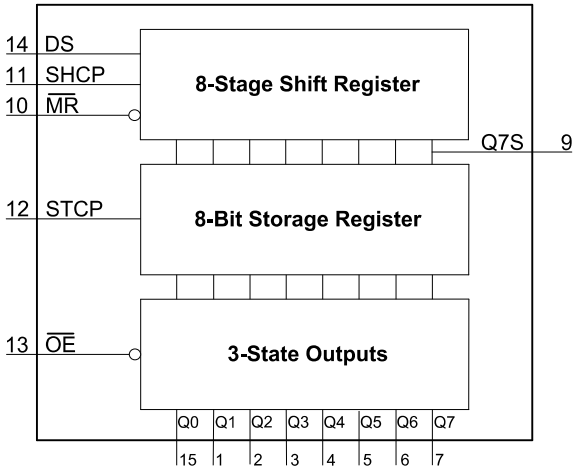


Fig. 4. Functional Diagram

7. Functional Description

Control				Input	Output		Function
SHCP	STCP	$\overline{OE}$	$\overline{MR}$	DS	Q7S	Qn	
X	X	L	L	X	L	NC	a LOW-level on MR only affects the shift registers
X	↑	L	L	X	L	L	empty shift register loaded into storage register
X	X	H	L	X	L	Z	shift register clear; parallel outputs in high-impedance OFF-state
↑	X	L	H	H	Q6S	NC	logic HIGH-level shifted into shift register stage 0. Contents of all shift register stages shifted through, eg. previous state of stage 6 (internal Q6S) appears on the serial output (Q7S)

X	↑	L	H	X	NC	QnS	contents of shift register stages (internal QnS) are transferred to the storage register and parallel output stages
↑	↑	L	H	X	Q6S	QnS	contents of shift register shifted through; previous contents of the shift register is transferred to the storage register and the parallel output stages

H=HIGH Voltage State

L=LOW Voltage State

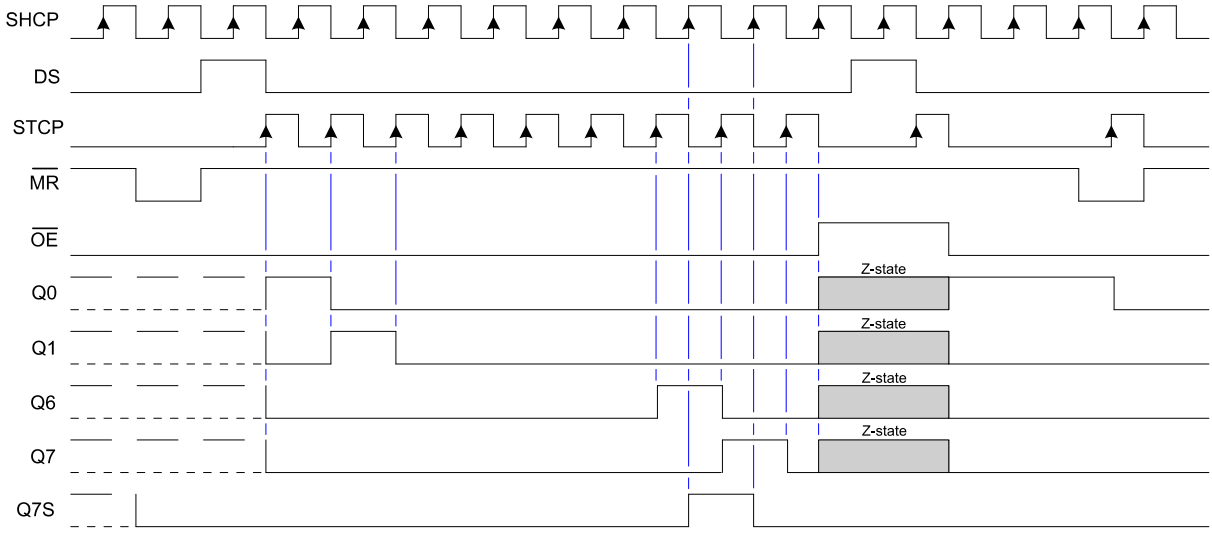
↑=LOW to HIGH Transition

X= Don'T Care – High or Low (Not Floating)

NC= No Change

Z= High-Impedance State

8. Timing Diagram



9. Electrical Parameter

Absolute Maximum Ratings

(Voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V_{CC}	-		-0.5	+7.0	V
input clamping current	I_{IK}	$V_I < -0.5V$ or $V_I > V_{CC}+0.5V$		-	±20	mA
output clamping current	I_{OK}	$V_O < -0.5V$ or $V_O > V_{CC}+0.5V$		-	±20	mA
output current	I_O	V_O= -0.5V to (V_{CC}+0.5V)	pin Q7S	-	±25	mA
			pins Qn	-	±35	mA
supply current	I_{CC}	-		-	70	mA
ground current	I_{GND}	-		-70	-	mA
storage temperature	T_{stg}	-		-65	+150	˚C
total power dissipation	P_{tot}	-		-	500	mW
soldering temperature	T_L	10s	DIP	245		˚C
			SOIC/TSSOP	260		˚C

10. Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
74HC595						
supply voltage	V_{CC}	-	2.0	5.0	6.0	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
ambient temperature	T_{amb}	-	-40	-	+125	˚C
74HCT595						
supply voltage	V_{CC}	-	4.5	5.0	5.5	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
ambient temperature	T_{amb}	-	-40	-	+125	˚C

11. Electrical Characteristics

DC Characteristics 1

(T_{amb}=-40˚C to +85˚C, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
74HC595							
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	1.2	-	V
		V_{CC}=4.5V		3.15	2.4	-	V
		V_{CC}=6.0V		4.2	3.2	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	0.8	0.5	V
		V_{CC}=4.5V		-	1.35	1.0	V
		V_{CC}=6.0V		-	1.8	1.5	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	all outputs; I_O=-20uA; V_{CC}=2.0V	1.9	2.0	-	V
			all outputs; I_O=-20uA; V_{CC}=4.5V	4.4	4.5	-	V
			all outputs; I_O=-20uA; V_{CC}=6.0V	5.9	6.0	-	V
			Q7S output; I_O=-4.0mA; V_{CC}=4.5V	3.84	4.32	-	V
			Q7S output; I_O=-5.2mA; V_{CC}=6.0V	5.34	5.81	-	V
			Qn bus driver outputs; I_O=-6.0mA; V_{CC}=4.5V	3.84	4.32	-	V
			Qn bus driver outputs; I_O=-7.8mA; V_{CC}=6.0V	5.34	5.81	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	all outputs; I_O=20uA; V_{CC}=2.0V	-	0	0.1	V
			all outputs; I_O=20uA; V_{CC}=4.5V	-	0	0.1	V
			all outputs; I_O=20uA; V_{CC}=6.0V	-	0	0.1	V
			Q7S output; I_O=4.0mA; V_{CC}=4.5V	-	0.15	0.33	V
			Q7S output; I_O=5.2mA; V_{CC}=6.0V	-	0.16	0.33	V
			Qn bus driver outputs; I_O=6.0mA; V_{CC}=4.5V	-	0.15	0.33	V

			Qn bus driver outputs; I_O=7.8mA; V_{CC}=6.0V	-	0.16	0.33	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
input leakage current	I_I	V_I=V_{IH} or V_{IL}; V_{CC}=6.0V; V_O=V_{CC} or GND		-	-	±5.0	uA
OFF-state output current	I_{OZ}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	80	uA
input capacitance	C_I	-		-	3.5	-	pF
74HCT595							
HIGH-level input voltage	V_{IH}	V_{CC}=4.5V to 5.5V		2.0	1.6	-	V
LOW-level input voltage	V_{IL}	V_{CC}=4.5V to 5.5V		-	1.2	0.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	all outputs; I_O=-20uA	4.4	4.5	-	V
			Q7S output; I_O=-4.0mA	3.84	4.32	-	V
			Qn bus driver outputs; I_O=-6.0mA	3.7	4.32	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	all outputs; I_O=20uA	-	0	0.1	V
			Q7S output; I_O=4.0mA	-	0.15	0.33	V
			Qn bus driver outputs; I_O=6.0mA	-	0.16	0.33	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±1.0	uA
OFF-state output current	I_{OZ}	V_I=V_{IH} or V_{IL}; V_{CC}=5.5V; V_O=V_{CC} or GND		-	-	±5.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	80	uA
additional supply current	ΔI_{CC}	per input pin; V_I=V_{CC}-2.1V; other inputs at V_{CC} or GND; I_O=0A; V_{CC}=4.5V to 5.5V	pins $\overline{MR}$, SHCP, STCP, $\overline{OE}$	-	150	675	uA
			pin DS	-	25	113	uA
input capacitance	C_I	-		-	3.5	-	pF

12. DC Characteristics 2

(T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
74HC595							
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.0	V
		V_{CC}=6.0V		-	-	1.5	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	all outputs; I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
			all outputs; I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			all outputs; I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
			Q7S output; I_O=-4.0mA; V_{CC}=4.5V	3.7	-	-	V
			Q7S output; I_O=-5.2mA; V_{CC}=6.0V	5.2	-	-	V
			Qn bus driver outputs; I_O=-6.0mA; V_{CC}=4.5V	3.7	-	-	V
			Qn bus driver outputs; I_O=-7.8mA; V_{CC}=6.0V	5.2	-	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	all outputs; I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
			all outputs; I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			all outputs; IO=20uA; V_{CC}=6.0V	-	-	0.1	V
			Q7S output; IO=4.0mA; V_{CC}=4.5V	-	-	0.4	V
			Q7S output; IO=5.2mA; V_{CC}=6.0V	-	-	0.4	V
			Qn bus driver outputs; IO=6.0mA; V_{CC}=4.5V	-	-	0.4	V
			Qn bus driver outputs; IO=7.8mA; V_{CC}=6.0V	-	-	0.4	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
OFF-state output current	I_{OZ}	V_I=V_{IH} or V_{IL}; V_{CC}=6.0V; V_O=V_{CC} or GND		-	-	±10	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	160	uA
74HCT595							
HIGH-level input voltage	V_{IH}	V_{CC}=4.5V to 5.5V		2.0	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=4.5V to 5.5V		-	-	0.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	all outputs; I_O=-20uA	4.4	-	-	V
			Q7S output; I_O=-4.0mA	3.7	-	-	V

			Qn bus driver outputs; I_O=-6.0mA	3.7	-	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	all outputs; I_O=20uA	-	-	0.1	V
			Q7S output; I_O=4.0mA	-	-	0.4	V
			Qn bus driver outputs; I_O=6.0mA	-	-	0.4	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±1.0	uA
OFF-state output current	I_{OZ}	V_I=V_{IH} or V_{IL}; V_{CC}=5.5V; V_O=V_{CC} or GND		-	-	±10	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	160	uA
additional supply current	ΔI_{CC}	per input pin; V_I=V_{CC}-2.1V; other inputs at V_{CC} or GND; I_O=0A; V_{CC}=4.5V to 5.5V	pins $\overline{MR}$, SHCP, STCP, $\overline{OE}$	-	-	735	uA
			pin DS	-	-	123	uA

AC Characteristics 1

(T_{amb}=25°C, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.[1]	Max.	Unit
74HC595							
propagation delay	t_{PLH}, t_{PHL}	SHCP to Q7S; see Figure 6	V_{CC}=2.0V	-	75	160	ns
			V_{CC}=4.5V	-	19	32	ns
			V_{CC}=6.0V	-	15	27	ns
		STCP to Qn; see Figure 7	V_{CC}=2.0V	-	85	175	ns
			V_{CC}=4.5V	-	20	35	ns
			V_{CC}=6.0V	-	16	30	ns
HIGH to LOW propagation delay	t_{PHL}	$\overline{MR}$ to Q7S; see Figure 9	V_{CC}=2.0V	-	47	175	ns
			V_{CC}=4.5V	-	17	35	ns
			V_{CC}=6.0V	-	14	30	ns
$\overline{OE}$ to Qn enable time	t_{PZH}, t_{PZL}	see Figure 10	V_{CC}=2.0V	-	47	150	ns
			V_{CC}=4.5V	-	17	30	ns
			V_{CC}=6.0V	-	14	26	ns
$\overline{OE}$ to Qn disable time	t_{PLZ}, t_{PHZ}	see Figure 10	V_{CC}=2.0V	-	41	150	ns
			V_{CC}=4.5V	-	15	30	ns
			V_{CC}=6.0V	-	12	27	ns
pulse width	t_W	SHCP HIGH or LOW; see Figure 6	V_{CC}=2.0V	75	17	-	ns
			V_{CC}=4.5V	15	6	-	ns
			V_{CC}=6.0V	13	5	-	ns
		STCP HIGH or LOW; see Figure 7	V_{CC}=2.0V	75	11	-	ns
			V_{CC}=4.5V	15	4	-	ns
			V_{CC}=6.0V	13	3	-	ns
		$\overline{MR}$ LOW; see Figure 9	V_{CC}=2.0V	75	17	-	ns
			V_{CC}=4.5V	15	6	-	ns

			V_{CC}=6.0V	13	5	-	ns
set-up time	t_{su}	DS to SHCP; see Figure 8	V_{CC}=2.0V	50	11	-	ns
			V_{CC}=4.5V	10	4	-	ns
			V_{CC}=6.0V	9	3	-	ns
		SHCP to STCP; see Figure 7	V_{CC}=2.0V	75	22	-	ns
			V_{CC}=4.5V	15	8	-	ns
			V_{CC}=6.0V	13	7	-	ns
DS to SHCP hold time	t_h	see Figure 8	V_{CC}=2.0V	3	-6	-	ns
			V_{CC}=4.5V	3	-2	-	ns
			V_{CC}=6.0V	3	-2	-	ns
$\overline{MR}$ to SHCP recovery time	t_{rec}	see Figure 9	V_{CC}=2.0V	50	-19	-	ns
			V_{CC}=4.5V	10	-7	-	ns
			V_{CC}=6.0V	9	-6	-	ns
maximum frequency	f_{max}	SHCP or STCP; see Figure 6 and Figure 7	V_{CC}=2.0V	9	-	-	MHz
			V_{CC}=4.5V	30	-	-	MHz
			V_{CC}=6.0V	35	-	-	MHz
74HCT595; V_{CC}=4.5V to 5.5V							
Propagation delay	t_{PLH}, t_{PHL}	SHCP to Q7S; see Figure 6		-	25	42	ns
		STCP to Qn; see Figure 7		-	24	40	ns
HIGH to LOW propagation delay	t_{PHL}	$\overline{MR}$ to Q7S; see Figure 9		-	23	40	ns
$\overline{OE}$ to Qn enable time	t_{PZH}, t_{PZL}	see Figure 10		-	21	35	ns
$\overline{OE}$ to Qn disable time	t_{PLZ}, t_{PHZ}	see Figure 10		-	18	30	ns
pulse width	t_W	SHCP HIGH or LOW; see Figure 6		16	6	-	ns
		STCP HIGH or LOW; see Figure 7		16	5	-	ns
		$\overline{MR}$ LOW; see Figure 9		20	8	-	ns
set-up time	t_{su}	DS to SHCP; see Figure 8		16	5	-	ns
		SHCP to STCP; see Figure 7		16	8	-	ns
DS to SHCP hold time	t_h	see Figure 8		3	-2	-	ns
$\overline{MR}$ to SHCP recovery time	t_{rec}	see Figure 9		10	-7	-	ns
maximum frequency	f_{max}	SHCP or STCP; see Figure 6 and Figure 7		30	-	-	MHz

Note: [1] Typical values are measured at nominal supply voltage.

AC Characteristics 2

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
74HC595							
propagation delay	t_{PLH}, t_{PHL}	SHCP to Q7S; see Figure 6	V_{CC}=2.0V	-	-	200	ns
			V_{CC}=4.5V	-	-	40	ns
			V_{CC}=6.0V	-	-	34	ns
		STCP to Qn; see Figure 7	V_{CC}=2.0V	-	-	220	ns
			V_{CC}=4.5V	-	-	44	ns
			V_{CC}=6.0V	-	-	37	ns
HIGH to LOW propagation delay	t_{PHL}	$\overline{MR}$ to Q7S; see Figure 9	V_{CC}=2.0V	-	-	220	ns
			V_{CC}=4.5V	-	-	44	ns
			V_{CC}=6.0V	-	-	37	ns
$\overline{OE}$ to Qn enable time	t_{PZH}, t_{PZL}	see Figure 10	V_{CC}=2.0V	-	-	190	ns
			V_{CC}=4.5V	-	-	38	ns
			V_{CC}=6.0V	-	-	33	ns
$\overline{OE}$ to Qn disable time	t_{PLZ}, t_{PHZ}	see Figure 10	V_{CC}=2.0V	-	-	190	ns
			V_{CC}=4.5V	-	-	38	ns
			V_{CC}=6.0V	-	-	33	ns
pulse width	t_W	SHCP HIGH or LOW; see Figure 6	V_{CC}=2.0V	95	-	-	ns
			V_{CC}=4.5V	19	-	-	ns
			V_{CC}=6.0V	16	-	-	ns
		STCP HIGH or LOW; see Figure 7	V_{CC}=2.0V	95	-	-	ns
			V_{CC}=4.5V	19	-	-	ns
			V_{CC}=6.0V	16	-	-	ns
		$\overline{MR}$ LOW; see Figure 9	V_{CC}=2.0V	95	-	-	ns
			V_{CC}=4.5V	19	-	-	ns
			V_{CC}=6.0V	16	-	-	ns
set-up time	t_{su}	DS to SHCP; see Figure 8	V_{CC}=2.0V	65	-	-	ns
			V_{CC}=4.5V	13	-	-	ns
			V_{CC}=6.0V	11	-	-	ns
		SHCP to STCP; see Figure 7	V_{CC}=2.0V	95	-	-	ns
			V_{CC}=4.5V	19	-	-	ns
			V_{CC}=6.0V	16	-	-	ns
DS to SHCP hold time	t_h	see Figure 8	V_{CC}=2.0V	3	-	-	ns
			V_{CC}=4.5V	3	-	-	ns
			V_{CC}=6.0V	3	-	-	ns
$\overline{MR}$ to SHCP recovery time	t_{rec}	see Figure 9	V_{CC}=2.0V	65	-	-	ns
			V_{CC}=4.5V	13	-	-	ns
			V_{CC}=6.0V	11	-	-	ns

maximum frequency	f_{max}	SHCP or STCP; see Figure 6 and Figure 7	V_{CC}=2.0V	4.8	-	-	MHz
			V_{CC}=4.5V	24	-	-	MHz
			V_{CC}=6.0V	28	-	-	MHz
74HCT595; V_{CC}=4.5V to 5.5V							
Propagation delay	t_{PLH}, t_{PHL}	SHCP to Q7S; see Figure 6		-	-	53	ns
		STCP to Qn; see Figure 7		-	-	50	ns
HIGH to LOW propagation delay	t_{PHL}	$\overline{MR}$ to Q7S; see Figure 9		-	-	50	ns
$\overline{OE}$ to Qn enable time	t_{PZH}, t_{PZL}	see Figure 10		-	-	44	ns
$\overline{OE}$ to Qn disable time	t_{PLZ}, t_{PHZ}	see Figure 10		-	-	38	ns
pulse width	t_W	SHCP HIGH or LOW; see Figure 6		20	-	-	ns
		STCP HIGH or LOW; see Figure 7		20	-	-	ns
		$\overline{MR}$ LOW; see Figure 9		25	-	-	ns
set-up time	t_{su}	DS to SHCP; see Figure 8		20	-	-	ns
		SHCP to STCP; see Figure 7		20	-	-	ns
DS to SHCP hold time	t_h	see Figure 8		3	-	-	ns
$\overline{MR}$ to SHCP recovery time	t_{rec}	see Figure 9		13	-	-	ns
maximum frequency	f_{max}	SHCP or STCP; see Figure 6 and Figure 7		24	-	-	MHz

AC Characteristics 3

(T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
74HC595							
propagation delay	t_{PLH}, t_{PHL}	SHCP to Q7S; see Figure 6	V_{CC}=2.0V	-	-	240	ns
			V_{CC}=4.5V	-	-	48	ns
			V_{CC}=6.0V	-	-	41	ns
		STCP to Qn; see Figure 7	V_{CC}=2.0V	-	-	265	ns
			V_{CC}=4.5V	-	-	53	ns
			V_{CC}=6.0V	-	-	45	ns
HIGH to LOW propagation delay	t_{PHL}	$\overline{MR}$ to Q7S; see Figure 9	V_{CC}=2.0V	-	-	265	ns
			V_{CC}=4.5V	-	-	53	ns
			V_{CC}=6.0V	-	-	45	ns
$\overline{OE}$ to Qn enable time	t_{PZH}, t_{PZL}	see Figure 10	V_{CC}=2.0V	-	-	225	ns
			V_{CC}=4.5V	-	-	45	ns
			V_{CC}=6.0V	-	-	38	ns
$\overline{OE}$ to Qn disable time	t_{PLZ}, t_{PHZ}	see Figure 10	V_{CC}=2.0V	-	-	225	ns
			V_{CC}=4.5V	-	-	45	ns

			V_{CC}=6.0V	-	-	38	ns
pulse width	t_W	SHCP HIGH or LOW; see Figure 6	V_{CC}=2.0V	110	-	-	ns
			V_{CC}=4.5V	22	-	-	ns
			V_{CC}=6.0V	19	-	-	ns
		STCP HIGH or LOW; see Figure 7	V_{CC}=2.0V	110	-	-	ns
			V_{CC}=4.5V	22	-	-	ns
			V_{CC}=6.0V	19	-	-	ns
		$\overline{MR}$ LOW; see Figure 9	V_{CC}=2.0V	110	-	-	ns
			V_{CC}=4.5V	22	-	-	ns
			V_{CC}=6.0V	19	-	-	ns
set-up time	t_{su}	DS to SHCP; see Figure 8	V_{CC}=2.0V	75	-	-	ns
			V_{CC}=4.5V	15	-	-	ns
			V_{CC}=6.0V	13	-	-	ns
		SHCP to STCP; see Figure 7	V_{CC}=2.0V	110	-	-	ns
			V_{CC}=4.5V	22	-	-	ns
			V_{CC}=6.0V	19	-	-	ns
DS to SHCP hold time	t_h	see Figure 8	V_{CC}=2.0V	3	-	-	ns
			V_{CC}=4.5V	3	-	-	ns
			V_{CC}=6.0V	3	-	-	ns
$\overline{MR}$ to SHCP recovery time	t_{rec}	see Figure 9	V_{CC}=2.0V	75	-	-	ns
			V_{CC}=4.5V	15	-	-	ns
			V_{CC}=6.0V	13	-	-	ns
maximum frequency	f_{max}	SHCP or STCP; see Figure 6 and Figure 7	V_{CC}=2.0V	4	-	-	MHz
			V_{CC}=4.5V	20	-	-	MHz
			V_{CC}=6.0V	24	-	-	MHz
74HCT595; V_{CC}=4.5V to 5.5V							
Propagation delay	t_{PLH}, t_{PHL}	SHCP to Q7S; see Figure 6		-	-	63	ns
		STCP to Qn; see Figure 7		-	-	60	ns
HIGH to LOW propagation delay	t_{PHL}	$\overline{MR}$ to Q7S; see Figure 9		-	-	60	ns
$\overline{OE}$ to Qn enable time	t_{PZH}, t_{PZL}	see Figure 10		-	-	53	ns
$\overline{OE}$ to Qn disable time	t_{PLZ}, t_{PHZ}	see Figure 10		-	-	45	ns
pulse width	t_W	SHCP HIGH or LOW; see Figure 6		24	-	-	ns
		STCP HIGH or LOW; see Figure 7		24	-	-	ns
		$\overline{MR}$ LOW; see Figure 9		30	-	-	ns
set-up time	t_{su}	DS to SHCP; see Figure 8		24	-	-	ns
		SHCP to STCP; see Figure 7		24	-	-	ns
DS to SHCP hold time	t_h	see Figure 8		3	-	-	ns

$\overline{MR}$ to SHCP recovery time	t_{rec}	see Figure 9	15	-	-	ns
maximum frequency	f_{max}	SHCP or STCP; see Figure 6 and Figure 7	20	-	-	MHz

13. Testing Circuit

AC Testing Circuit

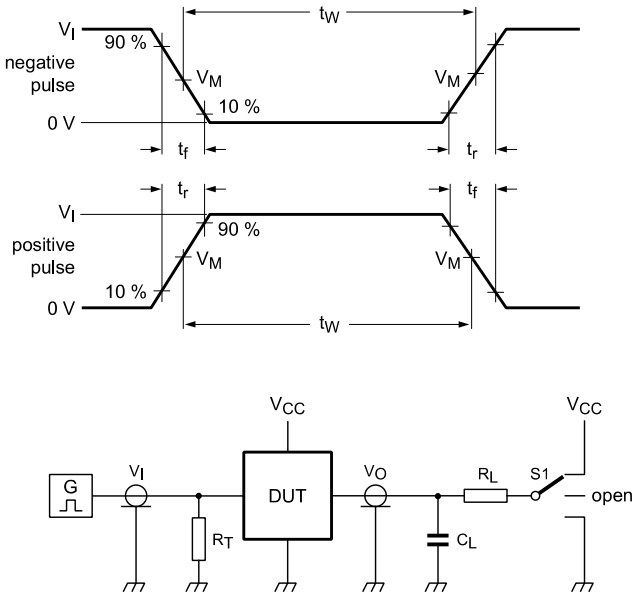


Fig. 5. Test circuit for measuring switching times

Definitions for test circuit:

R_L=Load resistance.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to the output impedance Zo of the pulse generator.

S1=Test selection switch.

AC Testing Waveforms

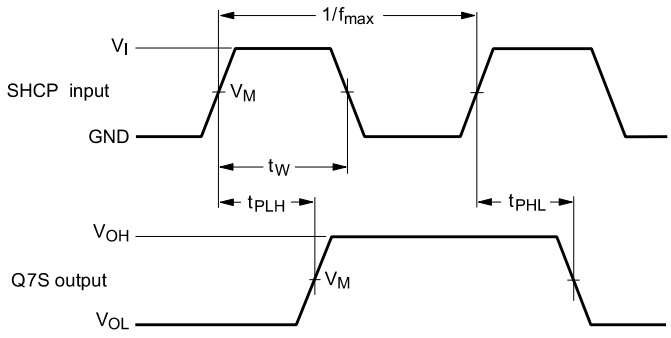


Fig. 6. Shift clock pulse, maximum frequency and input to output propagation delays

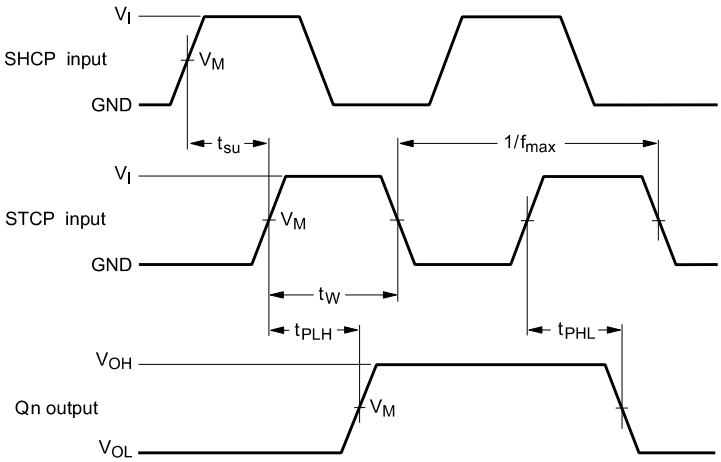


Fig. 7. Storage clock to output propagation delays

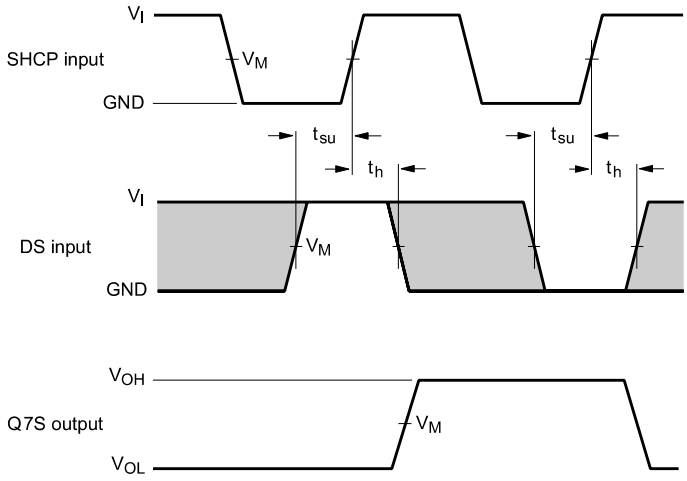


Fig. 8. Data set-up and hold times

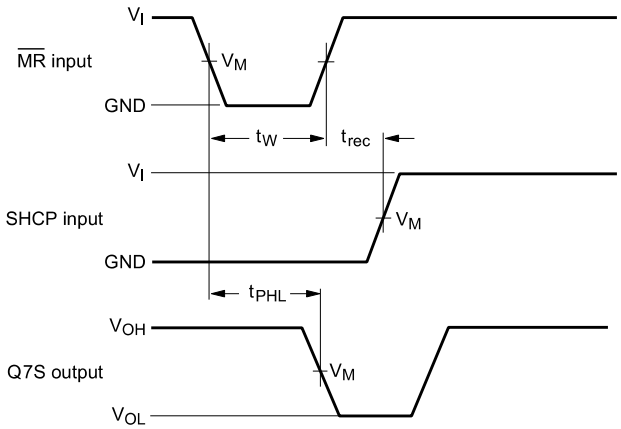


Fig. 9. Master reset to output propagation delays

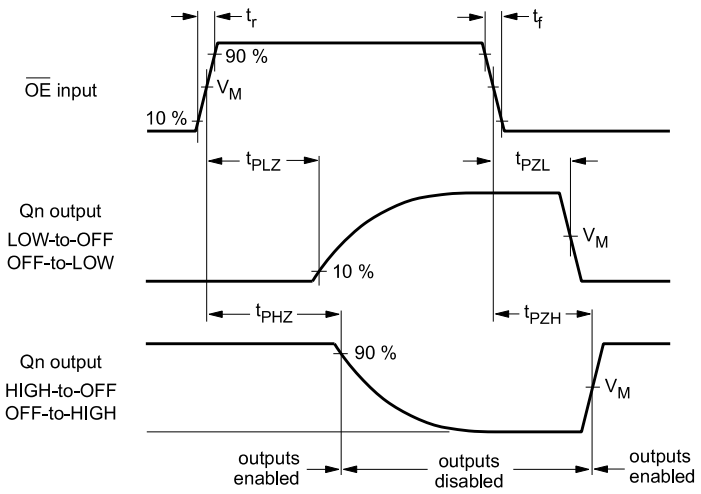


Fig. 10. Enable and disable times

Measurement Points

Type	Input	Output
	V_M	V_M
74HC595	0.5×V_{CC}	0.5×V_{CC}
74HCT595	1.3V	1.3V

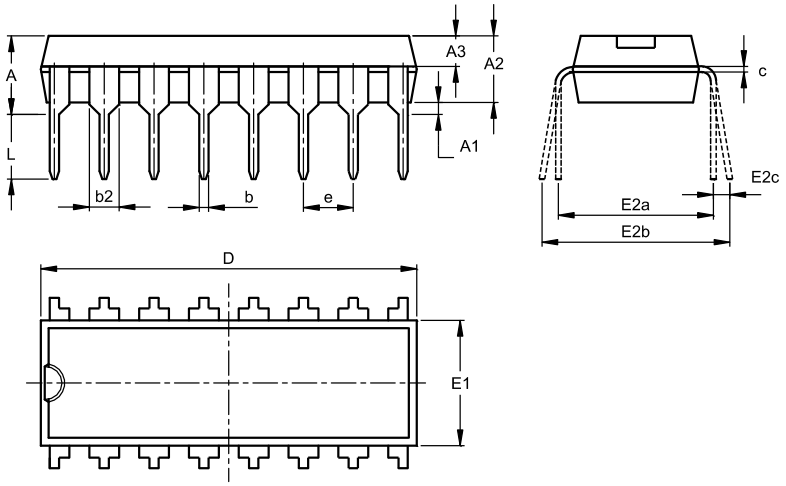
Test Data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC595	V_{CC}	6ns	50pF	1kΩ	open	GND	V_{CC}
74HCT595	3V	6ns	50pF	1kΩ	open	GND	V_{CC}

14. Package outlines

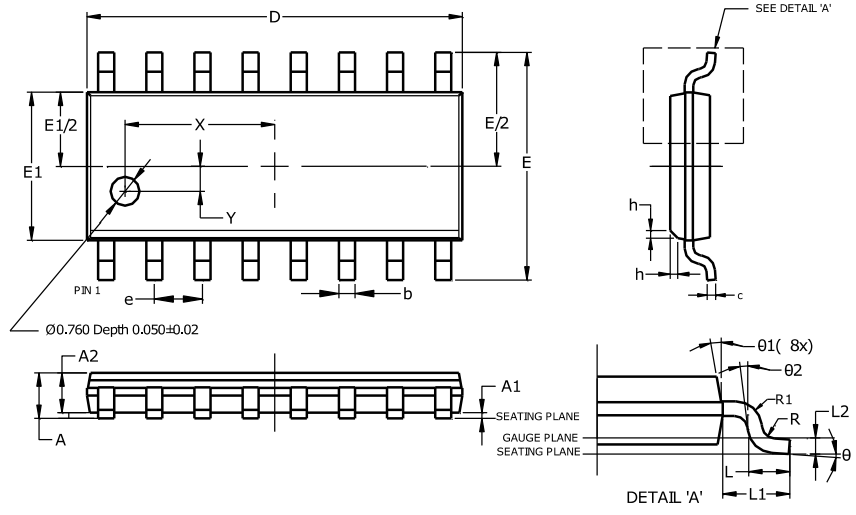
DIP-16

PDIP-16



PDIP-16			
Dim	Min	Max	Nom
A	3.60	4.00	3.80
A1	0.51	-	
A2	3.20	3.40	3.30
A3	1.47	1.57	1.52
b	0.44	0.53	–
b2	1.52BSC		
c	0.25	0.31	–
D	18.90	19.30	19.10
E1	6.15	6.55	6.35
E2a	7.62 BSC		
E2b	7.62	9.30	–
E2c	0.00	0.84	–
e	2.54BSC		
L	3.00	–	–
All Dimensions in mm			

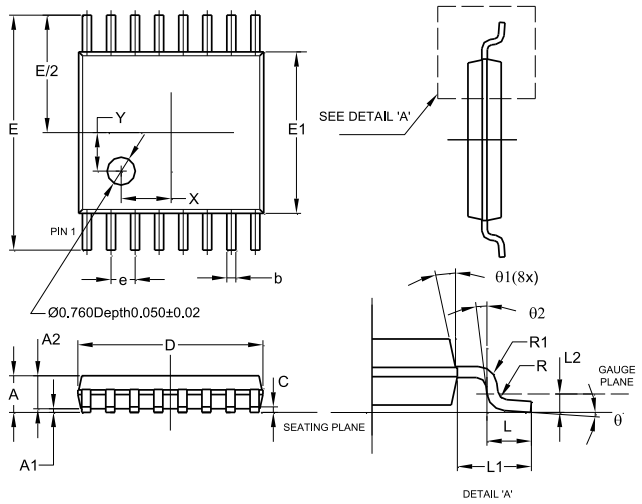
SOIC-16



SOIC-16			
Dim	Min	Max	Typ
A	–	1.260	–
A1	0.10	0.23	–
A2	1.02	--	–
b	0.31	0.51	–
c	0.10	0.25	–
D	9.80	10.00	–
E	5.90	6.10	–
E1	3.80	4.00	–
e	1.27 BSC		
h	0.15	0.25	0.20
L	0.40	1.27	–
L1	1.04 REF		
L2	0.25 BSC		
R	0.07	--	–
R1	0.07	--	–
X	3.945 REF		
Y	0.661 REF		
θ	0°	8°	–
θ1	5°	15°	–
θ2	0°	--	–
All Dimensions in mm			

TSSOP-16

TSSOP-16



TSSOP-16			
Dim	**Min**	**Max**	**Typ**
A	-	1.08	-
A1	0.05	0.15	-
A2	0.80	0.93	-
b	0.19	0.30	-
c	0.09	0.20	-
D	4.90	5.10	-
E	6.40 BSC		
E1	4.30	4.50	-
e	0.65 BSC		
L	0.45	0.75	-
L1	1.00 REF		
L2	0.25 BSC		
R / R1	0.09	-	-
X	-	-	1.350
Y	-	-	1.050
θ	0°	8°	-
θ1	5°	15°	-
θ2	0°	-	-
All Dimensions in mm			

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