8-Bit Shift Register With Input Flip-Flops

1. Description

The 74HC597; 74HCT597 is an 8-bit shift register with input flip-flops. It consists of an 8-bit storage register feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and the shift register have positive edge-triggered clocks. The shift register also has direct load (from storage) and clear inputs. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}

2. Features

- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Input levels:
  - For 74HC597: CMOS level
  - For 74HCT597: TTL level
- 8-bit parallel storage register inputs
- Shift register has direct overriding load and clear
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering Information

Type Number	Package Type	Packing	Notes
74HC597D	SOIC-16	Tape & Reel	
74HCT597D	SOIC-16	Tape & Reel	
74HC597PW	TSSOP-16	Tape & Reel	
74HCT597PW	TSSOP-16	Tape & Reel	

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

4. Pinning

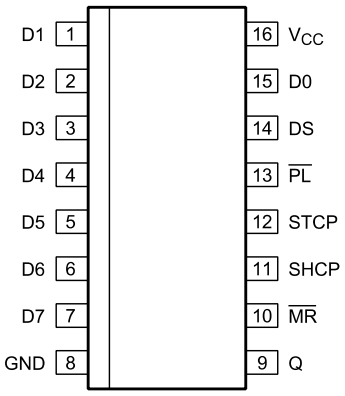


Fig. 1. Pin Configuration

Pin Description

Symbol	Pin	Description
GND	8	ground (0 V)
Q	9	serial data output
MR	10	asynchronous master reset input (active LOW)
SHCP	11	shift register clock input (LOW-to-HIGH, edge-triggered)
STCP	12	storage register clock input (LOW-to-HIGH, edge-triggered)
PL	13	parallel load input (active LOW)
DS	14	serial data input
D0, D1, D2, D3, D4, D5, D6, D7	15, 1, 2, 3, 4, 5, 6, 7	parallel data inputs
V_{CC}	16	supply voltage

5. Functional diagram

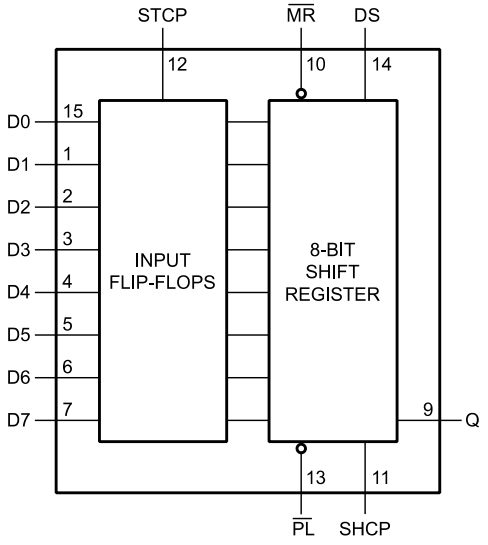


Fig. 2. Functional Diagram

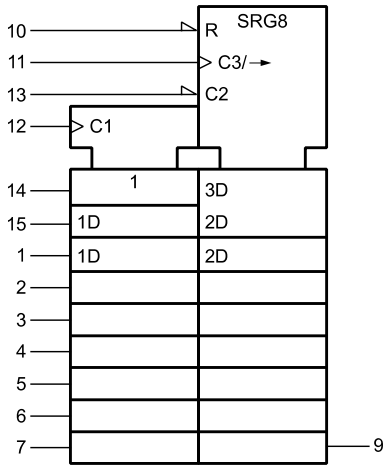


Fig. 3. IEC Logic symbol

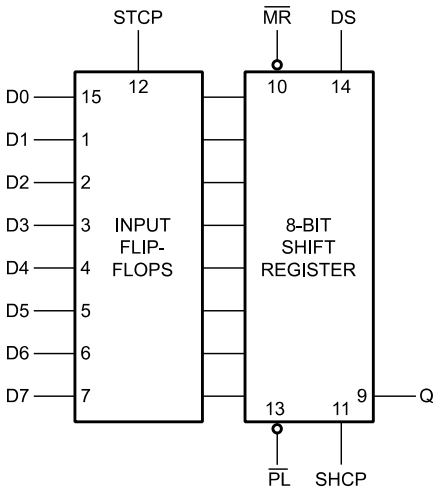


Fig. 4. Logic Symbol

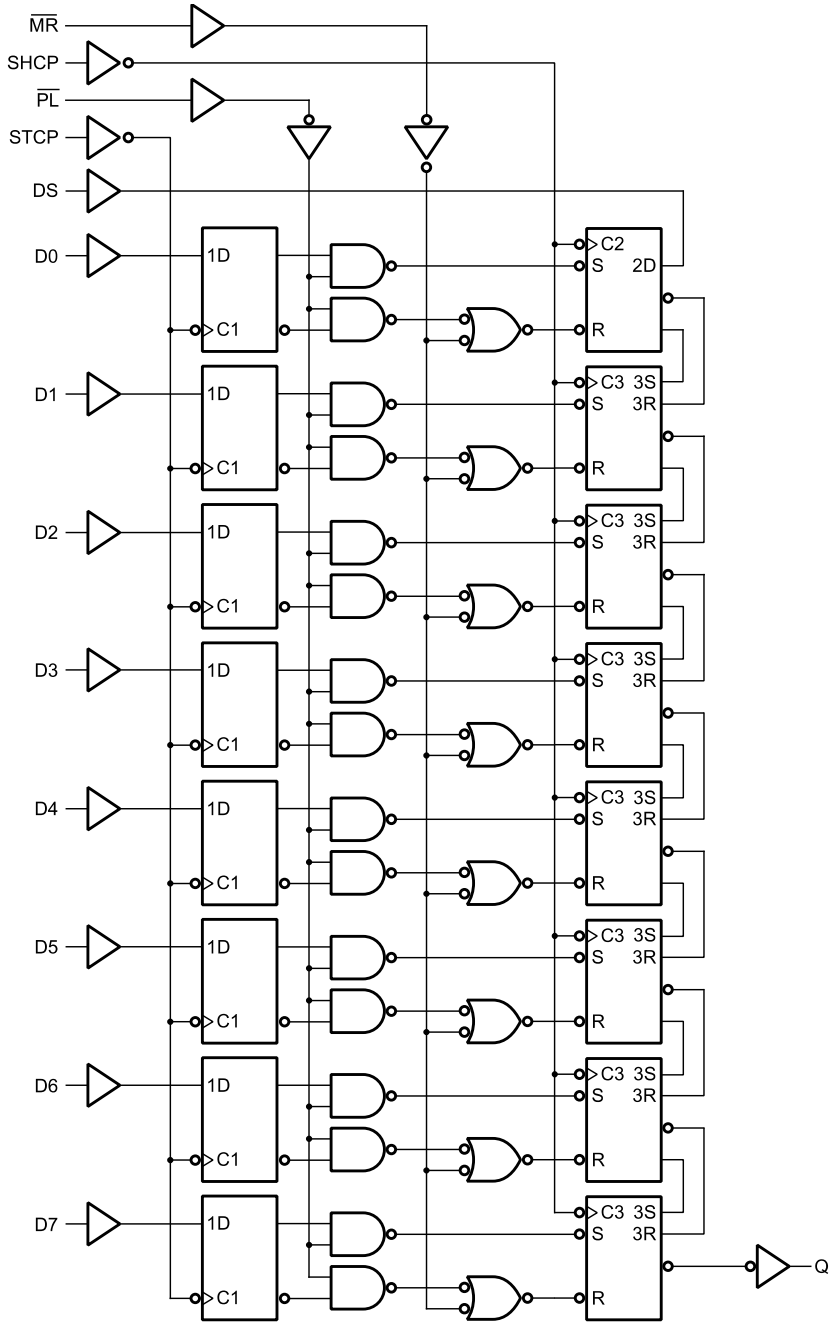


Fig. 5. Logic Diagram

6. Functional Description

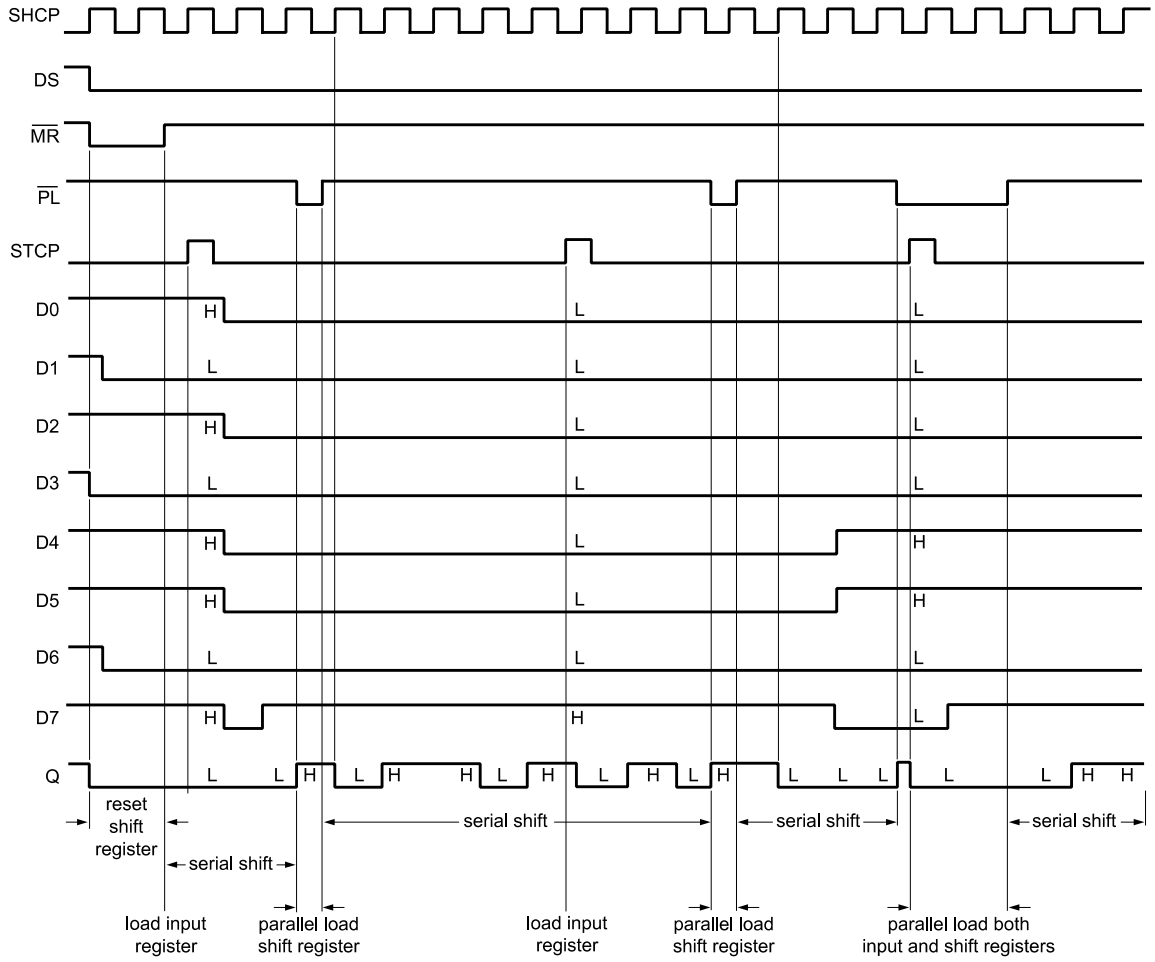


Fig. 6. Timing Diagram

Function Table

H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = positive-going transition.

Inputs				Function
STCP	SHCP	PL	MR	
↑	X	X	X	data loaded to input latches
↑	X	L	H	data loaded from inputs to shift register
no clock edge	X	L	H	data transferred from input flip-flops to shift register
X	X	L	L	invalid logic, state of shift register is indeterminate when signals removed
X	X	H	L	shift register cleared
X	↑	H	H	shift register clocked Qn = Qn-1, Q0 = DS

7. Limiting Values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	-	±20	mA
I_O	output current	$V_O = -0.5$ V to ($V_{CC} + 0.5$ V)	-	±25	mA
I_{CC}	supply current		-	+50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation		-	500	mW

8. Recommended Operating Conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC597			74HCT597			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	^{V}CC	V
V_O	output voltage		0	-	V_{CC}	0	-	^{V}CC	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	$V_{CC} = 2.0$ V	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5$ V	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0$ V	-	-	83	-	-	-	ns/V

9. Static Characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC597										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = -20 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = -20 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -20 μA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = -4.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = -5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	-	80.0	-	160.0	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT597										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = 20 μA	-	0	0.1	-	0.1	-	0.1	V

		I_O = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	8.0	-	80.0	-	160.0	μA
ΔI_{CC}	additional supply current	V_I = V_{CC} - 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A								
		per input pin; DS input	-	25	90	-	112.5	-	122.5	μA
		per input pin; Dn inputs	-	30	108	-	135	-	147	μA
		per input pin; PL, MR inputs	-	150	540	-	675	-	735	μA
		per input pin; STCP, SHCP inputs	-	150	540	-	675	-	735	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic Characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified.

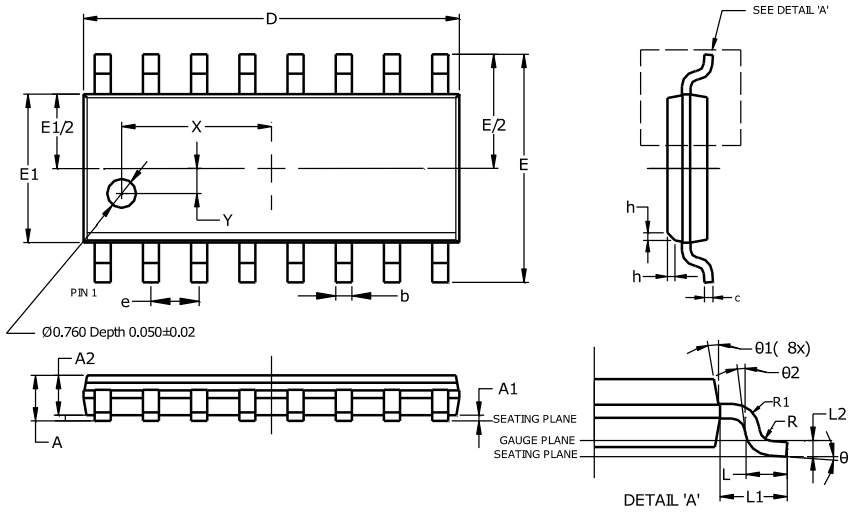
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC597										
t_{pd}	propagation delay	SHCP to Q								
		V_{CC} = 2.0 V	-	55	175	-	220	-	265	ns
		V_{CC} = 4.5 V	-	20	35	-	44	-	53	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	17	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	16	30	-	37	-	45	ns
		MR to Q								
		V_{CC} = 2.0 V	-	58	175	-	220	-	265	ns
		V_{CC} = 4.5 V	-	21	35	-	44	-	53	ns
		V_{CC} = 6.0 V	-	17	30	-	37	-	45	ns
		STCP to Q								
		V_{CC} = 2.0 V	-	80	250	-	315	-	375	ns
		V_{CC} = 4.5 V	-	29	50	-	63	-	75	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	25	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	23	43	-	54	-	64	ns
		PL to Q								
		V_{CC} = 2.0 V	-	69	215	-	270	-	325	ns
		V_{CC} = 4.5 V	-	25	43	-	54	-	65	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	21	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	20	37	-	46	-	55	ns
t_t	transition time	Q								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t_W	pulse width	STCP HIGH or LOW								
		V_{CC} = 2.0 V	80	11	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	4	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	3	-	17	-	20	-	ns
		SHCP HIGH or LOW								
		V_{CC} = 2.0 V	80	14	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	5	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	4	-	17	-	20	-	ns
		MR LOW_								

		V_{CC} = 2.0 V	80	22	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	8	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	6	-	17	-	20	-	ns
		PL LOW								
		V_{CC} = 2.0 V	80	22	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	8	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	6	-	17	-	20	-	ns
t_{rec}	recovery time	MR to SHCP								
		V_{CC} = 2.0 V	60	-3	-	75	-	90	-	ns
		V_{CC} = 4.5 V	12	-1	-	15	-	18	-	ns
		V_{CC} = 6.0 V	10	-1	-	13	-	15	-	ns
t_{su}	set-up time	Dn to STCP								
		V_{CC} = 2.0 V	60	8	-	75	-	90	-	ns
		V_{CC} = 4.5 V	12	3	-	15	-	18	-	ns
		V_{CC} = 6.0 V	10	2	-	13	-	15	-	ns
		DS to SHCP								
		V_{CC} = 2.0 V	60	11	-	75	-	90	-	ns
		V_{CC} = 4.5 V	12	4	-	15	-	18	-	ns
		V_{CC} = 6.0 V	10	3	-	13	-	15	-	ns
		PL to SHCP								
		V_{CC} = 2.0 V	60	11	-	75	-	90	-	ns
		V_{CC} = 4.5 V	12	4	-	15	-	18	-	ns
		V_{CC} = 6.0 V	10	3	-	13	-	15	-	ns
t_h	hold time	Dn to STCP								
		V_{CC} = 2.0 V	5	-3	-	5	-	5	-	ns
		V_{CC} = 4.5 V	5	-1	-	5	-	5	-	ns
		V_{CC} = 6.0 V	5	-1	-	5	-	5	-	ns
		PL, DS to SHCP								
		V_{CC} = 2.0 V	5	-6	-	5	-	5	-	ns
		V_{CC} = 4.5 V	5	-2	-	5	-	5	-	ns
		V_{CC} = 6.0 V	5	-2	-	5	-	5	-	ns
fmax	maximum frequency	SHCP								
		V_{CC} = 2.0 V	6.0	29	-	4.8	-	4.0	-	MHz
		V_{CC} = 4.5 V	30	87	-	24	-	20	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF	-	96	-	-	-	-	-	MHz
		V_{CC} = 6.0 V	35	104	-	28	-	24	-	MHz
CPD	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; V_I = GND to V_{CC}	-	29	-	-	-	-	-	pF
74HCT597										
t_{pd}	propagation delay	SHCP to Q								

		V_{CC} = 4.5 V	-	23	40	-	50	-	60	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	20	-	-	-	-	-	ns
		MR to Q								
		V_{CC} = 4.5 V	-	28	49	-	61	-	74	ns
		STCP to Q								
		V_{CC} = 4.5 V	-	33	57	-	71	-	86	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	29	-	-	-	-	-	ns
		PL to Q								
		V_{CC} = 4.5 V	-	30	52	-	65	-	78	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	26	-	-	-	-	-	ns
t_t	transition time	Q								
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		STCP HIGH or LOW								
		V_{CC} = 4.5 V	16	6	-	20	-	24	-	ns
		SHCP HIGH or LOW								
t_W	pulse width	V_{CC} = 4.5 V	16	7	-	20	-	24	-	ns
		MR LOW								
		V_{CC} = 4.5 V	25	14	-	31	-	38	-	ns
		PL LOW								
		V_{CC} = 4.5 V	20	10	-	25	-	30	-	ns
t_{rec}	recovery time	MR to SHCP								
		V_{CC} = 4.5 V	12	-2	-	15	-	18	-	ns
		Dn to STCP								
		V_{CC} = 4.5 V	12	5	-	15	-	18	-	ns
		DS to SHCP								
t_{su}	set-up time	V_{CC} = 4.5 V	12	2	-	15	-	18	-	ns
		PL to SHCP								
		V_{CC} = 4.5 V	12	4	-	15	-	18	-	ns
		Dn to STCP								
		V_{CC} = 4.5 V	5	-1	-	5	-	5	-	ns
t_h	hold time	PL, DS to SHCP								
		V_{CC} = 4.5 V	5	-2	-	5	-	5	-	ns
		SHCP								
f_{max}	maximum frequency	V_{CC} = 4.5 V	30	75	-	24	-	20	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF	-	83	-	-	-	-	-	MHz
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; V_I = GND to V_{CC} - 1.5 V	-	32	-	-	-	-	-	pF

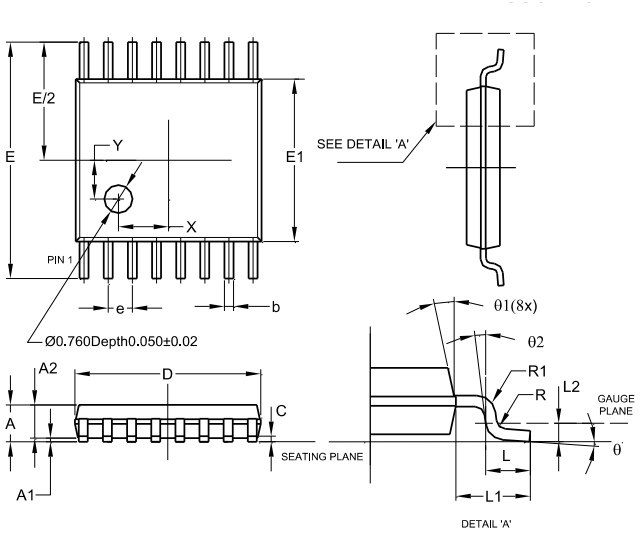
11. Package Outlines

SOIC-16



SOIC-16			
Dim	Min	Max	Typ
A	–	1.260	–
A1	0.10	0.23	–
A2	1.02	–	–
b	0.31	0.51	–
c	0.10	0.25	–
D	9.80	10.00	–
E	5.90	6.10	–
E1	3.80	4.00	–
e	1.27 BSC		
h	0.15	0.25	0.20
L	0.40	1.27	–
L1	1.04 REF		
L2	0.25 BSC		
R	0.07	–	–
R1	0.07	–	–
X	3.945 REF		
Y	0.661 REF		
θ	0°	8°	–
θ1	5°	15°	–
θ2	0°	–	–
All Dimensions in mm			

TSSOP-16



TSSOP-16			
Dim	Min	Max	Typ
A	-	1.08	-
A1	0.05	0.15	-
A2	0.80	0.93	-
b	0.19	0.30	-
c	0.09	0.20	-
D	4.90	5.10	-
E	6.40 BSC		
E1	4.30	4.50	-
e	0.65 BSC		
L	0.45	0.75	-
L1	1.00 REF		
L2	0.25 BSC		
R / R1	0.09	-	-
X	-	-	1.350
Y	-	-	1.050
θ	0°	8°	-
θ1	5°	15°	-
θ2	0°	-	-
All Dimensions in mm			

12. Disclaimers

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