1、General Description

The CD4043 is a quad R/S latch with 3-state outputs with a common output enable input (OE). Each latch has an active HIGH set input (1S to 4S), an active HIGH reset input (1R to 4R) and an active HIGH 3-state output (1Q to 4Q).

When OE is HIGH, the latch output (nQ) is determined by the nR and nS inputs as shown in function table. When OE is LOW, the latch outputs are in the high impedance OFF-state. OE does not affect the state of the latch. The high impedance off-state feature allows common bussing of the outputs.

It operates over a recommended V_{DD} power supply range of 3V to 15V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input.

Features:

- 5V, 10V, and 15V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40℃ to +85℃
- Packaging information: DIP16/SOIC16/TSSOP16

2、Block Diagram And Pin Description

2.1、Block Diagram

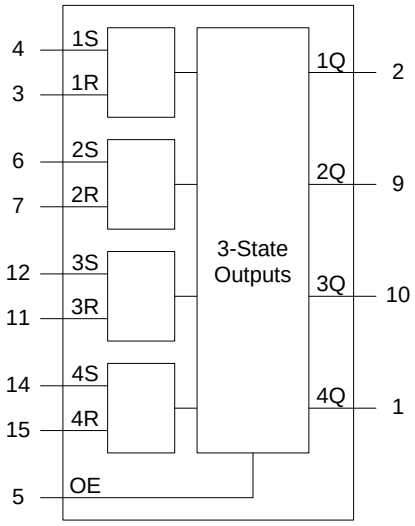


Figure 1. Functional diagram

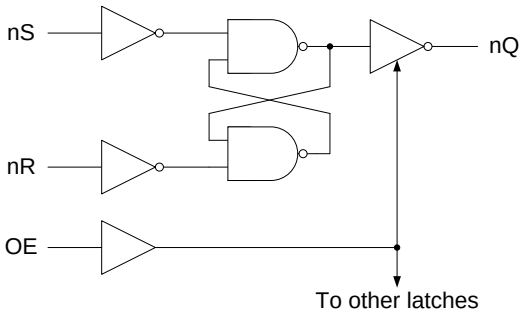
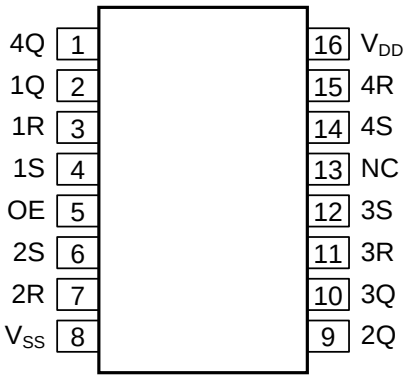


Figure 2. Logic diagram for one latch

2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1	4Q	3-state buffered latch output
2	1Q	3-state buffered latch output
3	1R	reset input (active HIGH)
4	1S	set input (active HIGH)
5	OE	common output enable input
6	2S	set input (active HIGH)
7	2R	reset input (active HIGH)
8	V_{SS}	ground supply voltage
9	2Q	3-state buffered latch output
10	3Q	3-state buffered latch output
11	3R	reset input (active HIGH)
12	3S	set input (active HIGH)
13	NC	not connected
14	4S	set input (active HIGH)
15	4R	reset input (active HIGH)
16	V_{DD}	supply voltage

2.4、Function Table

Inputs			Output
OE	**nS**	**nR**	**nQ**
L	X	X	Z
H	L	H	L
H	H	X	H
H	L	L	latched

Note: [1] H=HIGH voltage level; L=LOW voltage level; X=don't care; Z=high impedance state.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V_{DD}	-		-0.5	+18	V
input clamping current	I_{IK}	V_I<-0.5V or V_I>V_{DD}+0.5V		-	±10	mA
input voltage	V_I	-		-0.5	V_{DD}+0.5	V
output clamping current	I_{OK}	V_O<-0.5V or V_O>V_{DD}+0.5V		-	±10	mA
output current	I_O	V_O=0V to V_{CC}		-	±10	mA
supply current	I_{DD}	-		-	50	mA
total power dissipation	P_{tot}	-		-	500	mW
power dissipation	P_D	per output		-	100	mW
storage temperature	T_{stg}	-		-65	+150	℃
soldering temperature	T_L	10s	DIP	245		℃
			SOIC	260		℃

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{DD}	-	3	-	15	V
input voltage	V_I	-	0	-	V_{DD}	V
ambient temperature	T_{amb}	-	-40	-	+85	℃

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

(T_{amb}=25℃, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified)

Parameter	Symbol	Conditions (V)			T_{amb}=25℃			Unit
		V_O	V_{IN}	V_{DD}	Min.	Typ.	Max.	
supply current	I_{DD}	-	0, 5	5	-	-	20	uA
		-	0, 10	10	-	-	40	uA
		-	0, 15	15	-	-	80	uA
LOW-level output current	I_{OL}	0.4	0, 5	5	0.44	-	-	mA
		0.5	0, 10	10	1.1	-	-	mA
		1.5	0, 15	15	3.0	-	-	mA
HIGH-level output current	I_{OH}	4.6	0, 5	5	-	-	-0.44	mA
		2.5	0, 5	5	-	-	-1.4	mA
		9.5	0, 10	10	-	-	-1.1	mA
		13.5	0, 15	15	-	-	-3.0	mA
LOW-level output voltage	V_{OL}	-	0, 5	5	-	-	0.05	V
		-	0, 10	10	-	-	0.05	V
		-	0, 15	15	-	-	0.05	V
HIGH-level output voltage	V_{OH}	-	0, 5	5	4.95	-	-	V
		-	0, 10	10	9.95	-	-	V
		-	0, 15	15	14.95	-	-	V
LOW-level input voltage	V_{IL}	0.5, 4.5	-	5	-	-	1.5	V
		1, 9	-	10	-	-	3	V
		1.5, 13.5	-	15	-	-	4	V
HIGH-level input voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	-	V
		1, 9	-	10	7	-	-	V
		1.5, 13.5	-	15	11	-	-	V
input leakage current	I_I	-	0, 15	15	-	-	±1.0	uA
OFF-state output current	I_{OZ}	nQ output HIGH; returned to V_{DD}		15	-	-	1.6	uA
		nQ output LOW; returned to V_{SS}		15	-	-	1.6	uA
input capacitance	C_I	-		-	-	-	7.5	pF

3.3.2、DC Characteristics 2

(T_{amb}=-40℃ to +85℃, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified)

Parameter	Symbol	Conditions (V)			T_{amb}=-40℃		T_{amb}=+85℃		Unit
		V_O	V_{IN}	V_{DD}	Min.	Max.	Min.	Max.	
supply current	I_{DD}	-	0, 5	5	-	20	-	150	uA
		-	0, 10	10	-	40	-	300	uA
		-	0, 15	15	-	80	-	600	uA
LOW-level output current	I_{OL}	0.4	0, 5	5	0.52	-	0.36	-	mA
		0.5	0, 10	10	1.3	-	0.9	-	mA
		1.5	0, 15	15	3.6	-	2.4	-	mA
HIGH-level output current	I_{OH}	4.6	0, 5	5	-	-0.52	-	-0.36	mA
		2.5	0, 5	5	-	-1.7	-	-1.1	mA
		9.5	0, 10	10	-	-1.3	-	-0.9	mA
		13.5	0, 15	15	-	-3.6	-	-2.4	mA
LOW-level output voltage	V_{OL}	-	0, 5	5	-	0.05	-	0.05	V
		-	0, 10	10	-	0.05	-	0.05	V
		-	0, 15	15	-	0.05	-	0.05	V
HIGH-level output voltage	V_{OH}	-	0, 5	5	4.95	-	4.95	-	V
		-	0, 10	10	9.95	-	9.95	-	V
		-	0, 15	15	14.95	-	14.95	-	V
LOW-level input voltage	V_{IL}	0.5, 4.5	-	5	-	1.5	-	1.5	V
		1, 9	-	10	-	3	-	3	V
		1.5, 13.5	-	15	-	4	-	4	V
HIGH-level input voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	3.5	-	V
		1, 9	-	10	7	-	7	-	V
		1.5, 13.5	-	15	11	-	11	-	V
input leakage current	I_I	-	0, 15	15	-	±1.0	-	±1.0	uA
OFF-state output current	I_{OZ}	nQ output HIGH; returned to V_{DD}		15	-	1.6	-	12	uA
		nQ output LOW; returned to V_{SS}		15	-	1.6	-	12	uA

3.3.3、AC Characteristics

(T_{amb}=25℃, V_{SS}=0V, unless otherwise specified)

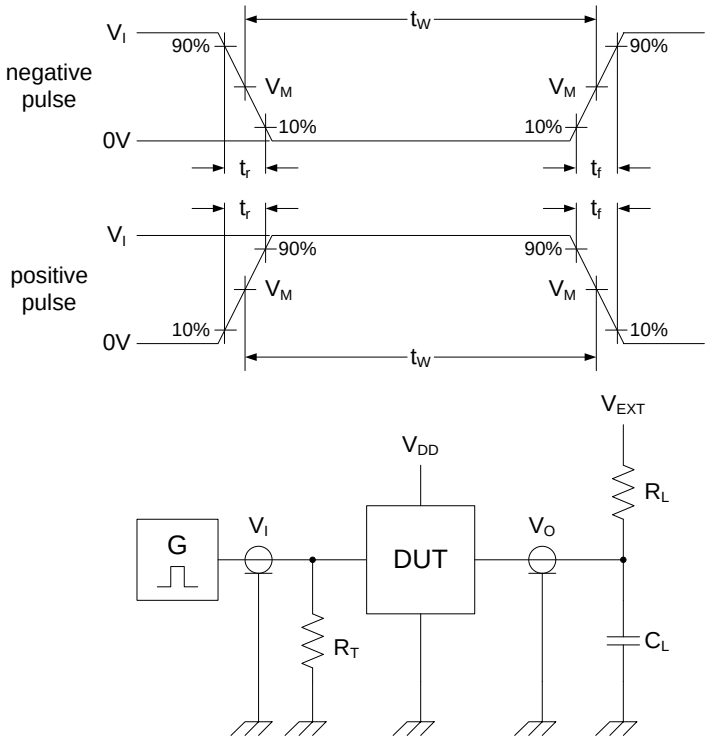
Parameter	Symbol	Conditions	V_{DD}	Min.	Typ.	Max.	Unit
HIGH to LOW propagation delay	t_{PHL}	nR→nQ; see Figure 4	5[1]	-	90	180	ns
			10	-	35	70	ns
			15	-	25	50	ns
LOW to HIGH propagation delay	t_{PLH}	nS→nQ; see Figure 4	5[1]	-	65	135	ns
			10	-	25	50	ns
			15	-	15	35	ns
transition time	t_{THL}, t_{TLH}	nQ output; see Figure 4	5[1][2]	-	60	120	ns
			10	-	30	60	ns
			15	-	30	60	ns
HIGH to OFF-state propagation delay	t_{PHZ}	OE→nQ; see Figure 5	5	-	45	90	ns
			10	-	25	50	ns
			15	-	20	40	ns
LOW to OFF-state propagation delay	t_{PLZ}	OE→nQ; see Figure 5	5	-	50	100	ns
			10	-	20	40	ns
			15	-	15	30	ns
OFF-state to HIGH propagation delay	t_{PZH}	OE→nQ; see Figure 5	5	-	40	80	ns
			10	-	26	60	ns
			15	-	25	50	ns
OFF-state to LOW propagation delay	t_{PZL}	OE→nQ; see Figure 5	5	-	45	90	ns
			10	-	30	60	ns
			15	-	30	60	ns
pulse width	t_W	nS input HIGH; minimum width; see Figure 4	5	30	15	-	ns
			10	20	10	-	ns
			15	16	8	-	ns
		nR input HIGH; minimum width; see Figure 4	5	30	15	-	ns
			10	20	10	-	ns
			15	16	8	-	ns

Note:

The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

4、Testing Circuit

4.1、AC Testing Circuit



Definitions test circuit:

DUT=Device Under Test.

R_L=Load resistance;

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT}=External voltage for measuring switching times.

Figure 3. Test circuit for measuring switching times

4.2、AC Testing Waveforms

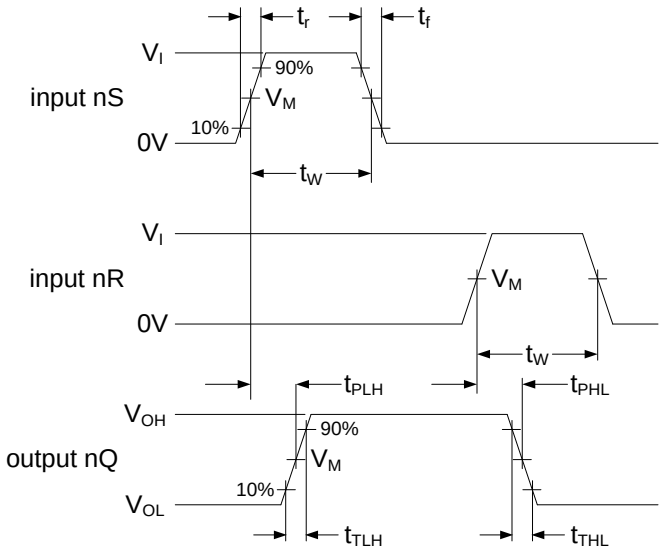


Figure 4. Input minimum set (nS) and reset (nR) pulse widths, inputs nS or nR to latch output (nQ) propagation delay and nQ transition time

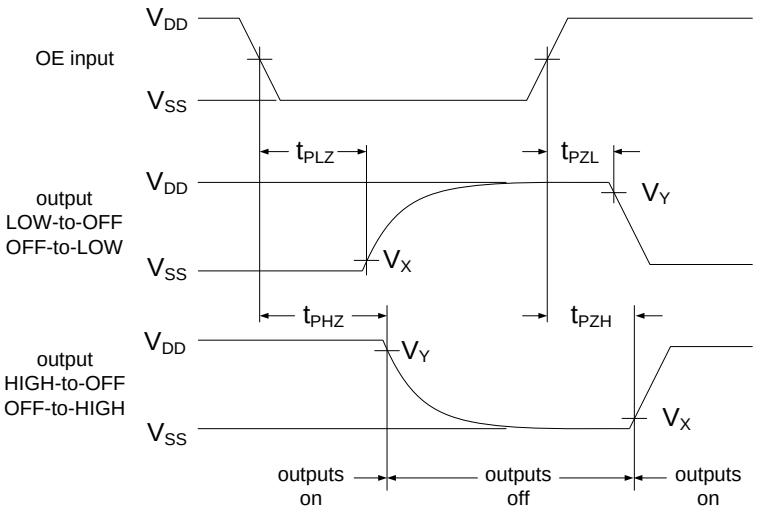


Figure 5. Output enable (OE) to latch output (nQ) enable time (t_{PZL} and t_{PZH}) and disable time (t_{PLZ} and t_{PHZ})

4.3、Measurement Points

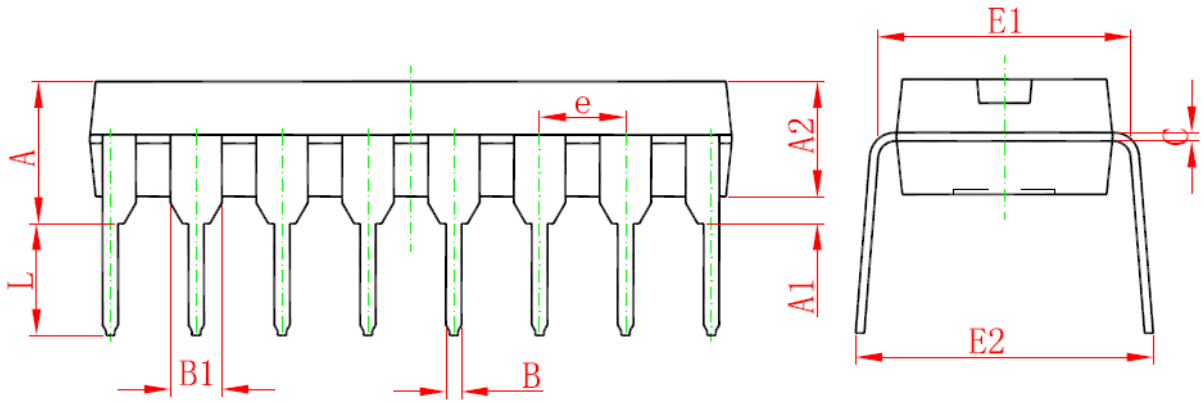
Supply voltage	Input		Output		
V_{DD}	V_I	V_M	V_M	V_X	V_Y
5V to 15V	V_{DD} or 0V	$0.5\times V_{DD}$	$0.5\times V_{DD}$	$0.1\times V_{DD}$	$0.9\times V_{DD}$

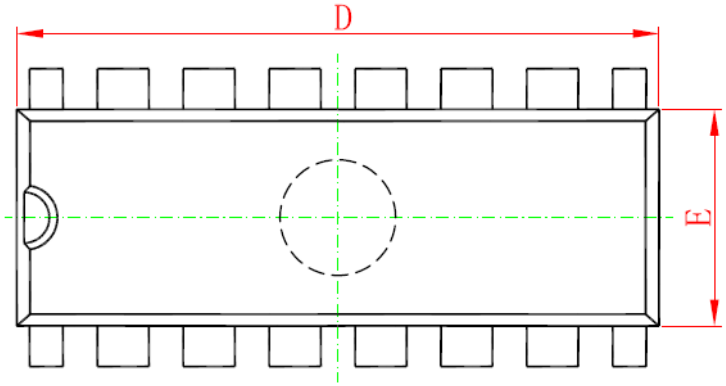
4.4、Test Data

Supply voltage	Input		Load		V_{EXT}		
V_{DD}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
5V to 15V	V_{DD}	≤20ns	50pF	1kΩ	open	V_{DD}	GND

5、Package Information

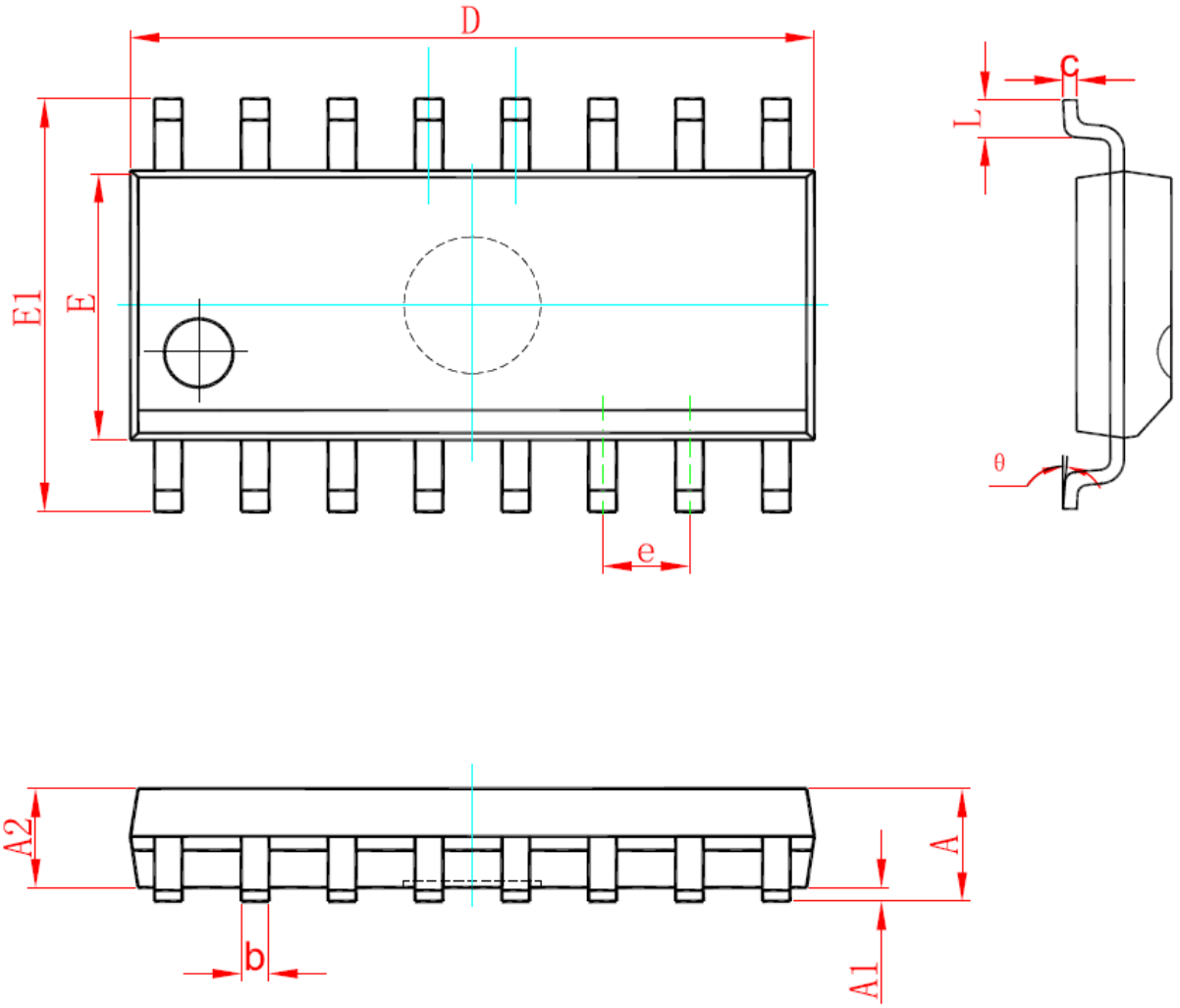
5.1、DIP16





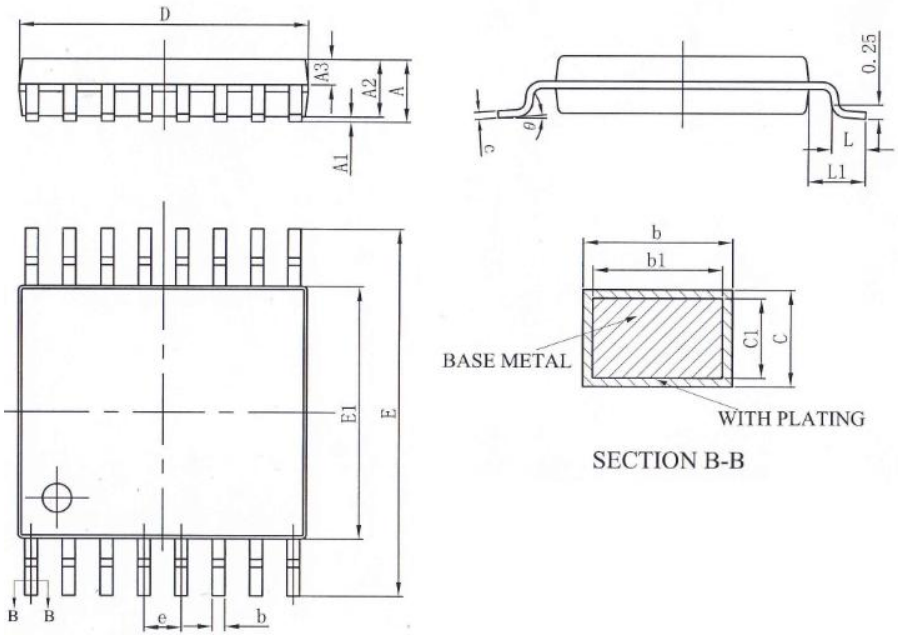
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524(BSC)		0.060(BSC)	
C	0.204	0.360	0.008	0.014
D	18.800	19.200	0.740	0.756
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540(BSC)		0.100(BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

5.2、SOIC16



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.200	0.386	0.402
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

5.3、TSSOP16



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.28
b1	0.19	0.22	0.25
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	4.90	5.00	5.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	—	8°

6、Ordering Information

Type Number	Package	Packing	Description
CD4043BE	DIP-16	Tube	
CD4043BD	SOIC-16	Tape & Reel	
CD4043BPW	TSSOP-16	Tape & Reel	