

600V Half-Bridge Driver

1. Description

The IR2104S is a high voltage, high speed power MOSFET and IGBT drivers with dependent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output,

down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600 V.

2. Features

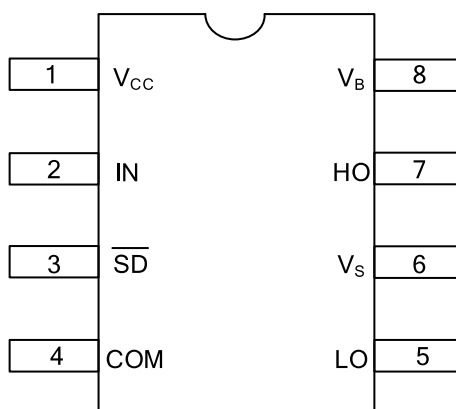
- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout
- 3.3 V, 5 V, and 15 V logic compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- Internal set deadtime
- Shutdown input turns off both channels
- RoHS compliant
- SOIC-8 and PDIP-8 package

3. Ordering Information

Type Number	Package Type	Packing
IR2104S	SOIC-8	Tape & Reel
IR2104	DIP-8	Tube

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

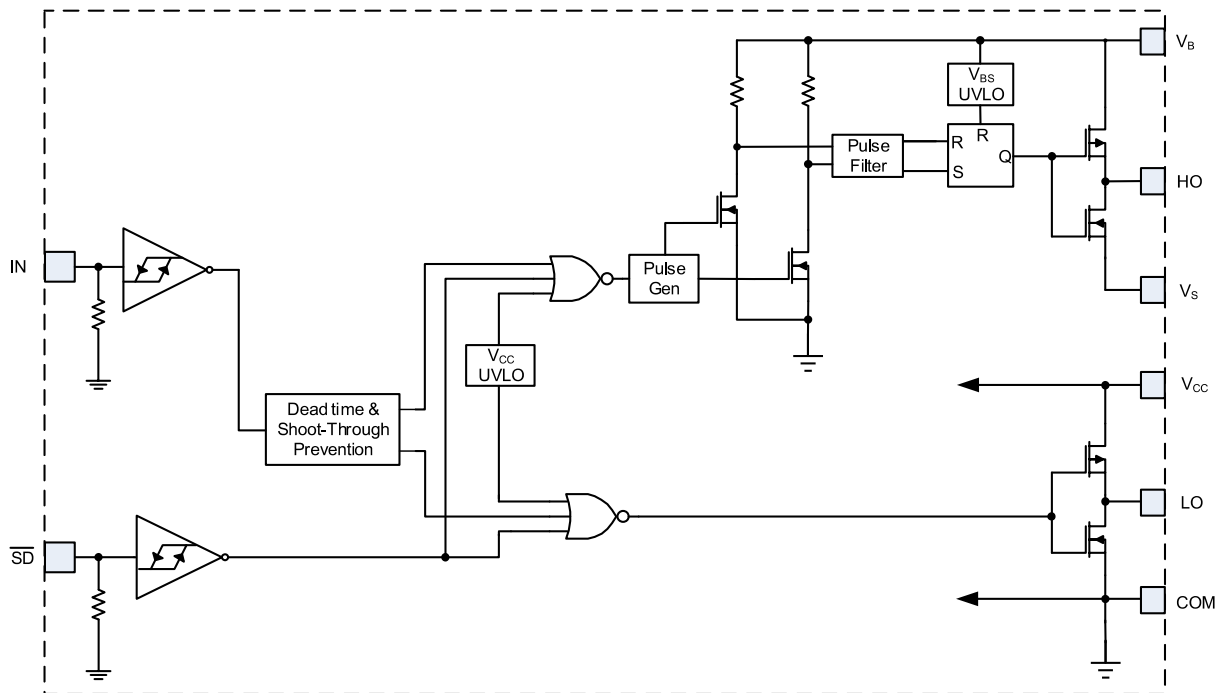
4. Pin Configuration



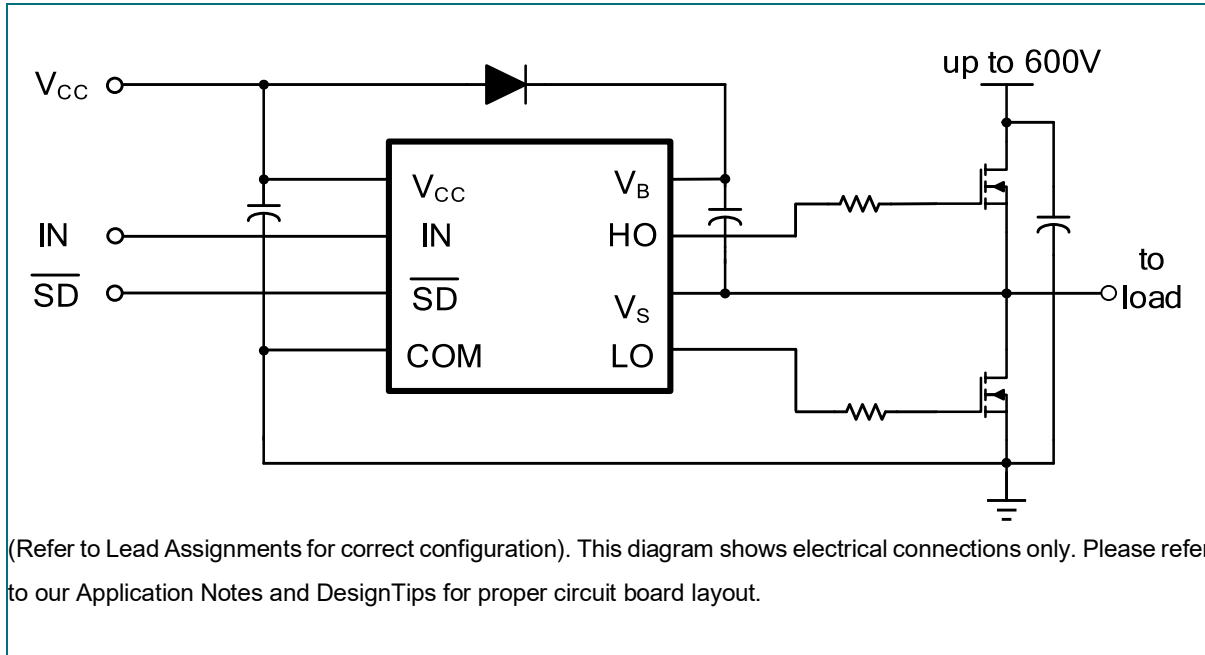
5. Pin Description

No.	Pin	Description
1	V _{CC}	Low-side and logic fixed supply
2	IN	Logic input for high-side and low-side gate driver outputs (HO and LO), in phase with HO
3	$\overline{\text{SD}}$	Logic input for shutdown
4	COM	Low-side return
5	LO	Low-side gate drive output
6	V _S	High-side floating supply return
7	HO	High-side gate drive output
8	V _B	High-side floating supply

6. Functional Block Diagram



7. Typical Application Circuit



8. DYNAMIC ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{CC} , V_{BS}) = 15 V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{on}	Turn-on propagation delay	$V_S = 0$ V	---	680	820	ns
t_{off}	Turn-off propagation delay	$V_S = 600$ V	---	150	220	
t_{sd}	Shutdown propagation delay		---	160	220	
t_r	Turn-on rise time		---	70	170	
t_f	Turn-off fall time		---	35	90	
DT	Deadtime, LS turn-off to HS turn-on & HS turn-on to LS turn-off		400	520	650	
MT	Delay matching, HS & LS turn-on/off		---	---	60	

9. STATIC ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{CC} , V_{BS}) = 15 V and T_A = 25°C unless otherwise specified. The V_{IN} , V_{TH} , and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	Logic "1" input voltage	$V_{CC} = 10\text{ V to }20\text{ V}$	2.5	---	---	V
V_{IL}	Logic "0" input voltage		---	---	0.8	
$V_{SD, TH+}$	SD input positive going threshold		2.5	---	---	
$V_{SD, TH-}$	SD input negative going threshold		---	---	0.8	
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	$I_O = 2\text{ mA}$	---	0.05	0.2	
V_{OL}	Low level output voltage, V_O		---	0.02	0.1	
I_{LK}	Offset supply leakage current	$V_B = V_S = 600\text{ V}$	---	---	50	μA
I_{QBS}	Quiescent V_{BS} supply current	$V_{IN} = 0\text{ V or }5\text{ V}$	---	60	75	
I_{QCC}	Quiescent V_{CC} supply current		---	170	270	
I_{IN+}	Logic "1" input bias current	$V_{IN} = 5\text{ V}$	---	3	10	
I_{IN-}	Logic "0" input bias current	$V_{IN} = 0\text{ V}$	---	---	5	
V_{CCUV+} V_{BSUV+}	V_{CC} & V_{BS} supply undervoltage positive going threshold		8	8.9	9.8	V
V_{CCUV-} V_{BSUV-}	V_{CC} & V_{BS} supply undervoltage negative going threshold		7.4	8.2	9	
I_{O+}	Output high short circuit pulsed current	$V_O = 0\text{ V}$, $V_{IN} = V_{IH}$ $P_W \leq 10\ \mu\text{s}$	130	290		mA
I_{O-}	Output low short circuit pulsed current	$V_O = 15\text{ V}$, $V_{IN} = V_{IL}$ $P_W \leq 10\ \mu\text{s}$	270	600		

10. DETAILED INFORMATION

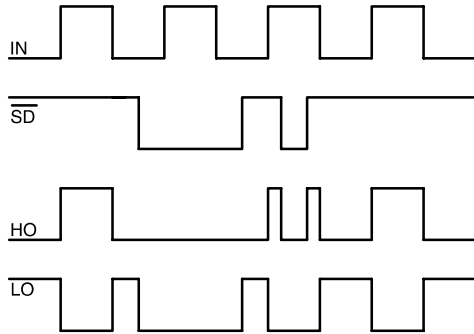


Figure 1. Input/Output Timing Diagram

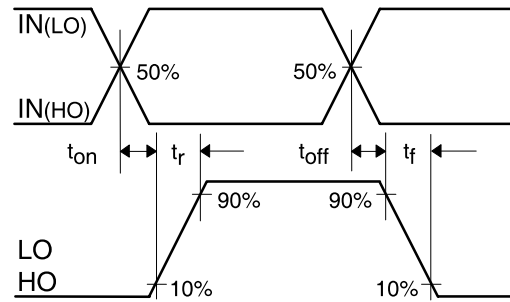


Figure 2. Switching Time Waveform Definitions

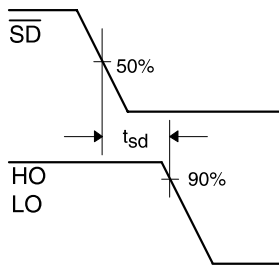


Figure 3. Shutdown Waveform Definitions

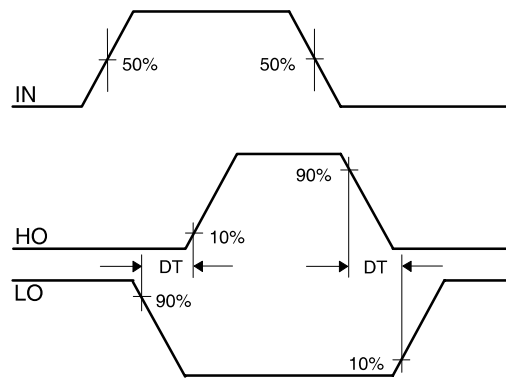


Figure 4. Deadtime Waveform Definitions

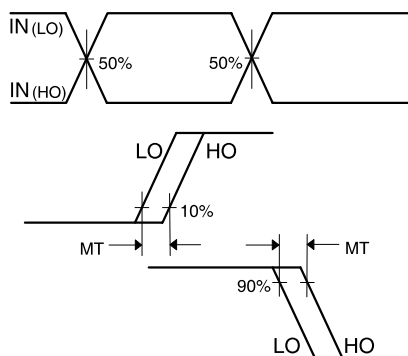
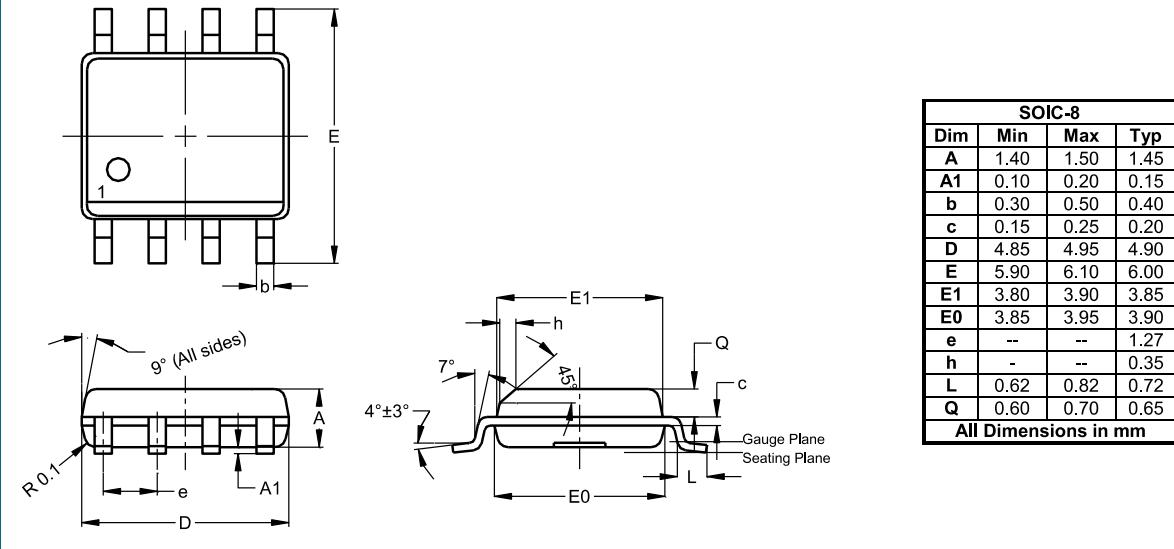


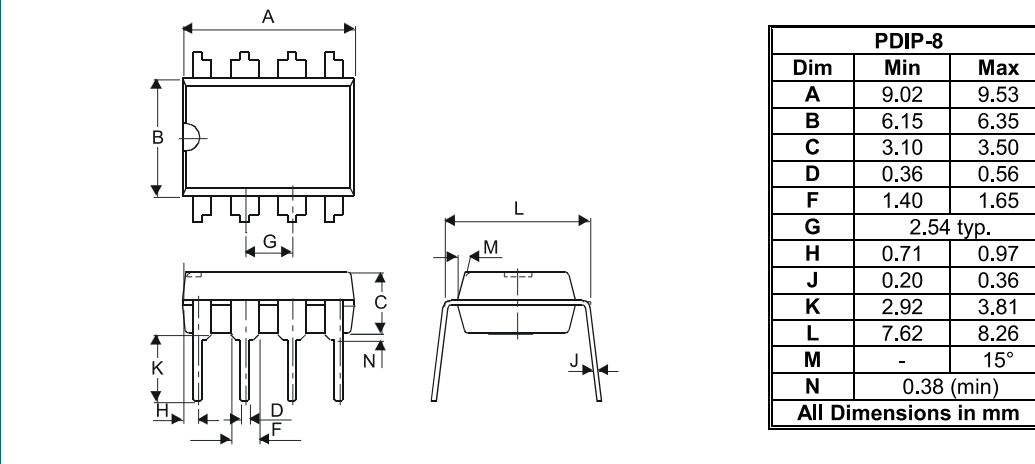
Figure 5. Delay Matching Waveform Definitions

11. Package Outlines

SOIC-8



DIP-8



12. Disclaimers

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