Rail-to-Rail Input/Output, 10 MHz Op Amps

1. Description

This production is wideband, low-noise, low-distortion dual operational amplifier, that offer rail-to-rail inputs/outputs and single supply operation down to 2.2V. They draw 1.6mA of quiescent supply current while featuring ultra-low distortion (0.0002% THD+N), as well as low input voltage-noise density (15nV/Hz) and low input current noise density (0.5fA/Hz). These features make the devices an ideal choice for applications that require low distortion and/or low noise.

These amplifiers have inputs and outputs which swing rail-to-rail and their input common mode voltage range includes ground. The maximum input offset of these amplifiers is less than 5mV.

This production is unity gain stable with a gain-band width of 10MHz. The extended temperature range of -40°C to +125°C over all supply voltages offers additional design flexibility.

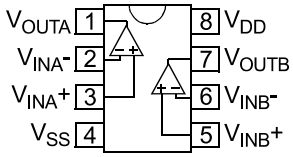
2. Features

- Single-Supply Operation from +2.2V ~ +5.5V
- Rail-to-Rail Input / Output
- Gain-Bandwidth Product: 10MHz (Typ.)
- Low Input Bias Current: 10pA (Typ.)
- Low Offset Voltage: 5mV (Max.)
- Quiescent Current: 800μA per Amplifier (Typ.)
- Operating Temperature: -40°C to +125°C

3. Applications

- Portable Equipment
- Mobile Communications
- Smoke Detector
- Sensor Interface
- Medical Instrumentation

4. Pinning Configuration



5. Ordering Information

Type Number	Package Type	Packing
MCP6022T-I/SN	SOIC-8	Tape & Reel
MCP6022T-E/SN	SOIC-8	Tape & Reel
MCP6022T-I/ST	TSSOP-8	Tape & Reel
MCP6022T-E/ST	TSSOP-8	Tape & Reel
MCP6022-I/P	DIP-8	Tube
MCP6022-E/P	DIP-8	Tube

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

6. Absolute Maximum Ratings

Condition	Min	Max
Power Supply Voltage (V_{DD} to V_{ss})	-0.5V	+7V
Analog Input Voltage (IN+ or IN-)	Vss-0.5V	V=+0.5V
PDB Input Voltage	Vss-0 .5V	+7V
Operating Temperature Range	-40°C	+125°C
Junction Temperature	+150°C	
Storage Temperature Range	-65°C	+150°C
Lead Temperature (soldering, 10sec)	+300°C	
Package Thermal Resistance (T_A=+25°C)		

7. Electrical Characteristics

(V_{DD} = +5V, V_{ss} = 0V, V_{CM} =0V, V_{OUT} = V_{DD}/2, R_L=100K tied to V_{DD}/2, SHDNB = V_{DD}, T_A = -40°C to +125°C，unless otherwise noted. Typical values are at T_A =+25°C) (Notes 1)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply Voltage Range	V_{DD}	Guaranteed by the PSRR test	2.2		5.5	V
Quiescent Supply Current (per Amplifier)	I_{DD}	V_{DD} = 3V		0.8		mA
		V_{DD} = 5V		0.8	1 .2	
Input Offset Voltage	V_{OS}	T_A = 25°C			土5	mV
		T_A =-40°C to +85°C				
		T_A =-40°C to +125°C			土1.5	
Input Offset Voltage Tempco	$\Delta V_{OS}/\Delta T$			±0.3	±6	μV / 它
Input Bias Current	I_B	(Note 3)		土1	土100	pA
Input Offset Current	I_{OS}	(Note 3)		土1	土100	pA
Input Common-Mode Voltage Range	V_{CM}	Guaranteed by the T_A =-40°C to +125°C	-。0.2		Voo+0.2	V
		CMRR test T_A = -40 ° C to +125°C			VD DO	
Common-Mode Rejection Ratio	CMRR	Vss-0.2V⩽V_{CM}⩽V_{DD}+0.2V T_A = 25°C		75		dB
		Vss⩽V_{CM}⩽5V T_A = +25°C	65	80		
		Vss-0.2V⩽V_{CM}⩽V_{DD}+0.2V T_A = -40°C to +125°C		65		
Power-Supply Rejection Ratio	PSRR	V_{DD} = +2.2V to +5.5V	75	90		dB
Open-Loop Voltage Gain	A_V	R_L=100kΩ to V_{DD}/2, 100mV⩽V_O⩽V_{DD} -125mV	90	100		dB
		R_L=1kΩ to V_{DD}/2, 200mV⩽V_O ⩽V_{DD} -250mV	75	85		
		R_L=500Ω to V_{DD}/2, 350mV⩽V_O ⩽V_{DD} -500mV	55	65		

Output Voltage Swing	V_{OUT}	$\|V_{IN+} - V_{IN-}\| \geqslant 10mV$ V_{DD} - V_{OH}		10	35	mV
		R_L = 10kΩ to $V_{DD}/2$ V_{OL}-V_{SS}		10	30	
		$\|V_{IN+} - V_{IN-}\| \geqslant 10mV$ V_{DD} - V_{OH}		80	200	
		R_L = 1kΩ to $V_{DD}/2$ V_{OL}-V_{SS}		50	150	
		$\|V_{IN+} - V_{IN-}\| \geqslant 10mV$ V_{DD} - V_{OH}		100	350	
		R_L =500Ω to $V_{DD}/2$ V_{OL}-V_{SS}		80	260	
Output Short-Circuit Current	I_{SC}	Sinking or Sourcing		±50		mA
PDB Logic Low	V_{IL}				0.8	V
PDB Logic High	V_{IH}		2			V
Turn-On Time	T_{ON}			2.2		μs
Turn-Off Time	T_{OFF}			0.8		μs
Output Leakage Current	I_{LEAK}	Shutdown Mode (PDB = V_{SS}), V_{OUT} = V_{SS} to V_{DD}		±0.001	⊥ 1.0	μA
Input Capacitance	C_{IN}			10		pF
Gain Bandwidth Product	GBW	A_V= +1V/V		10		MHz
Slew Rate	SR	A_V= +1V/V		4.5		V/μs
Full Power Bandwidth		A_V= +1V/V		0.4		MHz
Phase Margin	Φ_m	A_V= +1V/V		55		deg
Gain Margin	G_m	A_V= +1V/V		12		dB
Settling Time	t_s	To 0.01%, V_{OUT} = 2V step Av = +1V/V		1		μs
Capacitive-Load Stability	C_{LOAD}	No sustained oscillations. Av= +1V/V		200		pF
Peak-to-Peak Input Noise Voltage (Note 5)	e_n(p-p)	f = 0.1Hz to 10Hz		5		μVp-p
Input Voltage Noise Density	e_n	f = 10Hz		60		nV/$\sqrt{Hz}$
		f = 1kHz		30		
		f = 30kHz		15		
Input Current Noise Density	I_n	f = 1kHz				fA/$\sqrt{Hz}$
Total Harmonic Distortion plus Noise	THD+N	V_{OUT} = 2Vp-p,				%
		A_V = +1V/N, f = 1kHz		0.0001		
		RL = 10kΩ to GND f = 20kHz		0.002		
		V_{OUT} = 2Vp-p,				

		A_V= +1V/V, f = 1kHz		0.0002		
		RL = 1kΩ to GND f = 20kHz		0.004		

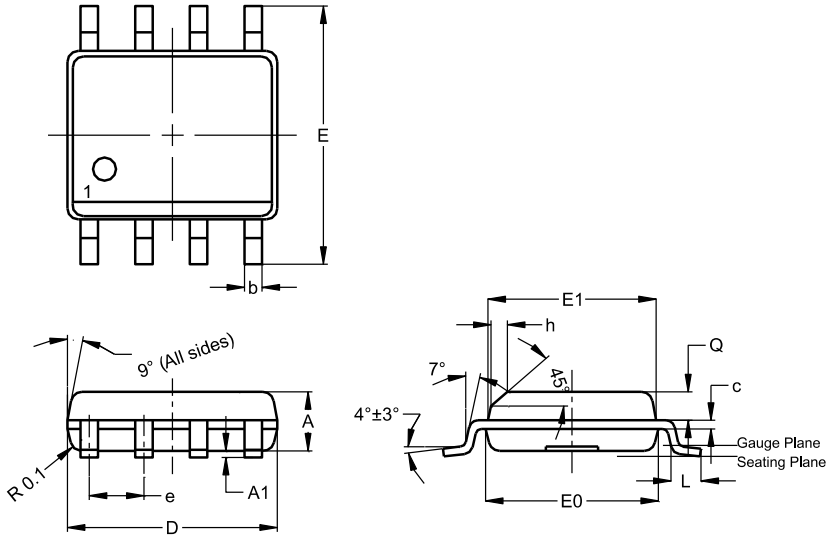
Note1: All devices are 100% production tested at T_A = +25°C, all specifications over the automotive temperature range are guaranteed by design, not production tested.

Note2: Parameter is guaranteed by design.

Note3: Peak-to-peak input noise voltage is defined as six times RMS value of input noise voltage

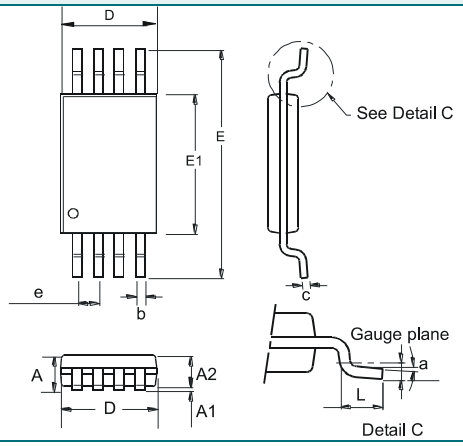
8. Package Outlines

SOIC-8



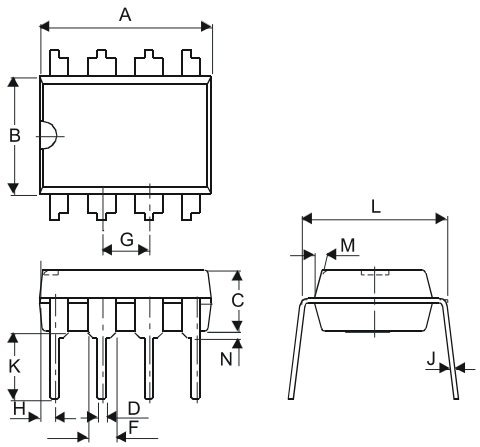
SOIC-8			
Dim	Min	Max	Typ
A	1.40	1.50	1.45
A1	0.10	0.20	0.15
b	0.30	0.50	0.40
c	0.15	0.25	0.20
D	4.85	4.95	4.90
E	5.90	6.10	6.00
E1	3.80	3.90	3.85
E0	3.85	3.95	3.90
e	--	--	1.27
h	-	--	0.35
L	0.62	0.82	0.72
Q	0.60	0.70	0.65
All Dimensions in mm			

TSSOP-8



TSSOP-8			
Dim	Min	Max	Typ
a	0.09	–	–
A	–	1.20	–
A1	0.05	0.15	–
A2	0.825	1.025	0.925
b	0.19	0.30	–
c	0.09	0.20	–
D	2.90	3.10	3.025
e	–	–	0.65
E	–	–	6.40
E1	4.30	4.50	4.425
L	0.45	0.75	0.60
All Dimensions in mm			

DIP-8



PDIP-8		
Dim	**Min**	**Max**
A	9.02	9.53
B	6.15	6.35
C	3.10	3.50
D	0.36	0.56
F	1.40	1.65
G	2.54 typ.	
H	0.71	0.97
J	0.20	0.36
K	2.92	3.81
L	7.62	8.26
M	-	15°
N	0.38 (min)	
All Dimensions in mm		

9. Disclaimers

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