Datasheet

APM32F405xG
APM32F407xExG

Arm® Cortex® -M4 core-based 32-bit MCU

Version: V1.1

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1 Product Characteristics

Core
- 32-bit Arm® Cortex®-M4 core with FPU
- Up to 168MHz working frequency

Memory and interface
- Flash: The capacity is up to 1MB
- SRAM: System (192KB) + backup (4KB)
- EMMC: Support CF card, SRAM, PSRAM, SDRAM, NOR and NAND memories

Clock
- HSECLK: 4~26MHz external crystal/ceramic oscillator supported
- LSECLK: 32.768KHz crystal/ceramic oscillator supported
- HSICLK: 16MHz RC oscillator calibrated by factory
- LSICLK: 28KHz RC oscillator supported
- PLL1: Phase locked loop; output frequency is configured by four parameters
- PLL2: Phase locked loop specially used to provide clock signals to I2S; output frequency is configured by three parameters

Reset and power management
- V_{DD} range: 1.8～3.6V
- V_{DDA} range: 1.8～3.6V
- V_{BAT} range of backup domain power supply: 1.65V～3.6V
- Power-on/power-down/brown-out reset (POR/PDR/BOR) supported
- Programmable power supply voltage detector (PVD) supported

Low-power mode
- Sleep, stop and standby modes supported

DMA
- Two DMA; each DMA has 8 data streams, 16 in total

Debugging interface
- JTAG
- SWD

I/O
- Up to 140 I/O
- All I/O can be mapped to external interrupt vector
- Up to 138 FT input I/O

Communication peripherals
- 4 USART, 2 UART, supporting ISO7816, LIN and IrDA functions
- 3 I2C, supporting SMBus/PMBus
- 3 SPI (2 reusable I2S)
- 2 CAN
- 3 USB_OTG controllers
- 1 SDIO interface

Analog peripherals
- 3 12-bit ADCs
- 2 12-bit DACs

Timer
- 2 16-bit advanced timers TMR1/8 that can provide 7-channel PWM output, support dead zone generation and braking input functions
- 2 32-bit general-purpose timers TMR2/5, each with up to 4 independent channels to support input capture, output comparison, PWM, pulse count and other functions
- 8 16-bit general-purpose timers TMR/3/4/9/10/11/12/13/14, each with up to 2 independent channels to support input capture, output comparison, PWM, pulse count and other functions
- 2 16-bit basic timers TMR6/7
- 2 watchdog timers: one independent watchdog IWDT and one window watchdog WWDT
- 1 24-bit autodecrement SysTick Timer

RTC
- Support calendar function
- Alarm and regular wake-up from stop/standby mode

CRC computing unit

96-bit unique device ID

Contents

Figure 2 Distribution Diagram of APM32F405xG 407xExG Series LQFP144 Pins

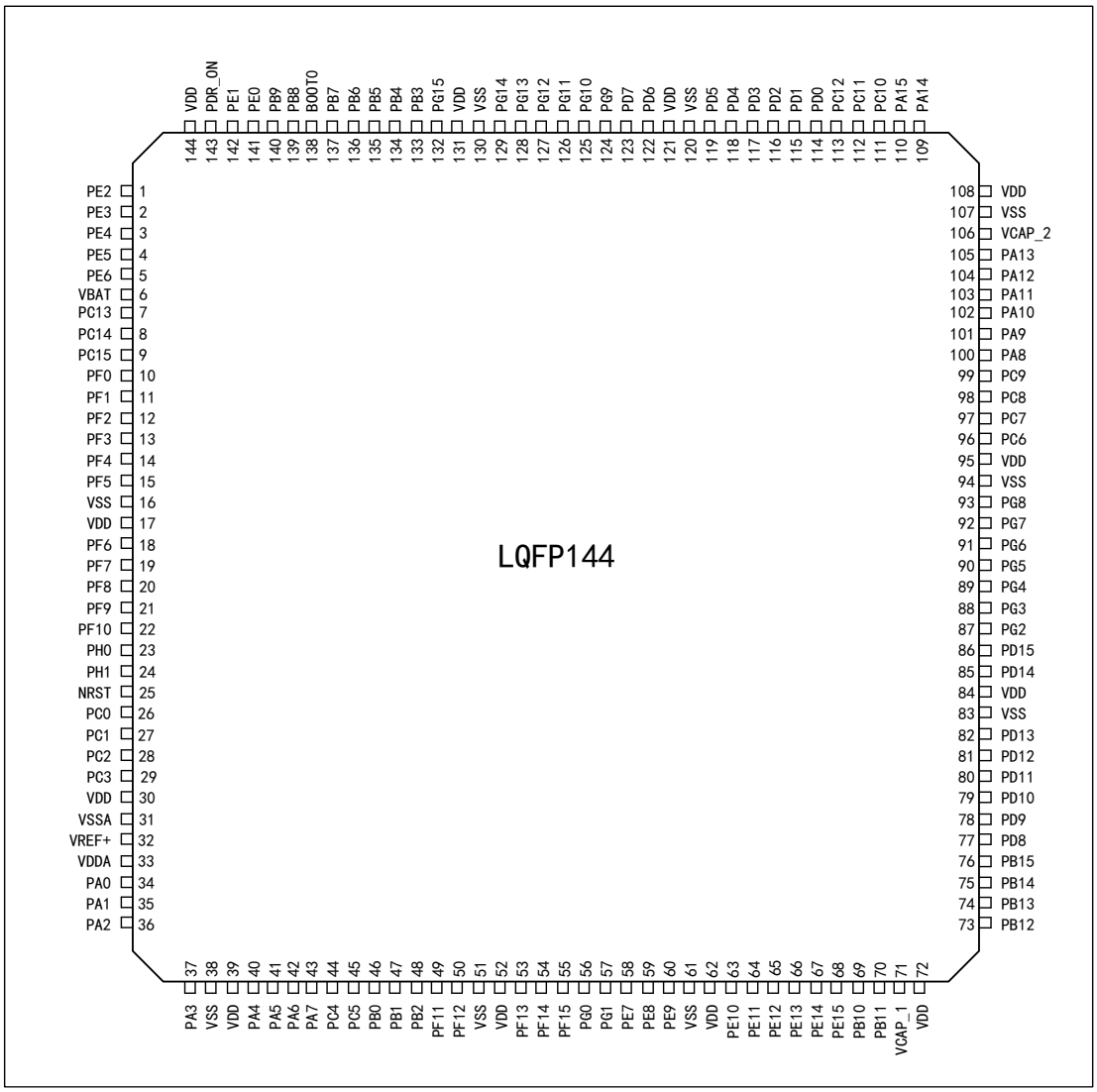


Figure 3 Distribution Diagram of APM32F405xG 407xExG Series LQFP100 Pins

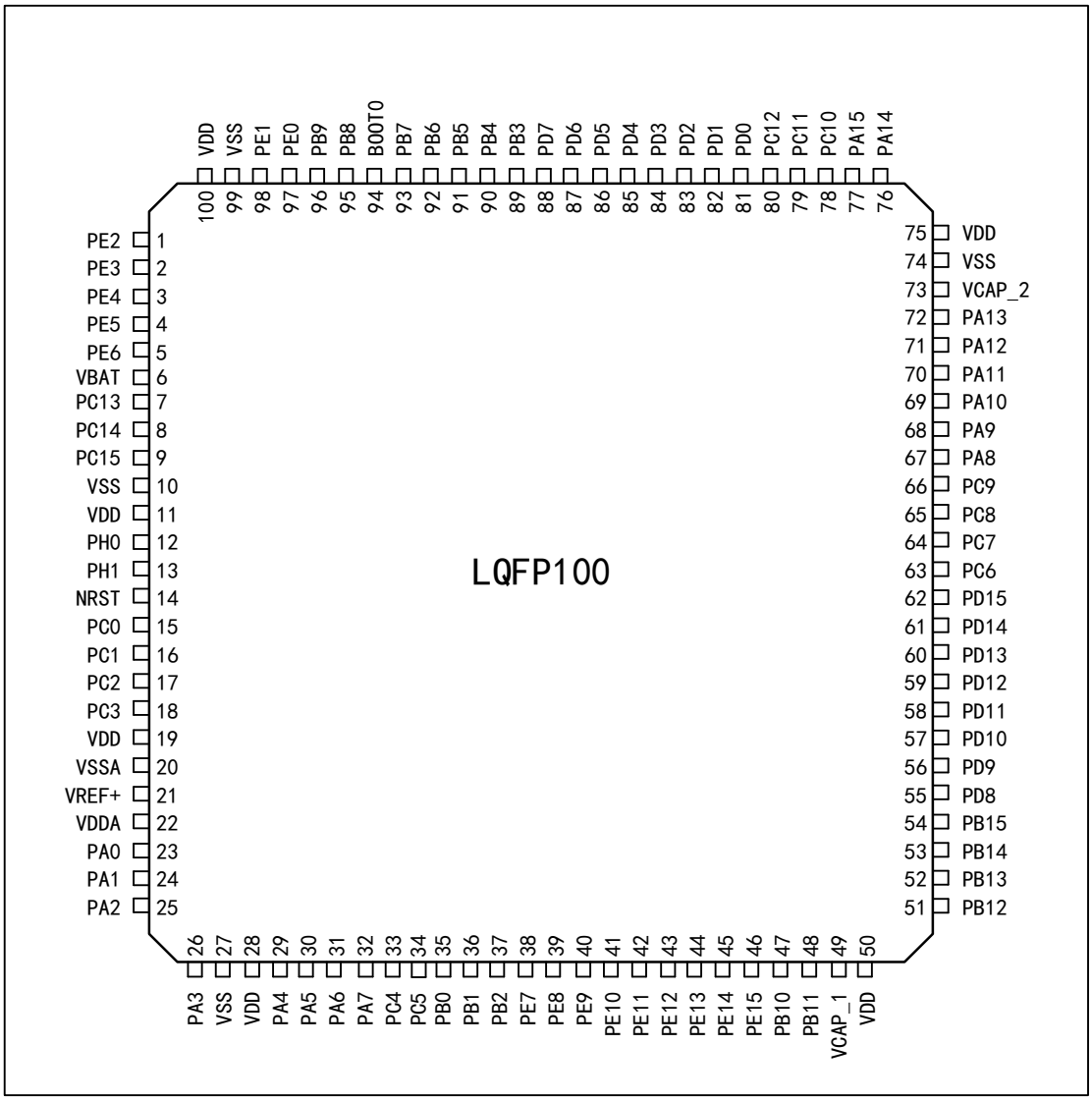
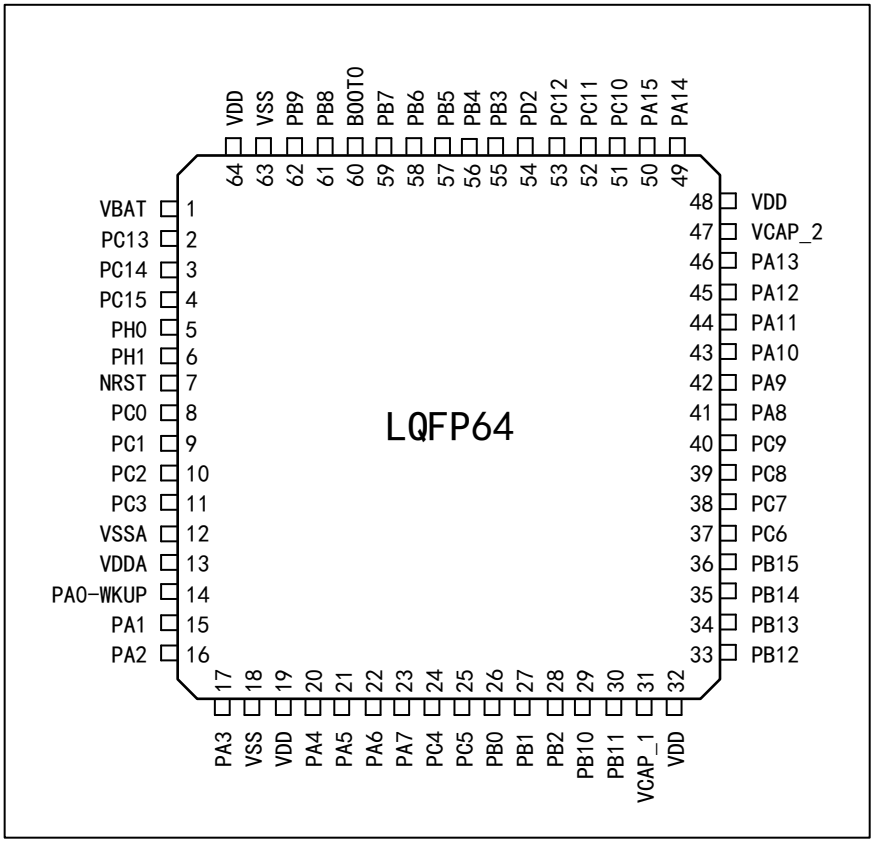


Figure 4 Distribution Diagram of APM32F405xG 407xExG Series LQFP64 Pins



3.2 Pin function description

Table 2 Legends/Abbreviations Used in Output Pin Table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in parentheses below the pin name, the pin functions during and after reset are the same as the actual pin name	
Pin type		P	Power pin
		I	Only input pin
		I/O	I/O pin
I/O structure		5T	FT I/O
		STDA	3.3V standard I/O, directly connected to ADC
		STD	3.3V standard I/O
		B	Dedicated Boot0 pin
		RST	Bidirectional reset pin with built-in pull-up resistor
Notes		Unless otherwise specified in the notes, all I/O is set as floating input during and after reset	
Pin function	Default multiplexing function	Function directly selected/enabled through peripheral register	

Name		Abbreviation	Definition
	Redefining function	Select this function through AFIO remapping register	

Table 3 Description of APM32F405xG 407xExG by Pin Number

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	LQFP64	LQFP100	LQFP144	LQFP176
PE2	I/O	5T	TRACECK, SMC_A23, ETH_MII_TXD3, EVENTOUT	-	-	1	1	1
PE3	I/O	5T	TRACED0, SMC_A19, EVENTOUT	-	-	2	2	2
PE4	I/O	5T	TRACED1, SMC_A20, DCI_D4, EVENTOUT	-	-	3	3	3
PE5	I/O	5T	TRACED2, SMC_A21, TMR9_CH1, DCI_D6, EVENTOUT	-	-	4	4	4
PE6	I/O	5T	TRACED3, SMC_A22, TMR9_CH2, DCI_D7, EVENTOUT	-	-	5	5	5
VBAT	P	-	-	-	1	6	6	6
PI8	I/O	5T	EVENTOUT	RTC_TAMP1, RTC_TAMP2, RTC_TS	-	-	-	7
PC13	I/O	5T	EVENTOUT	RTC_OUT, RTC_TAMP1, RTC_TS	2	7	7	8
PC14- OSC32_IN（PC14）	I/O	5T	EVENTOUT	OSC32_IN	3	8	8	9
PC15- OSC32_OUT（PC15）	I/O	5T	EVENTOUT	OSC32_OUT	4	9	9	10
PI9	I/O	5T	CAN1_RX, EVENTOUT	-	-	-	-	11
PI10	I/O	5T	ETH_MII_RX_ER, EVENTOUT	-	-	-	-	12

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	LQFP64	LQFP100	LQFP144	LQFP176
PI11	I/O	5T	OTG_HS_ULPI_DIR, EVENTOUT	-	-	-	-	13
VSS	P	-	-	-	-	-	-	14
VDD	P	-	-	-	-	-	-	15
PF0	I/O	5T	SMC_A0, I2C2_SDA, EVENTOUT	-	-	-	10	16
PF1	I/O	5T	SMC_A1, I2C2_SCL, EVENTOUT	-	-	-	11	17
PF2	I/O	5T	SMC_A2, I2C2_SMBAI, EVENTOUT	-	-	-	12	18
PF3	I/O	5T	SMC_A3, EVENTOUT	ADC3_IN9	-	-	13	19
PF4	I/O	5T	SMC_A4, EVENTOUT	ADC3_IN14	-	-	14	20
PF5	I/O	5T	SMC_A5, EVENTOUT	ADC3_IN15	-	-	15	21
VSS	P	-	-	-	-	10	16	22
VDD	P	-	-	-	-	11	17	23
PF6	I/O	5T	TMR10_CH1, SMC_NIORD, EVENTOUT	ADC3_IN4	-	-	18	24
PF7	I/O	5T	TMR11_CH1, SMC_NREG, EVENTOUT	ADC3_IN5	-	-	19	25
PF8	I/O	5T	TMR13_CH1, SMC_NIOWR, EVENTOUT	ADC3_IN6	-	-	20	26
PF9	I/O	5T	TMR14_CH1, SMC_CD, EVENTOUT	ADC3_IN7	-	-	21	27
PF10	I/O	5T	SMC_INTR, EVENTOUT	ADC3_IN8	-	-	22	28
PH0-OSC_IN (PH0)	I/O	5T	EVENTOUT	OSC_IN	5	12	23	29
PH1-OSC_OUT (PH1)	I/O	5T	EVENTOUT	OSC_OUT	6	13	24	30

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	LQFP64	LQFP100	LQFP144	LQFP176
NRST	I/O	RST	-	-	7	14	25	31
PC0	I/O	5T	OTG_HS_ULPI_STP, EVENTOUT	ADC123_IN10	8	15	26	32
PC1	I/O	5T	ETH_MDC, EVENTOUT	ADC123_IN11	9	16	27	33
PC2	I/O	5T	SPI2_MISO, OTG_HS_ULPI_DIR, ETH_MII_TXD2, I2S2ext_SD, EVENTOUT	ADC123_IN12	10	17	28	34
PC3	I/O	5T	SPI2_MOSI, I2S2_SD, OTG_HS_ULPI_NXT, ETH_MII_TX_CLK, EVENTOUT	ADC123_IN13	11	18	29	35
VDD	P	-	-	-	-	19	30	36
VSSA	P	-	-	-	12	20	31	37
VREF+	P	-	-	-	-	21	32	38
VDDA	P	-	-	-	13	22	33	39
PA0-WKUP (PA0)	I/O	5T	USART2_CTS, UART4_TX, ETH_MII_CRS, TMR2_CH1_ETR, TMR5_CH1, TMR8_ETR, EVENTOUT	WKUP, ADC123_IN0	14	23	34	40
PA1	I/O	5T	USART2_RTS, UART4_RX, ETH_RMII_REF_CLK, ETH_MII_RX_CLK, TMR5_CH2, TMR2_CH2, EVENTOUT	ADC123_IN1	15	24	35	41
PA2	I/O	5T	USART2_TX, TMR5_CH3, TMR9_CH1, TMR2_CH3, ETH_MDIO, EVENTOUT	ADC123_IN2	16	25	36	42

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	LQFP64	LQFP100	LQFP144	LQFP176
PH2	I/O	5T	ETH_MII_CRS, EVENTOUT	-	-	-	-	43
PH3	I/O	5T	ETH_MII_COL, EVENTOUT	-	-	-	-	44
PH4	I/O	5T	I2C2_SCL, OTG_HS_ULPI_NXT, EVENTOUT	-	-	-	-	45
PH5	I/O	5T	I2C2_SDA, EVENTOUT	-	-	-	-	46
PA3	I/O	5T	USART2_RX, TMR5_CH4, TMR9_CH2, TMR2_CH4, OTG_HS_ULPI_D0, ETH_MII_COL, EVENTOUT	ADC123_IN3	17	26	37	47
VSS	P	-	-	-	18	27	38	-
BYPASS_REG	I	5T	-	-	-	-	-	48
VDD	P	-	-	-	19	28	39	49
PA4	I/O	STDA	SPI1_NSS, SPI3_NSS, USART2_CK, DCI_HSYNC, OTG_HS_SOF, I2S3_WS, EVENTOUT	DAC_OUT1, ADC12_IN4	20	29	40	50
PA5	I/O	STDA	SPI1_SCK, OTG_HS_ULPI_CK, TMR2_CH1_ETR, TMR8_CH1N, EVENTOUT	DAC_OUT2, ADC12_IN5	21	30	41	51
PA6	I/O	5T	SPI1_MISO, TMR8_BKIN, TMR13_CH1, DCI_PIXCLK, TMR3_CH1, TMR1_BKIN, EVENTOUT	ADC12_IN6	22	31	42	52
PA7	I/O	5T	SPI1_MOSI,	ADC12_IN7	23	32	43	53

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	LQFP 64	LQFP 100	LQFP 144	LQFP 176
			DMC_DQ14, TMR4_CH4, EVENTOUT					
PG2	I/O	5T	SMC_A12, DMC_DQ15, EVENTOUT	-	-	-	87	106
PG3	I/O	5T	SMC_A13, DMC_DQ0, EVENTOUT	-	-	-	88	107
PG4	I/O	5T	SMC_A14, DMC_DQ1, EVENTOUT	-	-	-	89	108
PG5	I/O	5T	SMC_A15, DMC_DQ2, EVENTOUT	-	-	-	90	109
PG6	I/O	5T	SMC_INT2, DMC_DQ3 EVENTOUT	-	-	-	91	110
PG7	I/O	5T	SMC_INT3, USART6_CK, EVENTOUT	-	-	-	92	111
PG8	I/O	5T	DMC_DQ4 USART6_RTS, ETH_PPS_OUT, EVENTOUT	-	-	-	93	112
VSS	P	-	-	-	-	-	94	113
VDD	P	-	-	-	-	-	95	114
PC6	I/O	5T	I2S2_MCK, TMR8_CH1, SDIO_D6, USART6_TX, DCI_D0, TMR3_CH1, EVENTOUT	-	37	63	96	115
PC7	I/O	5T	I2S3_MCK, TMR8_CH2, SDIO_D7, USART6_RX, DCI_D1, TMR3_CH2,	-	38	64	97	116

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	LQFP 64	LQFP 100	LQFP 144	LQFP 176
			EVENTOUT					
PC8	I/O	5T	TMR8_CH3, SDIO_D0, TMR3_CH3, USART6_CK, DCI_D2, EVENTOUT	-	39	65	98	117
PC9	I/O	5T	I2S_CKIN, MCO2, TMR8_CH4, SDIO_D1, I2C3_SDA, DCI_D3, TMR3_CH4, EVENTOUT	-	40	66	99	118
PA8	I/O	5T	USART1_CK, TMR1_CH1, MCO, I2C3_SCL, OTG_FS_SOF, EVENTOUT	-	41	67	100	119
PA9	I/O	5T	USART1_TX, TMR1_CH2, I2C3_SMBAI, DCI_D0, EVENTOUT	OTG_FS_VBUS	42	68	101	120
PA10	I/O	5T	USART1_RX, TMR1_CH3, OTG_FS_ID, DCI_D1, EVENTOUT	-	43	69	102	121
PA11	I/O	5T	USART1_CTS, CAN1_RX, TMR1_CH4, OTG_FS_DM, EVENTOUT	-	44	70	103	122
PA12	I/O	5T	USART1_RTS, CAN1_TX, TMR1_ETR, OTG_FS_DP,	-	45	71	104	123

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	LQFP 64	LQFP 100	LQFP 144	LQFP 176
			EVENTOUT					
PA13 (JTMS-SWDIO)	I/O	5T	JTMS-SWDIO, EVENTOUT	PA13	46	72	105	124
VCAP_2	P	-	-	-	47	73	106	125
VSS	P	-	-	-	-	74	107	126
VDD	P	-	-	-	48	75	108	127
PH13	I/O	5T	TMR8_CH1N, CAN1_TX, EVENTOUT, DMC_DQ5	-	-	-	-	128
PH14	I/O	5T	TMR8_CH2N, DCI_D4, EVENTOUT	-	-	-	-	129
PH15	I/O	5T	TMR8_CH3N, DCI_D11, EVENTOUT, DMC_DQ6	-	-	-	-	130
PI0	I/O	5T	TMR5_CH4, SPI2_NSS, I2S2_WS, DCI_D13, EVENTOUT	-	-	-	-	131
PI1	I/O	5T	SPI2_SCK, I2S2_CK, DCI_D8, EVENTOUT	-	-	-	-	132
PI2	I/O	5T	TMR8_CH4, SPI2_MISO, DCI_D9, I2S2ext_SD, EVENTOUT	-	-	-	-	133
PI3	I/O	5T	TMR8_ETR, SPI2_MOSI, I2S2_SD, DCI_D10, EVENTOUT, DMC_DQ7	-	-	-	-	134
VSS	P	-	-	-	-	-	-	135
VDD	P	-	-	-	-	-	-	136

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	LQFP 64	LQFP 100	LQFP 144	LQFP 176
PA14 (JTCK/SWCLK)	I/O	5T	JTCK-SWCLK, EVENTOUT	-	49	76	109	137
PA15 (JTDI)	I/O	5T	JTDI, SPI3_NSS, I2S3_WS, TMR2_CH1_ETR, SPI1_NSS, EVENTOUT	-	50	77	110	138
PC10	I/O	5T	SPI3_SCK, I2S3_CK, UART4_TX, SDIO_D2, DCI_D8, USART3_TX, EVENTOUT	-	51	78	111	139
PC11	I/O	5T	UART4_RX, SPI3_MISO, SDIO_D3, DCI_D4, USART3_RX, I2S3ext_SD, EVENTOUT	-	52	79	112	140
PC12	I/O	5T	UART5_TX, SDIO_CK, DCI_D9, SPI3_MOSI, I2S3_SD, USART3_CK, EVENTOUT	-	53	80	113	141
PD0	I/O	5T	SMC_D2, CAN1_RX, EVENTOUT	-	-	81	114	142
PD1	I/O	5T	SMC_D3, CAN1_TX, EVENTOUT	-	-	82	115	143
PD2	I/O	5T	TMR3_ETR, UART5_RX, SDIO_CMD, DCI_D11, EVENTOUT	-	54	83	116	144

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	LQFP 64	LQFP 100	LQFP 144	LQFP 176
PD3	I/O	5T	SMC_CLK, USART2_CTS, EVENTOUT	-	-	84	117	145
PD4	I/O	5T	SMC_NOE, USART2_RTS, EVENTOUT	-	-	85	118	146
PD5	I/O	5T	SMC_NWE, USART2_TX, EVENTOUT	-	-	86	119	147
VSS	P	-	-	-	-	-	120	148
VDD	P	-	-	-	-	-	121	149
PD6	I/O	5T	SMC_NWAIT, USART2_RX, EVENTOUT	-	-	87	122	150
PD7	I/O	5T	SMC_NE1, SMC_NCE2, USART2_CK, EVENTOUT	-	-	88	123	151
PG9	I/O	5T	SMC_NE2, SMC_NCE3, USART6_RX, EVENTOUT	-	-	-	124	152
PG10	I/O	5T	SMC_NCE4_1, SMC_NE3, EVENTOUT	-	-	-	125	153
PG11	I/O	5T	SMC_NCE4_2, ETH_MII_TX_EN, ETH_RMII_TX_EN, EVENTOUT	-	-	-	126	154
PG12	I/O	5T	SMC_NE4, USART6_RTS, EVENTOUT	-	-	-	127	155
PG13	I/O	5T	SMC_A24, USART6_CTS, ETH_MII_TXD0, ETH_RMII_TXD0, EVENTOUT	-	-	-	128	156
PG14	I/O	5T	SMC_A25, USART6_TX, ETH_MII_TXD1,	-	-	-	129	157

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	LQFP 64	LQFP 100	LQFP 144	LQFP 176
			ETH_RMII_TXD1, EVENTOUT					
VSS	P	-	-	-	-	-	130	158
VDD	P	-	-	-	-	-	131	159
PG15	I/O	5T	DMC_LDQM, USART6_CTS, DCI_D13, EVENTOUT	-	-	-	132	160
PB3 (JTDO/TRACESWO)	I/O	5T	JTDO, TRACESWO, SPI3_SCK, I2S3_CK, TMR2_CH2, SPI1_SCK, EVENTOUT	-	55	89	133	161
PB4 (NJTRST)	I/O	5T	NJTRST, SPI3_MISO, TMR3_CH1, SPI1_MISO, I2S3ext_SD, EVENTOUT	-	56	90	134	162
PB5	I/O	-	I2C1_SMBAI, CAN2_RX, OTG_HS_ULPI_D7, ETH_PPS_OUT, TMR3_CH2, SPI1_MOSI, SPI3_MOSI, DCI_D10, I2S3_SD, EVENTOUT	-	57	91	135	163
PB6	I/O	5T	I2C1_SCL, TMR4_CH1, CAN2_TX, DCI_D5, USART1_TX, EVENTOUT	-	58	92	136	164
PB7	I/O	5T	I2C1_SDA, SMC_NL, DCI_VSYNC,	-	59	93	137	165

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	LQFP 64	LQFP 100	LQFP 144	LQFP 176
			USART1_RX, TMR4_CH2, EVENTOUT					
BOOT0	I	B	-	VPP	60	94	138	166
PB8	I/O	5T	TMR4_CH3, SDIO_D4, TMR10_CH1, DCI_D6, ETH_MII_TXD3, I2C1_SCL, CAN1_RX, EVENTOUT	-	61	95	139	167
PB9	I/O	5T	SPI2_NSS, I2S2_WS, TMR4_CH4, TMR11_CH1, SDIO_D5, DCI_D7, I2C1_SDA, CAN1_TX, EVENTOUT	-	62	96	140	168
PE0	I/O	5T	TMR4_ETR, SMC_NBL0, DCI_D2, EVENTOUT	-	-	97	141	169
PE1	I/O	5T	SMC_NBL1, DCI_D3, EVENTOUT	-	-	98	142	170
VSS	P	-	-	-	63	99	-	-
PDR_ON	I	5T	-	-	-	-	143	171
VDD	P	-	-	-	64	100	144	172
PI4	I/O	5T	TMR8_BKIN, DCI_D5, EVENTOUT	-	-	-	-	173
PI5	I/O	5T	TMR8_CH1, DCI_VSYNC, EVENTOUT	-	-	-	-	174
PI6	I/O	5T	TMR8_CH2, DCI_D6,	-	-	-	-	175

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	LQFP 64	LQFP 100	LQFP 144	LQFP 176
			EVENTOUT					
PI7	I/O	5T	TMR8_CH3, DCI_D7, EVENTOUT, DMC_WE	-	-	-	-	176

Note:

(1) PC13, PC14 and PC15 are powered through the power switch. Since the switch only sinks limited current (3mA), the use of GPIO from PC13 to PC15 in output mode is limited:

7 The speed shall not exceed 2MHz when the heavy load is 30pF;

8 Not used for current source (e.g. driving LED).

3.3 GPIO Multiplexing Function Configuration

Table 4 GPIOA Multiplexing Function Configuration

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA0	-	TMR2_CH1_ETR	TMR5_CH1	TMR8_ETR	-	-	-	USART2_CTS	UART4_TX	-	-	ETH_MII_CRS	-	-	-	EVENTOUT
PA1	-	TMR2_CH2	TMR5_CH2	-	-	-	-	USART2_RTS	UART4_RX	-	-	ETH_MII_RX_CLK ETH_RMII_REF_CLK	-	-	-	EVENTOUT
PA2	-	TMR2_CH3	TMR5_CH3	TMR9_CH1	-	-	-	USART2_TX	-	-	-	ETH_MDIO	-	-	-	EVENTOUT
PA3	-	TMR2_CH4	TMR5_CH4	TMR9_CH2	-	-	-	USART2_RX	-	-	OTG_HS_ULPI_D0	ETH_MII_COL	DMC_CKE	-	-	EVENTOUT
PA4	-	-	-	-	-	SPI1_NSS	SPI3_NSS I2S3_WS	USART2_CK	-	-	-	-	OTG_HS_SOF	DCI_HSYNC	-	EVENTOUT
PA5	-	TMR2_CH1_ETR		TMR8_CH1N	-	SPI1_SCK	-	-	-		OTG_HS_ULPI_CK	-	-	-	-	EVENTOUT
PA6	-	TMR1_BKIN	TMR3_CH1	TMR8_BKIN	-	SPI1_MISO	-	-	-	TMR13_CH1	-	-	-	DCI_PIXCK	-	EVENTOUT
PA7	-	TMR1_CH1N	TMR3_CH2	TMR8_CH1N	-	SPI1_MOSI	-	-	-	TMR14_CH1	-	ETH_MII_RX_DV ETH_RMII_CRS_DV	-	-	-	EVENTOUT

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA8	MCO1	TMR1_CH1	-	-	I2C3_SCL	-	-	USART1_CK	-	-	OTG_FS_SOF	-	-	-	-	EVENTOUT
PA9	-	TMR1_CH2	-	-	I2C3_SMBA	-	-	USART1_TX	-	-	-	-	-	DCI_D0	-	EVENTOUT
PA10	-	TMR1_CH3	-	-	-	-	-	USART1_RX	-	-	OTG_FS_ID	-	-	DCI_D1	-	EVENTOUT
PA11	-	TMR1_CH4	-	-	-	-	-	USART1_CTS	-	CAN1_RX	OTG_FS_DM	-	-	-	-	EVENTOUT
PA12	-	TMR1_ETR	-	-	-	-	-	USART1_RTS	-	CAN1_TX	OTG_FS_DP	-	-	-	-	EVENTOUT
PA13	JTMS_SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
PA14	JTCK_SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
PA15	JTDI	TMR2_CH1 TMR2_ETR	-	-	-	SPI1_NSS	SPI3_NSS I2C3_WS	-	-	-	-	-	-	-	-	EVENTOUT

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB11	-	TMR2_CH4	-	-	I2C2_SDA	-	-	USART3_RX	-	-	OTG_HS_ULPI_D4	ETH_MII_TX_EN ETH_RMII_TX_EN	-	-	-	EVENTOUT
PB12	-	TMR1_BKIN	-	-	I2C2_SMBA	SPI2_NSS I2S2_WS	-	USART3_CK	-	CAN2_RX	OTG_HS_ULPI_D5	ETH_RMII_TXD0 ETH_MII_TXD0	OTG_HS_ID	-	-	EVENTOUT
PB13	-	TMR1_CH1N	-	-	-	SPI2_SCK I2S2_CK	-	USART3_CTS	-	CAN2_TX	OTG_HS_ULPI_D6	ETH_RMII_TXD1 ETH_MII_TXD1	-	-	-	EVENTOUT
PB14	-	TMR1_CH2N	-	TMR8_CH2N	-	SPI2_MISO	I2S2ext_SD	USART3_RTS	-	TMR12_CH1	-	-	OTG_HS_DM	-	-	EVENTOUT
PB15	RTC_REFIN	TMR1_CH3N	-	TMR8_CH3N	-	SPI2_MOSII2S2_SD	-	-	-	TMR12_CH2	-	-	OTG_HS_DP	-	-	EVENTOUT

Table 7 GPIOD Multiplexing Function Configuration

Port	AF 0	AF 1	AF2	AF 3	AF 4	AF 5	AF 6	AF7	AF8	AF9	AF1 0	AF1 1	AF12	AF13	AF1 4	AF15
PD0	-	-	-	-	-	-	-	-	-	CAN1_R X	-	-	SMC_D2	-	-	EVENTOU T
PD1	-	-	-	-	-	-	-	-	-	CAN1_T X	-	-	SMC_D3	-	-	EVENTOU T
PD2	-	-	TMR3_ET R	-	-	-	-	-	UART5_R X	-	-	-	SDIO_CMD	DCI_D1 1	-	EVENTOU T
PD3	-	-	-	-	-	-	-	USART2_CT S	-	-	-	-	SMC_CLK	-	-	EVENTOU T
PD4	-	-	-	-	-	-	-	USART2_RT S	-	-	-	-	SMC_NOE	-	-	EVENTOU T
PD5	-	-	-	-	-	-	-	USART2_TX	-	-	-	-	SMC_NWE	-	-	EVENTOU T
PD6	-	-	-	-	-	-	-	USART2_RX	-	-	-	-	SMC_NWAIT	-	-	EVENTOU T
PD7	-	-	-	-	-	-	-	USART2_CK	-	-	-	-	SMC_NE1/SMC_NC E2	-	-	EVENTOU T
PD8	-	-	-	-	-	-	-	USART3_TX	-	-	-	-	SMC_D13	-	-	EVENTOU T

Table 8 GPIOE Multiplexing Function Configuration

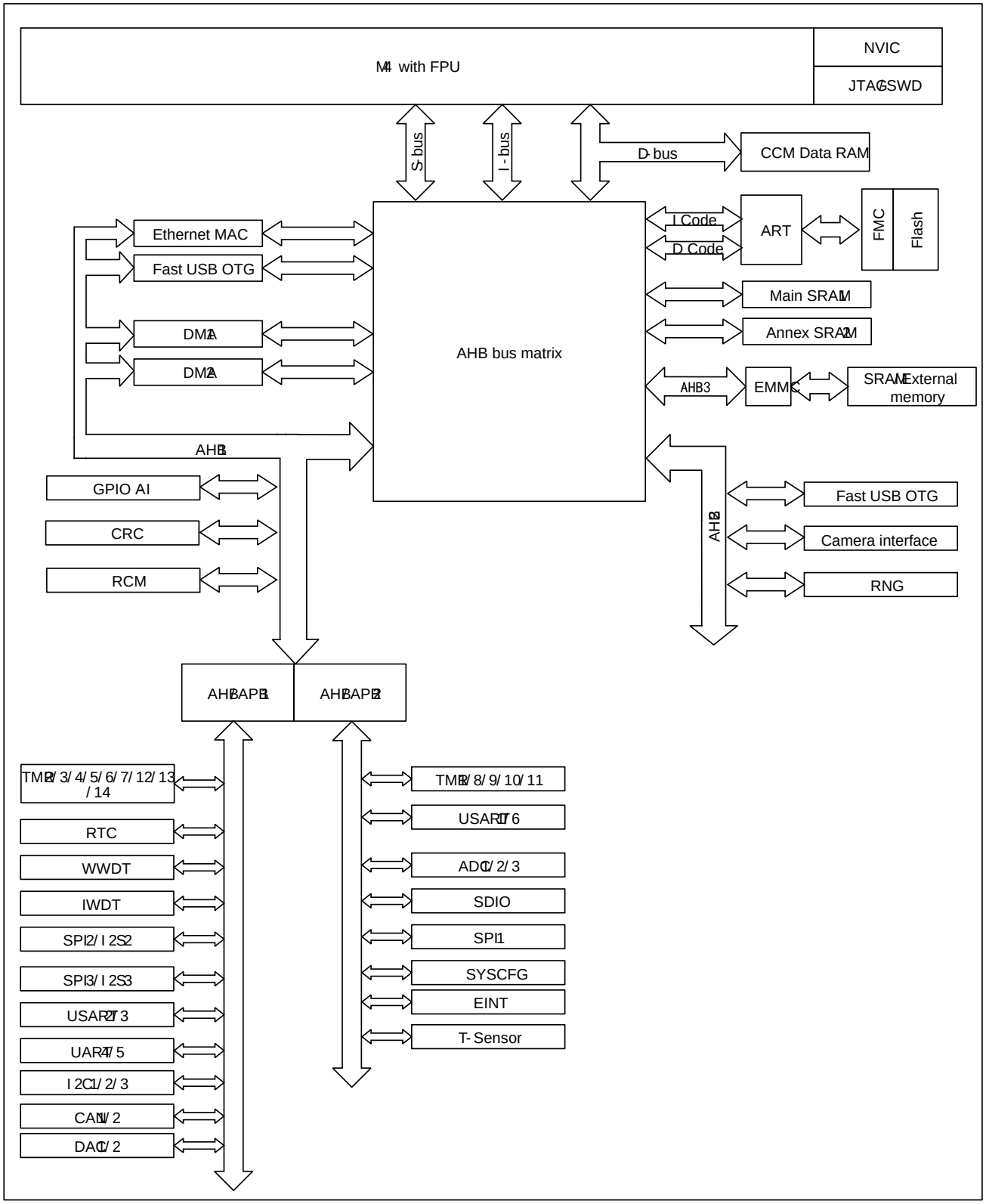
Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PE0	-	-	TMR4_ETR	-	-	-	-	-	-	-	-	-	SMC_NBL0	DCI_D2	-	EVENTOUT
PE1	-	-	-	-	-	-	-	-	-	-	-	-	SMC_NBL1	DCI_D3	-	EVENTOUT
PE2	TRACECLK	-	-	-	-	-	-	-	-	-	-	ETH_MII_TXD3	SMC_A23	-	-	EVENTOUT
PE3	TRACED0	-	-	-	-	-	-	-	-	-	-	-	SMC_A19	-	-	EVENTOUT
PE4	TRACED1	-	-	-	-	-	-	-	-	-	-	-	SMC_A20	DCI_D4	-	EVENTOUT
PE5	TRACED2	-	-	TMR9_CH1	-	-	-	-	-	-	-	-	SMC_A21	DCI_D6	-	EVENTOUT
PE6	TRACED3	-	-	TMR9_CH2	-	-	-	-	-	-	-	-	SMC_A22	DCI_D7	-	EVENTOUT
PE7	-	TMR1_ETR	-	-	-	-	-	-	-	-	-	-	SMC_D4	-	-	EVENTOUT
PE8	-	TMR1_CH1N	-	-	-	-	-	-	-	-	-	-	SMC_D5	-	-	EVENTOUT
PE9	-	TMR1_CH1	-	-	-	-	-	-	-	-	-	-	SMC_D6	-	-	EVENTOUT
PE10	-	TMR1_CH2N	-	-	-	-	-	-	-	-	-	-	SMC_D7	-	-	EVENTOUT
PE11	-	TMR1_CH2	-	-	-	-	-	-	-	-	-	-	SMC_D8	-	-	EVENTOUT

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PH12	-	-	TMR5_CH3	-	-	-	-	-	-	-	-	-	-	DCI_D3	-	EVENTOUT
PH13	-	-	-	TMR8_CH1N	-	-	-	-	-	CAN1_TX	-	-	DMC_DQ5	-	-	EVENTOUT
PH14	-	-	-	TMR8_CH2N	-	-	-	-	-	-	-	-	-	DCI_D4	-	EVENTOUT
PH15	-	-	-	TMR8_CH3N	-	-	-	-	-	-	-	-	DMC_DQ6	DCI_D11	-	EVENTOUT

4.1 System architecture

4.1.1 System block diagram

Figure 5 APM32F405xG 407xExG System Block Diagram



Parameter	Peripheral	Typical value (1) T_A=25 ; , V_{DD}=3.3V		Unit
		168MHz	144MHz	
	ADC2	0.27	0.22	
	ADC3	0.28	0.23	
	SPI1	0.12	0.11	
	USART1	0.22	0.18	
	USART6	0.21	0.18	
	SYSCFG	0.05	0.05	

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.7.7 Backup Domain Power Consumption

Table 33 V_{BAT} Power Consumption

Symbol	Parameter	Conditions	Typical value (1), T_A=25 ;		Maximum value (1), V_{BAT}=3.6V		Unit
			V_{BAT}=2.4V	V_{BAT}=3.3V	T_A=85 ;	T_A=105 ;	
I_{DD_VBAT}	LSECLK and RTC are in ON state	The backup SRAM is turned on, and the low-speed oscillator and RTC are turned on	1.894	2.262	6	11	μA
		The backup SRAM is turned off, and the low-speed oscillator and RTC are turned on	1.08	1.412	3	5	
		The backup SRAM is turned on, and the RTC is turned off	0.926	1.116	5	10	
		The backup SRAM is turned off, and the RTC is turned off	0.02	0.128	2	4	

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

5.8 Wake-up time in low-power mode

The measurement of wake-up time in low-power mode is from the start of wake-up event to the time when the user program reads the first instruction, in which V_{DD}=V_{DDA}.

Table 34 Wake-up Time in Low-power Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{WUSLEEP}$	Wake-up from sleep mode	-	39.00	59	61.20	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{WUSTOP}	Wake up from the stop mode	The regulator is in run mode, and Flash is in stop state	12.51	13.602	14.99	μs
		The regulator is in low-power mode, and Flash is in stop state	15.51	19.552	22.93	
		The regulator is in run mode, and Flash is in deep power-down mode	125.63	133.156	135.16	
		The regulator is in low-power mode, and Flash is in deep power-down mode	133.52	136.956	139.60	
$t_{WUSTDBY}$	Wake up from standby mode	-	173.03	214.056	227.96	

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.9 I/O port characteristics

Table 35 DC Characteristics (T_A=-40 - -105 - , V_{DD}=2~3.6V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low-level input voltage	STD and STDA I/O	-	-	$0.3V_{DD}$-0.04	V
		5T and 5Tf I/O	-	-	$0.3V_{DD}$	
		Boot0 pin	-	-	0.1_{DD}+0.1	
V_{IH}	High-level input voltage	STD and STDA I/O	$0.45V_{DD}$+0.3	-	-	V
		5T and 5Tf I/O	$0.7V_{DD}$	-	-	
		Boot0 pin	$0.17V_{DD}$+0.7	-	-	
V_{hys}	Schmidt trigger hysteresis	STD, STDA and 5T, 5Tf I/O	10% V_{DD}	-	-	mV
		Boot0 pin	0.1	-	-	
I_{lkg}	Input leakage current	STDA in digital mode, $V_{DDIOx} \le V_{IN} \le V_{DDA}$	-	-	±1	μA
		5T and 5Tf I/O, $V_{DDIOx} \le V_{IN} \le 5V$	-	-	3	
R_{PU}	Weak pull-up equivalent resistance	Except PA10 and PB12, $V_{IN}=V_{SS}$	30	40	50	kΩ
		PA10 and PB12	7	10	14	
R_{PD}	Weak pull-down equivalent resistance	Except PA10 and PB12, $V_{IN}=V_{DD}$	30	40	50	
		PA10 and PB12	7	10	14	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST low-level input voltage	CMOS port, 1.8V≤V_{DD}≤3.6V	-	-	0.3V_{DD}	
$V_{IH(NRST)}$	NRST high-level input voltage		0.7V_{DD}	-	-	
$V_{hys(NRST)}$	NRST Schmidt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistance	V_{IN}=V_{SS}	30	40	50	kΩ
$V_{F(NRST)}$	NRST input filter pulse	-	-	-	100	ns
$V_{NF(NRST)}$	NRST input unfiltered pulse	V_{DD} Ú2.7V	300	-	-	
T_{NRST_OUT}	Generated reset pulse duration	Reset internal source	20	-	-	μs

5.11 Communication peripherals

5.11.1 I2C peripheral characteristics

To achieve maximum frequency of I2C in standard mode, f_{PCLK1} must be greater than 2MHz. To achieve maximum frequency of I2C in fast mode, f_{PCLK1} must be greater than 4MHz.

Table 39 I2C Interface Characteristics (T_A=25 - , V_{DD}=3.3V)

Symbol	Parameter	Standard I2C		Fast I2C		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	μs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0	-	0	900	
$t_{r(SDA)}$/$t_{r(SCL)}$	SDA and SCL rise time	-	1000	20+0.1C_b	300	
$t_{f(SDA)}$/$t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	μs
$t_{su(STA)}$	Setup time of repeated start condition	4.7	-	0.6	-	
$t_{su(STO)}$	Setup time of stop condition	4.0	-	0.6	-	
$t_{w(STO:STA)}$	Time from stop condition to start condition (the bus is idle)	4.7	-	1.3	-	
C_b	Capacitive load of each bus	-	400	-	400	pF

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

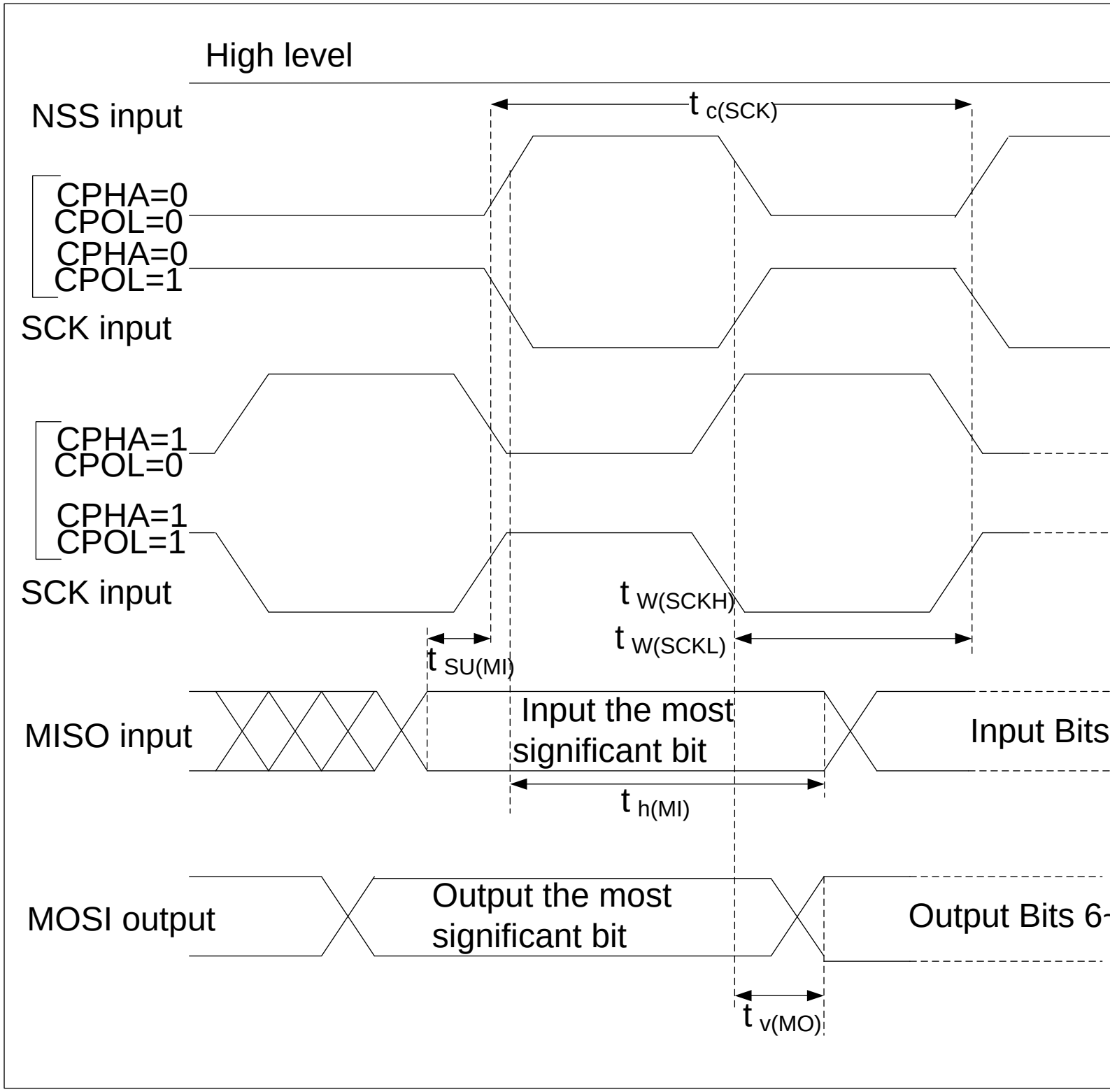
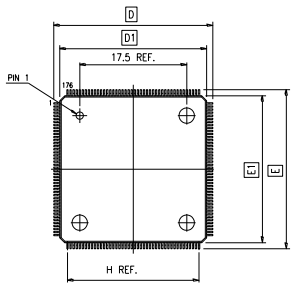
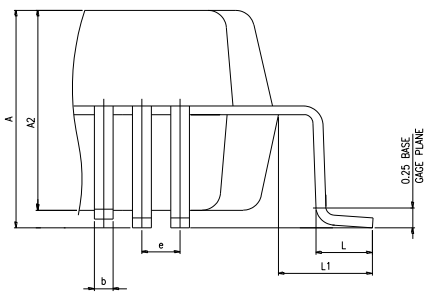

High level
NSS input
t c(SCK)
CPHA=0
CPOL=0
CPHA=0
CPOL=1
SCK input
CPHA=1
CPOL=0
CPHA=1
CPOL=1
SCK input
t W(SCKH)
t W(SCKL)
t SU(MI)
MISO input
Input the most significant bit
Input Bits
t h(MI)
MOSI output
Output the most significant bit
Output Bits 6-
t v(MO)

Table 44 DAC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog power supply voltage	-	1.8	-	3.6	V
R_{LOAD}	Resistive load	The buffer is turned on	5	-	-	kΩ
R_O	Output impedance	The resistive load between DAC_OUT and V_{SS} is 1.5MΩ with buffer off	-	-	15	kΩ
C_{LOAD}	Capacitive load	Maximum capacitive load at DAC_OUT pin with buffer on	-	-	50	pF
DAC_OUT min	Low DAC_OUT voltage with buffer	Maximum output offset of DAC, (0x0E0) corresponding to 12-bit input code to V_{REF+}= (0xF1C) at 3.6V and V_{REF+}= (0x1C7) at 1.8V and (0xE38)	0.2	-	-	V
DAC_OUT max	Higher DAC_OUT voltage with buffer		-	-	V_{DDA}-0.2	V
DAC_OUT min	Low DAC_OUT voltage without buffer	Maximum output offset of DAC	-	0.5	-	mV
DAC_OUT max	Higher DAC_OUT voltage without buffer		-	-	V_{REF+}-1LSB	V
DNL	Differential non-linear error	Configured with 12-bit DAC	-	-	±2	LSB
INL	Integral non-linear error	Configured with 12-bit DAC	-	-	±4	LSB
Offset	Offset error	V_{REF+}=3.6V, configuring 12-bit DAC	-	-	±12	LSB
Gain error	Gain error	Configured with 12-bit DAC	-	-	±0.5	%

Note: The data are obtained from a comprehensive evaluation and are not tested in production.


D
D1
17.5 REF.
PIN 1
176
E1
E
H REF.


A
A2
0.25 BASE
GAGE PLANE
e
L
L1
b

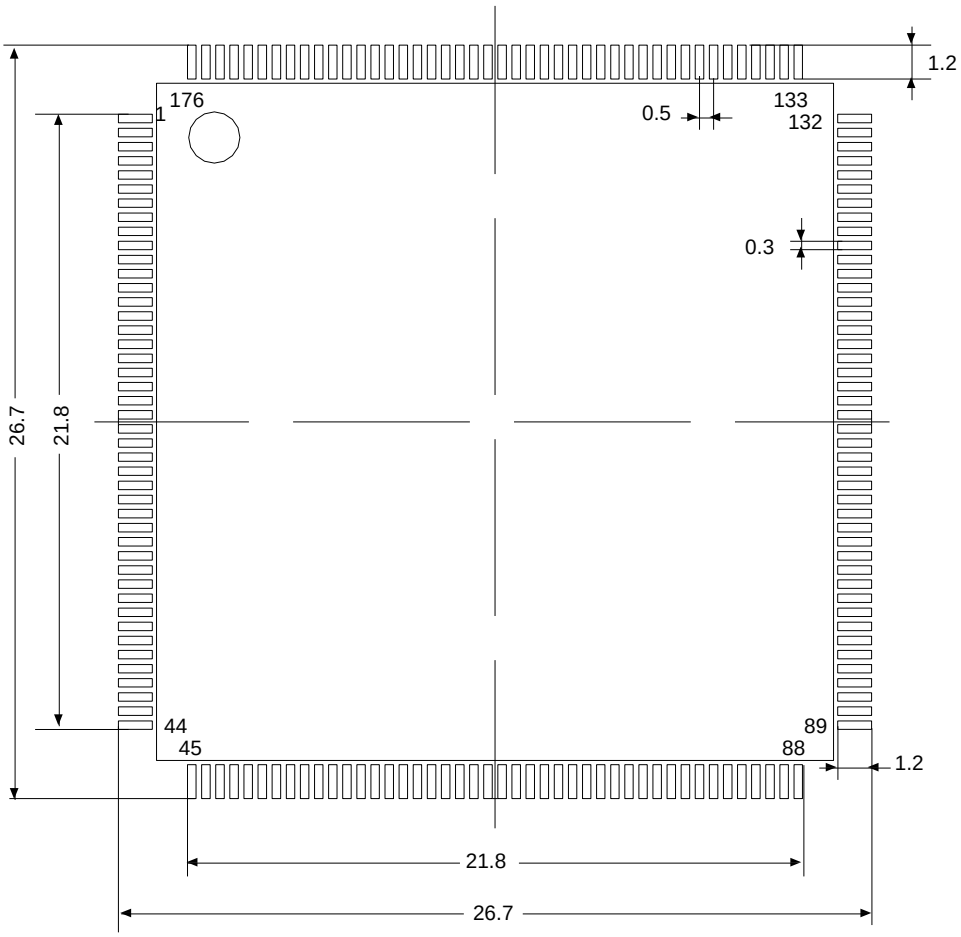

1.2
176
1
133
132
0.5
0.3
26.7
21.8
44
45
89
88
1.2
21.8
26.7

Figure 19 LQFP176 -176 Pins, 24 x24mm Schematic Diagram

6.2 **LQFP144 package information**

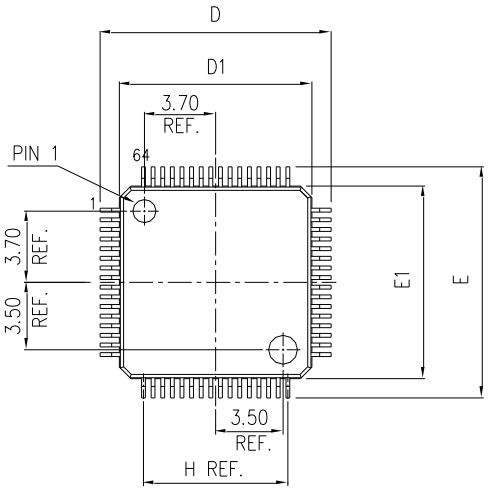
Figure 20 LQFP144 Package Diagram

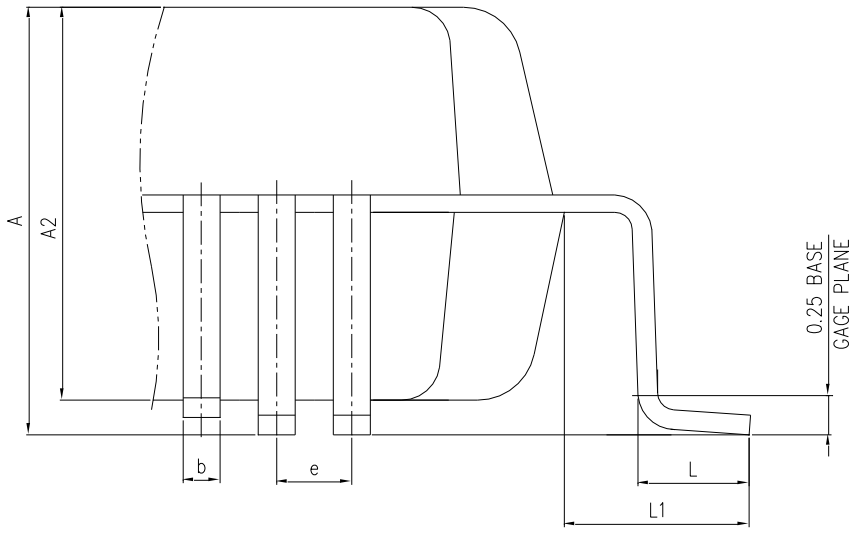
6.4 LQFP64 package information

Figure 26 LQFP64 Package Diagram

Ä1 Å The figure is not drawn to scale.

Ä2 Å All pins should be soldered to the PCB.


D
D1
3.70
REF.
PIN 1
64
1
3.70
REF.
3.50
REF.
E1
E
3.50
REF.
H REF.


A
A2
0.25 BASE
GAGE PLANE
b
e
L
L1