GigaDevice Semiconductor Inc.

GD32F407xx
Arm® Cortex®-M4 32-bit MCU

Datasheet

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1. General description

The GD32F407xx device belongs to the connectivity line of GD32 MCU family. It is a new 32-bit general-purpose microcontroller based on the Arm® Cortex®-M4 RISC core with best cost-performance ratio in terms of enhanced processing capacity, reduced power consumption and peripheral set. The Cortex®-M4 core features a Floating Point Unit (FPU) that accelerates single precision floating point math operations and supports all Arm® single precision instructions and data types. It implements a full set of DSP instructions to address digital signal control markets that demand an efficient, easy-to-use blend of control and signal processing capabilities. It also provides a Memory Protection Unit (MPU) and powerful trace technology for enhanced application security and advanced debug support.

The GD32F407xx device incorporates the Arm® Cortex®-M4 32-bit processor core operating at 168 MHz frequency with Flash accesses zero wait states to obtain maximum efficiency. It provides up to 3072 KB on-chip Flash memory and 192 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer up to three 12-bit 2.6 MSPS ADCs, two 12-bit DACs, up to eight general 16-bit timers, two 16-bit PWM advanced timers, two 32-bit general timers, and two 16-bit basic timers, as well as standard and advanced communication interfaces: up to three SPIs, three I2Cs, four USARTs and two UARTs, two I2Ss, two CANs, a SDIO, USBFS and USBHS, and an ENET. Additional peripherals as Digital camera interface (DCI), EXMC interface with SDRAM extension support are included.

The device operates from a 2.6 to 3.6V power supply and available in ï 40 to +85 °C temperature range. Three power saving modes provide the flexibility for maximum optimization of power consumption, an especially important consideration in low power applications.

The above features make GD32F407xx devices suitable for a wide range of interconnection and advanced applications, especially in areas such as industrial control, consumer and handheld equipment, embedded modules, human machine interface, security and alarm systems, graphic display, automotive navigation, drone, IoT and so on.

2. Device overview

2.1. Device information

Table 2-1. GD32F407xx devices features and peripheral list

Part Number		GD32F407xx											
		RE	RG	RK	VE	VG	VK	VE	VG	VK	ZE	ZG	ZK
Flash	Code area (KB)	512	512	512	512	512	512	512	512	512	512	512	512
	Data area (KB)	0	512	2560	0	512	2560	0	512	2560	0	512	2560
	Total (KB)	512	1024	3072	512	1024	3072	512	1024	3072	512	1024	3072
SRAM (KB)		192	192	192	192	192	192	192	192	192	192	192	192
Timers	General timer(16-bit)	8 (2-3, 8-13)	8 (2-3,8-13)	8 (2-3,8-13)	8 (2-3,8-13)	8 (2-3,8-13)	8 (2-3,8-13)	8 (2-3,8-13)	8 (2-3,8-13)	8 (2-3,8-13)	8 (2-3,8-13)	8 (2-3,8-13)	8 (2-3,8-13)
	General timer(32-bit)	2 (1, 4)	2 (1,4)	2 (1,4)	2 (1,4)	2 (1,4)	2 (1,4)	2 (1,4)	2 (1,4)	2 (1,4)	2 (1,4)	2 (1,4)	2 (1,4)
	Advanced timer(16-bit)	2 (0, 7)	2 (0,7)	2 (0,7)	2 (0,7)	2 (0,7)	2 (0,7)	2 (0,7)	2 (0,7)	2 (0,7)	2 (0,7)	2 (0,7)	2 (0,7)
	Basic timer(16-bit)	2 (5, 6)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)
	SysTick	1	1	1	1	1	1	1	1	1	1	1	1
	Watchdog	2	2	2	2	2	2	2	2	2	2	2	2
	RTC	1	1	1	1	1	1	1	1	1	1	1	1
Connectivity	USART	4	4	4	4	4	4	4	4	4	4	4	4
	UART	2	2	2	2	2	2	2	2	2	2	2	2
	I2C	3	3	3	3	3	3	3	3	3	3	3	3
	SPI/I2S	3/2 (0-2)/(1-2)	3/2 (0-2)/(1-2)	3/2 (0-2)/(1-2)	3/2 (0-2)/(1-2)	3/2 (0-2)/(1-2)	3/2 (0-2)/(1-2)	3/2 (0-2)/(1-2)	3/2 (0-2)/(1-2)	3/2 (0-2)/(1-2)	3/2 (0-2)/(1-2)	3/2 (0-2)/(1-2)	3/2 (0-2)/(1-2)
	SDIO	1	1	1	1	1	1	1	1	1	1	1	1
	CAN	2	2	2	2	2	2	2	2	2	2	2	2
	USB	FS+HS	FS+HS	FS+HS	FS+HS	FS+HS	FS+HS	FS+HS	FS+HS	FS+HS	FS+HS	FS+HS	FS+HS
	ENET	1	1	1	1	1	1	1	1	1	1	1	1
	DCI	1	1	1	1	1	1	1	1	1	1	1	1
GPIO		51	51	51	82	82	82	82	82	82	114	114	114

Part Number	GD32F407xx											
	RE	RG	RK	VE	VG	VK	VE	VG	VK	ZE	ZG	ZK
EXMC/SDRAM	0/0	0/0	0/0	1/0	1/0	1/0	1/0	1/0	1/0	1/1	1/1	1/1
ADC(CHs)	3(16)	3(16)	3(16)	3(16)	3(16)	3(16)	3(16)	3(16)	3(16)	3(24)	3(24)	3(24)
DAC	2	2	2	2	2	2	2	2	2	2	2	2
Package	LQFP64			LQFP100			BGA100			LQFP144		

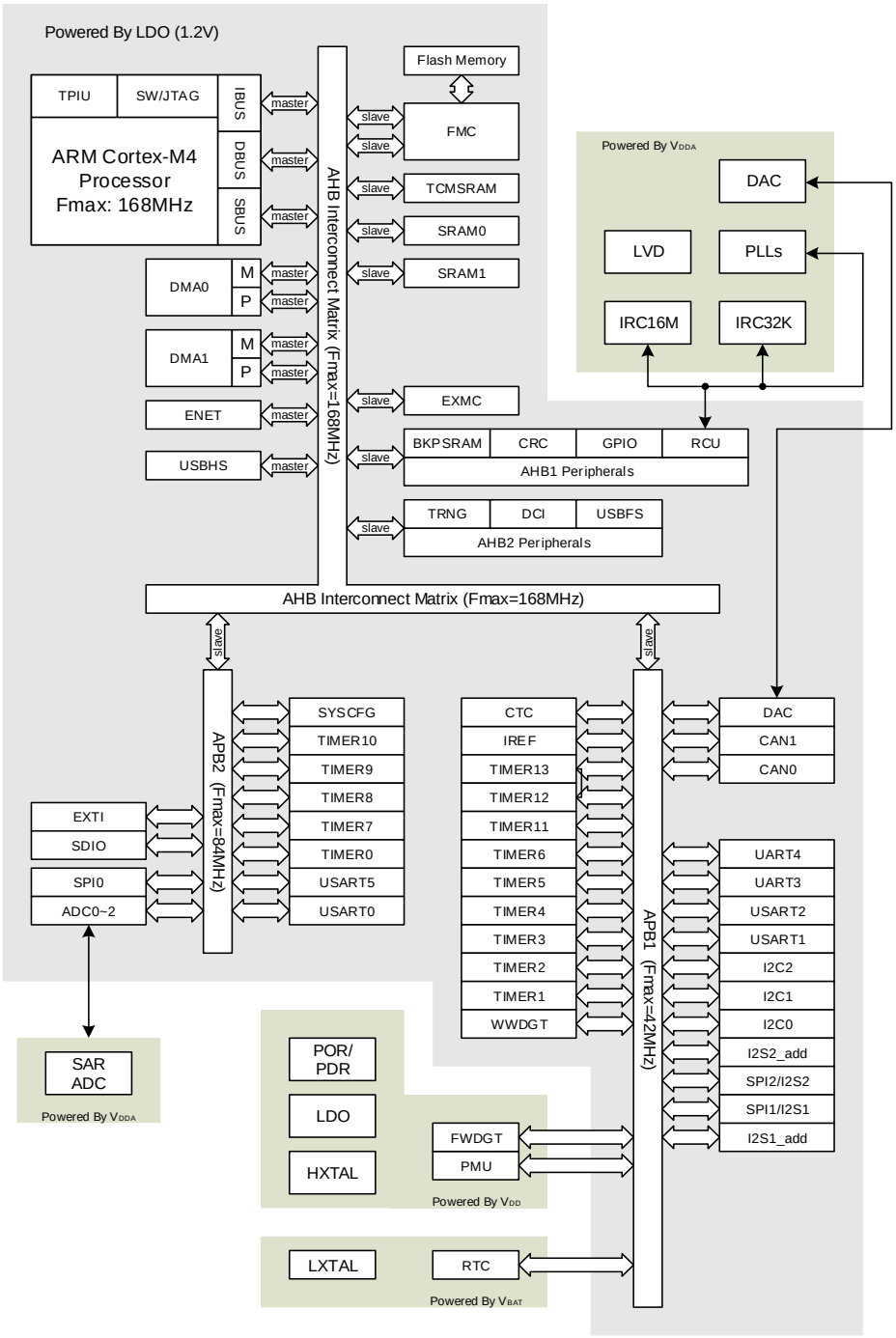
Table 2-2. GD32F407xx devices features and peripheral list (Cont.)

Part Number		GD32F407xx		
		IE	IG	IK
Flash	Code area (KB)	512	512	512
	Data area (KB)	0	512	2560
	Total (KB)	512	1024	3072
SRAM (KB)		192	192	192
Timers	General timer(16-bit)	8 (2-3,8-13)	8 (2-3,8-13)	8 (2-3,8-13)
	General timer(32-bit)	2 (1,4)	2 (1,4)	2 (1,4)
	Advanced timer(16-bit)	2 (0,7)	2 (0,7)	2 (0,7)
	Basic timer(16-bit)	2 (5,6)	2 (5,6)	2 (5,6)
	SysTick	1	1	1
	Watchdog	2	2	2
	RTC	1	1	1
Connectivity	USART	4	4	4
	UART	2	2	2
	I2C	3	3	3
	SPI/I2S	3/2 (0-2)/(1-2)	3/2 (0-2)/(1-2)	3/2 (0-2)/(1-2)
	SDIO	1	1	1
	CAN	2	2	2
	USB	FS+HS	FS+HS	FS+HS
	ENET	1	1	1
	DCI	1	1	1

Part Number	GD32F407xx		
	IE	IG	IK
GPIO	140	140	140
EXMC/SDRAM	1/1	1/1	1/1
ADC(CHs)	3(24)	3(24)	3(24)
DAC	2	2	2
Package	BGA176		

2.2. Block diagram

Figure 2-1. GD32F407xx block diagram



2.3. Pinouts and pin assignment

Figure 2-2. GD32F407Ix BGA176 pinouts

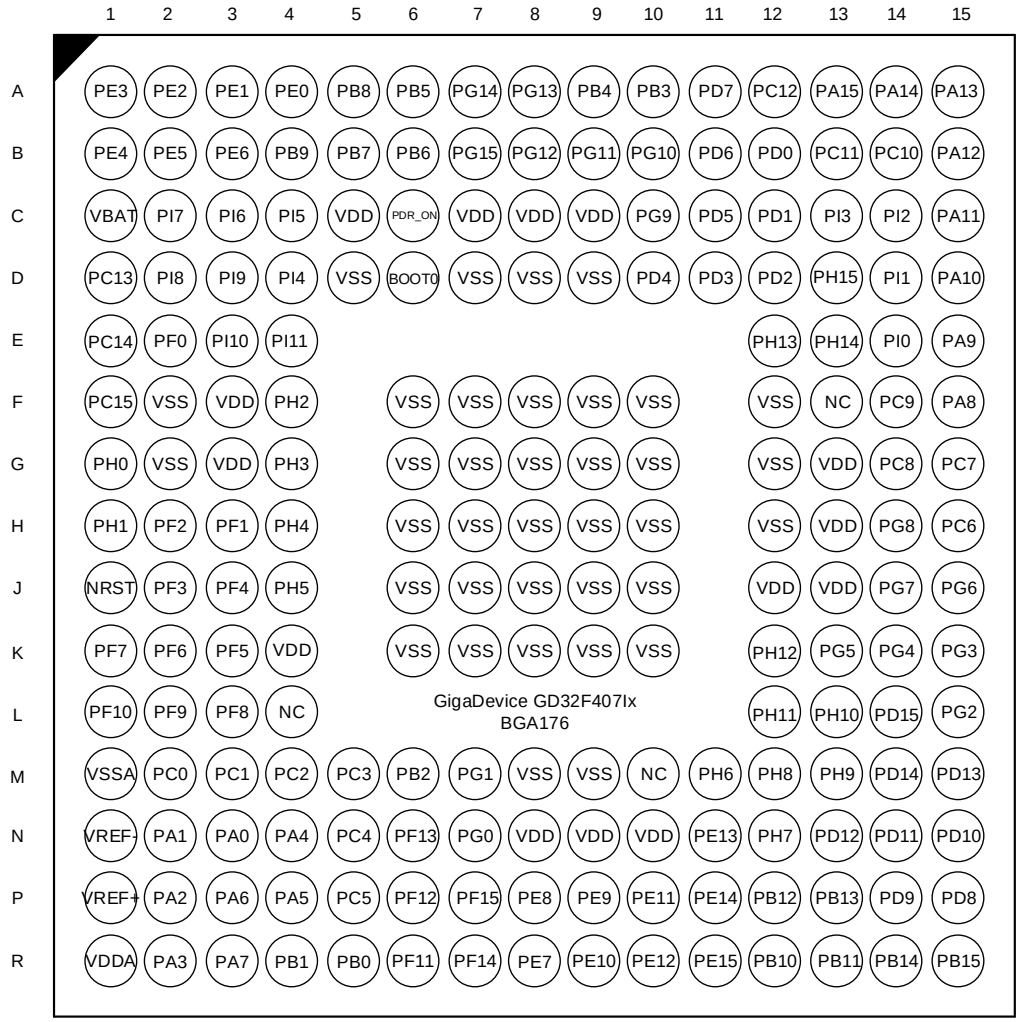


Figure 2-3. GD32F407Vx BGA100 pinouts

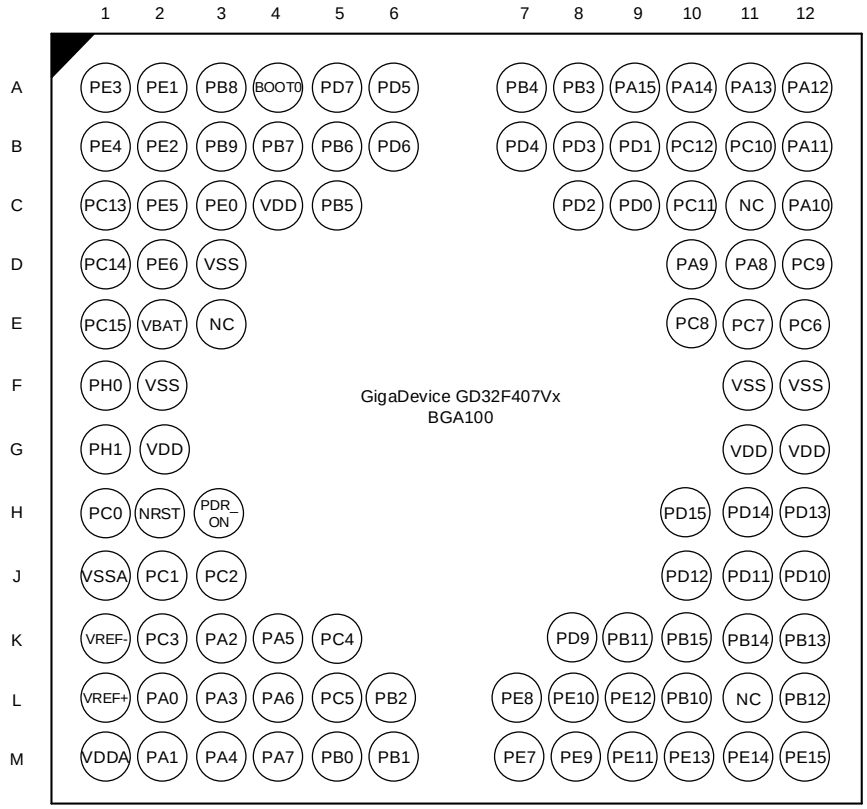


Figure 2-4. GD32F407Zx LQFP144 pinouts

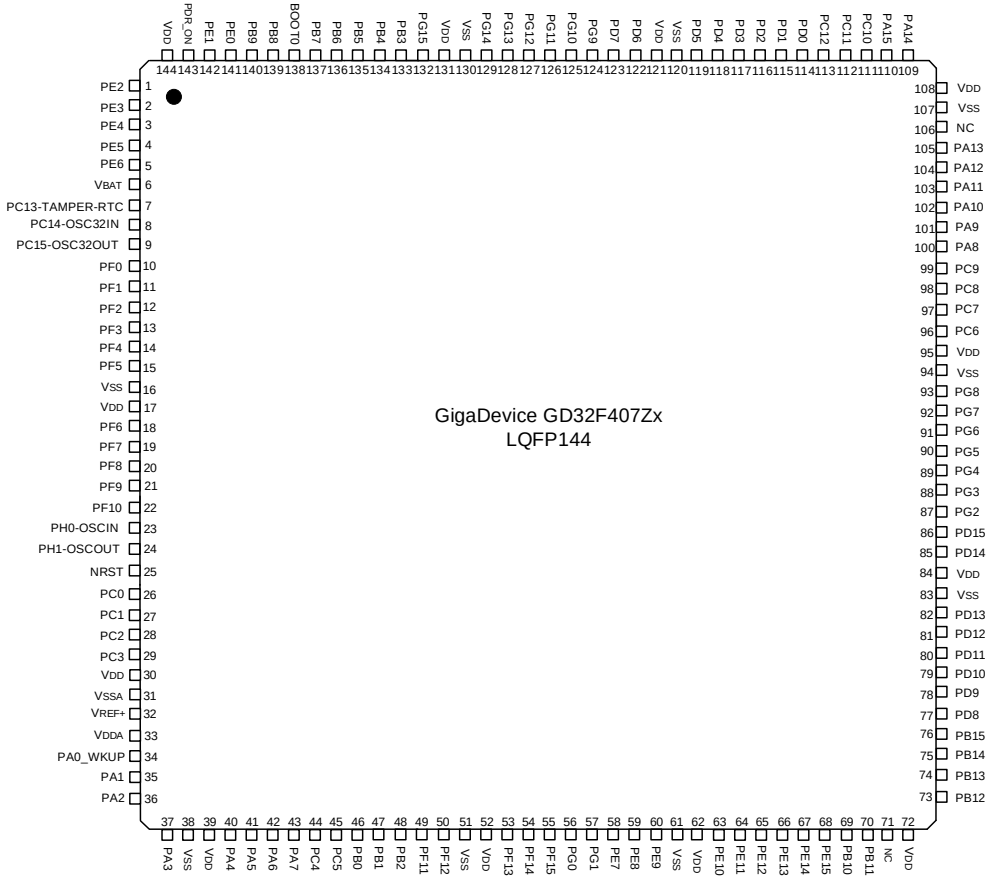


Figure 2-5. GD32F407Vx LQFP100 pinouts

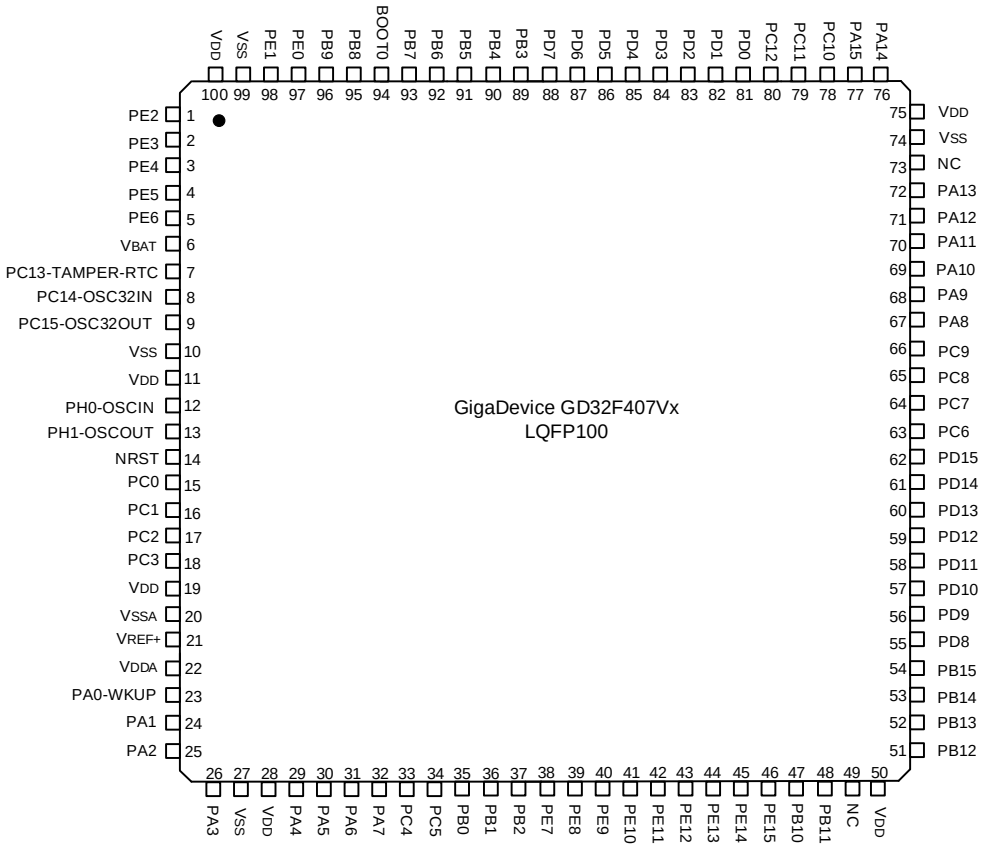


Figure 2-6. GD32F407Rx LQFP64 pinouts

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				EXMC_NL/EXMC_NADV, DCI_VSYNC, EVENTOUT
BOOT0	A4	I/O	5VT	Default: BOOT0
PB8	A3	I/O	5VT	Default: PB8 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER3_CH2, TIMER9_CH0, I2C0_SCL, CAN0_RX, ENET_MII_TXD3, SDIO_D4, DCI_D6, EVENTOUT
PB9	B3	I/O	5VT	Default: PB9 Alternate: TIMER1_CH1, TIMER3_CH3, TIMER10_CH0, I2C0_SDA, SPI1_NSS, I2S1_WS, CAN0_TX, SDIO_D5, DCI_D7, EVENTOUT
PE0	C3	I/O	5VT	Default: PE0 Alternate: TIMER3_ETI, EXMC_NBL0, DCI_D2, EVENTOUT
PE1	A2	I/O	5VT	Default: PE1 Alternate: TIMER0_CH1_ON, EXMC_NBL1, DCI_D3, EVENTOUT
V_{SS}	D3	P	-	Default: V_{SS}
PDR_ON	H3	P	-	Default: PDR_ON
V_{DD}	C4	P	-	Default: V_{DD}

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

2.6.5. GD32F407Rx LQFP64 pin definitions

Table 2-8. GD32F407Rx LQFP64 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
V_{BAT}	1	P	-	Default: V_{BAT}
PC13-TAMPER-RTC	2	I/O	5VT	Default: PC13 Alternate: EVENTOUT Additional: RTC_TAMP0, RTC_OUT, RTC_TS
PC14-OSC32IN	3	I/O	5VT	Default: PC14 Alternate: EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	4	I/O	5VT	Default: PC15 Alternate: EVENTOUT Additional: OSC32OUT
PH0	5	I/O	5VT	Default: PH0, OSCIN Alternate: EVENTOUT

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Additional: OSCIN
PH1	6	I/O	5VT	Default: PH1, OSCOUT Alternate: EVENTOUT Additional: OSCOUT
NRST	7	-	-	Default: NRST
PC0	8	I/O	5VT	Default: PC0 Alternate: USBHS_ULPI_STP, EVENTOUT Additional: ADC012_IN10
PC1	9	I/O	5VT	Default: PC1 Alternate: SPI2_MOSI, I2S2_SD, SPI1_MOSI, I2S1_SD, ENET_MDC, EVENTOUT Additional: ADC012_IN11
PC2	10	I/O	5VT	Default: PC2 Alternate: SPI1_MISO, I2S1_ADD_SD, USBHS_ULPI_DIR, ENET_MII_TXD2, EVENTOUT Additional: ADC012_IN12
PC3	11	I/O	5VT	Default: PC3 Alternate: SPI1_MOSI, I2S1_SD, USBHS_ULPI_NXT, ENET_MII_TX_CLK, EVENTOUT Additional: ADC012_IN13
V_{SSA}	12	P	-	Default: V_{SSA}
V_{DDA}	13	P	-	Default: V_{DDA}
PA0-WKUP	14	I/O	5VT	Default: PA0 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER4_CH0, TIMER7_ETI, USART1_CTS, UART3_TX, ENET_MII_CRS, EVENTOUT Additional: ADC012_IN0, WKUP
PA1	15	I/O	5VT	Default: PA1 Alternate: TIMER1_CH1, TIMER4_CH1, USART1_RTS, UART3_RX, ENET_MII_RX_CLK, ENET_RMII_REF_CLK, EVENTOUT Additional: ADC012_IN1
PA2	16	I/O	5VT	Default: PA2 Alternate: TIMER1_CH2, TIMER4_CH2, TIMER8_CH0, I2S_CKIN, USART1_TX, ENET_MDIO, EVENTOUT Additional: ADC012_IN2
PA3	17	I/O	5VT	Default: PA3 Alternate: TIMER1_CH3, TIMER4_CH3, TIMER8_CH1, I2S1_MCK, USART1_RX, USBHS_ULPI_D0, ENET_MII_COL, EVENTOUT Additional: ADC012_IN3

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
V_{SS}	18	P	-	Default: V_{SS}
V_{DD}	19	P	-	Default: V_{DD}
PA4	20	I/O		Default: PA4 Alternate: SPI0_NSS, SPI2_NSS, I2S2_WS, USART1_CK, USBHS_SOF, DCI_HSYNC, EVENTOUT Additional: ADC01_IN4, DAC_OUT0
PA5	21	I/O		Default: PA5 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER7_CH0_ON, SPI0_SCK, USBHS_ULPI_CK, EVENTOUT Additional: ADC01_IN5, DAC_OUT1
PA6	22	I/O	5VT	Default: PA6 Alternate: TIMER0_BRKIN, TIMER2_CH0, TIMER7_BRKIN, SPI0_MISO, I2S1_MCK, TIMER12_CH0, SDIO_CMD, DCI_PIXCLK, EVENTOUT Additional: ADC01_IN6
PA7	23	I/O	5VT	Default: PA7 Alternate: TIMER0_CH0_ON, TIMER2_CH1, TIMER7_CH0_ON, SPI0_MOSI, TIMER13_CH0, ENET_MII_RX_DV, ENET_RMII_CRS_DV, EVENTOUT Additional: ADC01_IN7
PC4	24	I/O	5VT	Default: PC4 Alternate: ENET_MII_RXD0, ENET_RMII_RXD0, EVENTOUT Additional: ADC01_IN14
PC5	25	I/O	5VT	Default: PC5 Alternate: USART2_RX, ENET_MII_RXD1, ENET_RMII_RXD1, EVENTOUT Additional: ADC01_IN15
PB0	26	I/O	5VT	Default: PB0 Alternate: TIMER0_CH1_ON, TIMER2_CH2, TIMER7_CH1_ON, SPI2_MOSI, I2S2_SD, USBHS_ULPI_D1, ENET_MII_RXD2, SDIO_D1, EVENTOUT Additional: ADC01_IN8, IREF
PB1	27	I/O	5VT	Default: PB1 Alternate: TIMER0_CH2_ON, TIMER2_CH3, TIMER7_CH2_ON, USBHS_ULPI_D2, ENET_MII_RXD3, SDIO_D2, EVENTOUT Additional: ADC01_IN9
PB2	28	I/O	5VT	Default: PB2, BOOT1 Alternate: TIMER1_CH3, SPI2_MOSI, I2S2_SD,

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				USBHS_ULPI_D4, SDIO_CK, EVENTOUT
PB10	29	I/O	5VT	Default: PB10 Alternate: TIMER1_CH2, I2C1_SCL, SPI1_SCK, I2S1_CK, I2S2_MCK, USART2_TX,USBHS_ULPI_D3, ENET_MII_RX_ER, SDIO_D7, EVENTOUT
PB11	30	I/O	5VT	Default: PB11 Alternate: TIMER1_CH3, I2C1_SDA, I2S_CKIN, USART2_RX, USBHS_ULPI_D4, ENET_MII_TX_EN, ENET_RMII_TX_EN, EVENTOUT
NC	31	-	-	-
V_{DD}	32	P	-	Default: V_{DD}
PB12	33	I/O	5VT	Default: PB12 Alternate: TIMER0_BRKIN, I2C1_SMBA, SPI1_NSS, I2S1_WS, USART2_CK, CAN1_RX, USBHS_ULPI_D5, ENET_MII_TXD0, ENET_RMII_TXD0, USBHS_ID, EVENTOUT
PB13	34	I/O	5VT	Default: PB13 Alternate: TIMER0_CH0_ON, SPI1_SCK, I2S1_CK, USART2_CTS, CAN1_TX, USBHS_ULPI_D6, ENET_MII_TXD1, ENET_RMII_TXD1, EVENTOUT, I2C1_TXFRAME Additional: USBHS_VBUS
PB14	35	I/O	5VT	Default: PB14 Alternate: TIMER0_CH1_ON, TIMER7_CH1_ON, SPI1_MISO, I2S1_ADD_SD, USART2_RTS, TIMER11_CH0, USBHS_DM, EVENTOUT
PB15	36	I/O	5VT	Default: PB15 Alternate: RTC_REFIN, TIMER0_CH2_ON, TIMER7_CH2_ON, SPI1_MOSI, I2S1_SD, TIMER11_CH1, USBHS_DP, EVENTOUT
PC6	37	I/O	5VT	Default: PC6 Alternate: TIMER2_CH0, TIMER7_CH0, I2S1_MCK, USART5_TX, SDIO_D6, DCI_D0, EVENTOUT
PC7	38	I/O	5VT	Default: PC7 Alternate: TIMER2_CH1, TIMER7_CH1, SPI1_SCK, I2S1_CK, I2S2_MCK, USART5_RX, SDIO_D7, DCI_D1, EVENTOUT
PC8	39	I/O	5VT	Default: PC8 Alternate: TRACED0, TIMER2_CH2, TIMER7_CH2, USART5_CK, SDIO_D0, DCI_D2, EVENTOUT
PC9	40	I/O	5VT	Default: PC9

				86$57 B7; 6',2B &,B (9(17287 $GGLWLRQDO 86%)6B9%86
3$		, 2	97	'HIDXOW 3$ $OWHU7QDWLYH&+86$57 B58;86%)6B,''&,B' (9(17287 , & B7;)5$0(
3$		, 2	97	'HIDXOW 3$ $OWHU7QDWLYH&+86$57 B&7866$57 B7; &$1 B5; 86%)6B'0 (9(17287
3$		, 2	97	'HIDXOW 3$ $OWHU7QDWLYH(78;86$57 B5786$57 B5; &$1 B7; 86%)6B'3 (9(17287
3$		, 2	97	'HIDXOW -706 6:',2 3$ $OWHUQDWH (9(17287
1&				
9''		3		'HIDXOW 9
3$		, 2	97	'HIDXOW -7&. 6:&/. 3$ $OWHUQDWH (9(17287
3$		, 2	97	'HIDXOW -7', 3$ $OWHU7QDWLYH&+7,0(5 B(76;3, B166 63, B166 , 6 B:6 86$57 B7; (9(17287
3&		, 2	97	'HIDXOW 3& $OWHU6QDWLYH&. 6 B&.86$57 B7; 8$57 B 6',2B' '&,B' (9(17287
3&		, 2	97	'HIDXOW 3& $OWHUQDWLYH'B6'63, B0,6286$57 B5; 8$57 B5; 6',2B' '&,B' (9(17287
3&		, 2	97	'HIDXOW 3& $OWHUQDWLYH&DB6'63, B026,,6 B6'86$57 B&. 8$57 B7; 6',2B&. '&,B' (9(17287
3'		, 2	97	'HIDXOW 3' $OWHU7QDWLYH(78$57 B56;',2B&0''&,B' (9(17287
3%		, 2	97	'HIDXOW -7'2 3%

				SPI2_MOSI, I2S2_SD, CAN1_RX, USBHS_ULPI_D7, ENET_PPS_OUT, DCI_D10, EVENTOUT
PB6	58	I/O	5VT	Default: PB6 Alternate: TIMER3_CH0, I2C0_SCL, USART0_TX, CAN1_TX, DCI_D5, EVENTOUT
PB7	59	I/O	5VT	Default: PB7 Alternate: TIMER3_CH1, I2C0_SDA, USART0_RX, DCI_VSYNC, EVENTOUT
BOOT0	60	I/O	5VT	Default: BOOT0
PB8	61	I/O	5VT	Default: PB8 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER3_CH2, TIMER9_CH0, I2C0_SCL, CAN0_RX, ENET_MII_TXD3, SDIO_D4, DCI_D6, EVENTOUT
PB9	62	I/O	5VT	Default: PB9 Alternate: TIMER1_CH1, TIMER3_CH3, TIMER10_CH0, I2C0_SDA, SPI1_NSS, I2S1_WS, CAN0_TX, SDIO_D5, DCI_D7, EVENTOUT
V_{SS}	63	P	-	Default: V_{SS}
V_{DD}	64	P	-	Default: V_{DD}

1 R W H V

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolera

2.6.6. *') [[SLQ DOWHUQDWH IXQFWLRQV

Table 2-9. Port A alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA0		TIMER1_CH0/TIMER1_ETI	TIMER4_CH0	TIMER7_ETI				USART1_CTS	UART3_TX			ENET_MII_CRS				EVENTOUT
PA1		TIMER1_CH1	TIMER4_CH1					USART1_RTS	UART3_RX			ENET_MII_RX_CLK/ ENET_RMII_REF_CLK				EVENTOUT
PA2		TIMER1_CH2	TIMER4_CH2	TIMER8_CH0		I2S_CKIN		USART1_TX				ENET_MDIO				EVENTOUT
PA3		TIMER1_CH3	TIMER4_CH3	TIMER8_CH1		I2S1_MCK		USART1_RX			USBHS_ULPI_D0	ENET_MII_COL				EVENTOUT
PA4						SPI0_NSS	SPI2_NSS/ I2S2_WS	USART1_CK					USBHS_SOF	DCI_HSYNC		EVENTOUT
PA5		TIMER1_CH0/TIMER1_ETI		TIMER7_CH0_ON		SPI0_SCK					USBHS_ULPI_CK					EVENTOUT
PA6		TIMER0_BRKIN	TIMER2_CH0	TIMER7_BRKIN		SPI0_MISO	I2S1_MCK			TIMER12_CH0			SDIO_CMD	DCI_PIXCLK		EVENTOUT
PA7		TIMER0_CH0_ON	TIMER2_CH1	TIMER7_CH0_ON		SPI0_MOSI				TIMER13_CH0		ENET_MII_RX_DV/ENET_RMII_CRS_DV	EXMC_SDNWE			EVENTOUT
PA8	CK_OUT0	TIMER0_CH0			I2C2_SCL			USART0_CK		CTC_SYNC	USBFS_SOF		SDIO_D1			EVENTOUT
PA9		TIMER0_CH1			I2C2_SMBA	SPI1_SCK/ I2S1_CK		USART0_TX					SDIO_D2	DCI_D0		EVENTOUT
PA10		TIMER0_CH2			I2C2_TXFRAME			USART0_RX			USBFS_ID			DCI_D1		EVENTOUT
PA11		TIMER0_CH3						USART0_CTS	USART5_TX	CAN0_RX	USBFS_DM					EVENTOUT
PA12		TIMER0_ETI						USART0_RTS	USART5_RX	CAN0_TX	USBFS_DP					EVENTOUT

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB12		TIMER0_BRKIN			I2C1_SMBA	SPI1_NSS/I2S1_WS		USART2_CK		CAN1_RX	USBHS_ULPI_D5	ENET_MII_TXD0/ENET_RMII_TXD0	USBHS_ID			EVENTOUT
PB13		TIMER0_CH0_ON			I2C1_TXFRAME	SPI1_SCK/I2S1_CK		USART2_CTS		CAN1_TX	USBHS_ULPI_D6	ENET_MII_TXD1/ENET_RMII_TXD1				EVENTOUT
PB14		TIMER0_CH1_ON		TIMER7_CH1_ON		SPI1_MISO	I2S1_ADD_SD	USART2_RTS		TIMER11_CH0			USBHS_DM			EVENTOUT
PB15	RTC_REFIN	TIMER0_CH2_ON		TIMER7_CH2_ON		SPI1_MOSI/I2S1_SD				TIMER11_CH1			USBHS_DP			EVENTOUT

Table 2-11. Port C alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC0											USBHS_ULPI_STP		EXMC_SDNWE			EVENTOUT
PC1						SPI2_MOSI/I2S2_SD		SPI1_MOSI/I2S1_SD				ENET_MDC				EVENTOUT
PC2						SPI1_MISO	I2S1_ADD_SD				USBHS_ULPI_DIR	ENET_MII_TXD2	EXMC_SDNE0			EVENTOUT
PC3						SPI1_MOSI/I2S1_SD					USBHS_ULPI_NXT	ENET_MII_TX_CLK	EXMC_SDCKE0			EVENTOUT
PC4												ENET_MII_RXD0/ENET_RMII_RXD0	EXMC_SDNE0			EVENTOUT
PC5								USART2_RX				ENET_MII_RXD1/ENET_RMII_RXD1	EXMC_SDCKE0			EVENTOUT
PC6			TIMER2_CH0	TIMER7_CH0		I2S1_MCK			USART5_TX				SDIO_D6	DCI_D0		EVENTOUT
PC7			TIMER2_CH1	TIMER7_CH1		SPI1_SCK/I2S1_CK	I2S2_MCK		USART5_RX				SDIO_D7	DCI_D1		EVENTOUT
PC8	TRACED0		TIMER2_CH2	TIMER7_CH2					USART5_CK				SDIO_D0	DCI_D2		EVENTOUT

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC9	CK_OUT1		TIMER2_CH3	TIMER7_CH3	I2C2_SDA	I2S_CKIN							SDIO_D1	DCI_D3		EVENTOUT
PC10							SPI2_SCK/I2S2_CK	USART2_TX	UART3_TX				SDIO_D2	DCI_D8		EVENTOUT
PC11						I2S2_ADD_SD	SPI2_MISO	USART2_RX	UART3_RX				SDIO_D3	DCI_D4		EVENTOUT
PC12					I2C1_SDA		SPI2_MOSI/I2S2_SD	USART2_CK	UART4_TX				SDIO_CK	DCI_D9		EVENTOUT
PC13																EVENTOUT
PC14																EVENTOUT
PC15																EVENTOUT

Table 2-12. Port D alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PD0							SPI2_MOSI/I2S2_SD			CAN0_RX			EXMC_D2			EVENTOUT
PD1								SPI1_NSS/I2S1_WS		CAN0_TX			EXMC_D3			EVENTOUT
PD2			TIMER2_ETI						UART4_RX				SDIO_CMD	DCI_D11		EVENTOUT
PD3	TRACED1					SPI1_SCK/I2S1_CK		USART1_CTS					EXMC_CLK	DCI_D5		EVENTOUT
PD4								USART1_RTS					EXMC_NOE			EVENTOUT
PD5								USART1_TX					EXMC_NWE			EVENTOUT
PD6						SPI2_MOSI/I2S2_SD		USART1_RX					EXMC_NWAIT	DCI_D10		EVENTOUT
PD7								USART1_CK					EXMC_NE0/EXMC_NCE1			EVENTOUT

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PD8								USART2_TX					EXMC_D13			EVENTOUT
PD9								USART2_RX					EXMC_D14			EVENTOUT
PD10								USART2_CK					EXMC_D15			EVENTOUT
PD11								USART2_CTS					EXMC_A16/EXMC_CLE			EVENTOUT
PD12			TIMER3_CH0					USART2_RTS					EXMC_A17/EXMC_ALE			EVENTOUT
PD13			TIMER3_CH1										EXMC_A18			EVENTOUT
PD14			TIMER3_CH2										EXMC_D0			EVENTOUT
PD15	CTC_SYNC		TIMER3_CH3										EXMC_D1			EVENTOUT

Table 2-13. Port E alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PE0			TIMER3_ETI										EXMC_NBL0	DCI_D2		EVENTOUT
PE1		TIMER0_CH1_ON											EXMC_NBL1	DCI_D3		EVENTOUT
PE2	TRACECK											ENET_MII_TXD3	EXMC_A23			EVENTOUT
PE3	TRACED0												EXMC_A19			EVENTOUT
PE4	TRACED1												EXMC_A20	DCI_D4		EVENTOUT
PE5	TRACED2			TIMER8_CH0									EXMC_A21	DCI_D6		EVENTOUT

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PE6	TRACED3			TIMER8_CH1									EXMC_A22	DCI_D7		EVENTOUT
PE7		TIMER0_ETI											EXMC_D4			EVENTOUT
PE8		TIMER0_CH0_ON											EXMC_D5			EVENTOUT
PE9		TIMER0_CH0											EXMC_D6			EVENTOUT
PE10		TIMER0_CH1_ON											EXMC_D7			EVENTOUT
PE11		TIMER0_CH1											EXMC_D8			EVENTOUT
PE12		TIMER0_CH2_ON											EXMC_D9			EVENTOUT
PE13		TIMER0_CH2											EXMC_D10			EVENTOUT
PE14		TIMER0_CH3											EXMC_D11			EVENTOUT
PE15		TIMER0_BRKIN											EXMC_D12			EVENTOUT

Table 2-14. Port F alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PF0	CTC_SYNC				I2C1_SDA								EXMC_A0			EVENTOUT
PF1					I2C1_SCL								EXMC_A1			EVENTOUT
PF2					I2C1_SMBA								EXMC_A2			EVENTOUT
PF3					I2C1_TXFRAME								EXMC_A3			EVENTOUT
PF4													EXMC_A4			EVENTOUT
PF5													EXMC_A5			EVENTOUT

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PF6				TIMER9_CH0									EXMC_NIORD			EVENTOUT
PF7				TIMER10_CH0									EXMC_NREG			EVENTOUT
PF8										TIMER12_CH0			EXMC_NIOWR			EVENTOUT
PF9										TIMER13_CH0			EXMC_CD			EVENTOUT
PF10													EXMC_INTR	DCI_D11		EVENTOUT
PF11													EXMC_SDNRAS	DCI_D12		EVENTOUT
PF12													EXMC_A6			EVENTOUT
PF13													EXMC_A7			EVENTOUT
PF14													EXMC_A8			EVENTOUT
PF15													EXMC_A9			EVENTOUT

Table 2-15. Port G alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PG0													EXMC_A10			EVENTOUT
PG1													EXMC_A11			EVENTOUT
PG2													EXMC_A12			EVENTOUT
PG3													EXMC_A13			EVENTOUT
PG4													EXMC_A14			EVENTOUT
PG5													EXMC_A15			EVENTOUT
PG6													EXMC_INT1	DCI_D12		EVENTOUT

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PG7									USART5_CK				EXMC_INT2	DCI_D13		EVENTOUT
PG8									USART5_RTS			ENET_PPS_OUT	EXMC_SDCLK			EVENTOUT
PG9									USART5_RX				EXMC_NE1/EXMC_NCE2	DCI_VSYNC		EVENTOUT
PG10													EXMC_NCE3_0/EXMC_NE2	DCI_D2		EVENTOUT
PG11												ENET_MII_TX_EN/ENET_RMII_TX_EN	EXMC_NCE3_1	DCI_D3		EVENTOUT
PG12									USART5_RTS				EXMC_NE3			EVENTOUT
PG13	TRACED2								USART5_CTS			ENET_MII_TXD0/ENET_RMII_TXD0	EXMC_A24			EVENTOUT
PG14	TRACED3								USART5_TX			ENET_MII_TXD1/ENET_RMII_TXD1	EXMC_A25			EVENTOUT
PG15									USART5_CTS				EXMC_SDNCAS	DCI_D13		EVENTOUT

Table 2-16. Port H alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PH0																EVENTOUT
PH1																EVENTOUT
PH2												ENET_MII_CRS	EXMC_SDCKE0			EVENTOUT
PH3					I2C1_TXFRAME							ENET_MII_COL	EXMC_SDNE0			EVENTOUT

PH4					I2C1_SCL						USBHS_ULPI_NXT					EVENTOUT
PH5					I2C1_SDA								EXMC_SDNWE			EVENTOUT
PH6					I2C1_SMBA					TIMER11_CH0		ENET_MII_RXD2	EXMC_SDNE1	DCI_D8		EVENTOUT
PH7					I2C2_SCL							ENET_MII_RXD3	EXMC_SDCKE1	DCI_D9		EVENTOUT
PH8					I2C2_SDA								EXMC_D16	DCI_HSYNC		EVENTOUT
PH9					I2C2_SMBA					TIMER11_CH1			EXMC_D17	DCI_D0		EVENTOUT
PH10			TIMER4_CH0		I2C2_TXFRAME								EXMC_D18	DCI_D1		EVENTOUT
PH11			TIMER4_CH1										EXMC_D19	DCI_D2		EVENTOUT
PH12			TIMER4_CH2										EXMC_D20	DCI_D3		EVENTOUT
PH13				TIMER7_CH0_ON						CAN0_TX			EXMC_D21			EVENTOUT
PH14				TIMER7_CH1_ON									EXMC_D22	DCI_D4		EVENTOUT
PH15				TIMER7_CH2_ON									EXMC_D23	DCI_D11		EVENTOUT

Table 2-17. Port I alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PI0			TIMER4_CH3			SPI1_NSS/I2S1_WS							EXMC_D24	DCI_D13		EVENTOUT
PI1						SPI1_SCK/I2S1_CK							EXMC_D25	DCI_D8		EVENTOUT
PI2				TIMER7_CH3		SPI1_MISO	I2S1_ADD_SD						EXMC_D26	DCI_D9		EVENTOUT
PI3				TIMER7_ETI		SPI1_MOSI/I2S1_SD							EXMC_D27	DCI_D10		EVENTOUT

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11
PI4				TIMER7_BRKIN								
PI5				TIMER7_CH0								
PI6				TIMER7_CH1								
PI7				TIMER7_CH2								
PI8												
PI9										CAN0_RX		
PI10												ENET_M_RX_ER
PI11											USBHS_ULPI_DIR	

3.4. Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from main Flash memory (default)
- Boot from system memory
- Boot from on-chip SRAM

The boot loader is located in the internal 30KB of information blocks for the boot ROM memory (system memory). It is used to reprogram the Flash memory by using USART0 (PA9 and PA10), USART2 (PB10 and PB11, or PC10 and PC11), and USBFS (PA9, PA10, PA11 and PA12) in device mode. It also can be used to transfer and update the Flash memory code, the data and the vector table sections. In default condition, boot from bank 0 of Flash memory is selected. It also supports to boot from bank 1 of Flash memory by setting a bit in option bytes.

3.5. Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are sleep mode, deep-sleep mode, and standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Sleep** mode
  In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt/event can wake up the system.
- **Deep-sleep** mode
  In deep-sleep mode, all clocks in the 1.2V domain are off, and all of the high speed crystal oscillator (IRC16M, HXTAL) and PLL are disabled. Only the contents of SRAM and registers are retained. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep mode including the 16 external lines, the RTC alarm, RTC Tamper and TimeStamp event, the LVD output, ENET wakeup, RTC wakeup and USB wakeup. When exiting the deep-sleep mode, the IRC16M is selected as the system clock.
- **Standby** mode
  In standby mode, the whole 1.2V domain is power off, the LDO is shut down, and all of IRC16M, HXTAL and PLL are disabled. The contents of SRAM and registers (except backup registers) are lost. There are four wakeup sources for the standby mode, including the external reset from NRST pin, the RTC, the FWDGT reset, and the rising edge on WKUP pin.

3.6. Analog to digital converter (ADC)

- 12-bit SAR ADC's conversion rate is up to 2.6 MSPS

- 12-bit, 10-bit, 8-bit or 6-bit configurable resolution
- Hardware oversampling ratio adjustable from 2x to 256x improves resolution to 16-bit
- Input voltage range: V_{SSA} to V_{DDA} (2.6 V ÒV$_{DDA}$ Ò3.6 V)
- Temperature sensor

Up to three 12-bit 2.6 MSPS multi-channel ADCs are integrated in the device. It has a total of 19 multiplexed channels: 16 external channels, 1 channel for internal temperature sensor (V_{SENSE}), 1 channel for internal reference voltage (V_{REFINT}) and 1 channel for external battery power supply (V_{BAT}). The input voltage range is between 2.6 V and 3.6 V. An on-chip hardware oversampling scheme improves performance while off-loading the related computational burden from the CPU. An analog watchdog block can be used to detect the channels, which are required to remain within a specific threshold window. A configurable channel management block can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced use.

The ADC can be triggered from the events generated by the general level 0 timers (TIMERx) and the advanced timers (TIMER0 and TIMER7) with internal connection. The temperature sensor can be used to generate a voltage that varies linearly with temperature. It is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage in a digital value.

3.7. Digital to analog converter (DAC)

- Two 12-bit DAC converter of independent output channel
- 8-bit or 12-bit mode in conjunction with the DMA controller

The two 12-bit buffered DACs are used to generate variable analog outputs. The DAC channels can be triggered by the timer or EXTI with DMA support. In dual DAC channel operation, conversions could be done independently or simultaneously. The maximum output value of the DAC is V_{REF+}.

3.8. DMA

- 16 channels DMA controller and each channel are configurable (8 for DMA0 and 8 for DMA1)
- Support independent 8, 16, 32-bit memory and peripheral transfer
- Peripherals supported: Timers, ADC, SPIs, I2Cs, USARTs, UARTs, DAC, I2S, SDIO and DCI

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory.

Each channel is connected to fixed hardware DMA requests. The priorities of DMA channel

requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.

3.9. General-purpose inputs/outputs (GPIOs)

- Up to 140 fast GPIOs, all mappable on 16 external interrupt lines
- Analog input/output configurable
- Alternate function input/output configurable

There are up to 140 general purpose I/O pins (GPIO) in GD32F407xx, named PA0 ~ PA15, PB0 ~ PB15, PC0 ~ PC15, PD0 ~ PD15, PE0 ~ PE15, PF0 ~ PF15, PG0 ~ PG15, PH0 ~ PH15 and PI0 ~ PI11 to implement logic input/output functions. Each of the GPIO ports has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the Interrupt/event controller (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current capable except for analog inputs.

3.10. Timers and PWM generation

- Two 16-bit advanced timer (TIMER0 & TIMER7), eight 16-bit general timers (TIMER2, TIMER3, TIMER8 ~ TIMER13), two 32-bit general timers (TIMER1 & TIMER4) and two 16-bit basic timer (TIMER5 & TIMER6)
- Up to 4 independent channels of PWM, output compare or input capture for each general timer and external trigger input
- 16-bit, motor control PWM advanced timer with programmable dead-time generation for output match
- Encoder interface controller with two inputs using quadrature decoder
- 24-bit SysTick timer down counter
- 2 watchdog timers (free watchdog timer and window watchdog timer)

The advanced timer (TIMER0 & TIMER7) can be used as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general timer. The 4 independent channels can be used for input capture, output compare, PWM generation (edge-aligned or center-aligned counting modes) and single pulse mode output. If configured as a general 16-bit timer, it has the same functions as the TIMERx timer. It can be synchronized with external signals or to interconnect with other general timers together which have the same architecture and features.

The general timer, can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation

or PWM output, up to 4 independent channels for input capture/output compare. TIMER1 & TIMER4 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TIMER2 & TIMER3 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. TIMER8 ~ TIMER13 is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. The general timer also supports an encoder interface with two inputs using quadrature decoder.

The basic timer, known as TIMER5 & TIMER6, are mainly used for DAC trigger generation. They can also be used as a simple 16-bit time base.

The GD32F407xx have two watchdog peripherals, free watchdog timer and window watchdog timer. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and an 8-bit prescaler. It is clocked from an independent 32 KHz internal RC and as it operates independently of the main clock, it can operate in deep-sleep and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog timer is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early wakeup interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.11. Real time clock (RTC) and backup registers

- Independent binary-coded decimal (BCD) format timer/counter with twenty 32-bit backup registers
- Calendar with sub-second, seconds, minutes, hours, week day, date, year and month automatically correction
- Alarm function with wake up from deep-sleep and standby mode capability
- On-the-fly correction for synchronization with master clock. Digital calibration with 1 ppm resolution for compensation of quartz crystal inaccuracy

The real time clock is an independent timer which provides a set of continuously running counters in backup registers to provide a real calendar function, and provides an alarm interrupt or an expected interrupt. It is not reset by a system or power reset, or when the device wakes up from standby mode. A prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 KHz from external crystal oscillator.

3.12. Inter-integrated circuit (I2C)

- Up to three I2C bus interfaces can support both master and slave mode with a frequency up to 400 KHz (Fast mode)
- Provide arbitration function, optional PEC (packet error checking) generation and checking
- Supports 7-bit and 10-bit addressing mode and general call addressing mode

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides transfer rate of up to 100 KHz in standard mode and up to 400 KHz in fast mode. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

3.13. Serial peripheral interface (SPI)

- Up to three SPI interfaces with a frequency of up to 30 MHz
- Support both master and slave mode
- Hardware CRC calculation and transmit automatic CRC error checking

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). Both SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking.

3.14. Universal synchronous/asynchronous receiver transmitter (USART/UART)

- Up to four USARTs and two UARTs with operating speed up to 10.5 MBit/s
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder support
- LIN break generation and detection
- ISO 7816-3 compliant smart card interface

The USART (USART0, USART1, USART2, USART5) and UART (UART3, UART4) are used to transfer data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART/UART includes a programmable baud rate generator

which is capable of dividing the system clock to produce a dedicated clock for the USART/UART transmitter and receiver. The USART/UART also supports DMA function for high speed data communication.

3.15. Inter-IC sound (I2S)

- Two I2S bus Interfaces with sampling frequency from 8 KHz to 192 KHz, multiplexed with SPI1 and SPI2
- Support either master or slave mode Audio
- Sampling frequencies from 8 KHz up to 192 KHz are supported

The Inter-IC sound (I2S) bus provides a standard communication interface for digital audio applications by 4-wire serial lines. GD32F407xx contain an I2S-bus interface that can be operated with 16/32 bit resolution in master or slave mode, pin multiplexed with SPI1 and SPI2. The audio sampling frequencies from 8 KHz to 192 KHz is supported.

3.16. Universal serial bus full-speed interface (USBFS)

- One USB device/host/OTG full-speed Interface with frequency up to 12 Mbit/s
- Internal 48 MHz oscillator support crystal-less operation
- Internal main PLL for USB CLK compliantly
- Internal USBFS PHY support

The Universal Serial Bus (USB) is a 4-wire bus with 4 bidirectional endpoints. The device controller enables 12 Mbit/s data exchange with integrated transceivers. Transaction formatting is performed by the hardware, including CRC generation and checking. It supports both host and device modes, as well as OTG mode with Host Negotiation Protocol (HNP) and Session Request Protocol (SRP). The controller contains a full-speed USB PHY internal. For full-speed or low-speed operation, no more external PHY chip is needed. It supports all the four types of transfer (control, bulk, Interrupt and isochronous) defined in USB 2.0 protocol. The required precise 48 MHz clock which can be generated from the internal main PLL (the clock source must use an HXTAL crystal oscillator) or by the internal 48 MHz oscillator in automatic trimming mode that allows crystal-less operation.

3.17. Universal serial bus high-speed interface (USBHS)

- One USB device/host/OTG high-speed Interface with frequency up to 480 Mbit/s
- An external PHY device connected to the ULPI is required when using in HS mode

USBHS supports both host and device modes, as well as OTG mode with Host Negotiation Protocol (HNP) and Session Request Protocol (SRP). The controller provides ULPI interface for external USB PHY integration and it also contains a full-speed USB PHY internal. For full-speed or low-speed operation, no more external PHY chip is needed. It supports all the four

types of transfer (control, bulk, Interrupt and isochronous) defined in USB 2.0 protocol. HUB connection is supported when USBHS operates at high-speed in host mode. There is also a DMA engine operating as an AHB bus master in USBHS to speed up the data transfer between USBHS and system.

3.18. Controller area network (CAN)

- Two CAN2.0B interface with communication frequency up to 1 Mbit/s
- Internal main PLL for CAN CLK compliantly

Controller area network (CAN) is a method for enabling serial communication in field bus. The CAN protocol has been used extensively in industrial automation and automotive applications. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three mailboxes for transmission and two FIFOs of three message deep for reception. It also provides 28 scalable/configurable identifier filter banks for selecting the incoming messages needed and discarding the others.

3.19. Ethernet (ENET)

- IEEE 802.3 compliant media access controller (MAC) for Ethernet LAN
- 10/100 Mbit/s rates with dedicated DMA controller and SRAM
- Support hardware precision time protocol (PTP) with conformity to IEEE 1588

The Ethernet media access controller (MAC) conforms to IEEE 802.3 specifications and fully supports IEEE 1588 standards. The embedded MAC provides the interface to the required external network physical interface (PHY) for LAN bus connection via an internal media independent interface (MII) or a reduced media independent interface (RMII). The number of MII signals provided up to 16 with 25 MHz output and RMII up to 7 with 50 MHz output. The function of 32-bit CRC checking is also available.

3.20. External memory controller (EXMC)

- Supported external memory: SRAM, PSRAM, ROM and NOR-Flash, NAND Flash and CF card, SDRAM with up to 32-bit data bus
- Provide ECC calculating hardware module for NAND Flash memory block
- Two SDRAM banks with independent configuration, up to 13-bits Row Address, 11-bits Column Address, 2-bits internal banks address
- SDRAM Memory size: 4x16Mx32bit (256 MB), 4x16Mx16bit (128 MB), 4x16Mx8bit (64 MB)

External memory controller (EXMC) is an abbreviation of external memory controller. It is divided in to several sub-banks for external device support, each sub-bank has its own chip selection signal but at one time, only one bank can be accessed. The EXMC supports code

execution from external memory except NAND Flash and CF card. The EXMC also can be configured to interface with the most common LCD module of Motorola 6800 and Intel 8080 series and reduce the system cost and complexity.

The EXMC of GD32F407xx in LQFP144 & BGA176 package also supports synchronous dynamic random access memory (SDRAM). It translates AHB transactions into the appropriate SDRAM protocol, and meanwhile, makes sure the access time requirements of the external SDRAM devices are satisfied.

3.21. Secure digital input and output card interface (SDIO)

- Support SD2.0/SDIO2.0/MMC4.2 host interface

The Secure Digital Input and Output Card Interface (SDIO) provides access to external SD memory cards specifications version 2.0, SDIO card specification version 2.0 and multi-media card system specification version 4.2 with DMA supported. In addition, this interface is also compliant with CE-ATA digital protocol rev1.1.

3.22. Digital camera interface (DCI)

- Digital video/picture capture
- 8/10/12/14 data width supported
- High transfer efficiency with DMA interface
- Video/picture crop supported
- Various pixel formats supported including JPEG/YCrCb/RGB
- Hard/embedded synchronous signals supported

DCI is an 8-bit to 14-bit parallel interface that able to capture video or picture from a camera via Digital Camera Interface. It supports 8/10/12/14 bits data width through DMA operation.

3.23. Debug mode

- Serial wire JTAG debug port (SWJ-DP)

The Arm® SWJ-DP Interface is embedded and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

3.24. Package and operation temperature

- BGA176 (GD32F407Ix), BGA100 (GDF407VxH), LQFP144 (GD32F407Zx), LQFP100 (GD32F407Vx) and LQFP64 (GD32F407Rx)
- Operation temperature range: -40ÁC to +85ÁC (industrial level)

4. Electrical characteristics

4.1. $EVROXWH PD[LPXP UDWLQJV

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-1. Absolute maximum ratings(1)(4)

Symbol	Parameter	Min	Max	Unit
V_{DD}	External voltage range(2)	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{DDA}	External analog supply voltage	V_{SSA} - 0.3	V_{SSA} + 3.6	V
V_{BAT}	External battery supply voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{IN}	Input voltage on 5V tolerant pin(3)	V_{SS} - 0.3	V_{DD} + 3.6	V
	Input voltage on other I/O	V_{SS} - 0.3	3.6	V
|qpV$_{DDX}$|	Variations between different V_{DD} power pins	ð	50	mV
|V$_{SSX}$ ī V$_{SS}$|	Variations between different ground pins	ð	50	mV
I_{IO}	Maximum current for GPIO pins	ð	25	mA
T_A	Operating temperature range	-40	+85	°C
P_D	Power dissipation at T_A = 85°C of BGA176	ð	888	mW
	Power dissipation at T_A = 85°C of LQFP144	ð	820	
	Power dissipation at T_A = 85°C of BGA100	ð	511	
	Power dissipation at T_A = 85°C of LQFP100	ð	697	
	Power dissipation at T_A = 85°C of LQFP64	ð	772	
T_{STG}	Storage temperature range	-65	+150	°C
T_J	Maximum junction temperature	ð	125	°C

(1) Guaranteed by design, not tested in production.
(2) All main power and ground pins should be connected to an external power source within the allowable range.
(3) V_{IN} maximum value cannot exceed 5.5 V.
(4) It is recommended that V_{DD} and V_{DDA} are powered by the same source. The maximum difference between V_{DD} and V_{DDA} does not exceed 300 mV during power-up and operation.

4.2. 2SHUDWLQJ FRQGLWLRQV FKDUDFWHULVWLF

Table 4-2. DC operating conditions

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DD}	Supply voltage	ð	2.6	3.3	3.6	V
V_{DDA}	Analog supply voltage	Same as V_{DD}	2.6	3.3	3.6	V
V_{BAT}	Battery supply voltage	ð	1.8	ð	3.6	V

(1) Based on characterization, not tested in production.

Table 4-6. Power saving mode wakeup timings characteristics(1)(2)

Symbol	Parameter	Typ	Unit
t_{Sleep}	Wakeup from Sleep mode	1.5	εs
$t_{Deep-sleep}$	Wakeup from Deep-sleep mode ÄLDO On Å	3.3	
	Wakeup from Deep-sleep mode ÄLDO in low power mode Å	3.3	
$t_{Standby}$	Wakeup from Standby mode	143	ms

(1) Based on characterization, not tested in production.

(2) The wakeup time is measured from the wakeup event to the point at which the application code reads the first instruction under the below conditions: V_{DD} = V_{DDA} = 3.3 V, IRC16M = System clock = 16 MHz.

4.3. 3RZHU FRQVXPSWLRQ

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications.

Table 4-7. 3RZHU FRQVXPSWLRQ IRU DFWHULVWLFV

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
I_{DD}+I_{DDA}	Supply current (Run mode)	V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 168 MHz, All peripherals enabled	ð	83.00	ð	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 168 MHz, All peripherals disabled	ð	50.90	ð	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 120 MHz, All peripherals enabled	ð	60.74	ð	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 120 MHz, All peripherals disabled	ð	37.34	ð	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 108 MHz, All peripherals enabled	ð	55.36	ð	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 108 MHz, All peripherals disabled	ð	34.76	ð	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 90 MHz, All peripherals enabled	ð	46.22	ð	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 90 MHz, All peripherals disabled	ð	29.52	ð	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 60 MHz, All peripherals enabled	ð	31.98	ð	mA

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 60 MHz, All peripherals disabled	ð	20.64	ð	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 30 MHz, All peripherals enabled	ð	18.06	ð	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 30 MHz, All peripherals disabled	ð	12.16	ð	mA
		V_{DD} = V_{DDA} = 3.3 V, IRC16M = 16 MHz, System clock = 25 MHz, All peripherals enabled	ð	14.4	ð	mA
		V_{DD} = V_{DDA} = 3.3 V, IRC16M = 16 MHz, System clock = 25 MHz, All peripherals disabled	ð	9.48	ð	mA
		V_{DD} = V_{DDA} = 3.3 V, IRC16M = 16 MHz,System clock = 16 MHz, All peripherals enabled	ð	10.1	ð	mA
		V_{DD} = V_{DDA} = 3.3 V, IRC16M = 16 MHz, System clock = 16 MHz, All peripherals disabled	ð	6.96	ð	mA
		V_{DD} = V_{DDA} = 3.3 V, IRC16M = 16 MHz, System clock = 8 MHz, All peripherals enabled	ð	6.38	ð	mA
		V_{DD} = V_{DDA} = 3.3 V, IRC16M = 16 MHz, System clock = 8 MHz, All peripherals disabled	ð	4.78	ð	mA
		V_{DD} = V_{DDA} = 3.3 V, IRC16M = 16 MHz, System clock = 4 MHz, All peripherals enabled	ð	4.28	ð	mA
		V_{DD} = V_{DDA} = 3.3 V, IRC16M = 16 MHz, System clock = 4 MHz, All peripherals disabled	ð	3.5	ð	mA
		V_{DD} = V_{DDA} = 3.3 V, IRC16M = 16 MHz, System clock = 2 MHz, All peripherals enabled	ð	3.4	ð	mA
		V_{DD} = V_{DDA} = 3.3 V, IRC16M = 16 MHz, System clock = 2 MHz, All peripherals disabled	ð	2.99	ð	mA
	Supply current (Sleep mode)	V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 168 MHz, CPU clock off, All peripherals enabled	ð	56.00	ð	mA

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 168 MHz, CPU clock off, All peripherals disabled	ð	24.3	ð	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 120 MHz, CPU clock off, All peripherals enabled	ð	41.64	ð	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 120 MHz, CPU clock off, All peripherals disabled	ð	18.72	ð	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 108 MHz, CPU clock off, All peripherals enabled	ð	38.58	ð	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 108 MHz, CPU clock off, All peripherals disabled	ð	17.96	ð	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 90 MHz, CPU clock off, All peripherals enabled	ð	31.94	ð	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 90 MHz, CPU clock off, All peripherals disabled	ð	14.94	ð	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 60 MHz, CPU clock off, All peripherals enabled	ð	22.48	ð	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 60 MHz, CPU clock off, All peripherals disabled	ð	11.16	ð	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 30 MHz, CPU clock off, All peripherals enabled	ð	13.34	ð	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 30 MHz, CPU clock off, All peripherals disabled	ð	7.58	ð	mA
		V_{DD} = V_{DDA} = 3.3 V, IRC16M = 16 MHz, System clock = 25 MHz, CPU clock off, All peripherals enabled	ð	10.52	ð	mA
		V_{DD} = V_{DDA} = 3.3 V, IRC16M = 16 MHz, System clock = 25 MHz, CPU clock off, All peripherals disabled	ð	5.7	ð	mA
		V_{DD} = V_{DDA} = 3.3 V, IRC16M = 16 MHz,System clock = 16 MHz, CPU clock off, All peripherals enabled	ð	7.58	ð	mA

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		V_{DD} = V_{DDA} = 3.3 V, IRC16M = 16 MHz, System clock = 16 MHz, CPU clock off, All peripherals disabled	ð	4.54	ð	mA
		V_{DD} = V_{DDA} = 3.3 V, IRC16M = 16 MHz, System clock = 8 MHz, CPU clock off, All peripherals enabled	ð	5.18	ð	mA
		V_{DD} = V_{DDA} = 3.3 V, IRC16M = 16 MHz, System clock = 8 MHz, CPU clock off, All peripherals disabled	ð	3.58	ð	mA
		V_{DD} = V_{DDA} = 3.3 V, IRC16M = 16 MHz, System clock = 4 MHz, CPU clock off, All peripherals enabled	ð	3.78	ð	mA
		V_{DD} = V_{DDA} = 3.3 V, IRC16M = 16 MHz, System clock = 4 MHz, CPU clock off, All peripherals disabled	ð	3	ð	mA
		V_{DD} = V_{DDA} = 3.3 V, IRC16M = 16 MHz, System clock = 2 MHz, CPU clock off, All peripherals enabled	ð	3.14	ð	mA
		V_{DD} = V_{DDA} = 3.3 V, IRC16M = 16 MHz, System clock = 2 MHz, CPU clock off, All peripherals disabled	ð	2.74	ð	mA
	Supply current (Deep-Sleep mode)	V_{DD} = V_{DDA} = 3.3 V, LDO in normal power and normal driver mode, IRC32K off, RTC off, All GPIOs analog mode	ð	1.21	11	mA
		V_{DD} = V_{DDA} = 3.3 V, LDO in normal power and low driver mode, IRC32K off, RTC off, All GPIOs analog mode	ð	1.18	11	mA
		V_{DD} = V_{DDA} = 3.3 V, LDO in low power and normal driver mode , IRC32K off, RTC off, All GPIOs analog mode	ð	0.83	11	mA
		V_{DD} = V_{DDA} = 3.3 V, LDO in low power and low driver mode, IRC32K off, RTC off, All GPIOs analog mode	ð	0.8	11	mA
	Supply current (Standby mode)	V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC32K on, RTC on SRAM ON	ð	6.84	16.5	εA
		V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC32K on, RTC off SRAM ON	ð	6.5	16.5	εA
		V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC32K off, RTC off SRAM ON	ð	5.92	16.5	εA
		V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC32K on, RTC on SRAM OFF	ð	5.22	16.5	εA

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC32K on, RTC off SRAM OFF	ð	4.87	16.5	εA
		V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC32K off, RTC off SRAM OFF	ð	4.3	16.5	εA
I_{BAT}	Battery supply current (Backup mode)	V_{DD} off, V_{DDA} off, V_{BAT} = 3.6 V, LXTAL on with external crystal, RTC on, LXTAL High driving SRAM ON	ð	3.84	ð	εA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.3 V, LXTAL on with external crystal, RTC on, LXTAL High driving SRAM ON	ð	3.46	ð	εA
		V_{DD} off, V_{DDA} off, V_{BAT} = 2.6 V, LXTAL on with external crystal, RTC on, LXTAL High driving SRAM ON	ð	3.26	ð	εA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.6 V, LXTAL on with external crystal, RTC on, LXTAL High driving SRAM OFF	ð	1.99	ð	εA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.3 V, LXTAL on with external crystal, RTC on, LXTAL High driving SRAM OFF	ð	1.82	ð	εA
		V_{DD} off, V_{DDA} off, V_{BAT} = 2.6 V, LXTAL on with external crystal, RTC on, LXTAL High driving, SRAM OFF	ð	1.52	ð	εA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.6 V, LXTAL on with external crystal, RTC on, LXTAL Low driving, SRAM ON	ð	3.2	ð	εA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.3 V, LXTAL on with external crystal, RTC on, LXTAL Low driving, SRAM ON	ð	2.9	ð	εA
		V_{DD} off, V_{DDA} off, V_{BAT} = 2.6 V, LXTAL on with external crystal, RTC on, LXTAL Low driving, SRAM ON	ð	2.65	ð	εA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.6 V, LXTAL on with external crystal, RTC on, LXTAL Low driving, SRAM OFF	ð	1.36	ð	εA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.3 V, LXTAL on with external crystal, RTC on, LXTAL Low driving, SRAM OFF	ð	1.25	ð	εA
		V_{DD} off, V_{DDA} off, V_{BAT} = 2.6 V, LXTAL on with external crystal, RTC on, LXTAL Low driving, SRAM OFF	ð	0.91	ð	εA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.6 V, LXTAL off with external crystal, RTC off, SRAM ON	ð	1.98	ð	εA

APB1	DAC1+DAC2(2)	4.49	
	PMU	0.25	
	CAN1	0.22	
	CAN0	0.25	
	I2C2	0.13	
	I2C1	0.14	
	I2C0	0.15	
	UART4	0.11	
	UART3	0.08	
	USART2	0.16	
	USART1	0.14	
	SPI2/I2S2(3)	0.05/0.10	
	SPI1/I2S1(3)	0.05/0.13	
	WWDG	0.77	
	TIMER13	0.77	
	TIMER12	0.85	
	TIMER11	0.86	
	TIMER6	0.66	
	TIMER5	0.65	
	TIMER4	1.05	
	TIMER3	0.97	
	TIMER2	0.96	
	TIMER1	1.04	
APB2	SPI5	0.03	
	SPI4	0.03	
	TIMER10	0.54	
	TIMER9	0.53	
	TIMER8	0.58	
	SYSCFG	0.02	
	SPI3	0.05	
	SPI0	0.76	
	SDIO	1.26	
	ADC2(4)	1.06	
	ADC1(4)	1.08	
	ADC0(4)	1.41	
	USART5	0.98	
	USART0	0.89	
	TIMER7	1.87	
	TIMER0	1.84	
ADDAPB1	IREF	0.36	
	CTC	0.78	

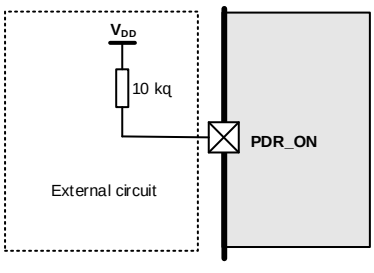
(1) Based on characterization, not tested in production.

(2) DEN0 and DEN1 bits in the DAC_CTL register are set to 1, and the converted value set to 0x800.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		LVDT<2:0> = 001(rising edge)	ð	2.28	ð	
		LVDT<2:0> = 001(falling edge)	ð	2.17	ð	
		LVDT<2:0> = 010(rising edge)	ð	2.43	ð	
		LVDT<2:0> = 010(falling edge)	ð	2.31	ð	
		LVDT<2:0> = 011(rising edge)	ð	2.56	ð	
		LVDT<2:0> = 011(falling edge)	ð	2.45	ð	
		LVDT<2:0> = 100(rising edge)	ð	2.7	ð	
		LVDT<2:0> = 100(falling edge)	ð	2.59	ð	
		LVDT<2:0> = 101(rising edge)	ð	2.84	ð	
		LVDT<2:0> = 101(falling edge)	ð	2.73	ð	
		LVDT<2:0> = 110(rising edge)	ð	2.98	ð	
		LVDT<2:0> = 110(falling edge)	ð	2.87	ð	
		LVDT<2:0> = 111(rising edge)	ð	3.12	ð	
		LVDT<2:0> = 111(falling edge)	ð	3.01	ð	
$V_{LVDhyst}$(2)	LVD hystersis	ð	ð	100	ð	mV
V_{POR}(1)	Power on reset threshold	ð	ð	2.40	ð	V
V_{PDR}(1)	Power down reset threshold	ð	ð	1.80	ð	V
$V_{PDRhyst}$(2)	PDR hysteresis	ð	ð	600	ð	mV
V_{BOR3}(2)	Brownout level 3 threshold	Falling edge	ð	2.79	ð	V
		Rising edge	ð	2.88	ð	V
V_{BOR2}(2)	Brownout level 2 threshold	Falling edge	ð	2.49	ð	V
		Rising edge	ð	2.58	ð	V
V_{BOR1}(2)	Brownout level 1 threshold	Falling edge	ð	2.19	ð	V
		Rising edge	ð	2.29	ð	V
$V_{BORhyst}$(2)	BOR hysteresis	ð	ð	100	ð	mV
$t_{RSTTEMPO}$(2)	Reset temporization	ð	ð	2	ð	ms

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.


V_{DD}
10 kΩ
PDR_ON
External circuit

characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL}(1)	Crystal or ceramic frequency	2.6 V ÒV$_{DD}$ Ò3.6 V	4	8	32	MHz
R_F(2)	Feedback resistor	V_{DD} = 3.3 V	ð	400	ð	kq
C_{HXTAL}(2) (3)	Recommended matching capacitance on OSCIN and OSCOUT	ð	ð	20	30	pF
Ducy$_{(HXTAL)}$(2)	Crystal or ceramic duty cycle	ð	30	50	70	%
g_m(2)	Oscillator transconductance	Startup	ð	25	ð	mA/V
$I_{DDHXTAL}$(1)	Crystal or ceramic operating current	V_{DD} = 3.3 V, f_{HCLK} = f_{IRC16M} = 16 MHz	ð	1	ð	mA
$t_{SUHXTAL}$(1)	Crystal or ceramic startup time	V_{DD} = 3.3 V, f_{HCLK} = f_{IRC16M} = 16 MHz	ð	1.8	ð	ms

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) C_{HXTAL1} = C_{HXTAL2} = 2*(C_{LOAD} - C_S), For C_{HXTAL1} and C_{HXTAL2}, it is recommended matching capacitance on OSCIN and OSCOUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

Table 4-15. High speed external clock characteristics (HXTAL in bypass mode)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL_ext}(1)	External clock source or oscillator frequency	2.6 V ÒV$_{DD}$ Ò 3.6 V	1	ð	50	MHz
V_{HXTALH}(2)	OSCIN input pin high level voltage	V_{DD} = 3.3 V	0.7 V_{DD}	ð	V_{DD}	V
V_{HXTALL}(2)	OSCIN input pin low level voltage		V_{SS}	ð	0.3 V_{DD}	V
$t_{H/L(HXTAL)}$ (2)	OSCIN high or low time	ð	5	ð	ð	ns
$t_{R/F(HXTAL)}$ (2)	OSCIN rise or fall time	ð	ð	ð	10	ns
C_{IN}(2)	OSCIN input capacitance	ð	ð	5	ð	pF
Ducy$_{(HXTAL)}$ (2)	Duty cycle	ð	40	ð	60	%

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Table 4-16. Low speed external clock (LXTAL) generated from a crystal/ceramic

characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LXTAL}(1)	Crystal or ceramic frequency	V_{DD} = 3.3 V	ð	32.768	ð	kHz
C_{LXTAL}(2) (3)	Recommended matching capacitance on OSC32IN and OSC32OUT	ð	ð	15	ð	pF
$Ducy_{(LXTAL)}$(2)	Crystal or ceramic duty cycle	ð	30	ð	70	%
g_m(2)	Oscillator transconductance	Medium low driving capability	ð	6	ð	εA/V
		Higher driving capability	ð	18	ð	
$I_{DDLXTAL}$ (1)	Crystal or ceramic operating current	LXTALDRI[1:0]= 01	ð	0.9	ð	εA
		LXTALDRI[1:0]= 11	ð	1.5	ð	
$t_{SULXTAL}$(1) (4)	Crystal or ceramic startup time	ð	ð	1.8	ð	s

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) $C_{LXTAL1} = C_{LXTAL2} = 2*(C_{LOAD} - C_S)$, For C_{LXTAL1} and C_{LXTAL2}, it is recommended matching capacitance on OSC32IN and OSC32OUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

(4) $t_{SULXTAL}$ is the startup time measured from the moment it is enabled (by software) to the 32.768 kHz oscillator stabilization flags is SET. This value varies significantly with the crystal manufacturer.

Table 4-17. Low speed external user clock characteristics (LXTAL in bypass mode)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LXTAL_ext}(1)	External clock source or oscillator frequency	V_{DD} = 3.3 V	ð	32.768	1000	kHz
V_{LXTALH}(2)	OSC32IN input pin high level voltage	ð	0.7 V_{DD}	ð	V_{DD}	V
V_{LXTALL}(2)	OSC32IN input pin low level voltage	ð	V_{SS}	ð	0.3 V_{DD}	
$t_{H/L(LXTAL)}$ (2)	OSC32IN high or low time	ð	450	ð	ð	ns
$t_{R/F(LXTAL)}$ (2)	OSC32IN rise or fall time	ð	ð	ð	50	
C_{IN}(2)	OSC32IN input capacitance	ð	ð	5	ð	pF
$Ducy_{(LXTAL)}$ (2)	Duty cycle	ð	30	50	70	%

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

4.8. Internal clock characteristics

Table 4-18. High speed internal clock (IRC16M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC16M}	High Speed Internal Oscillator (IRC16M) frequency	V_{DD} = V_{DDA} = 3.3 V	ð	16	ð	MHz
ACC_{IRC16M}	IRC16M oscillator Frequency accuracy, Factory-trimmed	V_{DD} = V_{DDA} = 3.3 V, T_A = -40 ÁC ~ +85 ÁC(1)	-4.0	ð	+5.0	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = 0 ÁC ~ +85 ÁC(1)	-2.0	ð	+2.0	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = 25 ÁC	-1.0	ð	+1.0	%
	IRC16M oscillator Frequency accuracy, User trimming step	ð	ð	0.5	ð	%
$Ducy_{IRC16M}$(2)	IRC16M oscillator duty cycle	V_{DD} = V_{DDA} = 3.3 V	45	50	55	%
$I_{DDAIRC16M}$(1)	IRC16M oscillator operating current	V_{DD} = V_{DDA} = 3.3 V, f_{HCLK} = f_{HXTAL_PLL} = 168 MHz	ð	66	80	εA
$t_{SUIRC16M}$(1)	IRC16M oscillator startup time	V_{DD} = V_{DDA} = 3.3 V, f_{HCLK} = f_{HXTAL_PLL} = 168 MHz	ð	2.5	4	εs

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Table 4-19. High speed internal clock (IRC48M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC48M}	High Speed Internal Oscillator (IRC48M) frequency	V_{DD} = 3.3 V	ð	48	ð	MHz
ACC_{IRC48M}	IRC48M oscillator Frequency accuracy, Factory-trimmed	V_{DD} = V_{DDA} = 3.3 V, T_A = -40 ÁC ~ +85 ÁC(1)	-4.0	ð	+5.0	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = 0 ÁC ~ +85 ÁC (1)	-3.0	ð	+3.0	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = 25 ÁC	-2.0	ð	+2.0	%
	IRC48M oscillator Frequency accuracy, User trimming step	ð	ð	0.12	ð	%
$Ducy_{IRC48M}$(2)	IRC48M oscillator duty cycle	V_{DD} = V_{DDA} = 3.3 V	45	50	55	%
$I_{DDAIRC48M}$(1)	IRC48M oscillator operating current	V_{DD} = V_{DDA} = 3.3 V, f_{HCLK} = f_{HXTAL_PLL} = 168 MHz	ð	240	300	εA
$t_{SUIRC48M}$(1)	IRC48M oscillator startup time	V_{DD} = V_{DDA} = 3.3 V, f_{HCLK} = f_{HXTAL_PLL} = 168 MHz	ð	2.5	4	εs

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Table 4-20. Low speed internal clock (IRC32K) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC32K}(1)	Low Speed Internal oscillator (IRC32K) frequency	V_{DD} = V_{DDA} = 3.3 V, T_A = -40 ÁC ~ +85 ÁC	ð	32	ð	kHz
$I_{DDIRC32K}$(2)	IRC32K oscillator operating current	V_{DD} = V_{DDA} = 3.3 V, f_{HCLK} = f_{HXTAL_PLL} = 168 MHz,	ð	0.4	0.6	εA
$t_{SUIRC32K}$(2)	IRC32K oscillator startup time	V_{DD} = V_{DDA} = 3.3 V, f_{HCLK} = f_{HXTAL_PLL} = 168 MHz,	ð	110	150	εs

(1) Guaranteed by design, not tested in production.

(2) Based on characterization, not tested in production.

4.9. 3// FKDUDFWHULVWLFV

Table 4-21. PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}(1)	PLL input clock frequency	ð	1	ð	4	MHz
f_{PLLOUT}(2)	PLL output clock frequency	ð	100	ð	500	MHz
f_{VCO}(2)	PLL VCO output clock frequency	ð	32	ð	344	MHz
t_{LOCK}(2)	PLL lock time	VCO freq = 100 MHz	ð	80	168	εs
		VCO freq = 500 MHz	ð	100	300	
I_{DDA}(1)(3)	Current consumption on VDDA	VCO freq = 500 MHz	ð	1100	ð	εA
$Jitter_{PLL}$	Cycle to cycle Jitter(rms)	System clock	ð	40	ð	ps
	Cycle to cycle Jitter Äpeak to peak Å		ð	400	ð	

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) System clock = IRC16M = 16 MHz, PLL clock source = IRC16M/2 = 8 MHz, f_{PLLOUT} = 168 MHz.

(4) Value given with main PLL running.

Table 4-22. PLLI2S characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}(1)	PLLI2S input clock frequency	ð	1	ð	4	MHz
f_{PLLOUT}(2)	PLLI2S output clock frequency	ð	100	ð	500	MHz
f_{VCO}(2)	PLLI2S VCO output clock frequency	ð	32	ð	344	MHz
t_{LOCK}(2)	PLLI2S lock time	VCO freq = 100 MHz	ð	80	168	εs
		VCO freq = 500 MHz	ð	100	300	
I_{DDA}(1)(3)	Current consumption on VDDA	VCO freq = 500 MHz	ð	1100	ð	εA
$Jitter_{PLL}$	Cycle to cycle Jitter(rms)	System clock	ð	40	ð	ps
	Cycle to cycle Jitter Äpeak to peak Å		ð	400	ð	

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) System clock = IRC16M = 16 MHz, PLL clock source = IRC16M/2 = 8 MHz, f_{PLLOUT} = 168 MHz.
(4) Value given with main PLLI2S running.

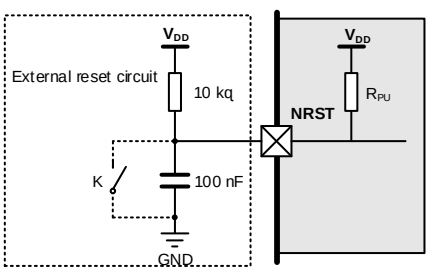
Table 4-23. PLLSAI characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}(1)	PLLSAI input clock frequency	ð	1	ð	4	MHz
f_{PLLOUT}(2)	PLLSAI output clock frequency	ð	100	ð	500	MHz
f_{VCO}(2)	PLLSAI VCO output clock frequency	ð	32	ð	344	MHz
t_{LOCK}(2)	PLLSAI lock time	VCO freq = 100 MHz	ð	80	168	εs
		VCO freq = 500 MHz	ð	100	300	
I_{DDA}(1)(3)	Current consumption on VDDA	VCO freq = 500 MHz	ð	1100	ð	εA
$Jitter_{PLL}$	Cycle to cycle Jitter(rms)	System clock	ð	40	ð	ps
	Cycle to cycle Jitter Äpeak to peak Å		ð	400	ð	

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) System clock = IRC16M = 16 MHz, PLL clock source = IRC16M/2 = 8 MHz, f_{PLLOUT} = 168 MHz.
(4) Value given with main PLLSAI running.

Table 4-24. PLL spread spectrum clock generation (SSCG) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{mod}	Modulation frequency	ð	ð	ð	10	KHz
mdamp	Peak modulation amplitude	ð	ð	ð	2	%
MODCNT* MODSTEP	ð	ð	ð	ð	2^{15}-1	ð


V_{DD}
External reset circuit
10 kΩ
K
100 nF
GND
V_{DD}
R_{PU}
NRST

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Table 4-31. ADC dynamic accuracy at f_{ADC} = 30 MHz(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 30 MHz	10.5	10.6	ð	bits
SNDR	Signal-to-noise and distortion ratio	V_{DDA} = V_{REF+} = 2.6 V	65	65.6	ð	dB
SNR	Signal-to-noise ratio	Input Frequency = 110 kHz	65.5	66	ð	
THD	Total harmonic distortion	Temperature = 25 -	-74	-76	ð	

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Table 4-32. ADC dynamic accuracy at f_{ADC} = 30 MHz(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 30 MHz	10.7	10.8	ð	bits
SNDR	Signal-to-noise and distortion ratio	V_{DDA} = V_{REF+} = 3.3 V	66.2	65.8	ð	dB
SNR	Signal-to-noise ratio	Input Frequency = 110 kHz	66.8	67.4	ð	
THD	Total harmonic distortion	Temperature = 25 -	-71	-75	ð	

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Table 4-33. ADC dynamic accuracy at f_{ADC} = 36 MHz(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 36 MHz	10.3	10.4	ð	bits
SNDR	Signal-to-noise and distortion ratio	V_{DDA} = V_{REF+} = 3.3 V	63.8	64.4	ð	dB
SNR	Signal-to-noise ratio	Input Frequency = 110 kHz	64.2	65	ð	
THD	Total harmonic distortion	Temperature = 25 -	-70	-72	ð	

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Table 4-34. ADC dynamic accuracy at f_{ADC} = 40 MHz(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 40 MHz	9.9	10.0	ð	bits
SNDR	Signal-to-noise and distortion ratio	V_{DDA} = V_{REF+} = 3.3 V	61.4	62	ð	dB
SNR	Signal-to-noise ratio	Input Frequency = 110 kHz	62	62.4	ð	
THD	Total harmonic distortion	Temperature = 25 -	-68	-70	ð	

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Table 4-35. ADC static accuracy at f_{ADC} = 15 MHz(1)

Symbol	Parameter	Test conditions	Typ	Max	Unit
Offset	Offset error	f_{ADC} = 15 MHz	Ñ2	Ñ3	LSB
DNL	Differential linearity error	V_{DDA} = V_{REF+} = 3.3 V	Ñ0.9	Ñ1.2	
INL	Integral linearity error		Ñ1.1	Ñ1.5	

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

4.14. Temperature sensor characteristics

Table 4-36. Temperature sensor characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
T_L	V_{SENSE} linearity with temperature	ð	Ñ1.5	ð	-
Avg_Slope	Average slope	ð	4.1	ð	mV/ -
V_{25}	Voltage at 25 °C	ð	1.45	ð	V
t_{S_temp} (2)	ADC sampling time when reading the temperature	ð	17.1	ð	εs

(1) Based on characterization, not tested in production.
(2) Shortest sampling time can be determined in the application by multiple iterations.

4.15. DAC characteristics

Table 4-37. DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}(1)	Operating voltage	ð	2.6	3.3	3.6	V
V_{REF+}(2)	Positive Reference Voltage	ð	2.6	ð	V_{DDA}	V
V_{REF-}(2)	Negative Reference Voltage	ð	ð	V_{SSA}	ð	V
R_{LOAD}(2)	Resistive load	Resistive load with buffer ON	5	ð	ð	kq
Ro(2)	Impedance output	Impedance output with buffer OFF	ð	ð	15	kq
C_{LOAD}(2)	Capacitive load	Capacitive load with buffer ON	ð	ð	50	pF
DAC_OUT min(2)	Lower DAC_OUT voltage	Lower DAC_OUT voltage with buffer ON	0.2	ð	ð	V
		Lower DAC_OUT voltage with buffer OFF	0.5	ð	ð	mV
DAC_OUT max(2)	Higher DAC_OUT voltage	Higher DAC_OUT voltage with buffer ON	ð	ð	V_{DDA}-0.2	V
		Higher DAC_OUT voltage with buffer OFF	ð	ð	V_{DDA}-1LSB	V
I_{DDA}(1)	DAC current consumption in quiescent mode	With no load, middle code(0x800) on the input, V_{REF+} = 3.6 V	ð	ð	500	εA
		With no load, worst code(0xF1C) on the input, V_{REF+} = 3.6 V	ð	ð	560	
$I_{DDVREF+}$(1)	DAC current consumption in quiescent mode	With no load, middle code(0x800) on the input, V_{REF+} = 3.6 V	ð	86	ð	εA

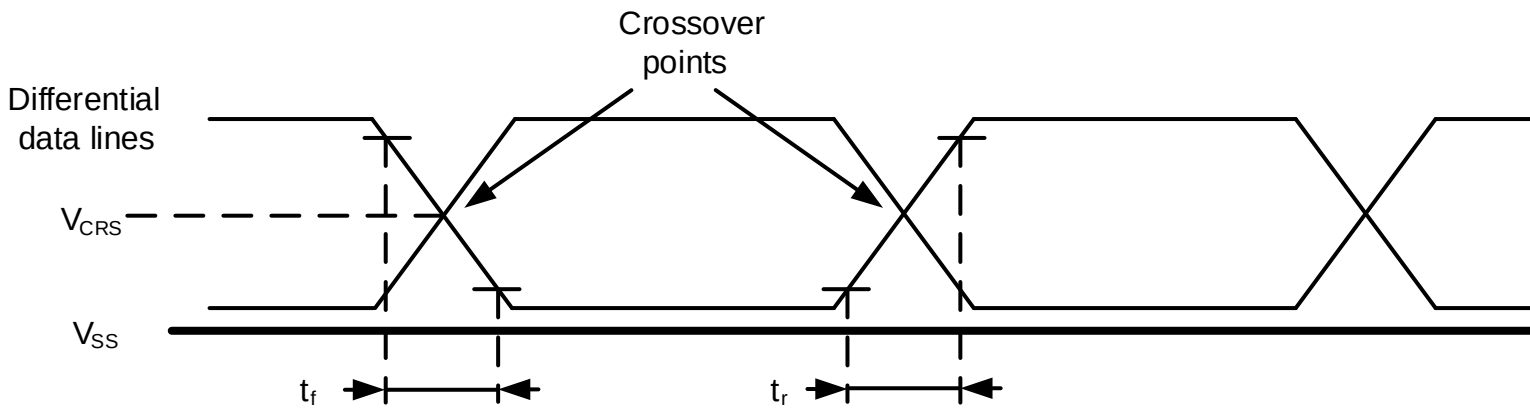
4.18. , 6 F K D U D F W H U L V W L F V

Table 4-40. I2S characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	Clock frequency	Master mode (data: 16 bits, Audio frequency = 96 kHz)	ð	3.078	ð	MHz
		Slave mode	ð	10	ð	
t_H	Clock high time	ü	ð	162	ð	ns
t_L	Clock low time		ð	163	ð	ns
$t_{V(WS)}$	WS valid time	Master mode	ð	2	ð	ns
$t_{H(WS)}$	WS hold time	Master mode	ð	2	ð	ns
$t_{SU(WS)}$	WS setup time	Slave mode	0	ð	ð	ns
$t_{H(WS)}$	WS hold time	Slave mode	3	ð	ð	ns
$Ducy_{(SCK)}$	I2S slave input clock duty cycle	Slave mode	ð	50	ð	%
$t_{SU(SD\_MR)}$	Data input setup time	Master mode	0	ð	ð	ns
$t_{su(SD\_SR)}$	Data input setup time	Slave mode	0	ð	ð	ns
$t_{H(SD\_MR)}$	Data input hold time	Master receiver	1	ð	ð	ns
$t_{H(SD\_SR)}$		Slave receiver	3	ð	ð	ns
$t_{V(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	ð	12	ð	ns
$t_{H(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	ð	10	ð	ns
$t_{V(SD\_MT)}$	Data output valid time	Master transmitter (after enable edge)	ð	10	ð	ns
$t_{H(SD\_MT)}$	Data output hold time	Master transmitter (after enable edge)	ð	7	ð	ns

(1) Guaranteed by design, not tested in production.

(2) Based on characterization, not tested in production.


Crossover
points
Differential
data lines
V_{CRS}
V_{SS}
t_f
t_r

4.23. USBHS characteristics

Table 61. USBHS clock timing parameters(1)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	USBHS operating voltage	3.0	ð	3.6	V
f_{HCLK}	f_{HCLK} value to guarantee proper operation of USBHS interface	30	ð	ð	MHz
F_{START_8BIT}	Frequency (first transition) 8-bit ± 10%	54	60	66	MHz
F_{STEADY}	Frequency (steady state) ±500 ppm	59.97	60	60.63	MHz
D_{START_8BIT}	Duty cycle (first transition) 8-bit ± 10%	40	50	60	%
D_{STEADY}	Duty cycle (steady state) ±500 ppm	49.975	50	50.025	%

(1) Guaranteed by design, not tested in production.

Table 62. USB-ULPI Dynammic characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{SC}	Control in (ULPI_DIR, ULPI_NXT) setup time	ð	ð	2	ns
t_{HC}	Control in (ULPI_DIR, ULPI_NXT) hold time	0.5	ð	ð	ns
t_{SD}	Data in setup time	ð	ð	2	ns
t_{HD}	Data in hold time	0	ð	ð	ns

(1) Guaranteed by design, not tested in production.

4.24. EXMC characteristics

Table 4-46. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	EXMC_NE low time	28.75	30.75	ns
$t_{V(NOE\_NE)}$	EXMC_NEx low to EXMC_NOE low	0	ð	ns
$t_{w(NOE)}$	EXMC_NOE low time	28.75	30.75	ns
$t_{h(NE\_NOE)}$	EXMC_NOE high to EXMC_NE high hold time	0	ð	ns
$t_{v(A\_NE)}$	EXMC_NEx low to EXMC_A valid	0	ð	ns
$t_{v(BL\_NE)}$	EXMC_NEx low to EXMC_BL valid	0	ð	ns
$t_{su(DATA\_NE)}$	Data to EXMC_NEx high setup time	22.8	ð	ns
$t_{su(DATA\_NOE)}$	Data to EXMC_NOEx high setup time	22.8	ð	ns
$t_{h(DATA\_NOE)}$	Data hold time after EXMC_NOE high	0	ð	ns
$t_{h(DATA\_NE)}$	Data hold time after EXMC_NEx high	0	ð	ns
$t_{v(NADV\_NE)}$	EXMC_NEx low to EXMC_NADV low	0	ð	ns
$t_{w(NADV)}$	EXMC_NADV low time	4.95	6.95	ns

(1) C_L = 30 pF.

(2) Guaranteed by design, not tested in production.

(3) Based on configure: f_{HCLK} = 168 MHz, AddressSetupTime = 0, AddressHoldTime = 1, DataSetupTime = 1.

Table 4-47. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	EXMC_NE low time	16.85	18.85	ns
$t_{V(NWE\_NE)}$	EXMC_NEx low to EXMC_NWE low	4.95	ð	ns
$t_{w(NWE)}$	EXMC_NWE low time	4.95	6.95	ns
$t_{h(NE\_NWE)}$	EXMC_NWE high to EXMC_NE high hold time	4.95	6.95	ns
$t_{v(A\_NE)}$	EXMC_NEx low to EXMC_A valid	0	ð	ns
$t_{V(NADV\_NE)}$	EXMC_NEx low to EXMC_NADV low	0	ð	ns
$t_{w(NADV)}$	EXMC_NADV low time	4.95	6.95	ns
$t_{h(AD\_NADV)}$	EXMC_AD(address) valid hold time after EXMC_NADV high	10.9	ð	ns
$t_{h(A\_NWE)}$	Address hold time after EXMC_NWE high	4.95	ð	ns
$t_{h(BL\_NWE)}$	EXMC_BL hold time after EXMC_NWE high	4.95	ð	ns
$t_{v(BL\_NE)}$	EXMC_NEx low to EXMC_BL valid	0	ð	ns
$t_{v(DATA\_NADV)}$	EXMC_NADV high to DATA valid	0	ð	ns
$t_{h(DATA\_NWE)}$	Data hold time after EXMC_NWE high	4.95	ð	ns

(1) C_L = 30 pF.

(2) Guaranteed by design, not tested in production.

(3) Based on configure: f_{HCLK} = 168 MHz, AddressSetupTime = 0, AddressHoldTime = 1, DataSetupTime = 1.

Table 4-48. Asynchronous multiplexed PSRAM/NOR read timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	EXMC_NE low time	40.65	42.65	ns
$t_{V(NOE\_NE)}$	EXMC_NEx low to EXMC_NOE low	16.85	ð	ns
$t_{w(NOE)}$	EXMC_NOE low time	22.8	24.8	ns
$t_{h(NE\_NOE)}$	EXMC_NOE high to EXMC_NE high hold time	0	ð	ns
$t_{v(A\_NE)}$	EXMC_NEx low to EXMC_A valid	0	ð	ns
$t_{v(A\_NOE)}$	Address hold time after EXMC_NOE high	0	ð	ns
$t_{v(BL\_NE)}$	EXMC_NEx low to EXMC_BL valid	0	ð	ns
$t_{h(BL\_NOE)}$	EXMC_BL hold time after EXMC_NOE high	0	ð	ns
$t_{su(DATA\_NE)}$	Data to EXMC_NEx high setup time	22.8	ð	ns
$t_{su(DATA\_NOE)}$	Data to EXMC_NOEx high setup time	22.8	ð	ns
$t_{h(DATA\_NOE)}$	Data hold time after EXMC_NOE high	0	ð	ns
$t_{h(DATA\_NE)}$	Data hold time after EXMC_NEx high	0	ð	ns
$t_{v(NADV\_NE)}$	EXMC_NEx low to EXMC_NADV low	0	ð	ns
$t_{w(NADV)}$	EXMC_NADV low time	4.95	6.95	ns
$T_{h(AD\_NADV)}$	EXMC_AD(adress) valid hold time after EXMC_NADV high	4.95	6.95	ns

(1) C_L = 30 pF.

(2) Guaranteed by design, not tested in production.

(3) Based on configure: f_{HCLK}= 168 MHz, AddressSetupTime = 0, AddressHoldTime = 1, DataSetupTime = 1.

Table 4-49. Asynchronous multiplexed PSRAM/NOR write timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	EXMC_NE low time	28.75	30.75	ns

$t_{d(CLKH-NWEH)}$	EXMC_CLK high to EXMC_NWE high	10.9	ð	ns
$t_{d(CLKL-ADIV)}$	EXMC_CLK low to EXMC_AD invalid	0	ð	ns
$t_{d(CLKL-DATA)}$	EXMC_A/D valid data after EXMC_CLK low	0	ð	ns
$t_{h(CLKL-NBLH)}$	EXMC_CLK low to EXMC_NBL high	0	ð	ns

(1) C_L = 30 pF.

(2) Guaranteed by design, not tested in production.

(3) Based on configure: f_{HCLK} = 168 MHz, BurstAccessMode = Enable; MemoryType = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by HCLK); DataLatency = 1.

Table 4-52. Synchronous non-multiplexed PSRAM/NOR read timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	EXMC_CLK period	23.8	ð	ns
$t_{d(CLKL-NExL)}$	EXMC_CLK low to EXMC_NEx low	0	ð	ns
$t_{d(CLKH-NExH)}$	EXMC_CLK high to EXMC_NEx high	10.9	ð	ns
$t_{d(CLKL-NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	ð	ns
$t_{d(CLKL-NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	ð	ns
$t_{d(CLKL-AV)}$	EXMC_CLK low to EXMC_Ax valid	0	ð	ns
$t_{d(CLKH-AIV)}$	EXMC_CLK high to EXMC_Ax invalid	10.9	ð	ns
$t_{d(CLKL-NOEL)}$	EXMC_CLK low to EXMC_NOE low	0	ð	ns
$t_{d(CLKH-NOEH)}$	EXMC_CLK high to EXMC_NOE high	10.9	ð	ns

(1) C_L = 30 pF.

(2) Guaranteed by design, not tested in production.

(3) Based on configure: f_{HCLK} = 168 MHz, BurstAccessMode = Enable; MemoryType = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by HCLK); DataLatency = 1.

Table 4-53. Synchronous non-multiplexed PSRAM write timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	EXMC_CLK period	23.8	ð	ns
$t_{d(CLKL-NExL)}$	EXMC_CLK low to EXMC_NEx low	0	ð	ns
$t_{d(CLKH-NExH)}$	EXMC_CLK high to EXMC_NEx high	10.9	ð	ns
$t_{d(CLKL-NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	ð	ns
$t_{d(CLKL-NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	ð	ns
$t_{d(CLKL-AV)}$	EXMC_CLK low to EXMC_Ax valid	0	ð	ns
$t_{d(CLKH-AIV)}$	EXMC_CLK high to EXMC_Ax invalid	10.9	ð	ns
$t_{d(CLKL-NWEL)}$	EXMC_CLK low to EXMC_NWE low	0	ð	ns
$t_{d(CLKH-NWEH)}$	EXMC_CLK high to EXMC_NWE high	10.9	ð	ns
$t_{d(CLKL-DATA)}$	EXMC_A/D valid data after EXMC_CLK low	0	ð	ns
$t_{h(CLKL-NBLH)}$	EXMC_CLK low to EXMC_NBL high	0	ð	ns

(1) C_L = 30 pF.

(2) Guaranteed by design, not tested in production.

(3) Based on configure: f_{HCLK} = 168 MHz, BurstAccessMode = Enable; MemoryType = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by HCLK); DataLatency = 1.

4.25. TIMER characteristics

Table 4-54. TIMER characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{res}	Timer resolution time	ð	1	ð	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 168 MHz	5.95	ð	ns
f_{EXT}	Timer external clock frequency	ð	0	$f_{TIMERxCLK}/2$	MHz
		$f_{TIMERxCLK}$ = 168 MHz	0	84	MHz
RES	Timer resolution	TIMERx (except TIMER1 & TIMER4)	ð	16	bit
		TIMER1 & TIMER4	ð	32	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	ð	1	65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 168 MHz	0.006	390.95	εs
t_{MAX_COUNT}	Maximum possible count	ð	ð	65536x65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 168 MHz	ð	25.57	s

(1) Guaranteed by design, not tested in production.

4.26. DCI characteristics

Table 4-55. DCI characteristics(1)

Symbol	Parameter	Min	Max	Unit
Frequency ratio	DCI_PIXCLK /fHCLK	ð	0.4	
DCI_PIXCLK	Pixel clock input	ð	80	MHz
D_{Pixel}	Pixel clock input duty cycle	30	70	%
$t_{su(DATA)}$	Data input setup time	2.5	ð	ns
$t_{h(DATA)}$	Data output valid time	1	ð	ns
$t_{su(HS)}$	DCI_HS input setup time	2	ð	ns
$t_{su(VS)}$	DCI_VS input setup time	2	ð	ns
$t_{h(HS)}$	DCI_HS input hold time	0.5	ð	ns
$t_{h(VS)}$	DCI_VS input hold time	0.5	ð	ns

(1) Guaranteed by design, not tested in production.

4.27. WDGT characteristics

Table 4-56. FWDGT min/max timeout period at 32 kHz (IRC32K)(1)

Prescaler divider	PSC[2:0] bits	Min timeout RLD[11:0] = 0x000	Max timeout RLD[11:0] = 0xFFF	Unit
1/4	000	0.03125	511.90625	ms
1/8	001	0.03125	1023.7812	
1/16	010	0.03125	2047.53125	
1/32	011	0.03125	4095.03125	
1/64	100	0.03125	8190.03125	
1/128	101	0.03125	16380.03125	
1/256	110 or 111	0.03125	32760.03125	

(1) Guaranteed by design, not tested in production.

Table 4-57. WWDGT min-max timeout value at 42 MHz (f_{PCLK1})(1)

Prescaler divider	PSC[1:0]	Min timeout value CNT[6:0] = 0x40	Unit	Max timeout value CNT[6:0] = 0x7F	Unit
1/1	00	97.52	εs	6.24	ms
1/2	01	195.05		12.48	
1/4	10	390.10		24.97	
1/8	11	780.19		49.93	

(1) Guaranteed by design, not tested in production.

4.28. Parameter conditions

Unless otherwise specified, all values given for V_{DD} = V_{DDA} = 3.3 V, T_A = 25 .

5. Package information

5.1 BGA176 package outline dimensions

Figure 5-1. BGA176 package outline

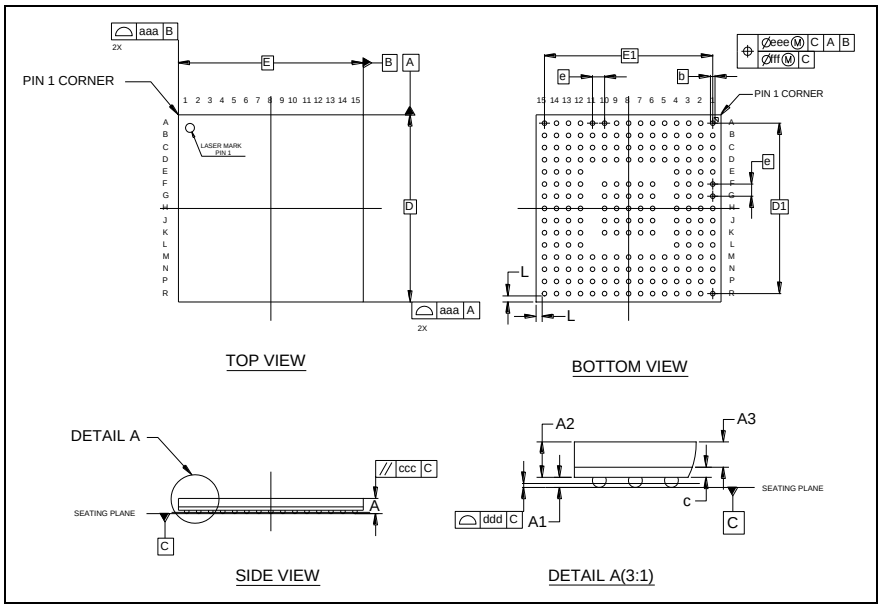
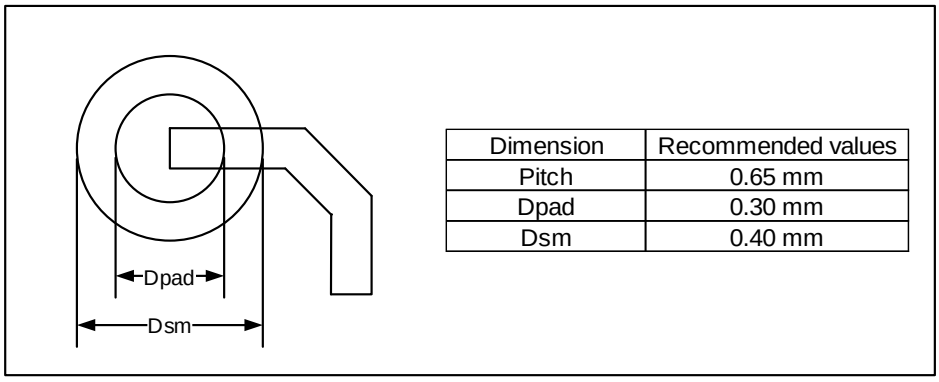


Table 5-1. BGA176 package dimensions

Symbol	Min	Typ	Max
A	ð	ð	0.89
A1	0.13	0.18	0.23
A2	0.58	0.63	0.68
A3	ð	0.45	ð
b	0.20	0.25	0.30
c	0.15	0.18	0.21
D	9.90	10.00	10.10
D1	ð	9.10	ð
E	9.90	10.00	10.10
E1	ð	9.10	ð
e	ð	0.65	ð
L	ð	0.325	ð
aaa	ð	0.10	ð
ccc	ð	0.20	ð
ddd	ð	0.08	ð
eee	ð	0.15	ð
fff	ð	0.08	ð

(Original dimensions are in millimeters)

Figure 5-2. BGA176 recommended footprint



Dimension	Recommended values
Pitch	0.65 mm
Dpad	0.30 mm
Dsm	0.40 mm

(Original dimensions are in millimeters)

5.2 LQFP144 package outline dimensions

Figure 5-3. LQFP144 package outline

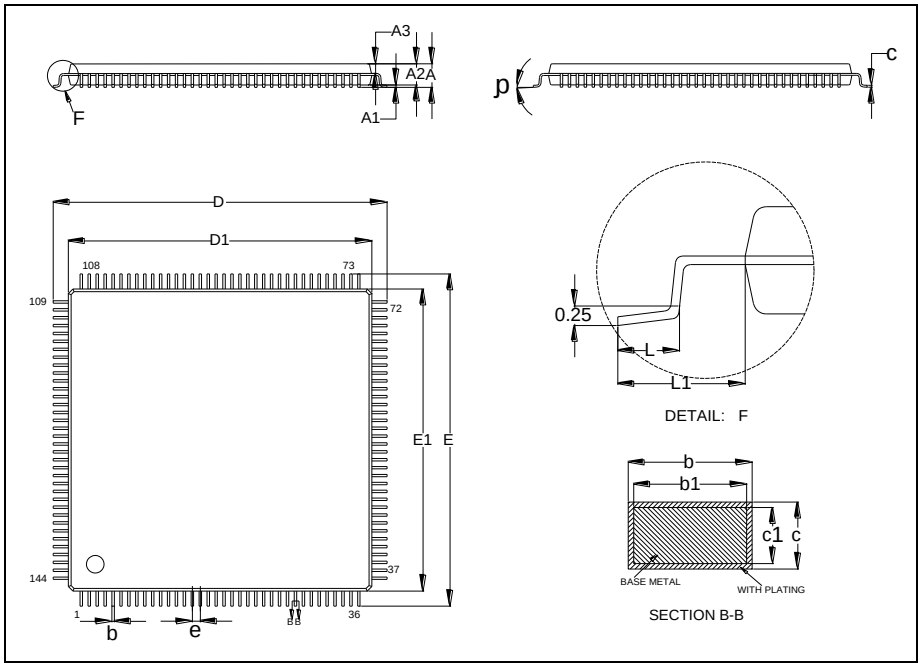
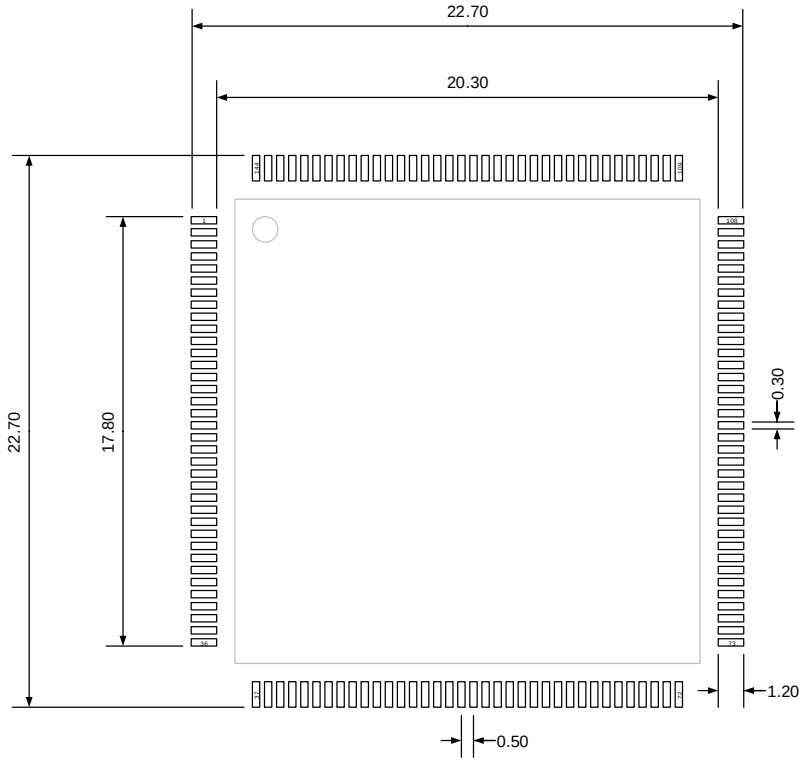


Table 5-2. LQFP144 package dimensions

Symbol	Min	Typ	Max
A	ð	ð	1.60
A1	0.05	ð	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	ð	0.26
b1	0.17	0.20	0.23
c	0.13	ð	0.17
c1	0.12	0.13	0.14
D	21.80	22.00	22.20
D1	19.90	20.00	20.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
e	ð	0.50	ð
L	0.45	ð	0.75
L1	ð	1.00	ð
ɗ	0 e	ð	7 e

(Original dimensions are in millimeters)

Figure 5-4. LQFP144 recommended footprint



(Original dimensions are in millimeters

5.3 BGA100 package outline dimensions

Figure 5-5. BGA100 package outline

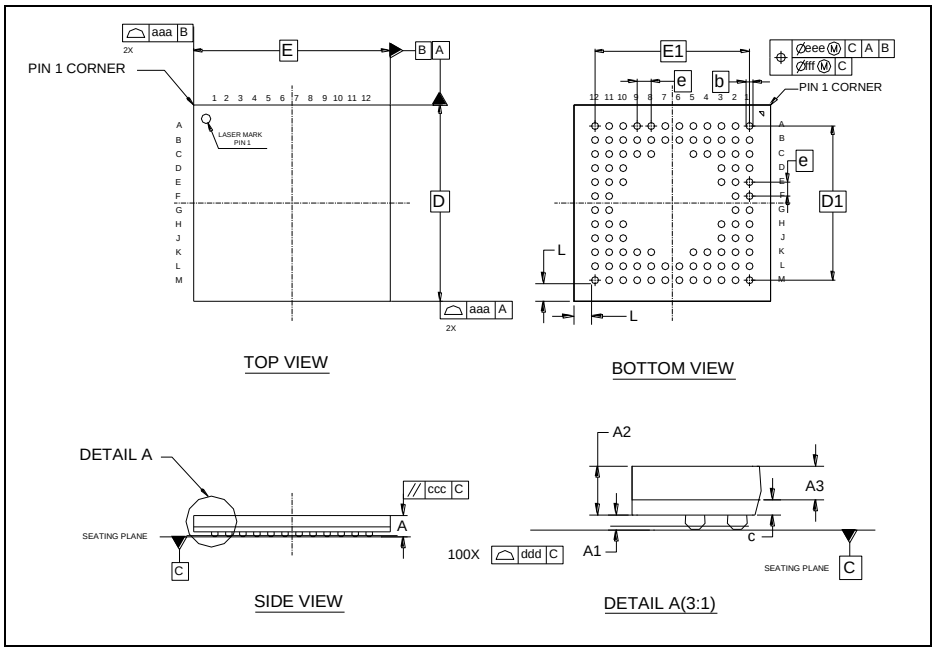
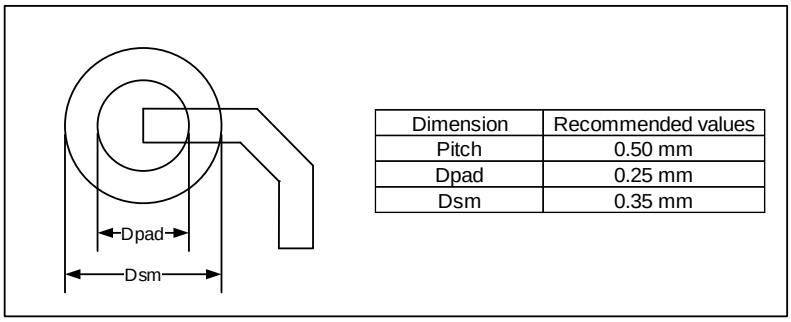


Table 5-3. BGA100 package dimensions

Symbol	Min	Typ	Max
A	ð	ð	0.84
A1	0.13	0.18	0.23
A2	0.53	0.58	0.63
A3	ð	0.40	ð
b	0.20	0.25	0.30
c	0.15	0.18	0.21
D	6.90	7.00	7.10
D1	ð	5.50	ð
E	6.90	7.00	7.10
E1	ð	5.50	ð
e	ð	0.50	ð
L	ð	0.625	ð
aaa	ð	0.10	ð
ccc	ð	0.20	ð
ddd	ð	0.08	ð
eee	ð	0.15	ð
fff	ð	0.08	ð

(Original dimensions are in millimeters)

Figure 5-6. BGA100 recommended footprint



Dimension	Recommended values
Pitch	0.50 mm
Dpad	0.25 mm
Dsm	0.35 mm

(Original dimensions are in millimeters)

5.4 LQFP100 package outline dimensions

Figure 5-7. LQFP100 package outline

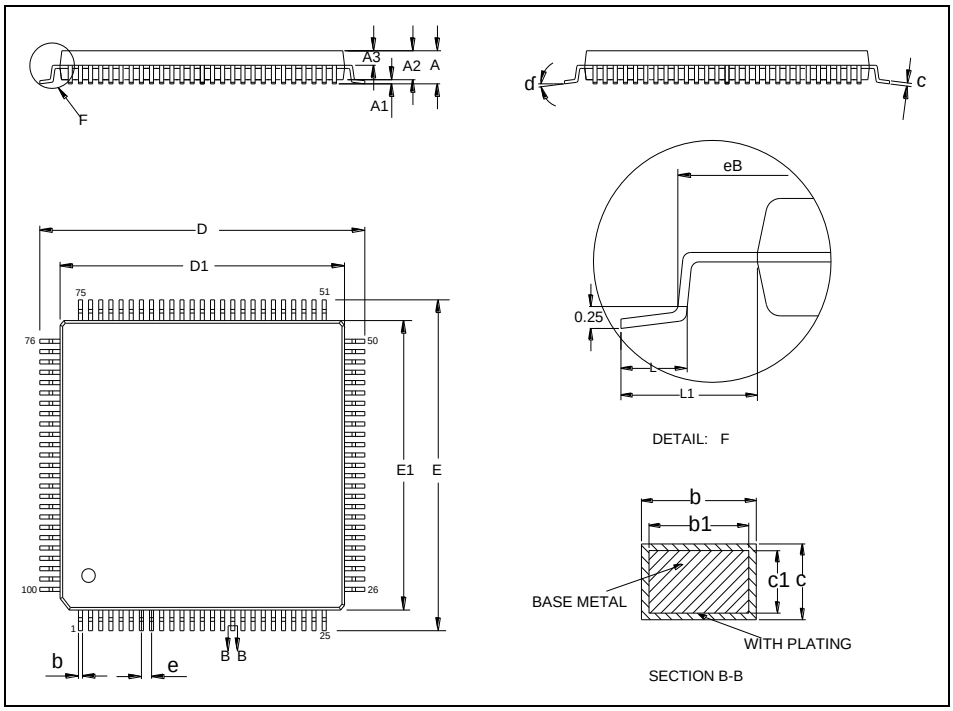
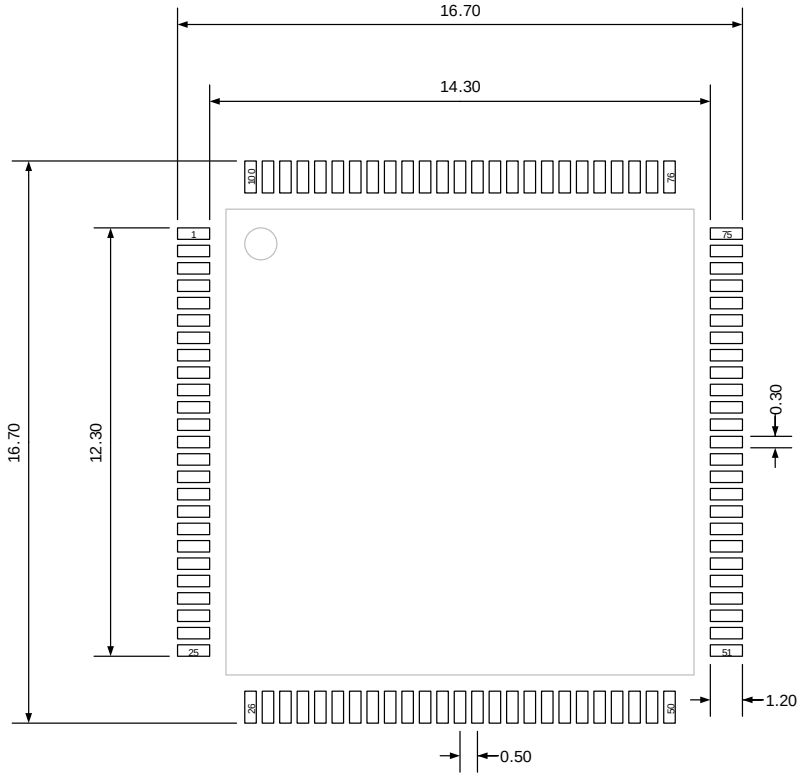


Table 5-4. LQFP100 package dimensions

Symbol	Min	Typ	Max
A	ð	ð	1.60
A1	0.05	ð	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	ð	0.26
b1	0.17	0.20	0.23
c	0.13	ð	0.17
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
e	ð	0.50	ð
eB	15.05	ð	15.35
L	0.45	ð	0.75
L1	ð	1.00	ð
ɗ	0 e	ð	7 e

(Original dimensions are in millimeters)

Figure 5-8. LQFP100 recommended footprint



(Original dimensions are in millimeters)

5.5 LQFP64 package outline dimensions

Figure 5-9. LQFP64 package outline

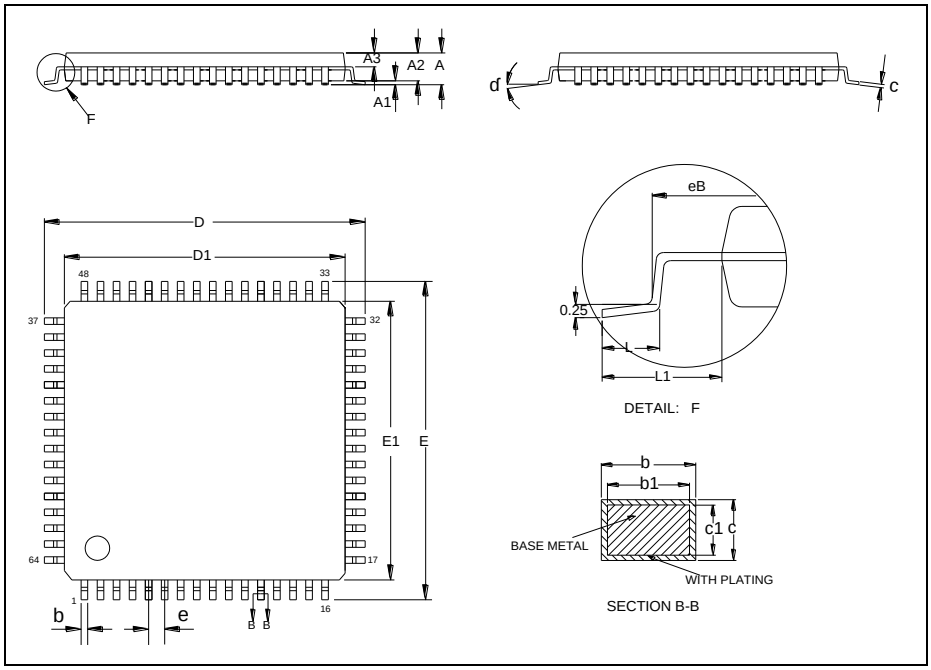
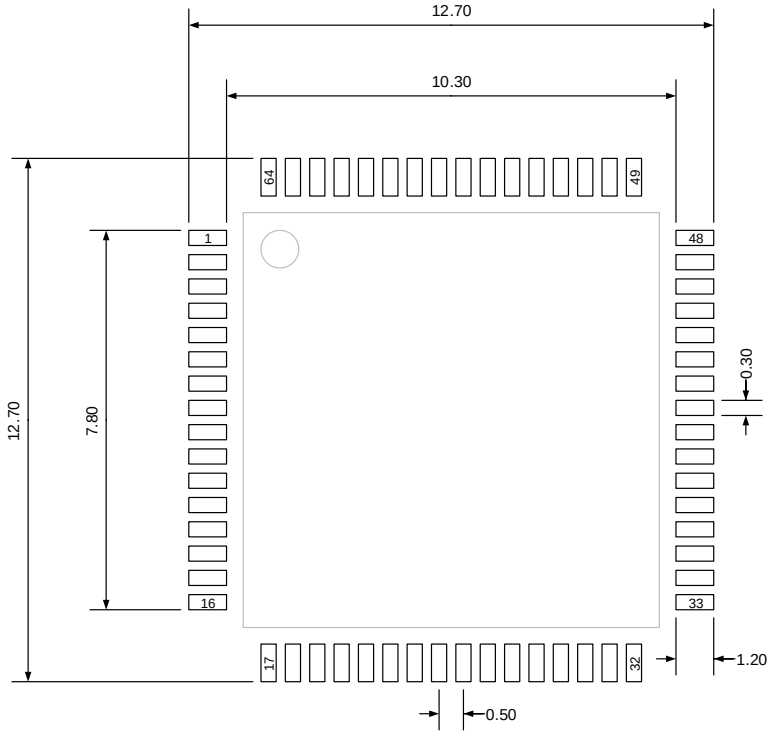


Table 5-5. LQFP64 package dimensions

Symbol	Min	Typ	Max
A	ð	ð	1.60
A1	0.05	ð	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	ð	0.26
b1	0.17	0.20	0.23
c	0.13	ð	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	ð	0.50	ð
eB	11.25	ð	11.45
L	0.45	ð	0.75
L1	ð	1.00	ð
ď	0 e	ð	7 e

(Original dimensions are in millimeters)

Figure 5-10. LQFP64 recommended footprint



(Original dimensions are in millimeters)

5.6 Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter ñdò For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

d_{JA}: Thermal resistance, junction-to-ambient.

d_{JB}: Thermal resistance, junction-to-board.

d_{JC}: Thermal resistance, junction-to-case.

ψ_{JB}: Thermal characterization parameter, junction-to-board.

ψ_{JT}: Thermal characterization parameter, junction-to-top center.

$$d_{JA}=(T_J-T_A)/P_D \quad (5\text{-}1)$$

$$d_{JB}=(T_J-T_B)/P_D \quad (5\text{-}2)$$

$$d_{JC}=(T_J-T_C)/P_D \quad (5\text{-}3)$$

Where, T_J = Junction temperature.

T_A = Ambient temperature

T_B = Board temperature

T_C = Case temperature which is monitoring on package surface

P_D = Total power dissipation

d_{JA} represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower d_{JA} can be considerate as better overall thermal performance. d_{JA} is generally used to estimate junction temperature.

d_{JB} is used to measure the heat flow resistance between the chip surface and the PCB board.

d_{JC} represents the thermal resistance between the chip surface and the package top case. d_{JC} is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

Table 5-6. Package thermal characteristics(1)

Symbol	Condition	Package	Value	Unit
d_{JA}	Natural convection, 2S2P PCB	BGA176	45.02	°C/W
		LQFP144	48.76	
		BGA100	78.32	
		LQFP100	57.42	
		LQFP64	51.81	
d_{JB}	Cold plate, 2S2P PCB	BGA176	26.55	°C/W
		LQFP144	35.00	

Symbol	Condition	Package	Value	Unit
		BGA100	55.27	
		LQFP100	31.68	
		LQFP64	33.36	
ψ_{JC}	Cold plate, 2S2P PCB	BGA176	9.93	°C/W
		LQFP144	12.03	
		BGA100	20.15	
		LQFP100	13.85	
		LQFP64	11.25	
Ψ_{JB}	Natural convection, 2S2P PCB	BGA176	28.31	°C/W
		LQFP144	35.32	
		BGA100	55.74	
		LQFP100	41.28	
		LQFP64	33.53	
Ψ_{JT}	Natural convection, 2S2P PCB	BGA176	0.69	°C/W
		LQFP144	1.86	
		BGA100	1.74	
		LQFP100	0.75	
		LQFP64	0.49	

(1) Thermal characteristics are based on simulation, and meet JEDEC specification.

6. Ordering information

Table 6-1. Part ordering code for GD32F407xx devices

Ordering code	Flash (KB)	Package	Package type	Temperature operating range
GD32F407IKH6	3072	BGA176	Green	Industrial -40ÁC to +85ÁC
GD32F407IGH6	1024	BGA176	Green	Industrial -40ÁC to +85ÁC
GD32F407IEH6	512	BGA176	Green	Industrial -40ÁC to +85ÁC
GD32F407ZKT6	3072	LQFP144	Green	Industrial -40ÁC to +85ÁC
GD32F407ZGT6	1024	LQFP144	Green	Industrial -40ÁC to +85ÁC
GD32F407ZET6	512	LQFP144	Green	Industrial -40ÁC to +85ÁC
GD32F407VKH6	3072	BGA100	Green	Industrial -40ÁC to +85ÁC
GD32F407VGH6	1024	BGA100	Green	Industrial -40ÁC to +85ÁC
GD32F407VEH6	512	BGA100	Green	Industrial -40ÁC to +85ÁC
GD32F407VKT6	3072	LQFP100	Green	Industrial -40ÁC to +85ÁC
GD32F407VGT6	1024	LQFP100	Green	Industrial -40ÁC to +85ÁC
GD32F407VET6	512	LQFP100	Green	Industrial -40ÁC to +85ÁC
GD32F407RKT6	3072	LQFP64	Green	Industrial -40ÁC to +85ÁC
GD32F407RGT6	1024	LQFP64	Green	Industrial -40ÁC to +85ÁC
GD32F407RET6	512	LQFP64	Green	Industrial -40ÁC to +85ÁC

7. Revision history

Table 7-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Oct.25, 2016
1.1	Repair history accumulation error	Jan.24, 2018
2.0	Repair history accumulation error and electrical characteristics updated	May.19, 2020
2.1	1. Update BGA176 / BGA100 parameter A max in 7DEOH %*$ SDFNDJH GLP / HTQDVE %*$ SDFNDJH GLP, the value RQ V changes from 0.84mm to 0.89mm. 2. Delete duplicate PG3 pin description in 7DEOH *') ,[%*$ SLQ GHILQLWLRQ 3. Update Memory characteristics in 7DEOH)ODVK PHPRU\ FKDUDFWHULVW 4. Modify the DCMI to DCI in chapter 'LJLWDO PH LQWHUIDFH'&, 5. Modify LDO in run mode to LDO in normal power and normal driver mode, LDO in low power mode to LDO in normal power and low driver mode, Main LDO in under drive mode to LDO in low power and normal drive mode, Low Power LDO in under driver mode to LDO in low power and low drive mode in 7DEOH 3RZHU FRQVXPS FKDUDFWHULVWLFV 6. Modify the second DAC_OUT min to DAC_OUT max in 7DEOH 7HPSHUDWXUH VH FKDUDFWHULVWLFV 7. Changed the range of T_{STG} from -55-+150°C to -65-150°C in 7DEOH $EVROXWH PD[L UDWLQJV 8. Delete Fast mode Plus and add parameter $t_{s(STA)}$, $t_{s(STO)}$ and t_{buff}, update I2C Timing diagram in ,QW LQWHJUDWHG&LUFXLW&KD 9. Update the SPI Timing diagram in chapter 6HULS SHULSKHUDO6,QWHUIDFH	May.31, 2021
2.2	1. Add information of GD32F407VET6, GD32F407VEH6 and GD32F407ZET6 in 7DEOH 3DUW RUGHULQJ FRGH IRU GHYLFHV	Sep.13, 2021
2.3	1. Correct the value of VREF+ in 7DEOH $'&	Oct.18, 2021

	FKDUDFWHULVWLFV.	
2.4	1. In note(3) of 7DEOH $EVROXWH PD[LUDWLQJV, VDD 6.5V is modified to 5.5V. 2. Modify 7DEOH 3RZHU FRQVXPSWLRQ FKDUDFWHULVWLFV, FLJXUH &E WLPLQJ GLDJUDP 63, WLPLQJ PDVWHU, PLJXUH 63, WLPLQJ VODYH and 7DEOH 6 FKDUDFWHULVWLFV. 3. Modify applicable standards for V_{ESD} (HBM) and V_{ESD} (CDM) in 7DEOH (6' FKDUDFWHULVWLFV 4. Modify the frequency range of IRC32K, delete the min and max value in 7DEOH /RZ VSHH LQWHUQDO FORFN ,5&. FKD 5. Modify the 7DEOH 1567 SLQ FKDUD 6. Modify the note for 7DEOH , 2 SRUW $& FKDUDFWHULVWLFV 7. Add)LJXUH 5HFRPPHQGHG 3SLQ2 FLUFXLW 8. Add description of EMI and 7DEOH (0, FKDUDFWHULVWLFV 9. Modify)LJXUH %*$ UHFRPPHQGH IRRWSULQW and)LJXUH /4)3 UHFRPPHQGHG IRRWSULQW.	Apr. 18, 2022

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