

**GigaDevice Semiconductor Inc.**

**GD32FFPRTGU6**

**ARM<sup>®</sup> Cortex<sup>®</sup>-M4 32-bit MCU**

Datasheet

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## 1 General description

The GD32FFPRTGU6 device belongs to the specific line of GD32 MCU Family. It is a new 32-bit general-purpose microcontroller based on the ARM® Cortex®-M4 RISC core with best cost-performance ratio in terms of enhanced processing capacity, reduced power consumption and peripheral set. The Cortex®-M4 core features implements a full set of DSP instructions to address digital signal control markets that demand an efficient, easy-to-use blend of control and signal processing capabilities. Its single precision FPU (floating point unit) speeds up software development. It also provides a Memory Protection Unit (MPU) and powerful trace technology for enhanced application security and advanced debug support.

The GD32FFPRTGU6 device incorporates the ARM® Cortex®-M4 32-bit processor core operating at 168 MHz frequency with Flash accesses zero wait states to obtain maximum efficiency. It provides up to 1024 KB on-chip Flash memory and 128 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The device offer four general-purpose 16-bit timers, a 16-bit advanced-control timer, two 12-bit 2.6M SPS ADCs, as well as standard and advanced communication interfaces: two USARTs, two SPIs, an I2C and an USB 2.0 FS.

The device operates from a 2.6 to 3.6 V power supply and available in –40 to +85 °C temperature range. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features make GD32FFPRTGU6 device specifically suitable for advanced fingerprint recognition application.



## 2 Device overview

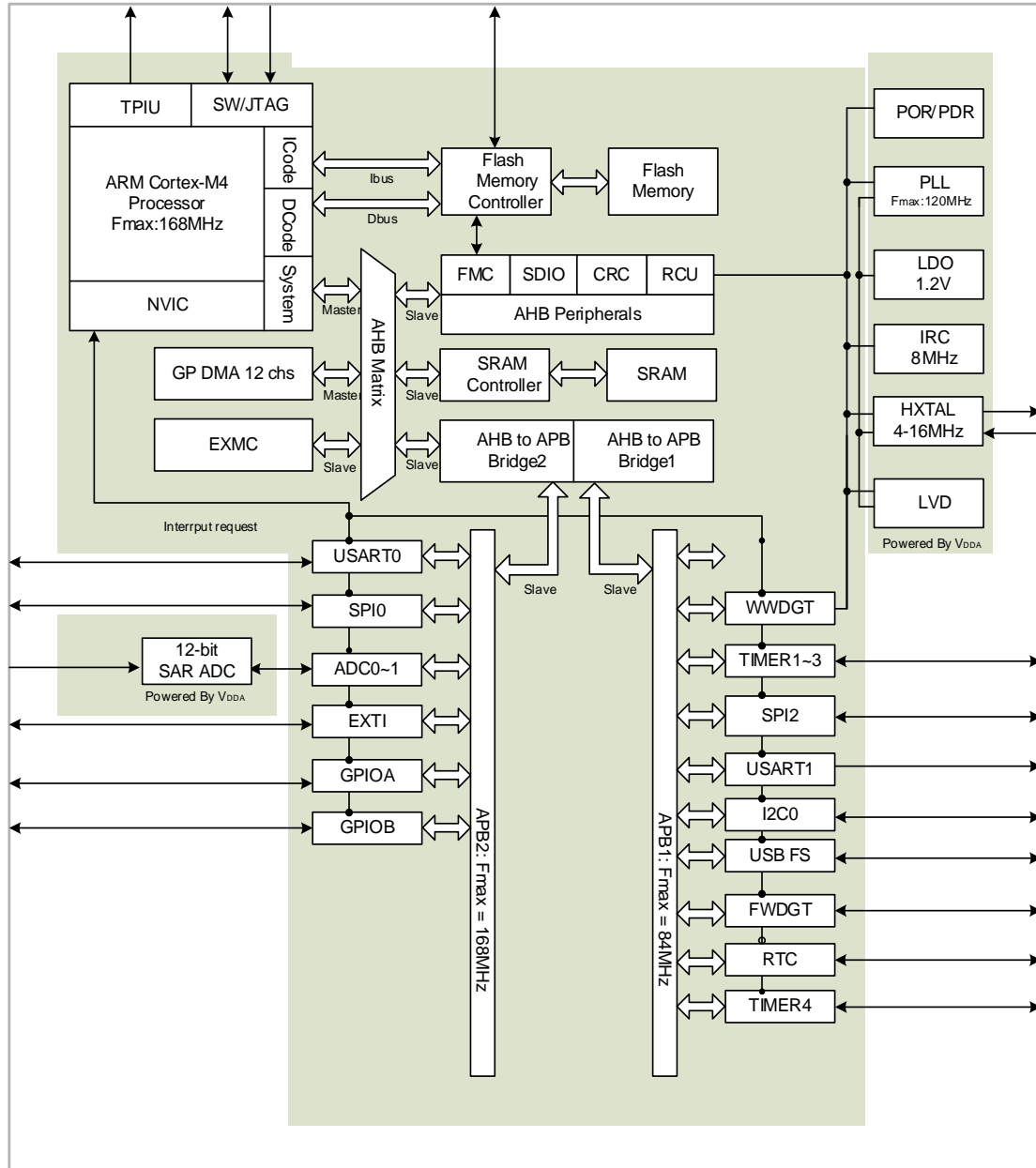
### 2.1 Device information

**Table 1. GD32FFPRTGU6 device features and peripheral list**

| Part Number    |                | GD32FFPRTGU6 |
|----------------|----------------|--------------|
| Flash          | Code Area (KB) | 256          |
|                | Data Area (KB) | 768          |
|                | Total (KB)     | 1024         |
| SRAM (KB)      |                | 128          |
| Timers         | 16-bit GPTM    | 4            |
|                | Adv. 16-bit TM | 1            |
|                | SysTick        | 1            |
|                | Watchdog       | 2            |
|                | RTC            | 1            |
| Connectivity   | USART          | 2            |
|                | I2C            | 1            |
|                | SPI            | 2            |
|                | USB 2.0 FS     | 1            |
| GPIO           |                | 26           |
| EXMC           |                | 0            |
| EXTI           |                | 16           |
| ADC Unit (CHs) |                | 2(10)        |
| Package        |                | QFN36        |

## 2.2 Block diagram

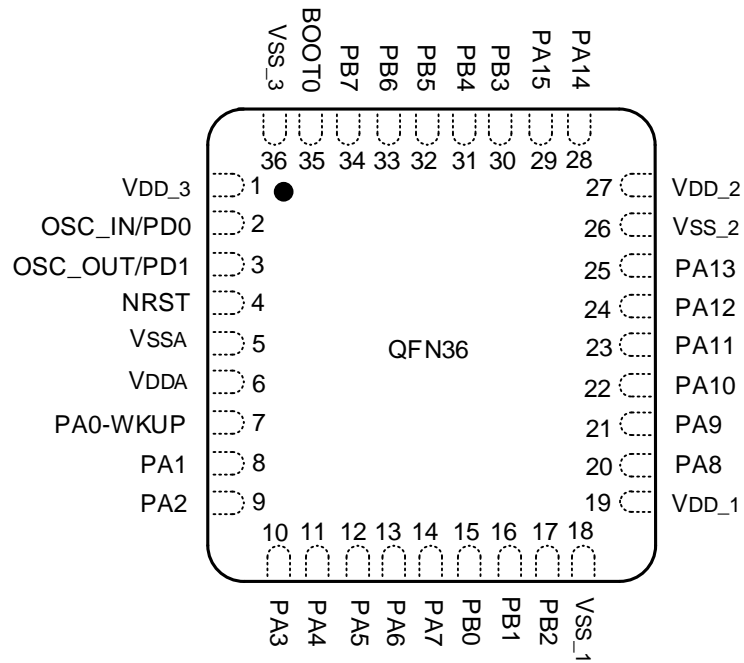
Figure 1. GD32FFPRTGU6 block diagram





## 2.3 Pinouts and pin assignment

Figure 2. GD32FFPRTGU6 QFN36 pinouts



## 2.4 Memory map

Figure 3. GD32FFPRTGU6 memory map

| Pre-defined Regions | Bus  | Address                   | Peripherals |
|---------------------|------|---------------------------|-------------|
| External device     | AHB3 | 0xA000 0000 - 0xA000 0FFF | Reserved    |
| External RAM        |      | 0x9000 0000 - 0x9FFF FFFF | Reserved    |
|                     |      | 0x7000 0000 - 0x8FFF FFFF | Reserved    |
|                     |      | 0x6000 0000 - 0x6FFF FFFF | Reserved    |
| Peripheral          | AHB1 | 0x5000 0000 - 0x5003 FFFF | Reserved    |
|                     |      | 0x4008 0000 - 0x4FFF FFFF | Reserved    |
|                     |      | 0x4004 0000 - 0x4007 FFFF | Reserved    |
|                     |      | 0x4002 BC00 - 0x4003 FFFF | Reserved    |
|                     |      | 0x4002 B000 - 0x4002 BBFF | Reserved    |
|                     |      | 0x4002 A000 - 0x4002 AFFF | Reserved    |
|                     |      | 0x4002 8000 - 0x4002 9FFF | Reserved    |
|                     |      | 0x4002 6800 - 0x4002 7FFF | Reserved    |
|                     |      | 0x4002 6400 - 0x4002 67FF | Reserved    |
|                     |      | 0x4002 6000 - 0x4002 63FF | Reserved    |
|                     |      | 0x4002 5000 - 0x4002 5FFF | Reserved    |
|                     |      | 0x4002 4000 - 0x4002 4FFF | Reserved    |
|                     |      | 0x4002 3C00 - 0x4002 3FFF | Reserved    |
|                     |      | 0x4002 3800 - 0x4002 3BFF | Reserved    |
|                     |      | 0x4002 3400 - 0x4002 37FF | Reserved    |
|                     |      | 0x4002 3000 - 0x4002 33FF | CRC         |
|                     |      | 0x4002 2C00 - 0x4002 2FFF | Reserved    |
|                     |      | 0x4002 2800 - 0x4002 2BFF | Reserved    |
|                     |      | 0x4002 2400 - 0x4002 27FF | Reserved    |
|                     |      | 0x4002 2000 - 0x4002 23FF | FMC         |
|                     |      | 0x4002 1C00 - 0x4002 1FFF | Reserved    |
|                     |      | 0x4002 1800 - 0x4002 1BFF | Reserved    |
|                     |      | 0x4002 1400 - 0x4002 17FF | Reserved    |
|                     |      | 0x4002 1000 - 0x4002 13FF | RCU         |
|                     |      | 0x4002 0C00 - 0x4002 0FFF | Reserved    |
|                     |      | 0x4002 0800 - 0x4002 0BFF | Reserved    |
|                     |      | 0x4002 0400 - 0x4002 07FF | DMA1        |
|                     |      | 0x4002 0000 - 0x4002 03FF | DMA0        |
|                     |      | 0x4001 8400 - 0x4001 FFFF | Reserved    |
|                     |      | 0x4001 8000 - 0x4001 83FF | Reserved    |

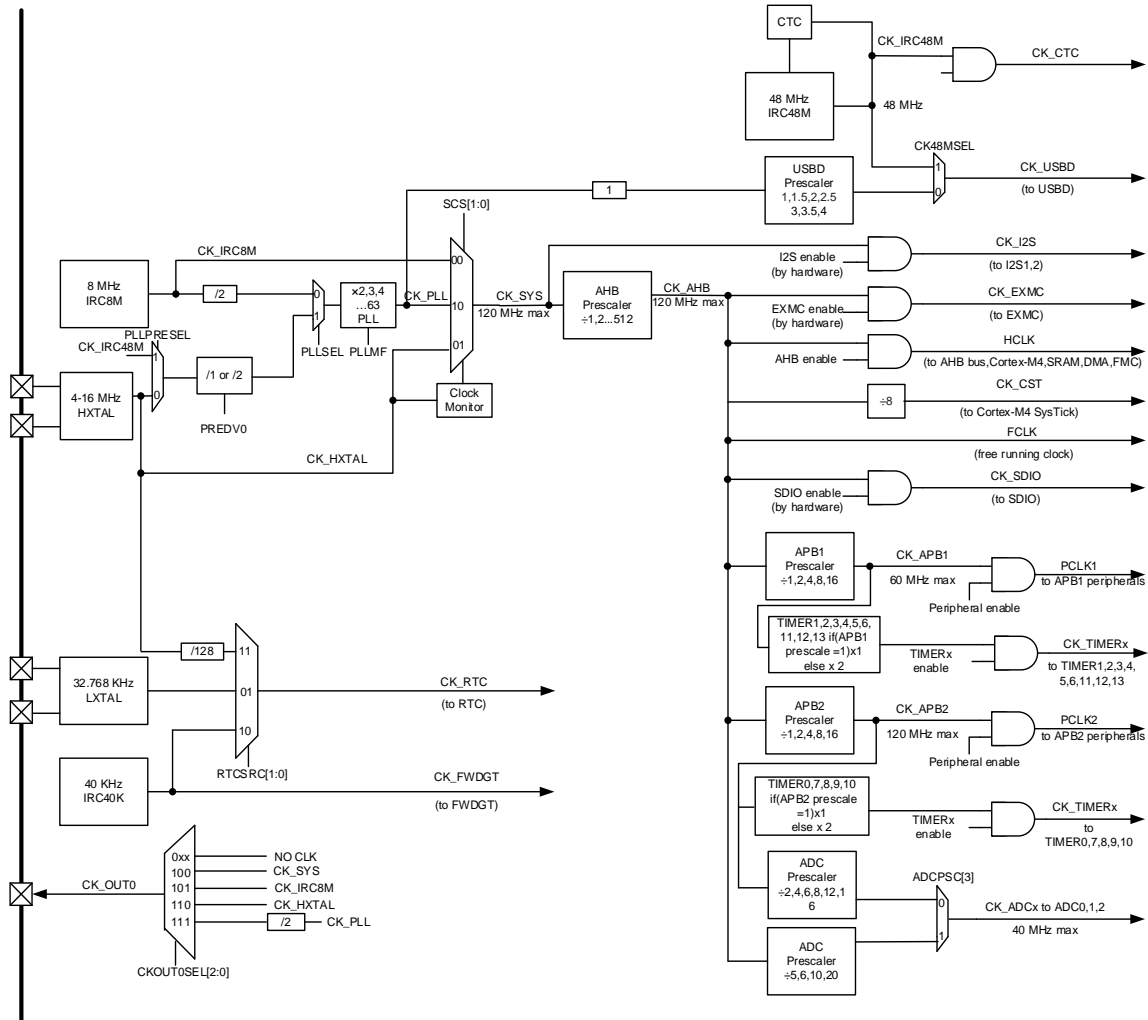
| Pre-defined Regions | Bus  | Address                   | Peripherals |
|---------------------|------|---------------------------|-------------|
|                     | APB2 | 0x4001 7C00 - 0x4001 7FFF | Reserved    |
|                     |      | 0x4001 7800 - 0x4001 7BFF | Reserved    |
|                     |      | 0x4001 7400 - 0x4001 77FF | Reserved    |
|                     |      | 0x4001 7000 - 0x4001 73FF | Reserved    |
|                     |      | 0x4001 6C00 - 0x4001 6FFF | Reserved    |
|                     |      | 0x4001 6800 - 0x4001 6BFF | Reserved    |
|                     |      | 0x4001 5C00 - 0x4001 67FF | Reserved    |
|                     |      | 0x4001 5800 - 0x4001 5BFF | Reserved    |
|                     |      | 0x4001 5400 - 0x4001 57FF | Reserved    |
|                     |      | 0x4001 5000 - 0x4001 53FF | Reserved    |
|                     |      | 0x4001 4C00 - 0x4001 4FFF | Reserved    |
|                     |      | 0x4001 4800 - 0x4001 4BFF | Reserved    |
|                     |      | 0x4001 4400 - 0x4001 47FF | Reserved    |
|                     |      | 0x4001 4000 - 0x4001 43FF | Reserved    |
|                     |      | 0x4001 3C00 - 0x4001 3FFF | Reserved    |
|                     |      | 0x4001 3800 - 0x4001 3BFF | USART0      |
|                     |      | 0x4001 3400 - 0x4001 37FF | Reserved    |
|                     |      | 0x4001 3000 - 0x4001 33FF | SPI0        |
|                     |      | 0x4001 2C00 - 0x4001 2FFF | Reserved    |
|                     |      | 0x4001 2800 - 0x4001 2BFF | ADC1        |
|                     |      | 0x4001 2400 - 0x4001 27FF | ADC0        |
|                     |      | 0x4001 2000 - 0x4001 23FF | Reserved    |
|                     |      | 0x4001 1C00 - 0x4001 1FFF | Reserved    |
|                     |      | 0x4001 1800 - 0x4001 1BFF | Reserved    |
|                     |      | 0x4001 1400 - 0x4001 17FF | Reserved    |
|                     |      | 0x4001 1000 - 0x4001 13FF | Reserved    |
|                     |      | 0x4001 0C00 - 0x4001 0FFF | GPIOB       |
|                     |      | 0x4001 0800 - 0x4001 0BFF | GPIOA       |
|                     |      | 0x4001 0400 - 0x4001 07FF | EXTI        |
|                     |      | 0x4001 0000 - 0x4001 03FF | AFIO        |
|                     | APB1 | 0x4000 CC00 - 0x4000 FFFF | Reserved    |
|                     |      | 0x4000 C800 - 0x4000 CBFF | Reserved    |
|                     |      | 0x4000 C400 - 0x4000 C7FF | Reserved    |
|                     |      | 0x4000 C000 - 0x4000 C3FF | Reserved    |
|                     |      | 0x4000 8000 - 0x4000 BFFF | Reserved    |
|                     |      | 0x4000 7C00 - 0x4000 7FFF | Reserved    |
|                     |      | 0x4000 7800 - 0x4000 7BFF | Reserved    |
|                     |      | 0x4000 7400 - 0x4000 77FF | Reserved    |
|                     |      | 0x4000 7000 - 0x4000 73FF | PMU         |
|                     |      | 0x4000 6C00 - 0x4000 6FFF | BKP         |

| Pre-defined Regions       | Bus      | Address                   | Peripherals          |
|---------------------------|----------|---------------------------|----------------------|
|                           |          | 0x4000 6800 - 0x4000 6BFF | Reserved             |
|                           |          | 0x4000 6400 - 0x4000 67FF | Reserved             |
|                           |          | 0x4000 6000 - 0x4000 63FF | USBDM SRAM 512 bytes |
|                           |          | 0x4000 5C00 - 0x4000 5FFF | USBDM                |
|                           |          | 0x4000 5800 - 0x4000 5BFF | Reserved             |
|                           |          | 0x4000 5400 - 0x4000 57FF | I2C0                 |
|                           |          | 0x4000 5000 - 0x4000 53FF | Reserved             |
|                           |          | 0x4000 4C00 - 0x4000 4FFF | Reserved             |
|                           |          | 0x4000 4800 - 0x4000 4BFF | Reserved             |
|                           |          | 0x4000 4400 - 0x4000 47FF | USART1               |
|                           |          | 0x4000 4000 - 0x4000 43FF | Reserved             |
|                           |          | 0x4000 3C00 - 0x4000 3FFF | SPI2                 |
|                           |          | 0x4000 3800 - 0x4000 3BFF | Reserved             |
|                           |          | 0x4000 3400 - 0x4000 37FF | Reserved             |
|                           |          | 0x4000 3000 - 0x4000 33FF | FWDGT                |
|                           |          | 0x4000 2C00 - 0x4000 2FFF | WWDGT                |
|                           |          | 0x4000 2800 - 0x4000 2BFF | RTC                  |
|                           |          | 0x4000 2400 - 0x4000 27FF | Reserved             |
|                           |          | 0x4000 2000 - 0x4000 23FF | Reserved             |
|                           |          | 0x4000 1C00 - 0x4000 1FFF | Reserved             |
|                           |          | 0x4000 1800 - 0x4000 1BFF | Reserved             |
|                           |          | 0x4000 1400 - 0x4000 17FF | Reserved             |
|                           |          | 0x4000 1000 - 0x4000 13FF | Reserved             |
|                           |          | 0x4000 0C00 - 0x4000 0FFF | TIMER4               |
|                           |          | 0x4000 0800 - 0x4000 0BFF | TIMER3               |
|                           |          | 0x4000 0400 - 0x4000 07FF | TIMER2               |
|                           |          | 0x4000 0000 - 0x4000 03FF | TIMER1               |
|                           |          | SRAM                      | AHB                  |
| 0x2006 0000 - 0x2006 FFFF | Reserved |                           |                      |
| 0x2003 0000 - 0x2005 FFFF | Reserved |                           |                      |
| 0x2002 0000 - 0x2002 FFFF | Reserved |                           |                      |
| 0x2001 C000 - 0x2001 FFFF | Reserved |                           |                      |
| 0x2001 8000 - 0x2001 BFFF | SRAM     |                           |                      |
| 0x2000 5000 - 0x2001 7FFF |          |                           |                      |
| 0x2000 0000 - 0x2000 4FFF |          |                           |                      |
| Code                      | AHB      | 0x1FFF F810 - 0x1FFF FFFF | Reserved             |
|                           |          | 0x1FFF F800 - 0x1FFF F80F | Option Bytes         |
|                           |          | 0x1FFF F000 - 0x1FFF F7FF | Boot loader          |
|                           |          | 0x1FFF C010 - 0x1FFF EFFF |                      |
|                           |          | 0x1FFF C000 - 0x1FFF C00F |                      |

| Pre-defined Regions | Bus | Address                   | Peripherals                          |
|---------------------|-----|---------------------------|--------------------------------------|
|                     |     | 0x1FFF B000 - 0x1FFF BFFF |                                      |
|                     |     | 0x1FFF 7A10 - 0x1FFF AFFF | Reserved                             |
|                     |     | 0x1FFF 7800 - 0x1FFF 7A0F | Reserved                             |
|                     |     | 0x1FFF 0000 - 0x1FFF 77FF | Reserved                             |
|                     |     | 0x1FFE C010 - 0x1FFE FFFF | Reserved                             |
|                     |     | 0x1FFE C000 - 0x1FFE C00F | Reserved                             |
|                     |     | 0x1001 0000 - 0x1FFE BFFF | Reserved                             |
|                     |     | 0x1000 0000 - 0x1000 FFFF | Reserved                             |
|                     |     | 0x083C 0000 - 0x0FFF FFFF | Reserved                             |
|                     |     | 0x0830 0000 - 0x083B FFFF | Reserved                             |
|                     |     | 0x0810 0000 - 0x082F FFFF | Main Flash                           |
|                     |     | 0x0802 0000 - 0x080F FFFF |                                      |
|                     |     | 0x0800 0000 - 0x0801 FFFF |                                      |
|                     |     | 0x0030 0000 - 0x07FF FFFF | Reserved                             |
|                     |     | 0x0010 0000 - 0x002F FFFF | Aliased to Main Flash or Boot loader |
|                     |     | 0x0002 0000 - 0x000F FFFF |                                      |
|                     |     | 0x0000 0000 - 0x0001 FFFF |                                      |

## 2.5 Clock tree

Figure 4. GD32FFPRTGU6 clock tree



**Legend:**

- HXTAL:** High speed crystal oscillator
- LXTAL:** Low speed crystal oscillator
- IRC8M:** Internal 8M RC oscillators
- IRC48M:** Internal 48M RC oscillators
- IRC32K:** Internal 32K RC oscillator

## 2.6 Pin definitions

**Table 2. GD32FFPRTGU6 pin definitions**

| Pin Name          | Pins | Pin Type <sup>(1)</sup> | I/O <sup>(2)</sup> Level | Functions description   |
|-------------------|------|-------------------------|--------------------------|---|
| OSC_IN            | 2    | I                       |                          | Default: OSC_IN   |
| OSC_OUT           | 3    | O                       |                          | Default: OSC_OUT  |
| NRST              | 4    | I/O                     |                          | Default: NRST   |
| V <sub>SSA</sub>  | 5    | P                       |                          | Default: V <sub>SSA</sub>   |
| V <sub>DDA</sub>  | 6    | P                       |                          | Default: V <sub>DDA</sub>   |
| PA0-WKUP          | 7    | I/O                     |                          | Default: PA0<br>Alternate: WKUP, USART1_CTS, ADC012_IN0, TIMER1_CH0_ETI, TIMER4_CH0     |
| PA1               | 8    | I/O                     |                          | Default: PA1<br>Alternate: USART1_RTS, ADC012_IN1, TIMER1_CH1, TIMER4_CH1               |
| PA2               | 9    | I/O                     |                          | Default: PA2<br>Alternate: USART1_TX, ADC012_IN2, TIMER1_CH2, TIMER4_CH2, SPI0_IO2      |
| PA3               | 10   | I/O                     |                          | Default: PA3<br>Alternate: USART1_RX, ADC012_IN3, TIMER1_CH3, TIMER4_CH3, SPI0_IO3      |
| PA4               | 11   | I/O                     |                          | Default: PA4<br>Alternate: SPI0_NSS, USART1_CK, ADC01_IN4<br>Remap: SPI2_NSS            |
| PA5               | 12   | I/O                     |                          | Default: PA5<br>Alternate: SPI0_SCK, ADC01_IN5  |
| PA6               | 13   | I/O                     |                          | Default: PA6<br>Alternate: SPI0_MISO, ADC01_IN6, TIMER2_CH0<br>Remap: TIMER0_BKIN       |
| PA7               | 14   | I/O                     |                          | Default: PA7<br>Alternate: SPI0_MOSI, ADC01_IN7, TIMER2_CH1<br>Remap: TIMER0_CH0_ON     |
| PB0               | 15   | I/O                     |                          | Default: PB0<br>Alternate: ADC01_IN8, TIMER2_CH2<br>Remap: TIMER0_CH1_ON                |
| PB1               | 16   | I/O                     |                          | Default: PB1<br>Alternate: ADC01_IN9, TIMER2_CH3<br>Remap: TIMER0_CH2_ON                |
| PB2               | 17   | I/O                     | 5VT                      | Default: PB2, BOOT1   |
| V <sub>SS_1</sub> | 18   | P                       |                          | Default: V <sub>SS_1</sub>  |
| V <sub>DD_1</sub> | 19   | P                       |                          | Default: V <sub>DD_1</sub>  |
| PA8               | 20   | I/O                     | 5VT                      | Default: PA8<br>Alternate: USART0_CK, TIMER0_CH0, CK_OUT0, V <sub>CORE</sub> , CTC_SYNC |
| PA9               | 21   | I/O                     | 5VT                      | Default: PA9<br>Alternate: USART0_TX, TIMER0_CH1  |

| Pin Name          | Pins | Pin Type <sup>(1)</sup> | I/O <sup>(2)</sup> Level | Functions description  |
|-------------------|------|-------------------------|--------------------------|--|
| PA10              | 22   | I/O                     | 5VT                      | Default: PA10<br>Alternate: USART0_RX, TIMER0_CH2  |
| PA11              | 23   | I/O                     | 5VT                      | Default: PA11<br>Alternate: USART0_CTS, USBDM, TIMER0_CH3                                |
| PA12              | 24   | I/O                     | 5VT                      | Default: PA12<br>Alternate: USART0_RTS, TIMER0_ETI, USBDP                                |
| PA13              | 25   | I/O                     | 5VT                      | Default: JTMS, SWDIO<br>Remap: PA13  |
| V <sub>SS_2</sub> | 26   | P                       |                          | Default: V <sub>SS_2</sub>   |
| V <sub>DD_2</sub> | 27   | P                       |                          | Default: V <sub>DD_2</sub>   |
| PA14              | 28   | I/O                     | 5VT                      | Default: JTCK, SWCLK<br>Remap: PA14  |
| PA15              | 29   | I/O                     | 5VT                      | Default: JTDI<br>Alternate: SPI2_NSS<br>Remap: TIMER1_CH0_ETI, PA15, SPI0_NSS            |
| PB3               | 30   | I/O                     | 5VT                      | Default: JTDO<br>Alternate: SPI2_SCK<br>Remap: PB3, TRACESWO, TIMER1_CH1, SPI0_SCK       |
| PB4               | 31   | I/O                     | 5VT                      | Default: NJTRST<br>Alternate: SPI2_MISO<br>Remap: TIMER2_CH0, PB4, SPI0_MISO             |
| PB5               | 32   | I/O                     |                          | Default: PB5<br>Alternate: I2C0_SMBA, SPI2_MOSI, I2S2_SD<br>Remap: TIMER2_CH1, SPI0_MOSI |
| PB6               | 33   | I/O                     | 5VT                      | Default: PB6<br>Alternate: I2C0_SCL, TIMER3_CH0<br>Remap: USART0_TX, SPI0_IO2            |
| PB7               | 34   | I/O                     | 5VT                      | Default: PB7<br>Alternate: I2C0_SDA, TIMER3_CH1<br>Remap: USART0_RX, SPI0_IO3            |
| BOOT0             | 35   | I                       |                          | Default: BOOT0   |
| V <sub>SS_3</sub> | 36   | P                       |                          | Default: V <sub>SS_3</sub>   |
| V <sub>DD_3</sub> | 1    | P                       |                          | Default: V <sub>DD_3</sub>   |

**Notes:**

1. Type: I = input, O = output, P = power.
2. I/O Level: 5VT = 5 V tolerant.



## 3 Functional description

### 3.1 ARM® Cortex®-M4 core

The ARM® Cortex®-M4 processor is a high performance embedded processor with DSP instructions which allow efficient signal processing and complex algorithm execution. It brings an efficient, easy-to-use blend of control and signal processing capabilities to meet the digital signal control markets demand. The processor is highly configurable enabling a wide range of implementations from those requiring memory protection and powerful trace technology to cost sensitive device requiring minimal area, while delivering outstanding computational performance and an advanced system response to interrupts.

32-bit ARM® Cortex®-M4 processor core

- Up to 168 MHz operation frequency
- Single-cycle multiplication and hardware divider
- Floating Point Unit (FPU)
- Integrated DSP instructions
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M4 processor is based on the ARMv7-M architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex®-M4:

- Internal Bus Matrix connected with ICode bus, DCode bus, system bus, Private Peripheral Bus (PPB) and debug accesses (AHB-AP)
- Nested Vectored Interrupt Controller (NVIC)
- Flash Patch and Breakpoint (FPB)
- Data Watchpoint and Trace (DWT)
- Instrument Trace Macrocell (ITM)
- Memory Protection Unit (MPU)
- Serial Wire JTAG Debug Port (SWJ-DP)
- Trace Port Interface Unit (TPIU)

## 3.2 On-chip memory

- Up to 1024 Kbytes of Flash memory, including code Flash and data Flash
- Up to 128 KB of SRAM

The ARM® Cortex®-M4 processor is structured in Harvard architecture which can use separate buses to fetch instructions and load/store data. 1024 Kbytes of inner Flash at most, which includes code Flash that available for storing programs and data, and accessed (R/W) at CPU clock speed with zero wait states. An extra data Flash is also included for storing data mainly. The Figure of GD32FFPRTGU6 memory map shows the memory of the GD32FFPRTGU6 series of device, including Flash, SRAM, peripheral, and other pre-defined regions.

## 3.3 Clock, reset and supply management

- Internal 8 MHz factory-trimmed RC and external 4 to 32 MHz crystal oscillator
- Internal 48 MHz RC oscillator
- Internal 32 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator
- 2.6 to 3.6 V application supply and I/Os
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD)

The Clock Control Unit (CCU) provides a range of oscillator and clock functions. These include internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AHB and two APB domains. The maximum frequency of the two AHB domains are 120 MHz. The maximum frequency of the two APB domains including APB1 is 60 MHz and APB2 is 120 MHz. See Figure 6 for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: system reset resets the processor core and peripheral IP components. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from/down to 2.6 V. The device remains in reset mode when  $V_{DD}$  is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- $V_{DD}$  range: 2.6 to 3.6 V, external power supply for I/Os and the internal regulator. Provided externally through  $V_{DD}$  pins.
- $V_{SSA}$ ,  $V_{DDA}$  range: 2.6 to 3.6 V, external analog power supplies for ADC, reset blocks, RCs and PLL.  $V_{DDA}$  and  $V_{SSA}$  must be connected to  $V_{DD}$  and  $V_{SS}$ , respectively.
- $V_{BAT}$  range: 1.8 to 3.6 V, power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when  $V_{DD}$  is not present.

## 3.4 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from main flash memory (default)
- Boot from system memory
- Boot from on-chip SRAM

The boot loader is located in the internal boot ROM memory (system memory). It is used to reprogram the Flash memory by using USART0, USART1 in device mode. It also can be used to transfer and update the Flash memory code, the data and the vector table sections. In default condition, boot from bank 1 of Flash memory is selected. It also supports to boot from bank 2 of Flash memory by setting a bit in option bytes.

## 3.5 Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are Sleep mode, Deep-sleep mode, and Standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Sleep mode**

In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt/event can wake up the system.

- **Deep-sleep mode**

In Deep-sleep mode, all clocks in the 1.2V domain are off, and all of the high speed crystal oscillator (IRC8M, HXTAL) and PLL are disabled. Only the contents of SRAM and registers are retained. Any interrupt or wakeup event from EXTI lines can wake up the system from the Deep-sleep mode including the 23 external lines, the RTC alarm, the LVD output, and USB wakeup. When exiting the Deep-sleep mode, the IRC8M is selected as the system clock.

- **Standby mode**

In Standby mode, the whole 1.2V domain is power off, the LDO is shut down, and all of IRC8M, HXTAL and PLL are disabled. The contents of SRAM and registers (except Backup Registers) are lost. There are four wakeup sources for the Standby mode, including the external reset from NRST pin, the RTC, the FWDG reset, and the rising edge on WKUP pin.

### 3.6 Analog to digital converter (ADC)

- 12-bit SAR ADC's conversion rate is up to 2.6MSPS
- 12-bit, 10-bit, 8-bit or 6-bit configurable resolution
- Hardware oversampling ratio adjustable from 2 to 256x improves resolution to 16-bit
- Input voltage range:  $V_{SSA}$  to  $V_{DDA}$  (2.6 to 3.6 V)
- Temperature sensor

Two 12-bit 2.6MSPS multi-channel ADCs are integrated in the device. It has a total of 12 multiplexed channels: 10 external channels, 1 channel for internal temperature sensor ( $V_{SENSE}$ ), 1 channel for internal reference voltage ( $V_{REFINT}$ ). The input voltage range is between 2.6 V and 3.6 V. An on-chip hardware oversampling scheme improves performance while off-loading the related computational burden from the CPU. An analog watchdog block can be used to detect the channels, which are required to remain within a specific threshold window. A configurable channel management block can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced use.

The ADC can be triggered from the events generated by the general-purpose level 0 timers (TMx) and the advanced-control timers (TM0) with internal connection. The temperature sensor can be used to generate a voltage that varies linearly with temperature. It is internally connected to the ADC\_IN16 input channel which is used to convert the sensor output voltage in a digital value.

### 3.7 DMA

- 7 channel DMA 0 controller and 5 channel DMA 1 controller
- Peripherals supported: Timers, ADC, SPIs, I<sup>2</sup>C, USARTs

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Four types of access method are supported: peripheral to peripheral, peripheral to memory, memory to peripheral, memory to memory

Each channel is connected to fixed hardware DMA requests. The priorities of DMA channel requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.

### 3.8 General-purpose inputs/outputs (GPIOs)

- Up to 26 fast GPIOs, all mappable on 16 external interrupt vectors (EXTI)
- Analog input/output configurable
- Alternate function input/output configurable

There are up to 26 general purpose I/O pins (GPIO) in GD32FFPRTGU6, named PA0 ~ PA15

and PB0 ~ PB7, to implement logic input/output functions. Each of the GPIO ports has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current capable except for analog inputs.

### 3.9 Timers and PWM generation

- A 16-bit advanced-control timer (TM0), four 16-bit general-purpose timers (TM1 ~ TM4)
- Up to 4 independent channels of PWM, output compare or input capture for each general-purpose timer (GPTM) and external trigger input
- 16-bit, motor control PWM advanced-control timer with programmable dead-time generation for output match
- Encoder interface controller with two inputs using quadrature decoder
- 24-bit SysTick timer down counter
- 2 watchdog timers (Free watchdog and window watchdog)

The advanced-control timer (TM0) can be used as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general-purpose timer. The 4 independent channels can be used for input capture, output compare, PWM generation (edge- or center-aligned counting modes) and single pulse mode output. If configured as a general-purpose 16-bit timer, it has the same functions as the TMx timer. It can be synchronized with external signals or to interconnect with other GPTMs together which have the same architecture and features.

The general-purpose timer (GPTM), can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TM1 ~ TM4 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. The GPTM also supports an encoder interface with two inputs using quadrature decoder.

The GD32FFPRTGU6 have two watchdog peripherals, Independent watchdog and window watchdog. They offer a combination of high safety level, flexibility of use and timing accuracy.

The independent watchdog timer includes a 12-bit down-counting counter and a 8-bit prescaler, It is clocked from an independent 40 kHz internal RC and as it operates independently of the main clock, it can operate in stop and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the

main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

### 3.10 Real time clock (RTC)

- 32-bit up-counter with a programmable 20-bit prescaler
- Alarm function
- Interrupt and wake-up event

The real time clock is an independent timer which provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and an expected interrupt. The RTC features a 32-bit programmable counter for long-term measurement using the compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz from external crystal oscillator.

### 3.11 Inter-integrated circuit (I2C)

- An I2C bus interfaces can support both master and slave mode with a frequency up to 1 MHz (Fast mode plus)
- Provide arbitration function, optional PEC (packet error checking) generation and checking
- Supports 7-bit and 10-bit addressing mode and general call addressing mode

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides several data transfer rates: 100 KHz of standard mode, 400 KHz of the fast mode and 1 MHz of the fast mode plus . The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

### 3.12 Serial peripheral interface (SPI)

- Two SPI interfaces with a frequency of up to 30 MHz
- Support both master and slave mode
- Hardware CRC calculation and transmit automatic CRC error checking

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). Both SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking.

### 3.13 Universal synchronous asynchronous receiver transmitter (USART)

- Two USARTs with operating frequency up to 10.5 MHz
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder support
- LIN break generation and detection
- USARTs support ISO 7816-3 compliant smart card interface

The USARTs (USART0, USART1) are used to translate data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART transmitter and receiver. The USART also supports DMA function for high speed data communication.

### 3.14 Universal serial bus full-speed (USB 2.0 FS)

- One full-speed USB Interface with frequency up to 12 Mbit/s
- Internal 48 MHz oscillator support crystal-less operation
- Internal main PLL for USB CLK compliantly

The Universal Serial Bus (USB) is a 4-wire bus with 4 bidirectional endpoints. The device controller enables 12 Mbit/s data exchange with integrated transceivers. Transaction formatting is performed by the hardware, including CRC generation and checking. It supports device modes. Transaction formatting is performed by the hardware, including CRC generation and checking. The status of a completed USB transfer or error condition is indicated by status registers. An interrupt is also generated if enabled. The required precise 48 MHz clock which can be generated from the internal main PLL (the clock source must use an HXTAL crystal oscillator) or by the internal 48 MHz oscillator in automatic trimming mode that allows crystal-less operation.

### 3.15 Debug mode

- Serial wire JTAG debug port (SWJ-DP)

The ARM® SWJ-DP Interface is embedded and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

### 3.16 Package and operation temperature

- QFN36
- Operation temperature range: -40°C to +85°C (industrial level)



## 4 Electrical characteristics

### 4.1 Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

**Table 3. Absolute maximum ratings**

| Symbol               | Parameter                                   | Min             | Max             | Unit |
|----------------------|---|-----------------|-----------------|------|
| $V_{DD}$             | External voltage range                      | $V_{SS} - 0.3$  | $V_{SS} + 3.6$  | V    |
| $V_{DDA}$            | External analog supply voltage              | $V_{SSA} - 0.3$ | $V_{SSA} + 3.6$ | V    |
| $V_{BAT}$            | External battery supply voltage             | $V_{SS} - 0.3$  | $V_{SS} + 3.6$  | V    |
| $V_{IN}$             | Input voltage on 5V tolerant pin            | $V_{SS} - 0.3$  | $V_{DD} + 4.0$  | V    |
|                      | Input voltage on other I/O                  | $V_{SS} - 0.3$  | 4.0             | V    |
| $ \Delta V_{DDx} $   | Variations between different VDD power pins | —               | 50              | mV   |
| $ V_{SSx} - V_{SS} $ | Variations between different ground pins    | —               | 50              | mV   |
| $I_{IO}$             | Maximum current for GPIO pins               | —               | 25              | mA   |
| $T_A$                | Operating temperature range                 | -40             | +85             | °C   |
| $T_{STG}$            | Storage temperature range                   | -55             | +150            | °C   |
| $T_J$                | Maximum junction temperature                | —               | 125             | °C   |

### 4.2 Recommended DC characteristics

**Table 4. DC operating conditions**

| Symbol    | Parameter              | Conditions       | Min | Typ | Max | Unit |
|-----------|------------------------|------------------|-----|-----|-----|------|
| $V_{DD}$  | Supply voltage         | —                | 2.6 | 3.3 | 3.6 | V    |
| $V_{DDA}$ | Analog supply voltage  | Same as $V_{DD}$ | 2.6 | 3.3 | 3.6 | V    |
| $V_{BAT}$ | Battery supply voltage | —                | 1.8 | —   | 3.6 | V    |

### 4.3 Power consumption

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications.

**Table 5. Power consumption characteristics**

| Symbol   | Parameter                        | Conditions  | Min  | Typ   | Max  | Unit |
|--|----------------------------------|---|--|-------|------|------|
| I <sub>DD</sub>  | Supply current (Run mode)        | V <sub>DD</sub> =V <sub>DDA</sub> =3.3V, HXTAL=25MHz, System clock=168MHz, All peripherals enabled                  | —  | 64.0  | —    | mA   |
|  |                                  | V <sub>DD</sub> =V <sub>DDA</sub> =3.3V, HXTAL =25MHz, System clock =168MHz, All peripherals disabled               | —  | 33.5  | —    | mA   |
|  |                                  | V <sub>DD</sub> =V <sub>DDA</sub> =3.3V, HXTAL =25MHz, System clock =108MHz, All peripherals enabled                | —  | 42.5  | —    | mA   |
|  |                                  | V <sub>DD</sub> =V <sub>DDA</sub> =3.3V, HXTAL =25MHz, System Clock =108MHz, All peripherals disabled               | —  | 22.5  | —    | mA   |
|  | Supply current (Sleep mode)      | V <sub>DD</sub> =V <sub>DDA</sub> =3.3V, HXTAL =25MHz, CPU clock off, System clock=168MHz, All peripherals enabled  | —  | 44.9  | —    | mA   |
|  |                                  | V <sub>DD</sub> =V <sub>DDA</sub> =3.3V, HXTAL =25MHz, CPU clock off, System clock=168MHz, All peripherals disabled | —  | 13.86 | —    | mA   |
|  | Supply current (Deep-Sleep mode) | V <sub>DD</sub> =V <sub>DDA</sub> =3.3V, Regulator in run mode, IRC32K on, RTC on, All GPIOs analog mode            | —  | 208   | —    | μA   |
|  |                                  | V <sub>DD</sub> =V <sub>DDA</sub> =3.3V, Regulator in low power mode, IRC32K on, RTC on, All GPIOs analog mode      | —  | 180   | —    | μA   |
|  | Supply current (Standby mode)    | V <sub>DD</sub> =V <sub>DDA</sub> =3.3V, LXTAL off, IRC32K on, RTC on   | —  | 5.10  | —    | μA   |
|  |                                  | V <sub>DD</sub> =V <sub>DDA</sub> =3.3V, LXTAL off, IRC32K on, RTC off  | —  | 4.90  | —    | μA   |
|  |                                  | V <sub>DD</sub> =V <sub>DDA</sub> =3.3V, LXTAL off, IRC32K off, RTC off   | —  | 4.30  | —    | μA   |
|  | I <sub>BAT</sub>                 | Battery supply current  | V <sub>DD</sub> not available, V <sub>BAT</sub> =3.6 V, LXTAL on with external crystal, RTC on, Higher driving | —     | 1.78 | —    |
| V <sub>DD</sub> not available, V <sub>BAT</sub> =3.3 V, LXTAL on with external crystal, RTC on, Higher driving |                                  |   | —  | 1.48  | —    | μA   |
| V <sub>DD</sub> not available, V <sub>BAT</sub> =2.6 V, LXTAL on with external crystal, RTC on, Higher driving |                                  |   | —  | 1.16  | —    | μA   |
| V <sub>DD</sub> not available, V <sub>BAT</sub> =3.6 V, LXTAL on with external crystal, RTC on, Lower driving  |                                  |   | —  | 1.11  | —    | μA   |

| Symbol | Parameter | Conditions  | Min | Typ  | Max | Unit |
|--------|-----------|---|-----|------|-----|------|
|        |           | V <sub>DD</sub> not available, V <sub>BAT</sub> =3.3 V, LXTAL on with external crystal, RTC on, Lower driving | —   | 0.83 | —   | μA   |
|        |           | V <sub>DD</sub> not available, V <sub>BAT</sub> =2.6 V, LXTAL on with external crystal, RTC on, Lower driving | —   | 0.51 | —   | μA   |

#### 4.4 EMC characteristics

EMS (electromagnetic susceptibility) includes ESD (Electrostatic discharge, positive and negative) and FTB (Burst of Fast Transient voltage, positive and negative) testing result is given in the following table, based on the EMS levels and classes compliant with IEC 61000 series standard.

**Table 6. EMS characteristics**

| Symbol           | Parameter  | Conditions  | Level/Class |
|------------------|--|---|-------------|
| V <sub>ESD</sub> | Voltage applied to all device pins to induce a functional disturbance  | V <sub>DD</sub> = 3.3 V, TA = +25 °C<br>conforms to IEC 61000-4-2 | 3B          |
| V <sub>FTB</sub> | Fast transient voltage burst applied to induce a functional disturbance through 100 pF on V <sub>DD</sub> and V <sub>SS</sub> pins | V <sub>DD</sub> = 3.3 V, TA = +25 °C<br>conforms to IEC 61000-4-4 | 4A          |

EMI (Electromagnetic Interference) emission testing result is given in the following table, compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

**Table 7. EMI characteristics**

| Symbol           | Parameter  | Conditions  | Tested frequency band | Conditions |      | Unit |
|------------------|------------|---|-----------------------|------------|------|------|
|                  |            |   |                       | 24M        | 48M  |      |
| S <sub>EMI</sub> | Peak level | V <sub>DD</sub> = 5.0 V,<br>TA = +25 °C,<br>compliant with IEC<br>61967-2 | 0.1 to 2 MHz          | <0         | <0   | dBμV |
|                  |            |   | 2 to 30 MHz           | -3.9       | -2.8 |      |
|                  |            |   | 30 to 130 MHz         | -7.2       | -8   |      |
|                  |            |   | 130 MHz to 1GHz       | -7         | -7   |      |

## 4.5 Power supply supervisor characteristics

**Table 8. Power supply supervisor characteristics**

| Symbol               | Parameter                  | Conditions | Min  | Typ  | Max  | Unit |
|----------------------|----------------------------|------------|------|------|------|------|
| V <sub>POR</sub>     | Power on reset threshold   | —          | 2.30 | 2.40 | 2.48 | V    |
| V <sub>PDR</sub>     | Power down reset threshold |            | 1.72 | 1.80 | 1.88 | V    |
| V <sub>HYST</sub>    | PDR hysteresis             |            | —    | 0.6  | —    | V    |
| T <sub>RSTTEMP</sub> | Reset temporization        |            | —    | 2    | —    | ms   |

## 4.6 Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample. Static latch-up (LU) test is based on the two measurement methods.

**Table 9. ESD characteristics**

| Symbol                | Parameter   | Conditions                         | Min | Typ | Max  | Unit |
|-----------------------|---|------------------------------------|-----|-----|------|------|
| V <sub>ESD(HBM)</sub> | Electrostatic discharge voltage (human body model)    | T <sub>A</sub> =25 °C; JESD22-A114 | —   | —   | 6000 | V    |
| V <sub>ESD(CDM)</sub> | Electrostatic discharge voltage (charge device model) | T <sub>A</sub> =25 °C; JESD22-C101 | —   | —   | 1000 | V    |

**Table 10. Static latch-up characteristics**

| Symbol | Parameter                        | Conditions                    | Min | Typ | Max  | Unit |
|--------|----------------------------------|-------------------------------|-----|-----|------|------|
| LU     | I-test                           | T <sub>A</sub> =25 °C; JESD78 | —   | —   | ±200 | mA   |
|        | V <sub>supply over voltage</sub> |                               | —   | —   | 5.4  | V    |

## 4.7 External clock characteristics

**Table 11. High speed external clock (HXTAL) generated from a crystal/ceramic characteristics**

| Symbol               | Parameter   | Conditions  | Min | Typ | Max | Unit       |
|----------------------|---|---|-----|-----|-----|------------|
| $f_{\text{HXTAL}}$   | High Speed External oscillator (HXTAL) frequency                  | $V_{\text{DD}}=5.0\text{V}$                                     | 4   | 8   | 32  | MHz        |
| $C_{\text{HXTAL}}$   | Recommended load capacitance on OSC_IN and OSC_OUT                | —   | —   | 20  | 30  | pF         |
| $R_{\text{FHXTAL}}$  | Recommended external feedback resistor between OSC_IN and OSC_OUT | —   | —   | 400 | —   | K $\Omega$ |
| $D_{\text{HXTAL}}$   | HXTAL oscillator duty cycle                                       | —   | 30  | 50  | 70  | %          |
| $I_{\text{DDHXTAL}}$ | HXTAL oscillator operating current                                | $V_{\text{DD}}=3.3\text{V}$ , $T_{\text{A}}=25^{\circ}\text{C}$ | —   | 1   | —   | mA         |
| $t_{\text{SUHXTAL}}$ | HXTAL oscillator startup time                                     | $V_{\text{DD}}=3.3\text{V}$ , $T_{\text{A}}=25^{\circ}\text{C}$ | —   | 2   | —   | ms         |

**Table 12. Low speed external clock (LXTAL) generated from a crystal/ceramic characteristics**

| Symbol               | Parameter  | Conditions                                 | Min | Typ    | Max | Unit          |
|----------------------|--|--|-----|--------|-----|---------------|
| $f_{\text{LXTAL}}$   | Low Speed External oscillator (LXTAL) frequency        | $V_{\text{DD}}=V_{\text{BAT}}=3.3\text{V}$ | —   | 32.768 | —   | KHz           |
| $C_{\text{LXTAL}}$   | Recommended load capacitance on OSC32_IN and OSC32_OUT | —  | —   | —      | 15  | pF            |
| $D_{\text{LXTAL}}$   | LXTAL oscillator duty cycle                            | —  | 30  | 50     | 70  | %             |
| $I_{\text{DDLXTAL}}$ | LXTAL oscillator operating current                     | Low Drive                                  | —   | 0.7    | —   | $\mu\text{A}$ |
|                      |  | High Drive                                 | —   | 1.3    | —   |               |
| $t_{\text{SULXTAL}}$ | LXTAL oscillator startup time                          | $V_{\text{DD}}=V_{\text{BAT}}=3.3\text{V}$ | —   | 2      | —   | s             |

## 4.8 Internal clock characteristics

**Table 13. High speed internal clock (IRC8M) characteristics**

| Symbol        | Parameter   | Conditions   | Min  | Typ | Max  | Unit    |
|---------------|---|--|------|-----|------|---------|
| $f_{IRC8M}$   | High Speed Internal Oscillator (IRC8M) frequency        | $V_{DD}=3.3V$                                      | —    | 8   | —    | MHz     |
| $ACC_{IRC8M}$ | IRC8M oscillator Frequency accuracy, Factory-trimmed    | $V_{DD}=3.3V, T_A=-40^{\circ}C \sim +105^{\circ}C$ | -4.0 | —   | +5.0 | %       |
|               |   | $V_{DD}=3.3V, T_A=0^{\circ}C \sim +85^{\circ}C$    | -2.0 | —   | +2.0 | %       |
|               |   | $V_{DD}=3.3V, T_A=25^{\circ}C$                     | -1.0 | —   | +1.0 | %       |
|               | IRC8M oscillator Frequency accuracy, User trimming step | —  | —    | 0.5 | —    | %       |
| $D_{IRC8M}$   | IRC8M oscillator duty cycle                             | $V_{DD}=3.3V, f_{IRC8M}=8MHz$                      | 45   | 50  | 55   | %       |
| $I_{DDIRC8M}$ | IRC8M oscillator operating current                      | $V_{DD}=3.3V, f_{IRC8M}=8MHz$                      | —    | 66  | 80   | $\mu A$ |
| $t_{SUIRC8M}$ | IRC8M oscillator startup time                           | $V_{DD}=3.3V, f_{IRC8M}=8MHz$                      | —    | 2.5 | 4    | us      |

**Table 14. High speed internal clock (IRC48M) characteristics**

| Symbol         | Parameter  | Conditions   | Min  | Typ  | Max  | Unit    |
|----------------|--|--|------|------|------|---------|
| $f_{IRC48M}$   | High Speed Internal Oscillator (IRC48M) frequency        | $V_{DD}=3.3V$                                      | —    | 48   | —    | MHz     |
| $ACC_{IRC48M}$ | IRC48M oscillator Frequency accuracy, Factory-trimmed    | $V_{DD}=3.3V, T_A=-40^{\circ}C \sim +105^{\circ}C$ | -4.0 | —    | +5.0 | %       |
|                |  | $V_{DD}=3.3V, T_A=0^{\circ}C \sim +85^{\circ}C$    | -3.0 | —    | +3.0 | %       |
|                |  | $V_{DD}=3.3V, T_A=25^{\circ}C$                     | -2.0 | —    | +2.0 | %       |
|                | IRC48M oscillator Frequency accuracy, User trimming step | —  | —    | 0.12 | —    | %       |
| $D_{IRC48M}$   | IRC48M oscillator duty cycle                             | $V_{DD}=3.3V, f_{IRC48M}=16MHz$                    | 45   | 50   | 55   | %       |
| $I_{DDIRC48M}$ | IRC48M oscillator operating current                      | $V_{DD}=3.3V, f_{IRC48M}=16MHz$                    | —    | 240  | 300  | $\mu A$ |
| $t_{SUIRC48M}$ | IRC48M oscillator startup time                           | $V_{DD}=3.3V, f_{IRC48M}=16MHz$                    | —    | 2.5  | 4    | us      |

**Table 15. Low speed internal clock (IRC32K) characteristics**

| Symbol                | Parameter  | Conditions  | Min | Typ | Max | Unit |
|-----------------------|--|---|-----|-----|-----|------|
| f <sub>IRC32K</sub>   | Low Speed Internal oscillator (IRC32K) frequency | V <sub>DD</sub> =V <sub>BAT</sub> =3.3V,<br>T <sub>A</sub> =-40°C ~ +85°C | 20  | 40  | 45  | KHz  |
| I <sub>DDIRC32K</sub> | IRC32K oscillator operating current              | V <sub>DD</sub> =V <sub>BAT</sub> =3.3V, T <sub>A</sub> =25°C             | —   | 0.4 | 0.6 | μA   |
| t <sub>SUIRC32K</sub> | IRC32K oscillator startup time                   | V <sub>DD</sub> =V <sub>BAT</sub> =3.3V, T <sub>A</sub> =25°C             | —   | 110 | 130 | μs   |

## 4.9 PLL characteristics

**Table 16. PLL characteristics**

| Symbol                | Parameter                      | Conditions      | Min | Typ | Max | Unit |
|-----------------------|--------------------------------|-----------------|-----|-----|-----|------|
| f <sub>PLLIN</sub>    | PLL input clock frequency      | —               | 1   | —   | 25  | MHz  |
| f <sub>PLLOUT</sub>   | PLL output clock frequency     | —               | 16  | —   | 168 | MHz  |
| f <sub>VCOOUT</sub>   | PLL VCO output clock frequency | —               | 32  | —   | 344 | MHz  |
| t <sub>LOCK</sub>     | PLL lock time                  | —               | —   | —   | 300 | μs   |
| I <sub>DD</sub>       | Current consumption on VDD     | VCO freq=344MHz | —   | 500 | —   | μA   |
| I <sub>DDA</sub>      | Current consumption on VDDA    | VCO freq=344MHz | —   | 750 | —   | μA   |
| Jitter <sub>PLL</sub> | Cycle to cycle Jitter          | System clock    | —   | 300 | —   | ps   |

**Table 17. PLL2/3 characteristics**

| Symbol                | Parameter                      | Conditions      | Min | Typ | Max | Unit |
|-----------------------|--------------------------------|-----------------|-----|-----|-----|------|
| f <sub>PLLIN</sub>    | PLL input clock frequency      | —               | 1   | —   | 25  | MHz  |
| f <sub>PLLOUT</sub>   | PLL output clock frequency     | —               | 16  | —   | 100 | MHz  |
| f <sub>VCOOUT</sub>   | PLL VCO output clock frequency | —               | 32  | —   | 200 | MHz  |
| t <sub>LOCK</sub>     | PLL lock time                  | —               | —   | —   | 300 | μs   |
| I <sub>DD</sub>       | Current consumption on VDD     | VCO freq=200MHz | —   | 290 | —   | μA   |
| I <sub>DDA</sub>      | Current consumption on VDDA    | VCO freq=200MHz | —   | 440 | —   | μA   |
| Jitter <sub>PLL</sub> | Cycle to cycle Jitter          | System clock    | —   | 300 | —   | ps   |

## 4.10 Memory characteristics

**Table 18. Flash memory characteristics**

| Symbol              | Parameter   | Conditions                    | Min | Typ | Max | Unit    |
|---------------------|---|-------------------------------|-----|-----|-----|---------|
| PE <sub>CYC</sub>   | Number of guaranteed program /erase cycles before failure (Endurance) | T <sub>A</sub> =-40°C ~ +85°C | 100 | —   | —   | kcycles |
| t <sub>RET</sub>    | Data retention time   | T <sub>A</sub> =125°C         | 20  | —   | —   | years   |
| t <sub>PROG</sub>   | Word programming time   | T <sub>A</sub> =-40°C ~ +85°C | 200 | —   | 400 | us      |
| t <sub>ERASE</sub>  | Page erase time   | T <sub>A</sub> =-40°C ~ +85°C | 60  | 100 | 450 | ms      |
| t <sub>MERASE</sub> | Mass erase time   | T <sub>A</sub> =-40°C ~ +85°C | 3.2 | —   | 9.6 | s       |



## 4.11 GPIO characteristics

**Table 19. I/O port characteristics**

| Symbol          | Parameter   |          | Conditions                                   | Min  | Typ | Max  | Unit |
|-----------------|---|----------|--|------|-----|------|------|
| V <sub>IL</sub> | Standard IO Low level input voltage               |          | V <sub>DD</sub> =2.6V                        | —    | —   | 0.97 | V    |
|                 |   |          | V <sub>DD</sub> =3.3V                        | —    | —   | 1.29 |      |
|                 |   |          | V <sub>DD</sub> =3.6V                        | —    | —   | 1.42 |      |
|                 | High Voltage tolerant IO Low level input voltage  |          | V <sub>DD</sub> =2.6V                        | —    | —   | 0.98 | V    |
|                 |   |          | V <sub>DD</sub> =3.3V                        | —    | —   | 1.29 |      |
|                 |   |          | V <sub>DD</sub> =3.6V                        | —    | —   | 1.41 |      |
| V <sub>IH</sub> | Standard IO High level input voltage              |          | V <sub>DD</sub> =2.6V                        | 1.67 | —   | —    | V    |
|                 |   |          | V <sub>DD</sub> =3.3V                        | 1.97 | —   | —    |      |
|                 |   |          | V <sub>DD</sub> =3.6V                        | 2.09 | —   | —    |      |
|                 | High Voltage tolerant IO High level input voltage |          | V <sub>DD</sub> =2.6V                        | 1.64 | —   | —    | V    |
|                 |   |          | V <sub>DD</sub> =3.3V                        | 1.97 | —   | —    |      |
|                 |   |          | V <sub>DD</sub> =3.6V                        | 2.07 | —   | —    |      |
| V <sub>OL</sub> | Low level output voltage                          |          | V <sub>DD</sub> =2.6V, I <sub>IO</sub> =8mA  | —    | —   | 0.17 | V    |
|                 |   |          | V <sub>DD</sub> =3.3V, I <sub>IO</sub> =8mA  | —    | —   | 0.15 |      |
|                 |   |          | V <sub>DD</sub> =3.6V, I <sub>IO</sub> =8mA  | —    | —   | 0.15 |      |
|                 |   |          | V <sub>DD</sub> =2.6V, I <sub>IO</sub> =20mA | —    | —   | 0.49 |      |
|                 |   |          | V <sub>DD</sub> =3.3V, I <sub>IO</sub> =20mA | —    | —   | 0.40 |      |
|                 |   |          | V <sub>DD</sub> =3.6V, I <sub>IO</sub> =20mA | —    | —   | 0.40 |      |
| V <sub>OH</sub> | High level output voltage                         |          | V <sub>DD</sub> =2.6V, I <sub>IO</sub> =8mA  | 2.40 | —   | —    | V    |
|                 |   |          | V <sub>DD</sub> =3.3V, I <sub>IO</sub> =8mA  | 3.11 | —   | —    |      |
|                 |   |          | V <sub>DD</sub> =3.6V, I <sub>IO</sub> =8mA  | 3.44 | —   | —    |      |
|                 |   |          | V <sub>DD</sub> =2.6V, I <sub>IO</sub> =20mA | 2.02 | —   | —    |      |
|                 |   |          | V <sub>DD</sub> =3.3V, I <sub>IO</sub> =20mA | 2.81 | —   | —    |      |
|                 |   |          | V <sub>DD</sub> =3.6V, I <sub>IO</sub> =20mA | 3.15 | —   | —    |      |
| R <sub>PU</sub> | Internal pull-up resistor                         | All pins | V <sub>IN</sub> =V <sub>SS</sub>             | 30   | 40  | 50   | kΩ   |
|                 |   | PA10     | —  | 7.5  | 10  | 13.5 |      |
| R <sub>PD</sub> | Internal pull-down resistor                       | All pins | V <sub>IN</sub> =V <sub>DD</sub>             | 30   | 40  | 50   | kΩ   |
|                 |   | PA10     | —  | 7.5  | 10  | 13.5 |      |

## 4.12 ADC characteristics

**Table 20. ADC characteristics**

| Symbol             | Parameter                                       | Conditions                      | Min    | Typ              | Max               | Unit                |
|--------------------|---|---------------------------------|--------|------------------|-------------------|---------------------|
| V <sub>DDA</sub>   | Operating voltage                               | —                               | 2.6    | 3.3              | 3.6               | V                   |
| V <sub>ADCIN</sub> | ADC input voltage range                         | —                               | 0      | —                | V <sub>REF+</sub> | V                   |
| f <sub>ADC</sub>   | ADC clock                                       | —                               | 0.1    | —                | 40                | MHz                 |
| f <sub>s</sub>     | Sampling rate                                   | 12-bit                          | 0.007  | —                | 2.86              | MSPS                |
|                    |   | 10-bit                          | 0.008  | —                | 3.33              |                     |
|                    |   | 8-bit                           | 0.01   | —                | 4.00              |                     |
|                    |   | 6-bit                           | 0.012  | —                | 5.00              |                     |
| V <sub>IN</sub>    | Analog input voltage                            | 16 external;2 internal          | 0      | —                | V <sub>DDA</sub>  | V                   |
| V <sub>REF+</sub>  | Positive Reference Voltage                      | —                               | —      | V <sub>DDA</sub> | —                 | V                   |
| V <sub>REF-</sub>  | Negative Reference Voltage                      | —                               | —      | 0                | —                 | V                   |
| R <sub>AIN</sub>   | External input impedance                        | See <i>Equation 2</i>           | —      | —                | 32.9              | kΩ                  |
| R <sub>ADC</sub>   | Input sampling switch resistance                | —                               | —      | —                | 0.55              | kΩ                  |
| C <sub>ADC</sub>   | Input sampling capacitance                      | No pin/pad capacitance included | —      | —                | 5.5               | pF                  |
| t <sub>CAL</sub>   | Calibration time                                | f <sub>ADC</sub> =40MHz         | —      | 3.275            | —                 | μs                  |
| t <sub>s</sub>     | Sampling time                                   | f <sub>ADC</sub> =40MHz         | 0.0375 | —                | 5.99              | μs                  |
| t <sub>CONV</sub>  | Total conversion time (including sampling time) | 12-bit                          | —      | 14               | —                 | 1/ f <sub>ADC</sub> |
|                    |   | 10-bit                          | —      | 12               | —                 |                     |
|                    |   | 8-bit                           | —      | 10               | —                 |                     |
|                    |   | 6-bit                           | —      | 8                | —                 |                     |
| t <sub>SU</sub>    | Startup time                                    | —                               | —      | —                | 1                 | μs                  |

**Equation 2:** R<sub>AIN</sub> max formula 
$$R_{AIN} < \frac{T_s}{f_{ADC} \cdot C_{ADC} \cdot \ln(2^{N+2})} - R_{ADC}$$

The formula above (Equation 2) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N=12 (from 12-bit resolution).

**Table 21. ADC R<sub>AIN</sub> max for f<sub>ADC</sub>=40MHz**

| T <sub>s</sub> (cycles) | t <sub>s</sub> (us) | R <sub>AIN</sub> max (KΩ) |
|-------------------------|---------------------|---------------------------|
| 1.5                     | 0.0375              | 0.15                      |
| 7.5                     | 0.1875              | 2.96                      |
| 13.5                    | 0.3375              | 5.77                      |
| 28.5                    | 0.7125              | 12.8                      |
| 41.5                    | 1.0375              | 18.9                      |
| 55.5                    | 1.3875              | 25.4                      |
| 71.5                    | 1.7875              | 32.9                      |
| 239.5                   | 5.9875              | N/A                       |

Note: Guaranteed by design, not tested in production.

**Table 22. ADC dynamic accuracy at  $f_{ADC} = 30$  MHz**

| Symbol | Parameter                            | Test conditions  | Min  | Typ  | Max | Unit |
|--------|--------------------------------------|--|------|------|-----|------|
| ENOB   | Effective number of bits             | $f_{ADC}=30\text{MHz}$<br>$V_{DDA}=V_{REFP}=2.6\text{V}$<br>Input Frequency=110KHz<br>Temperature=25°C | 10.5 | 10.6 | —   | bits |
| SNDR   | Signal-to-noise and distortion ratio |  | 65   | 65.6 | —   | dB   |
| SNR    | Signal-to-noise ratio                |  | 65.5 | 66   | —   |      |
| THD    | Total harmonic distortion            |  | -74  | -76  | —   |      |

**Table 23. ADC dynamic accuracy at  $f_{ADC} = 30$  MHz**

| Symbol | Parameter                            | Test conditions  | Min  | Typ  | Max | Unit |
|--------|--------------------------------------|--|------|------|-----|------|
| ENOB   | Effective number of bits             | $f_{ADC}=30\text{MHz}$<br>$V_{DDA}=V_{REFP}=3.3\text{V}$<br>Input Frequency=110KHz<br>Temperature=25°C | 10.7 | 10.8 | —   | bits |
| SNDR   | Signal-to-noise and distortion ratio |  | 66.2 | 65.8 | —   | dB   |
| SNR    | Signal-to-noise ratio                |  | 66.8 | 67.4 | —   |      |
| THD    | Total harmonic distortion            |  | -71  | -75  | —   |      |

**Table 24. ADC dynamic accuracy at  $f_{ADC} = 36$  MHz**

| Symbol | Parameter                            | Test conditions  | Min  | Typ  | Max | Unit |
|--------|--------------------------------------|--|------|------|-----|------|
| ENOB   | Effective number of bits             | $f_{ADC}=36\text{MHz}$<br>$V_{DDA}=V_{REFP}=3.3\text{V}$<br>Input Frequency=110KHz<br>Temperature=25°C | 10.3 | 10.4 | —   | bits |
| SNDR   | Signal-to-noise and distortion ratio |  | 63.8 | 64.4 | —   | dB   |
| SNR    | Signal-to-noise ratio                |  | 64.2 | 65   | —   |      |
| THD    | Total harmonic distortion            |  | -70  | -72  | —   |      |

**Table 25. ADC dynamic accuracy at  $f_{ADC} = 40$  MHz**

| Symbol | Parameter                            | Test conditions  | Min  | Typ  | Max | Unit |
|--------|--------------------------------------|--|------|------|-----|------|
| ENOB   | Effective number of bits             | $f_{ADC}=40\text{MHz}$<br>$V_{DDA}=V_{REFP}=3.3\text{V}$<br>Input Frequency=110KHz<br>Temperature=25°C | 9.9  | 10.0 | —   | bits |
| SNDR   | Signal-to-noise and distortion ratio |  | 61.4 | 62   | —   | dB   |
| SNR    | Signal-to-noise ratio                |  | 62   | 62.4 | —   |      |
| THD    | Total harmonic distortion            |  | -68  | -70  | —   |      |

**Table 26. ADC static accuracy at  $f_{ADC} = 15$  MHz**

| Symbol | Parameter                    | Test conditions  | Typ  | Max  | Unit |
|--------|------------------------------|--|------|------|------|
| Offset | Offset error                 | $f_{ADC}=15\text{MHz}$<br>$V_{DDA}=V_{REFP}=3.3\text{V}$ | ±2   | ±3   | LSB  |
| DNL    | Differential linearity error |  | ±0.9 | ±1.2 |      |
| INL    | Integral linearity error     |  | ±1.1 | ±1.5 |      |

## 4.13 DAC characteristics

**Table 27. DAC characteristics**

| Symbol                 | Parameter  | Conditions                                      | Min | Typ  | Max                    | Unit |
|------------------------|--|---|-----|------|------------------------|------|
| V <sub>DDA</sub>       | Operating voltage  | —   | 2.6 | 3.3  | 3.6                    | V    |
| R <sub>LOAD</sub>      | Resistive load   | Resistive load with buffer ON                   | 5   | —    | —                      | kΩ   |
| R <sub>O</sub>         | Impedance output   | Impedance output with buffer OFF                | —   | —    | 15                     | kΩ   |
| C <sub>LOAD</sub>      | Capacitive load  | Capacitive load with buffer ON                  | —   | —    | 50                     | pF   |
| DAC_OUT <sub>min</sub> | Lower DAC_OUT voltage  | Lower DAC_OUT voltage with buffer ON            | 0.2 | —    | —                      | V    |
|                        |  | Lower DAC_OUT voltage with buffer OFF           | 0.5 | —    | —                      | mV   |
| DAC_OUT <sub>max</sub> | Higher DAC_OUT voltage   | Higher DAC_OUT voltage with buffer ON           | —   | —    | V <sub>DDA</sub> -0.2  | V    |
|                        |  | Higher DAC_OUT voltage with buffer OFF          | —   | —    | V <sub>DDA</sub> -1LSB | V    |
| I <sub>DDA</sub>       | DC current consumption in quiescent mode with no load            | Middle code on the input                        | —   | —    | 500                    | μA   |
|                        |  | Worst code on the input                         | —   | —    | 560                    |      |
| DNL                    | Differential non linearity                                       | 10-bit configuration                            | —   | —    | ±0.5                   | LSB  |
|                        |  | 12-bit configuration                            | —   | —    | ±2                     |      |
| INL                    | Integral non linearity   | 10-bit configuration                            | —   | —    | ±1                     | LSB  |
|                        |  | 12-bit configuration                            | —   | —    | ±4                     |      |
| Gain error             | Gain error   | —   | —   | ±0.5 | —                      | %    |
| T <sub>SETTLING</sub>  | Settling time  | C <sub>LOAD</sub> ≤50pF, R <sub>LOAD</sub> ≥5kΩ | —   | 0.5  | 1                      | μs   |
| Update rate            | Max frequency for a correct DAC_OUT change from code i to i±1LSB | C <sub>LOAD</sub> ≤50pF, R <sub>LOAD</sub> ≥5kΩ | —   | —    | 4                      | MS/s |
| T <sub>WAKEUP</sub>    | Wakeup time from off state                                       | C <sub>LOAD</sub> ≤50pF, R <sub>LOAD</sub> ≥5kΩ | —   | 1    | 2                      | μs   |
| PSRR                   | Power supply rejection ratio                                     | No R <sub>Load</sub> , C <sub>LOAD</sub> =50pF  | —   | -90  | -75                    | dB   |

## 4.14 SPI characteristics

**Table 28. SPI characteristics**

| Symbol                 | Parameter                | Conditions               | Min | Typ | Max | Unit |
|------------------------|--------------------------|--------------------------|-----|-----|-----|------|
| f <sub>SCK</sub>       | SCK clock frequency      | —                        | —   | —   | 30  | MHz  |
| TSl <sub>K(H)</sub>    | SCK clock high time      | —                        | 16  | —   | —   | ns   |
| TSl <sub>K(L)</sub>    | SCK clock low time       | —                        | 16  | —   | —   | ns   |
| <b>SPI master mode</b> |                          |                          |     |     |     |      |
| t <sub>V(MO)</sub>     | Data output valid time   | —                        | —   | —   | 25  | ns   |
| t <sub>H(MO)</sub>     | Data output hold time    | —                        | 2   | —   | —   | ns   |
| t <sub>SU(MI)</sub>    | Data input setup time    | —                        | 5   | —   | —   | ns   |
| t <sub>H(MI)</sub>     | Data input hold time     | —                        | 5   | —   | —   | ns   |
| <b>SPI slave mode</b>  |                          |                          |     |     |     |      |
| t <sub>SU(NSS)</sub>   | NSS enable setup time    | f <sub>PCLK</sub> =54MHz | 74  | —   | —   | ns   |
| t <sub>H(NSS)</sub>    | NSS enable hold time     | f <sub>PCLK</sub> =54MHz | 37  | —   | —   | ns   |
| t <sub>A(SO)</sub>     | Data output access time  | f <sub>PCLK</sub> =54MHz | 0   | —   | 55  | ns   |
| t <sub>DIS(SO)</sub>   | Data output disable time | —                        | 3   | —   | 10  | ns   |
| t <sub>V(SO)</sub>     | Data output valid time   | —                        | —   | —   | 25  | ns   |
| t <sub>H(SO)</sub>     | Data output hold time    | —                        | 15  | —   | —   | ns   |
| t <sub>SU(SI)</sub>    | Data input setup time    | —                        | 5   | —   | —   | ns   |
| t <sub>H(SI)</sub>     | Data input hold time     | —                        | 4   | —   | —   | ns   |

## 4.15 I2C characteristics

**Table 29. I2C characteristics**

| Symbol              | Parameter           | Conditions | Standard mode |     | Fast mode |      | Unit |
|---------------------|---------------------|------------|---------------|-----|-----------|------|------|
|                     |                     |            | Min           | Max | Min       | Max  |      |
| f <sub>SCL</sub>    | SCL clock frequency | —          | 0             | 100 | 0         | 1000 | KHz  |
| TSl <sub>L(H)</sub> | SCL clock high time | —          | 4.0           | —   | 0.6       | —    | ns   |
| TSl <sub>L(L)</sub> | SCL clock low time  | —          | 4.7           | —   | 1.3       | —    | ns   |

## 4.16 USART characteristics

**Table 30. USART characteristics**

| Symbol              | Parameter           | Conditions | Min | Typ | Max | Unit |
|---------------------|---------------------|------------|-----|-----|-----|------|
| f <sub>SCK</sub>    | SCK clock frequency | —          | —   | —   | 84  | MHz  |
| TSl <sub>K(H)</sub> | SCK clock high time | —          | 5.5 | —   | —   | ns   |
| TSl <sub>K(L)</sub> | SCK clock low time  | —          | 5.5 | —   | —   | ns   |

## 5 Package information

### 5.1 QFN package outline dimensions

Figure 5. QFN package outline

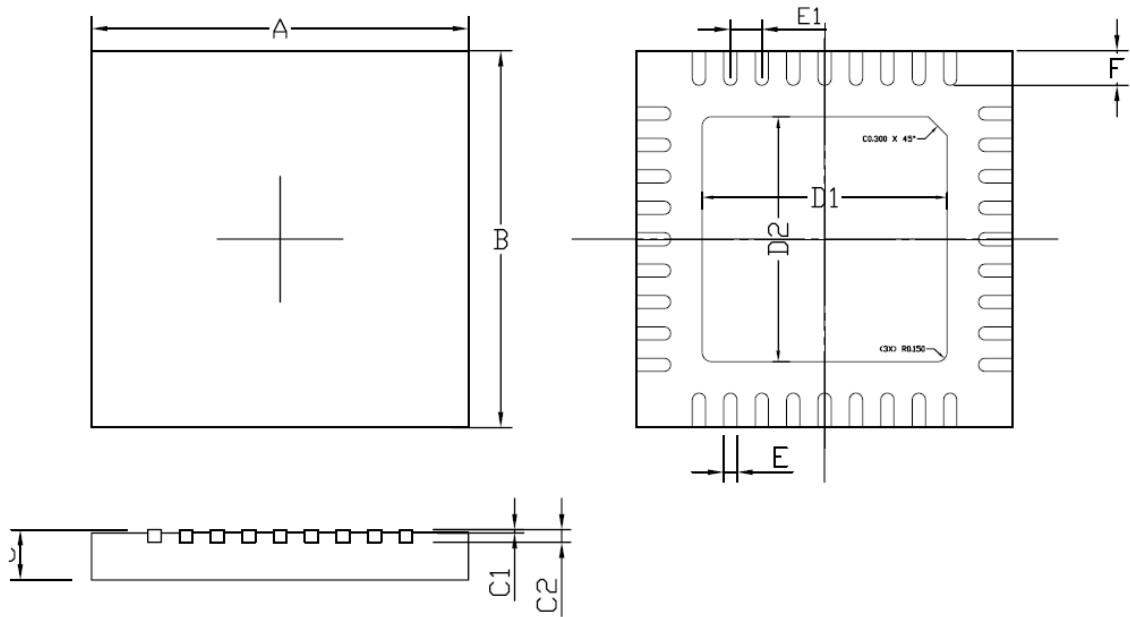


Table 31. QFN package dimensions

| Symbol | Dimensions (mm) |      | Symbol | Dimensions (mm) |     |
|--------|-----------------|------|--------|-----------------|-----|
|        | min             | max  |        | min             | max |
| A      | 6.0 ± 0.1       |      | D1     | 3.90 Typ        |     |
| B      | 6.0 ± 0.1       |      | D2     | 3.90 Typ        |     |
| C      | 0.85            | 0.95 | E      | 0.210 ± 0.025   |     |
| C1     | 0~0.050         |      | E1     | 0.500 Typ       |     |
| C2     | 0.203 Typ       |      | F      | 0.550 Typ       |     |

Note:

1. Formed lead shall be planar with respect to one another within 0.004 inches.
2. Both package length and width do not include mold flash and metal burr.

## 6 Ordering Information

Table 32. Part ordering code for GD32FFPRTGU6 device

| Ordering code | Flash (KB) | Package | Package type | Temperature operating range  |
|---------------|------------|---------|--------------|------------------------------|
| GD32FFPRTGU6  | 1024       | QFN36   | Green        | Industrial<br>-40°C to +85°C |

## 7 Revision History

**Table 33. Revision history**

| Revision No. | Description     | Date        |
|--------------|-----------------|-------------|
| 1.0          | Initial Release | Jun.6, 2017 |