

N-Channel Enhancement Mode Power MOSFET

Description

The HKTQ30N03 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

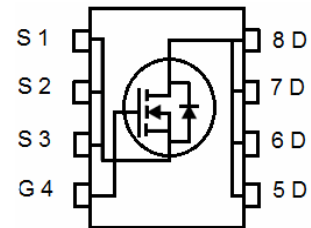
General Features

- High density cell design for ultra low R_{ds}
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

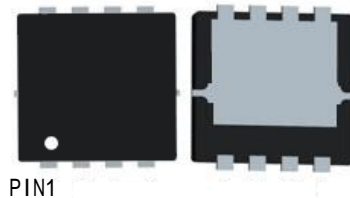
Application

- High current load applications
- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply

V_{DSS}	$R_{DS(ON)}$ Typ	I_D Max
30V	5.3m Ω @ 10V	30A
	9.8m Ω @ 4.5V	



Schematic Diagram



Top View

Bottom View

Package Marking and Ordering Information

Part ID	Package	Marking	Packing
HKTQ30N03	PDFN3*3-8L	Q30N03	5000PCS/Reel

PDFN3*3

Absolute Maximum Ratings ($T_C=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	30	A
Drain Current-Continuous($T_C=100^{\circ}C$)	$I_D (100)^{\circ}C$	21	A
Pulsed Drain Current (Note 1)	I_{DM}	115	A
Maximum Power Dissipation	P_D	21	W
Single pulse avalanche energy (Note 5)	E_{AS}	112	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-50 To 150	$^{\circ}C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case (Note 2)	$R_{\theta JC}$	7.1	$^{\circ}C/W$
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Electrical Characteristics (TC=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=30V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1	1.5	2.5	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=15A$	-	5.3	8.0	m Ω
		$V_{GS}=4.5V, I_D=15A$	-	9.8	14.0	
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=20A$	-	20	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{iss}	$V_{DS}=15V, V_{GS}=0V,$ $F=1.0MHz$	-	1015	-	PF
Output Capacitance	C_{oss}		-	200	-	PF
Reverse Transfer Capacitance	C_{rss}		-	160	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=20V, I_D=2A$ $V_{GS}=10V, R_{GEN}=3\Omega$	-	7	-	nS
Turn-on Rise Time	t_r		-	19	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	24	-	nS
Turn-Off Fall Time	t_f		-	24	-	nS
Total Gate Charge	Q_g	$V_{DS}=15V, I_D=20A,$ $V_{GS}=10V$	-	23	-	nC
Gate-Source Charge	Q_{gs}		-	3.9	-	nC
Gate-Drain Charge	Q_{gd}		-	7	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=15A$	-	0.82	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	30	A
Reverse Recovery Time	t_{rr}	$V_{GS}=0V, I_{SD}=15A$ $di/dt=100A/\mu s$ (Note3)	-	5	-	nS
Reverse Recovery Charge	Q_{rr}		-	0.2	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

A. Pulse Test: Pulse Width $\leq 300\mu s$, Duty cycle $\leq 2\%$.

B. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ Typical Performance Characteristics

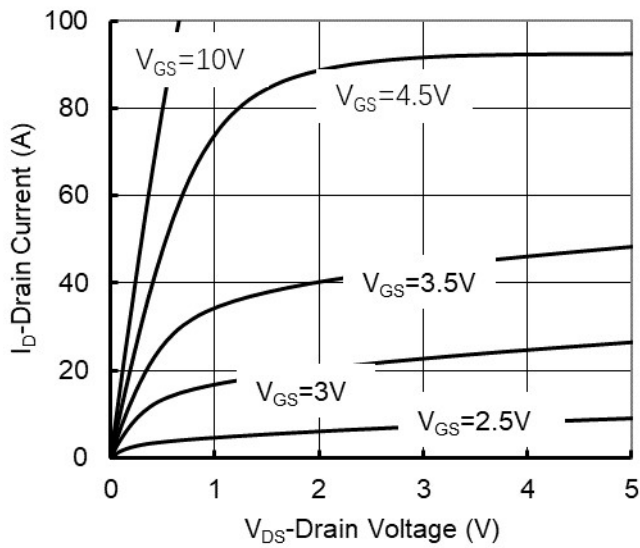


Figure1. Output Characteristics

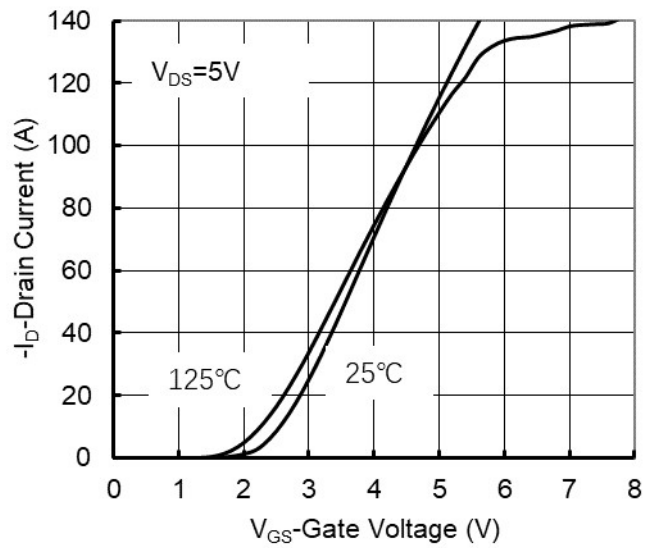


Figure2. Transfer Characteristics

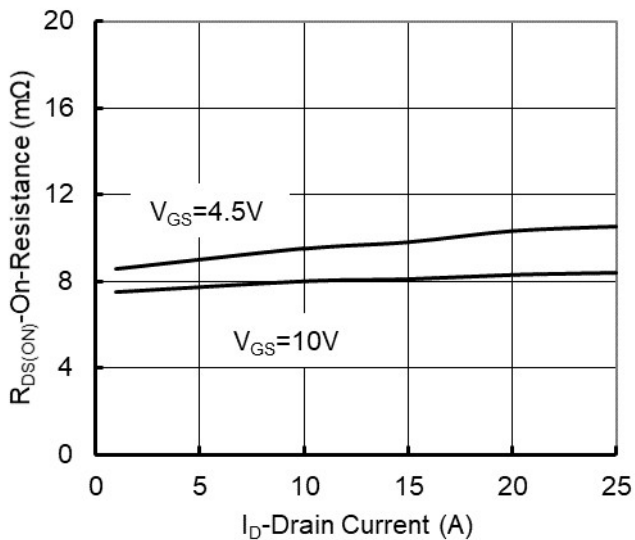


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

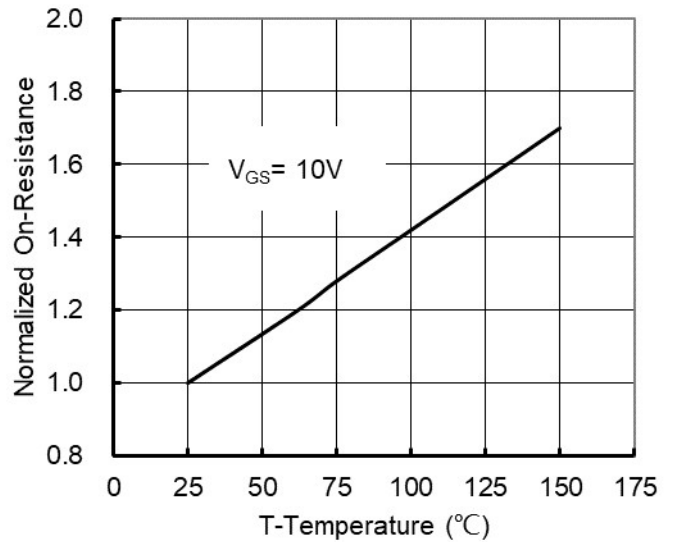


Figure 4: On-Resistance vs. Junction Temperature

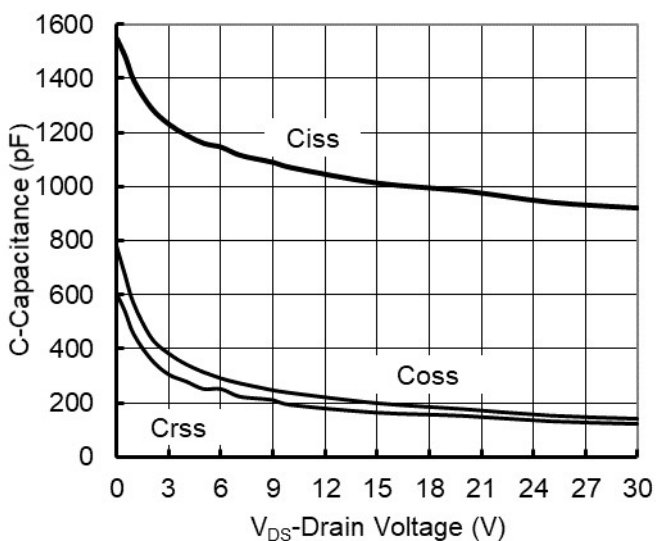


Figure5. Capacitance Characteristics

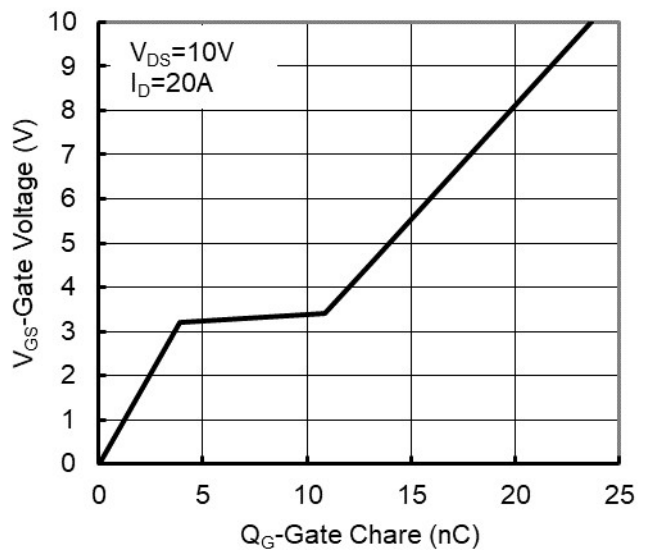


Figure6. Gate Charge

Figure7. Safe Operation Area

Figure8. Maximum Continuous Drain Current vs Case Temperature

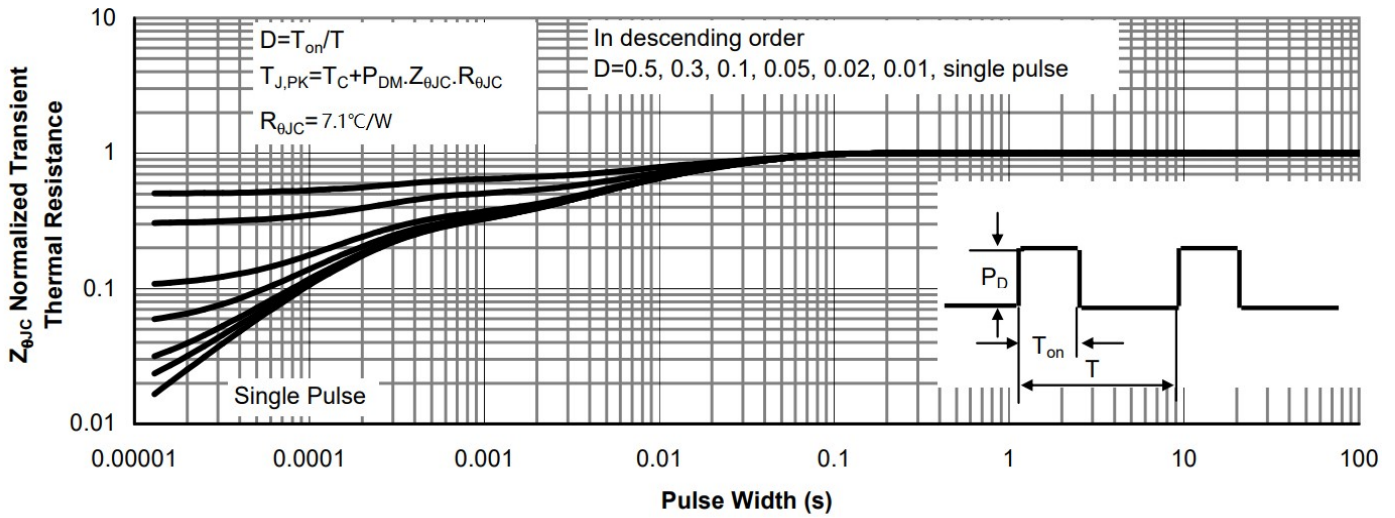


Figure9. Normalized Maximum Transient Thermal Impedance

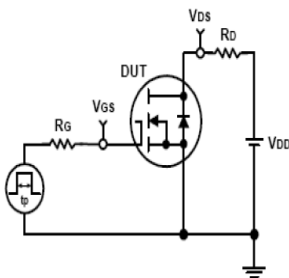


Fig10. Switching Time Test Circuit and waveforms

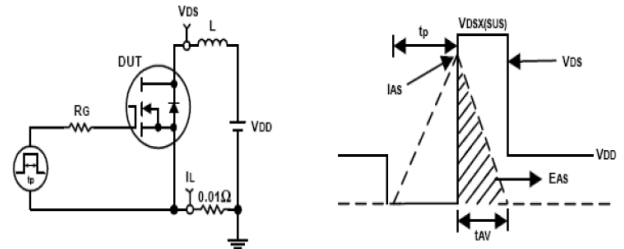
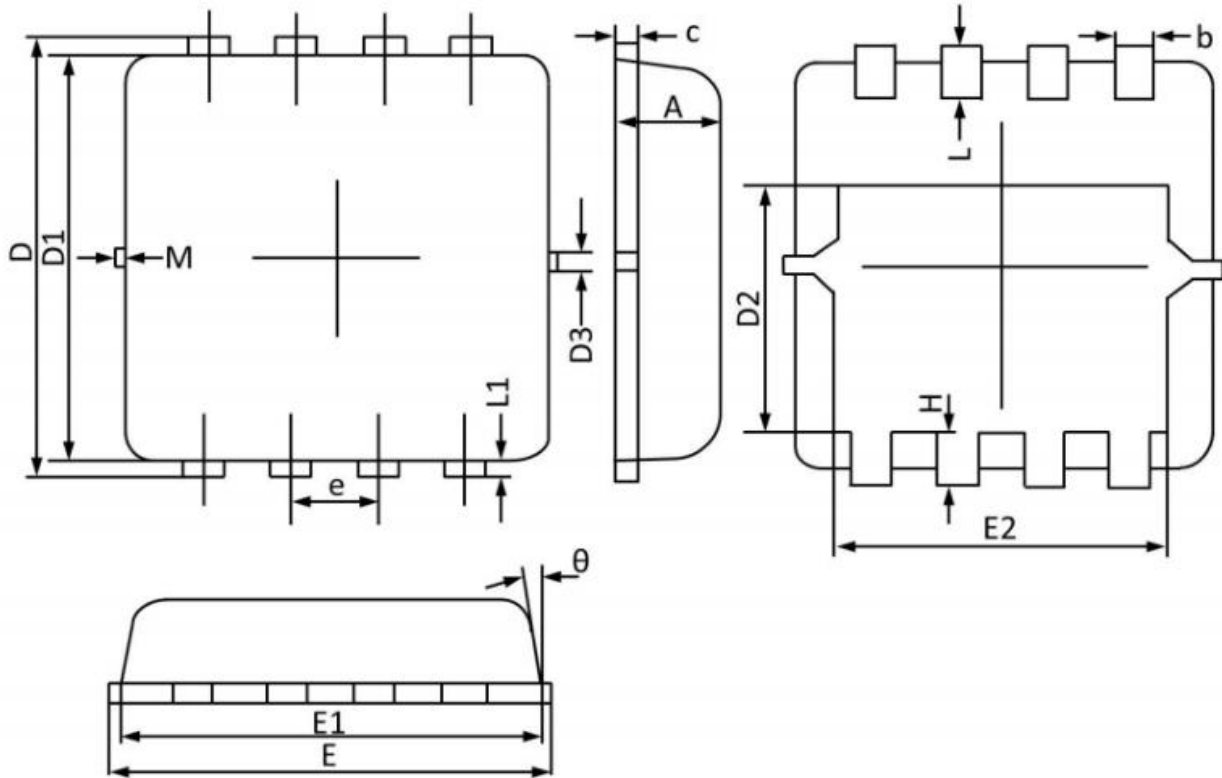


Fig11. Unclamped Inductive Test Circuit and waveforms

PDFN3*3 Package Information



DIMENSIONS (unit : mm)

Symbol	Min	Typ	Max	Symbol	Min	Typ	Max
A	0.70	0.75	0.80	b	0.25	0.30	0.35
C	0.10	0.15	0.25	D	3.25	3.35	3.45
D1	3.00	3.10	3.20	D2	1.78	1.88	1.98
D3	--	0.13	--	E	3.20	3.30	3.40
E1	3.00	3.15	3.20	E2	2.39	2.49	2.59
e	0.65BSC			H	0.30	0.39	0.50
L	0.30	0.40	0.50	L1	--	0.13	--
theta	--	10°	12°	M	*	*	0.15