

IRLML0060TRPbF

V_{DS}	60	V
V_{GS}	±16	V
$R_{DS(on) \text{ max}}$ (@ $V_{GS} = 10V$)	92	mΩ
$R_{DS(on) \text{ max}}$ (@ $V_{GS} = 4.5V$)	116	mΩ

FEATURES

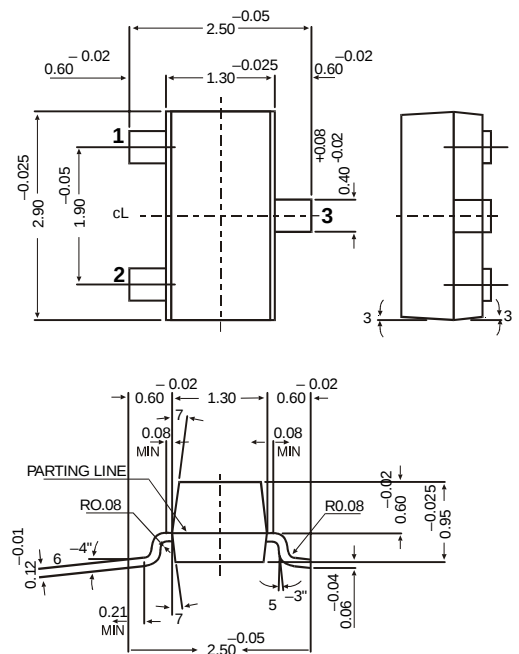
- Low $R_{DS(on)}$ ($\leq 92m\Omega$)
- Industry-standard pinout
- Compatible with existing Surface Mount Techniques
- RoHS compliant containing no lead, no bromide and no halogen
- MSL1, Industrial qualification

Benefits

- Lower switching losses
- Multi-vendor compatibility
- Easier manufacturing
- Environmentally friendly
- Increased reliability

Application(s)

- Load/ System Switch


SOT-23 Formed SMD Package

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	60	V
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	2.7	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	2.1	
I_{DM}	Pulsed Drain Current	11	
$P_D @ T_A = 25^\circ C$	Maximum Power Dissipation	1.25	W
$P_D @ T_A = 70^\circ C$	Maximum Power Dissipation	0.80	
	Linear Derating Factor	0.01	
V_{GS}	Gate-to-Source Voltage	± 16	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ③	—	100	°C/W
$R_{\theta JA}$	Junction-to-Ambient (t < 10s)	—	99	

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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.06	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	98	116	$m\Omega$	$V_{GS} = 4.5V, I_D = 2.2A$
		—	78	92		$V_{GS} = 10V, I_D = 2.7A$
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.5	V	$V_{DS} = V_{GS}, I_D = 25\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 60V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 60V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 16V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -16V$
R_G	Internal Gate Resistance	—	1.6	—	Ω	
g_{fs}	Forward Trans conductance	7.6	—	—	S	$V_{DS} = 25V, I_D = 2.7A$
Q_g	Total Gate Charge	—	2.5	—	nC	$I_D = 2.7A$
Q_{gs}	Gate-to-Source Charge	—	0.7	—		$V_{DS} = 30V$
Q_{gd}	Gate-to-Drain ('Miller') Charge	—	1.3	—		$V_{GS} = 4.5V$ ②
$t_{d(on)}$	Turn-On Delay Time	—	5.4	—	ns	$V_{DD} = 30V$ ②
t_r	Rise Time	—	6.3	—		$I_D = 1.0A$
$t_{d(off)}$	Turn-Off Delay Time	—	6.8	—		$R_G = 6.8\Omega$
t_f	Fall Time	—	4.2	—		$V_{GS} = 4.5V$
C_{iss}	Input Capacitance	—	290	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	37	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	21	—		$f = 1.0MHz$

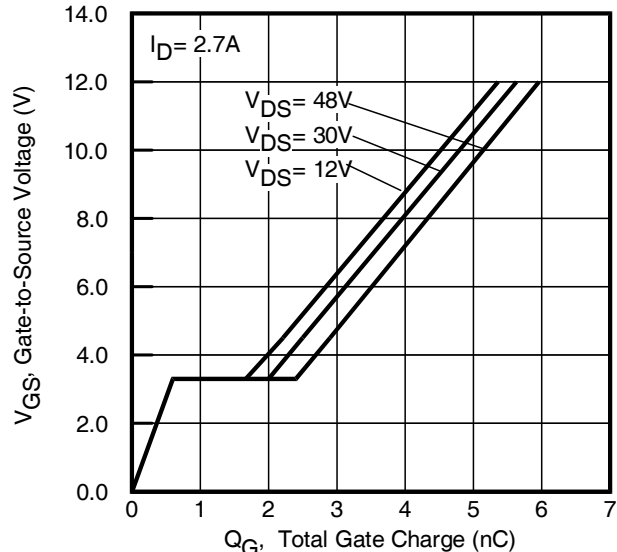
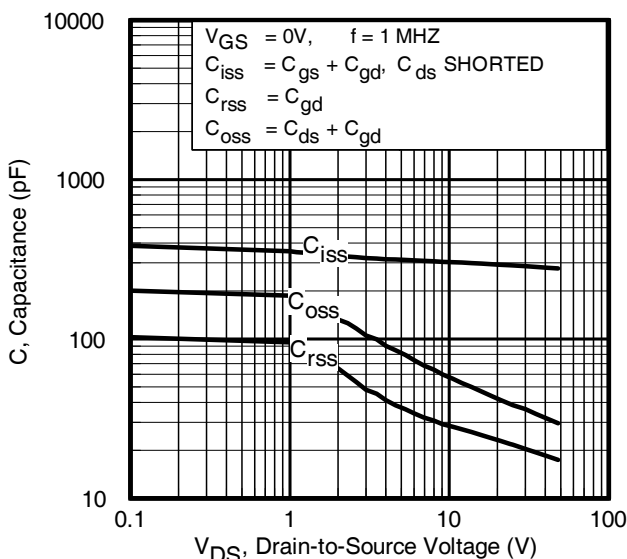
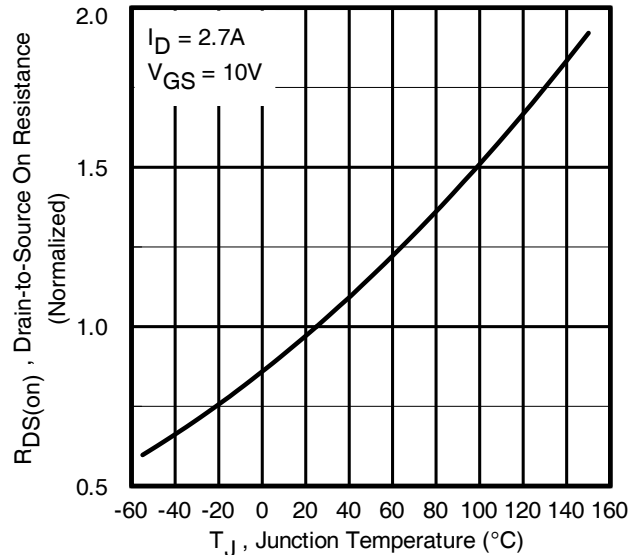
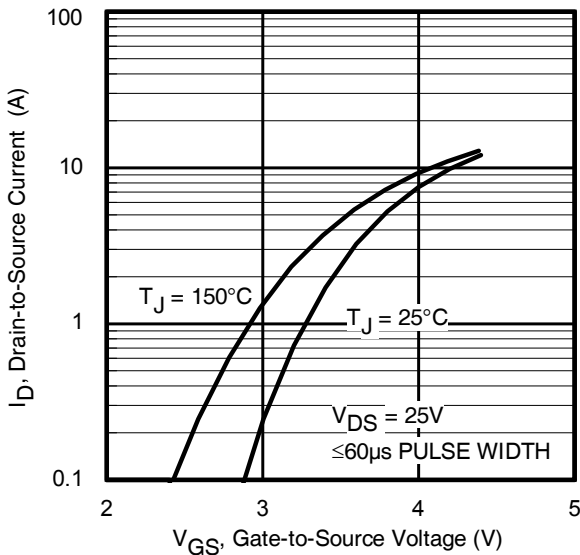
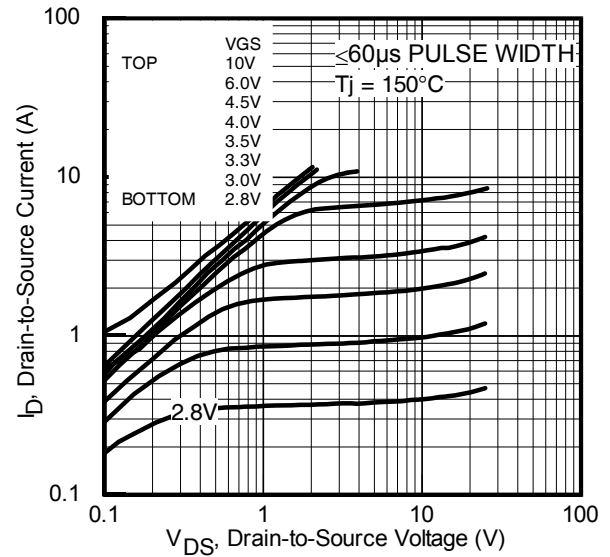
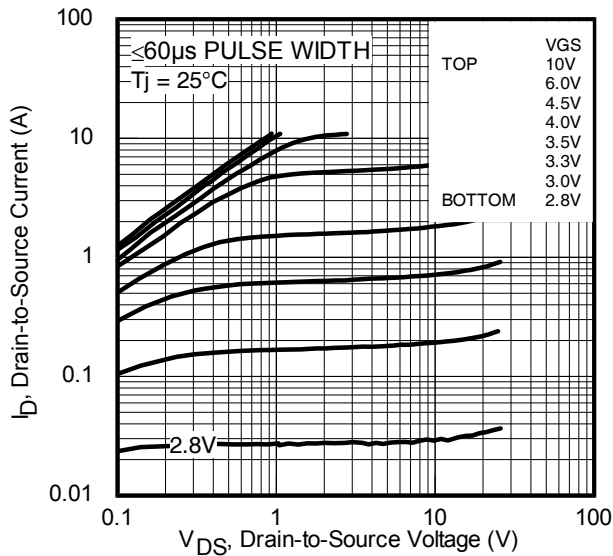
Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	1.6	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	11		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 2.7A, V_{GS} = 0V$ ②
t_{rr}	Reverse Recovery Time	—	14	21	ns	$T_J = 25^\circ\text{C}, V_R = 30V, I_F = 1.6A$
Q_{rr}	Reverse Recovery Charge	—	13	20	nC	

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
- ③ Surface mounted on 1 in square Cu board

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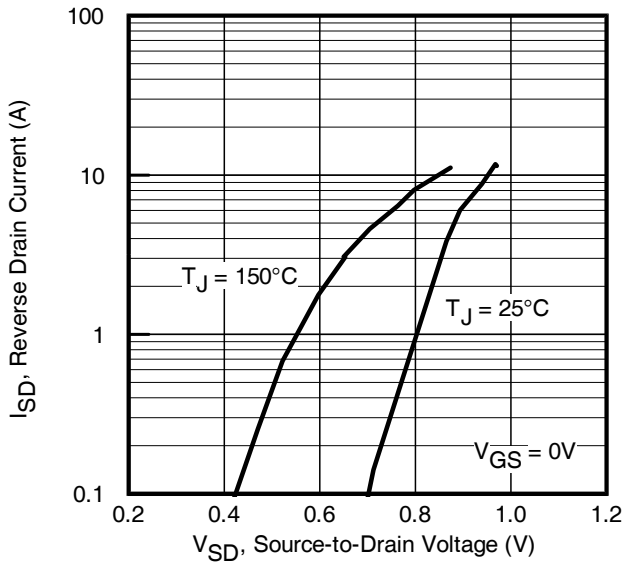


Fig. 7 Typical Source-to-Drain Diode Forward Voltage

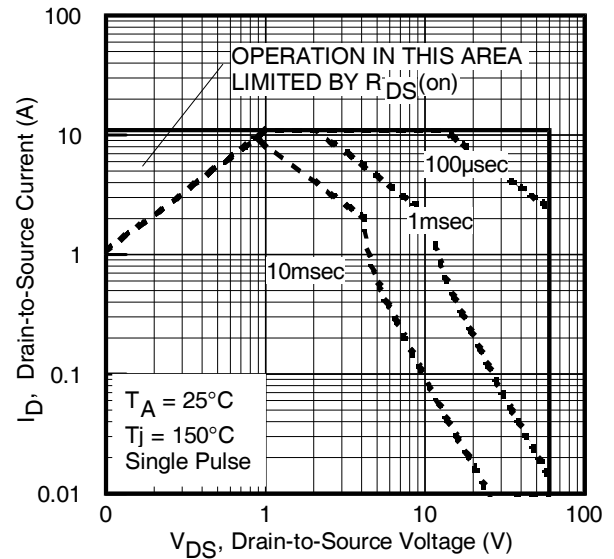


Fig. 8 Maximum Safe Operating Area

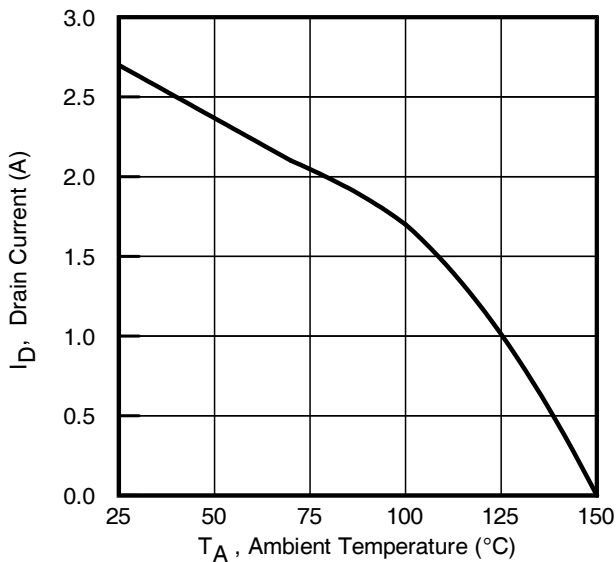


Fig. 9 Maximum Drain Current vs. Case Temperature

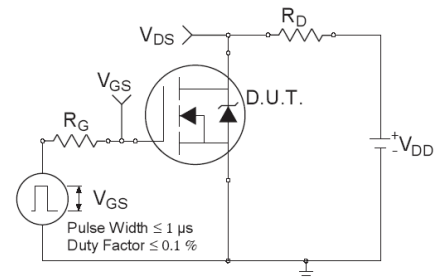


Fig. 10a. Switching Time Test Circuit

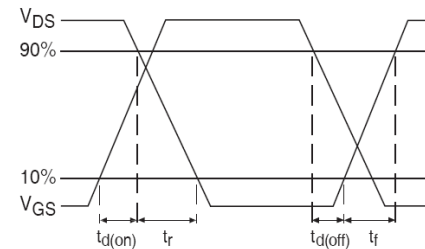


Fig. 10b. Switching Time Waveforms

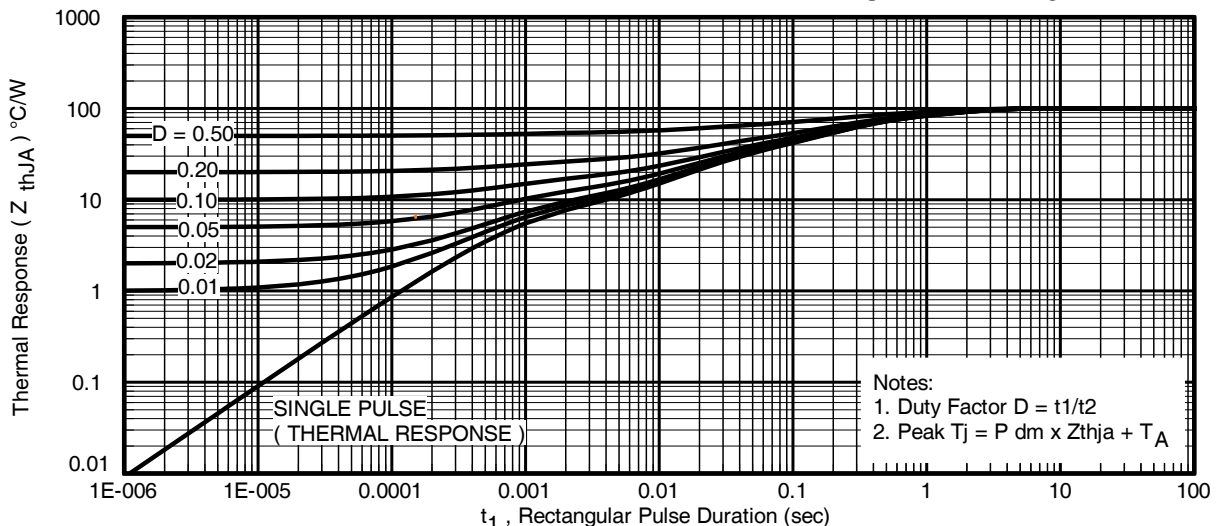


Fig. 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

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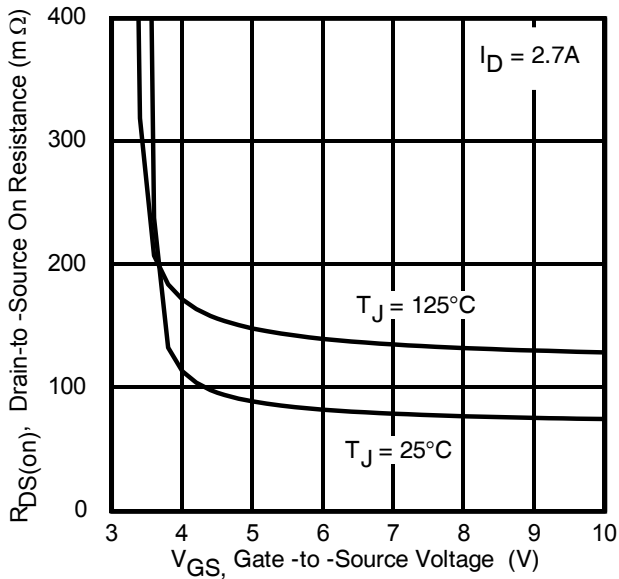


Fig 12. Typical On-Resistance Vs. Gate Voltage

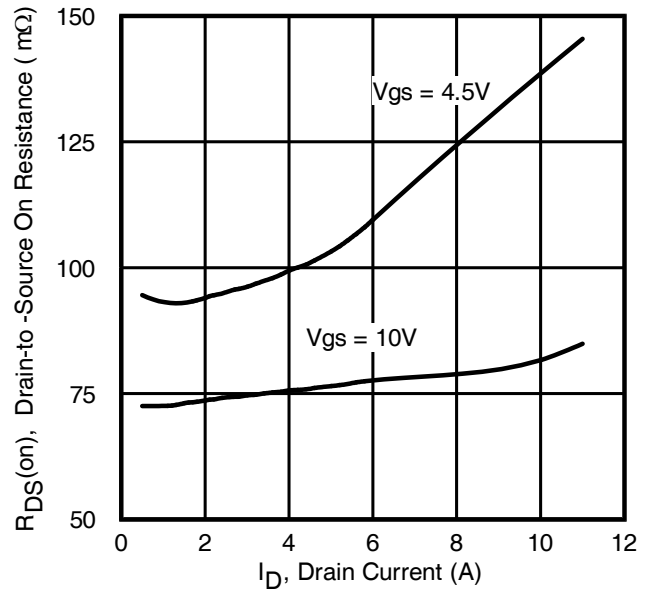


Fig 13. Typical On-Resistance Vs. Drain Current

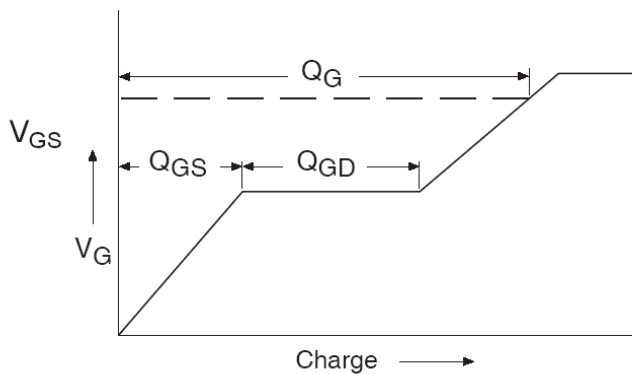


Fig 14a. Basic Gate Charge Waveform

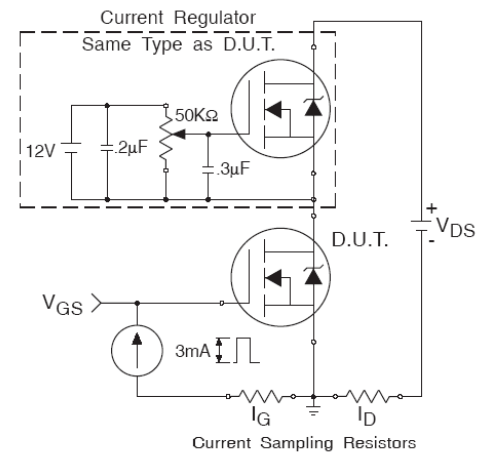


Fig 14b. Gate Charge Test Circuit

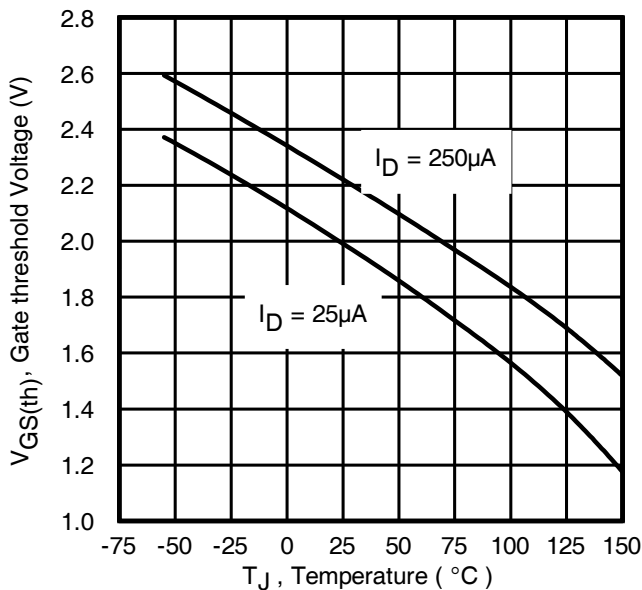


Fig 15. Typical Threshold Voltage Vs. Junction Temperature

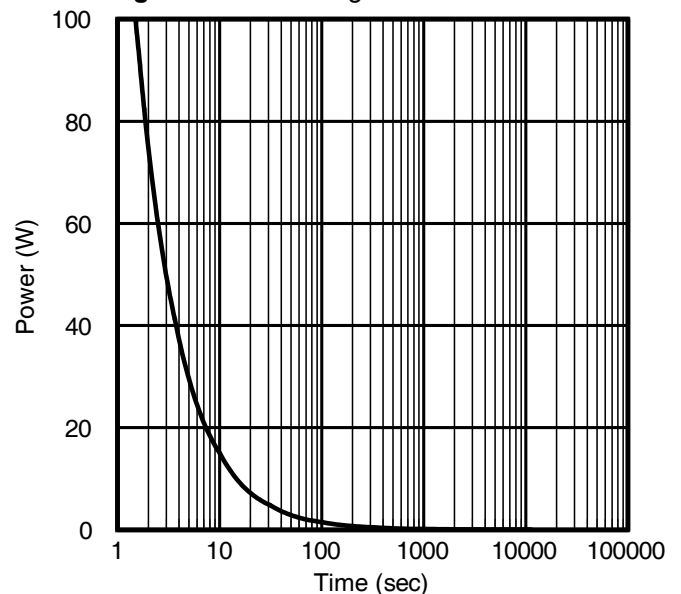


Fig 16. Typical Power Vs. Time