International IQR Rectifier

AUTOMOTIVE MOSFET

IRF1407PbF

HEXFET® Power MOSFET

Typical Applications
- Integrated Starter Alternator
- 42 Volts Automotive Electrical Systems
- Lead-Free

$V_{DSS} = 75V$
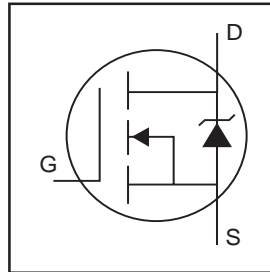
$R_{DS(on)} = 0.0078\Omega$

$I_D = 130A⑥$

Benefits
- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
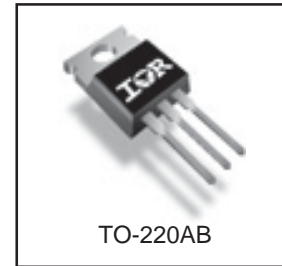- Repetitive Avalanche Allowed up to Tjmax

TO-220AB

Description

Specifically designed for Automotive applications, this Stripe Planar design of HEXFET® Power MOSFETs utilizes the lastest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this HEXFET power MOSFET are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These benefits combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	130⑥	
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	92⑥	A
I_{DM}	Pulsed Drain Current ①	520	
P_D @T_C = 25°C	Power Dissipation	330	W
	Linear Derating Factor	2.2	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	390	mJ
I_{AR}	Avalanche Current①	See Fig.12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche Energy⑦		mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.6	V/ns
T_J	Operating Junction and	-55 to + 175	
T_{STG}	Storage Temperature Range		°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	0.45	
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	——	°C/W
$R_{\theta JA}$	Junction-to-Ambient	——	62	

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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Parameter		Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	75	——	——	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.09	——	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	——	0.0078	Ω	V_{GS} = 10V, I_D = 78A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V_{DS} = 10V, I_D = 250µA
g_{fs}	Forward Transconductance	74	——	——	S	V_{DS} = 25V, I_D = 78A
I_{DSS}	Drain-to-Source Leakage Current	——	——	20	µA	V_{DS} = 75V, V_{GS} = 0V
		——	——	250		V_{DS} = 60V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	200	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-200		V_{GS} = -20V
Q_g	Total Gate Charge	——	160	250		I_D = 78A
Q_{gs}	Gate-to-Source Charge	——	35	52	nC	V_{DS} = 60V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	54	81		V_{GS} = 10V④
$t_{d(on)}$	Turn-On Delay Time	——	11	——		V_{DD} = 38V
t_r	Rise Time	——	150	——	ns	I_D = 78A
$t_{d(off)}$	Turn-Off Delay Time	——	150	——		R_G = 2.5Ω
t_f	Fall Time	——	140	——		V_{GS} = 10V ④
L_D	Internal Drain Inductance	——	4.5	——	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	——	7.5	——		
C_{iss}	Input Capacitance	——	5600	——		V_{GS} = 0V
C_{oss}	Output Capacitance	——	890	——	pF	V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	190	——		f = 1.0KHz, See Fig. 5
C_{oss}	Output Capacitance	——	5800	——		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0KHz
C_{oss}	Output Capacitance	——	560	——		V_{GS} = 0V, V_{DS} = 60V, f = 1.0KHz
C_{oss} eff.	Effective Output Capacitance ⑤	——	1100	——		V_{GS} = 0V, V_{DS} = 0V to 60V

Source-Drain Ratings and Characteristics

Parameter		Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	130⑥	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	520		
V_{SD}	Diode Forward Voltage	——	——	1.3	V	T_J = 25°C, I_S = 78A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	110	170	ns	T_J = 25°C, I_F = 78A
Q_{rr}	Reverse RecoveryCharge	——	390	590	nC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).

② Starting T_J = 25°C, L = 0.13mH
R_G = 25Ω, I_{AS} = 78A. (See Figure 12).

③ $I_{SD} \leq$ 78A, di/dt $\leq$ 320A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 175°C

④ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.

⑦ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
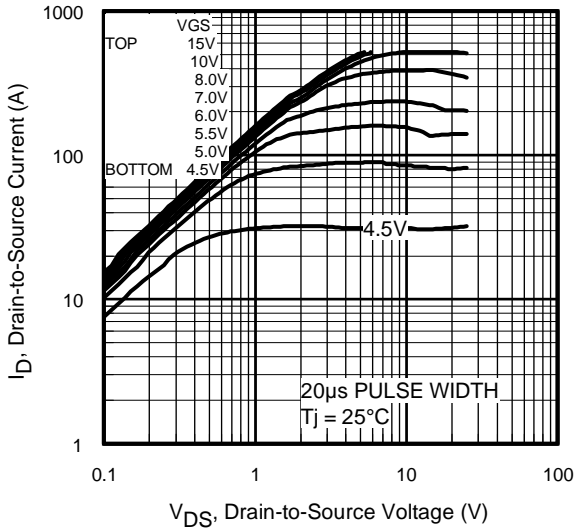
International **I⊕R** Rectifier

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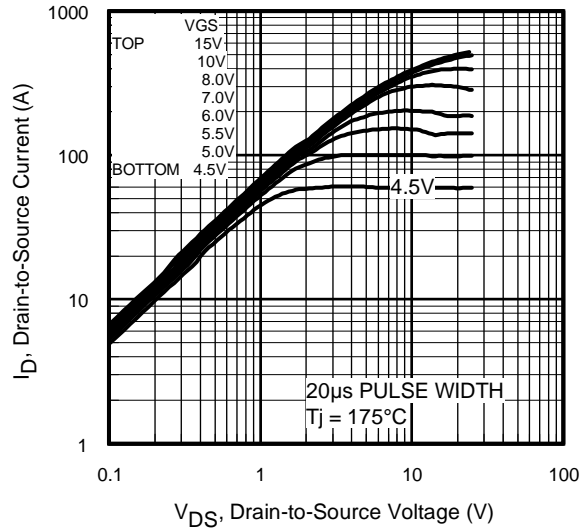
Fig 1. Typical Output Characteristics

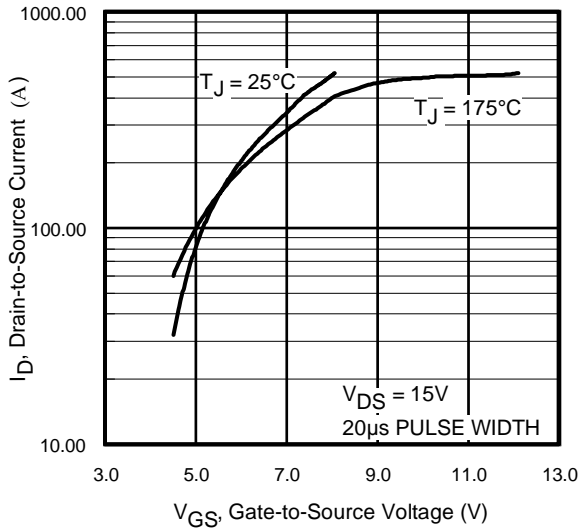**Fig 2.** Typical Output Characteristics

Fig 3. Typical Transfer Characteristics
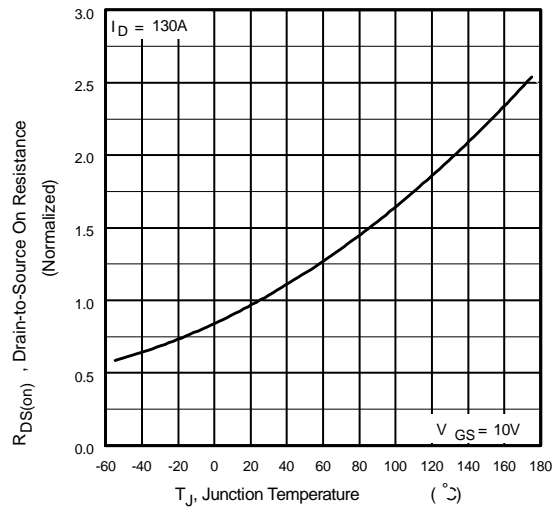

Fig 4. Normalized On-Resistance vs. Temperature
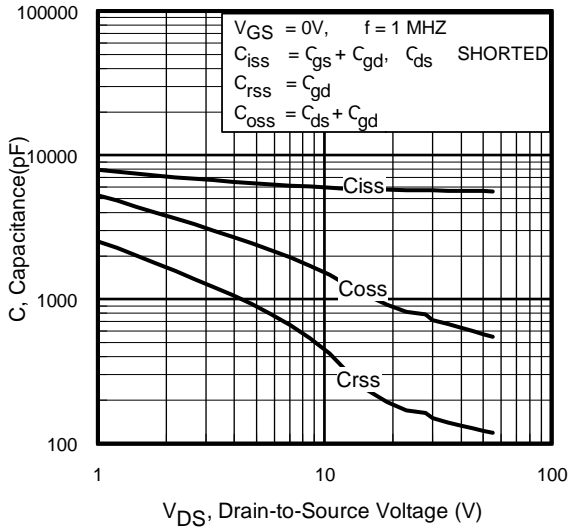
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Fig 5. Typical Capacitance vs.
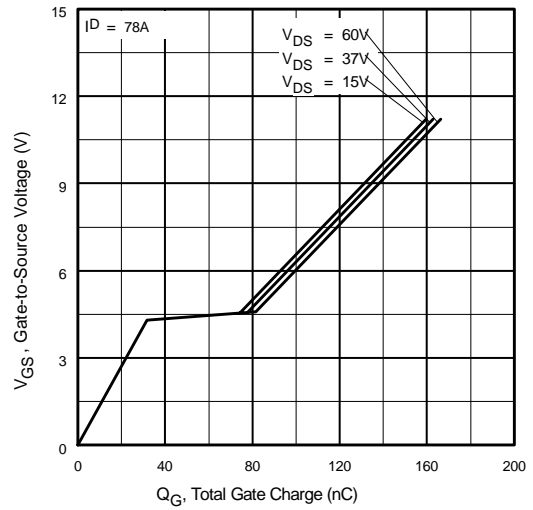Drain-to-Source Voltage

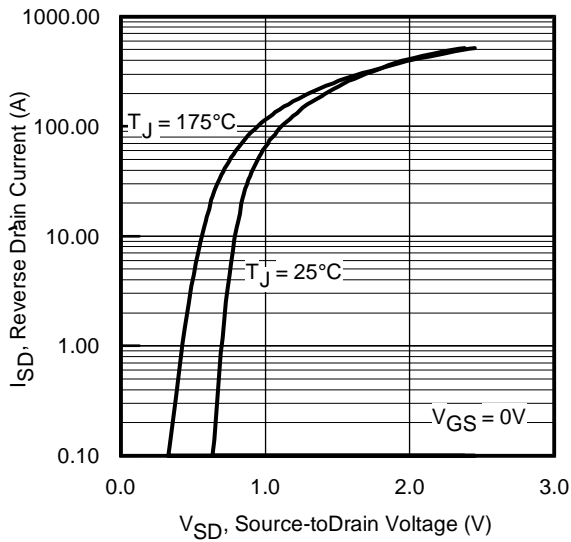**Fig 6.** Typical Gate Charge vs.
Gate-to-Source Voltage

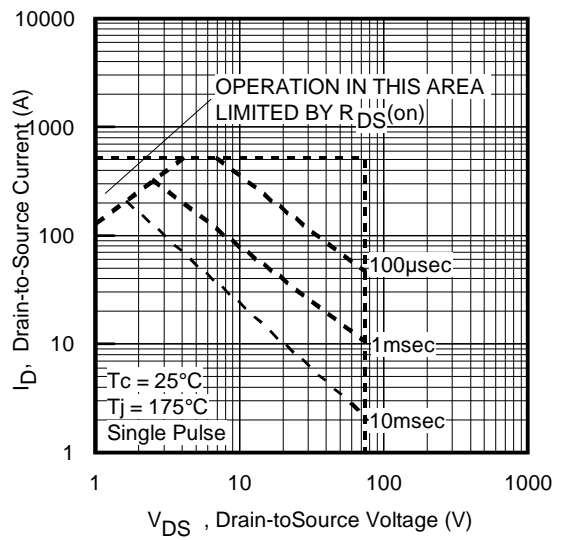**Fig 7.** Typical Source-Drain Diode
Forward Voltage

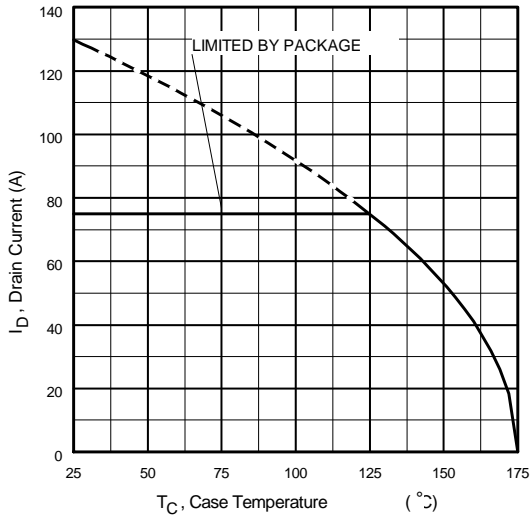**Fig 8.** Maximum Safe Operating Area

4

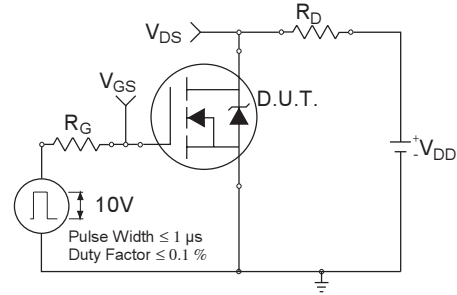**Fig 9.** Maximum Drain Current vs. Case Temperature

Fig 10a. Switching Time Test Circuit
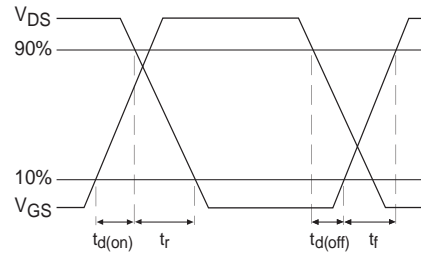

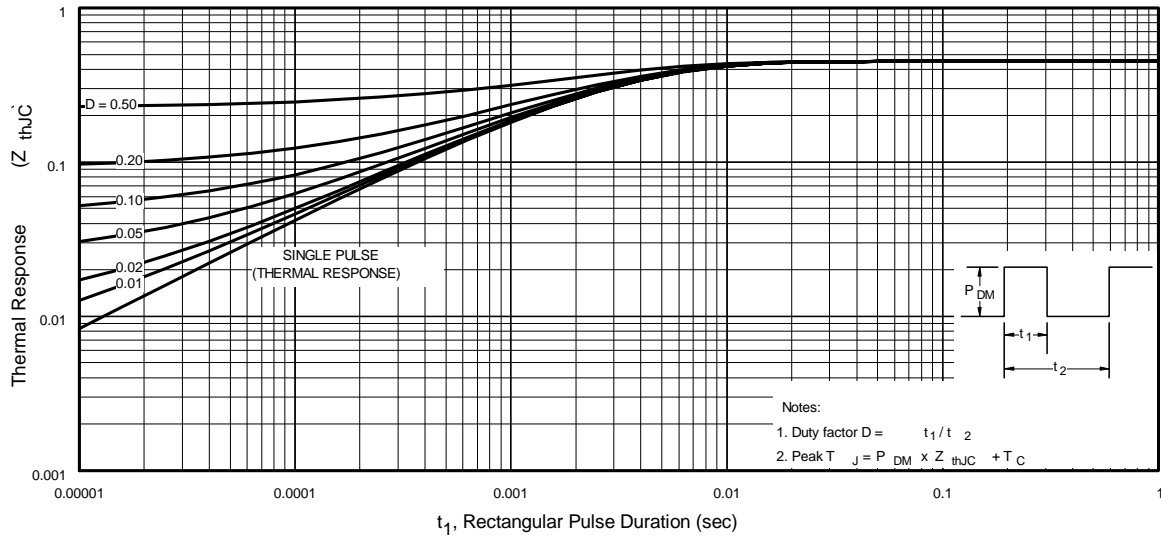**Fig 10b.** Switching Time Waveforms

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case
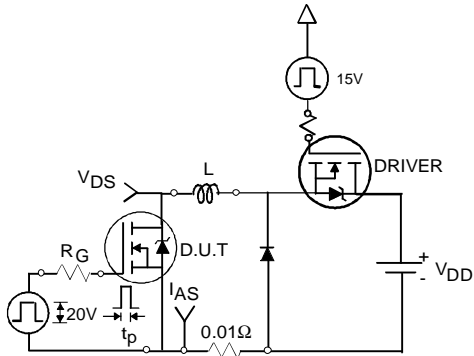
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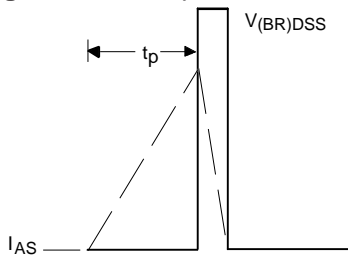**Fig 12a.** Unclamped Inductive Test Circuit

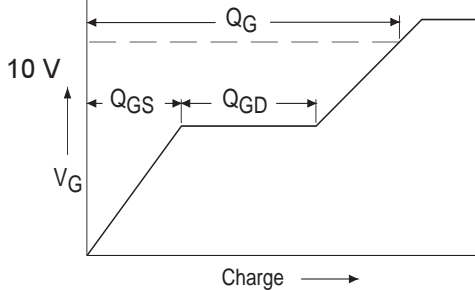**Fig 12b.** Unclamped Inductive Waveforms

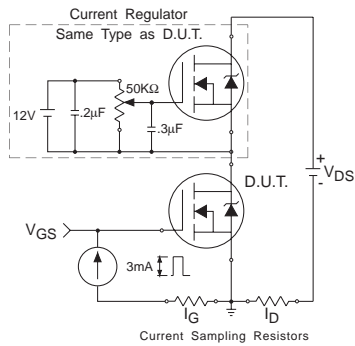**Fig 13a.** Basic Gate Charge Waveform

Fig 13b. Gate Charge Test Circuit

6

Fig 12c. Maximum Avalanche Energy
vs. Drain Current

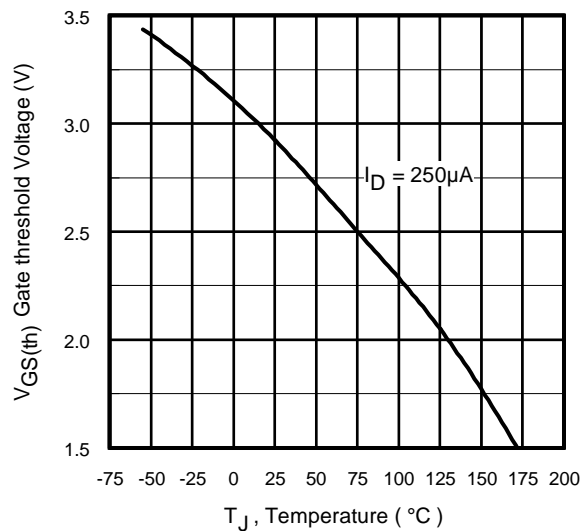**Fig 14.** Threshold Voltage vs. Temperature
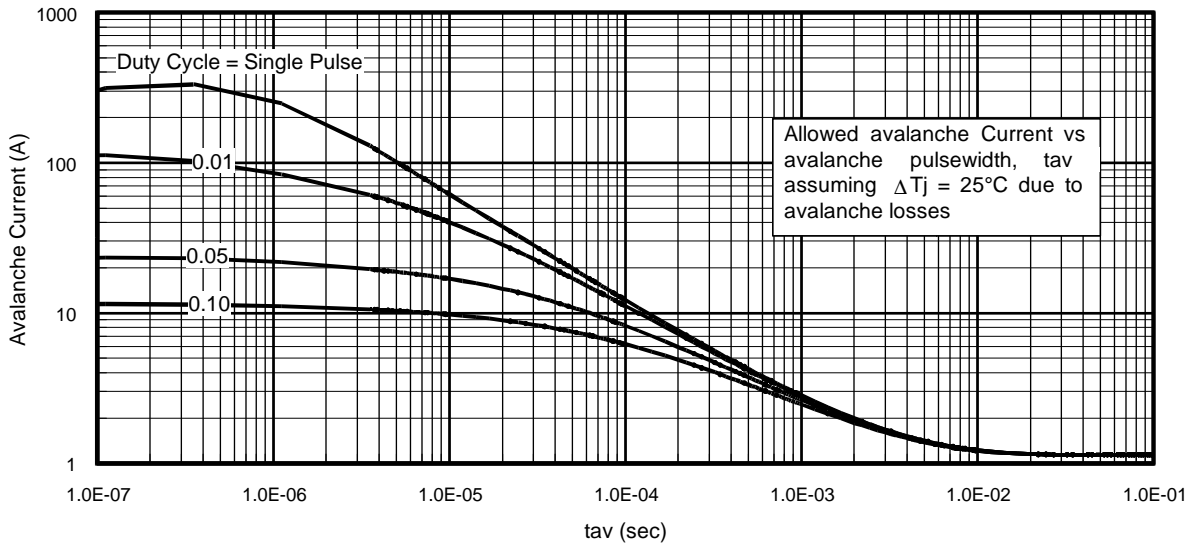www.irf.com

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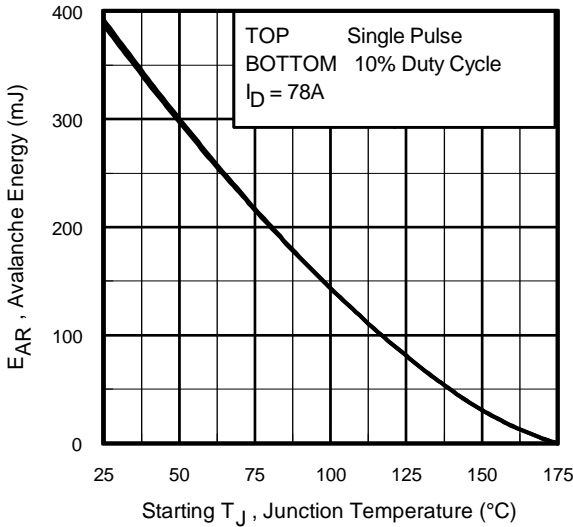**Fig 15.** Typical Avalanche Current vs.Pulsewidth

Fig 16. Maximum Avalanche Energy
vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)
1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a
   temperature far in excess of T_{jmax}. This is validated for
   every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is
   not exceeded.
3. Equation below based on circuit and waveforms shown in
   Figures 12a, 12b.
4. $P_{D (ave)}$ = Average power dissipation per single
   avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for
   voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed
   T_{jmax} (assumed as 25°C in Figure 15, 16).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
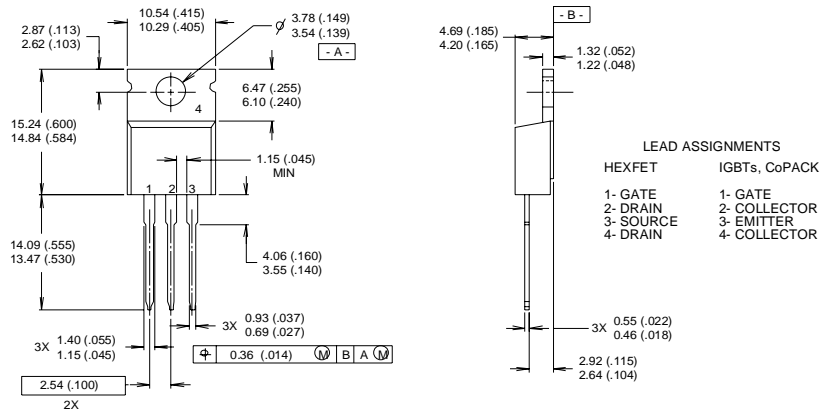 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D (ave)} = 1/2 \; (\; 1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS (AR)} = P_{D (ave)} \cdot t_{av}$$

Peak Diode Recovery dv/dt Test Circuit

D.U.T*

③

Circuit Layout Considerations
- Low Stray Inductance
- Ground Plane
- Low Leakage Inductance
  Current Transformer

②

④

①

R_G

- dv/dt controlled by R_G
- I_{SD} controlled by Duty Factor "D"
- D.U.T. - Device Under Test

V_{GS}

V_{DD}

* Reverse Polarity of D.U.T for P-Channel

① Driver Gate Drive

$$D = \frac{P.W.}{Period}$$

P.W.

Period

$[V_{GS}=10V]$ ***

② D.U.T. I_{SD} Waveform

Reverse
Recovery
Current

Body Diode Forward
Current

di/dt

③ D.U.T. V_{DS} Waveform

Diode Recovery
dv/dt

$[V_{DD}]$

Re-Applied
Voltage

Body Diode Forward Drop

④ Inductor Curent

Ripple ≤ 5%

$[I_{SD}]$

*** V_{GS} = 5.0V for Logic Level and 3V Drive Devices

Fig 17. For N-channel HEXFET® power MOSFETs

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)

LEAD ASSIGNMENTS

HEXFET	IGBTs, CoPACK
1- GATE	1- GATE
2- DRAIN	2- COLLECTOR
3- SOURCE	3- EMITTER
4- DRAIN	4- COLLECTOR

NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH

3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead-Free"

INTERNATIONAL RECTIFIER LOGO

PART NUMBER

DATE CODE
YEAR 7 = 1997
WEEK 19
LINE C

ASSEMBLY LOT CODE

Data and specifications subject to change without notice.
This product has been designed and qualified for the Automotive [Q101] market.
Qualification Standards can be found on IR's Web site.

International **IQR** Rectifier

Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/