KSZ8041TL/FTL/MLL

10BASE-T/100BASE-TX/100BASE-FX Physical Layer Transceiver

Features

- Single-Chip 10BASE-T/100BASE-TX/100BASE-FX Physical Layer Solution
- Fully Compliant with IEEE 802.3u Standard
- Low Power CMOS Design, Power Consumption of <180 mW
- HP Auto MDI/MDI-X for Reliable Detection and Correction for Straight-Through and Crossover Cables with Disable and Enable Option
- Robust Operation Over Standard Cables
- LinkMD® TDR-Based Cable Diagnostics for Identification of Faulty Copper Cabling
- Power Down and Power Saving Modes
- Fiber Support: 100BASE-FX (KSZ8041FTL Only)
- Back-to-Back Mode Support for 100 Mbps Repeater or Media Converter
- MII Interface Support
- RMII Interface Support with External 50 MHz System Clock (KSZ8041TL/FTL Only)
- SMII Interface Support with External 125 MHz System Clock and 12.5 MHz Sync Clock from MAC (KSZ8041TL/FTL Only)
- MIIM (MDC/MDIO) Management Bus to 12.5 MHz for Rapid PHY Register Configuration
- Interrupt Pin Option
- Programmable LED Outputs for Link, Activity, and Speed
- Single Power Supply (3.3V)
- Built-in 1.8V Regulator for Core
- Available in 48-Pin LQFP (KSZ8041MLL) or 48-Pin TQFP (KSZ8041TL/FTL) Packages

Applications

- Printer
- LOM
- Game Console
- IPTV
- IP Phone
- IP Set-Top Box
- Media Converter

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Table of Contents

1.0 INTRODUCTION

1.1 General Description

The KSZ8041TL is a single supply 10BASE-T/100BASE-TX Physical Layer Transceiver that provides MII/RMII/SMII interfaces to transmit and receive data. It utilizes a unique mixed-signal design to extend signaling distance while reducing power consumption.

HP Auto MDI/MDI-X provides the most robust solution for eliminating the need to differentiate between crossover and straight-through cables.

LinkMD® TDR-based cable diagnostics permit identification of faulty copper cabling.

The KSZ8041TL represents a new level of features and performance and is an ideal choice of physical layer transceiver for 10BASE-T/100BASE-TX applications.

The KSZ8041FTL has all the identical rich features of the KSZ8041TL plus 100BASE-FX support for fiber and media converter applications.

The KSZ8041MLL is the basic 10BASE-T/100BASE-TX physical layer transceiver version with MII support.

The KSZ8041TL and KSZ8041FTL are available in 48-pin, lead-free TQFP packages. The KSZ8041MLL is provided in the 48-pin, lead-free LQFP package.

FIGURE 1-1: SYSTEM BLOCK DIAGRAM, KSZ8041TL/FTL

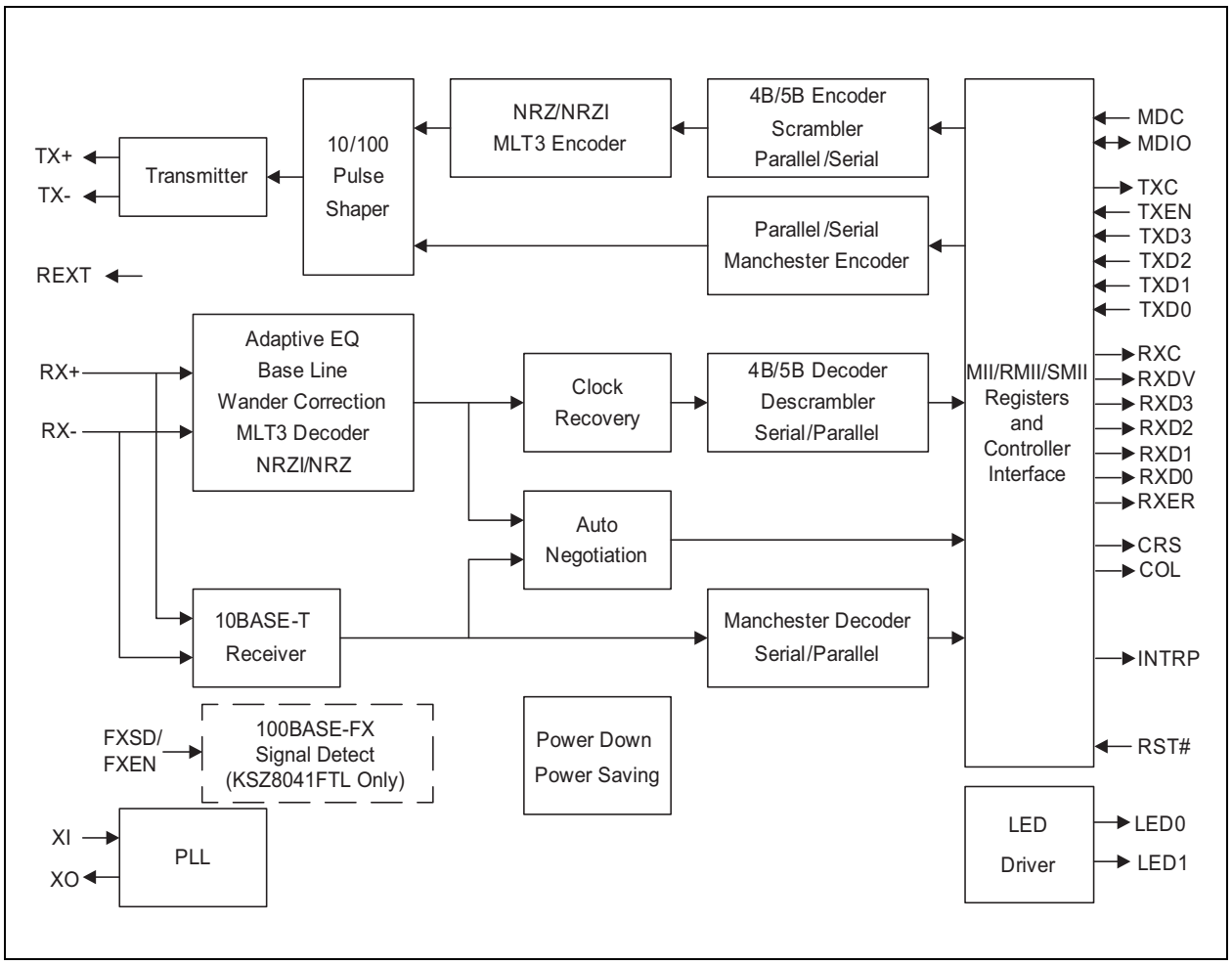
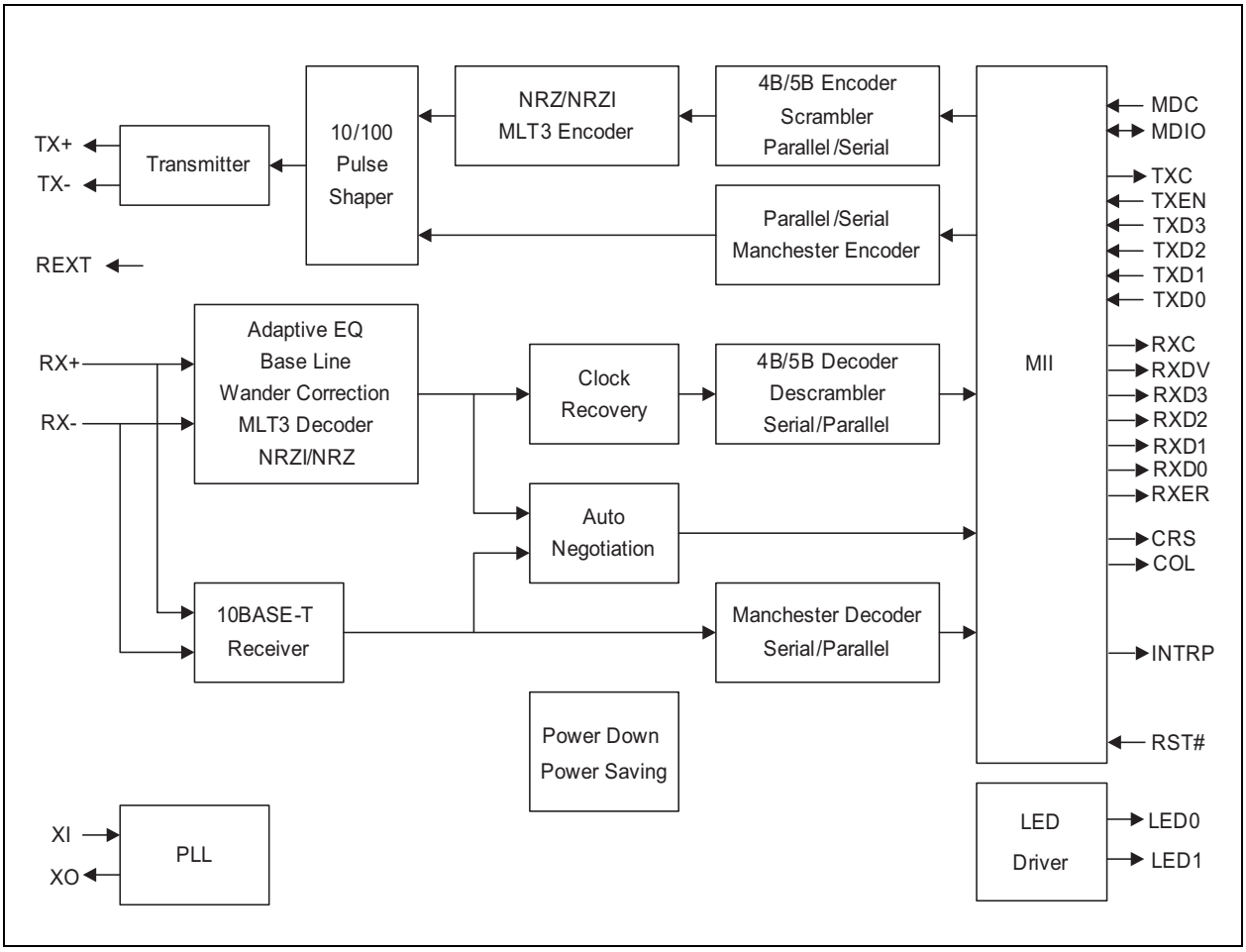


FIGURE 1-2: SYSTEM BLOCK DIAGRAM, KSZ8041MLL



2.0 PIN DESCRIPTION AND CONFIGURATION

FIGURE 2-1: KSZ8041TL 48-PIN TQFP ASSIGNMENT, (TOP VIEW)

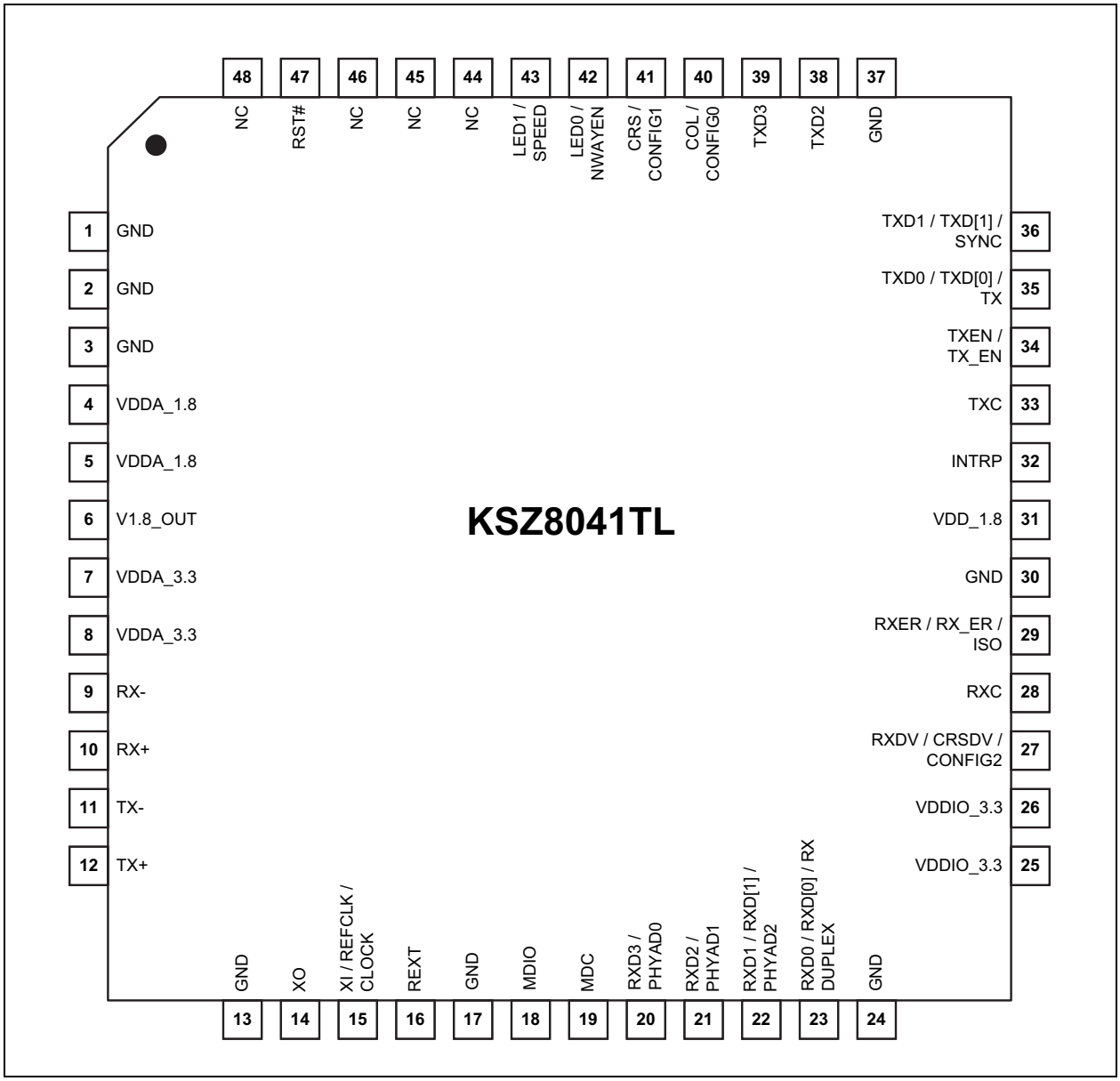


FIGURE 2-2: KSZ8041FTL 48-PIN TQFP ASSIGNMENT, (TOP VIEW)

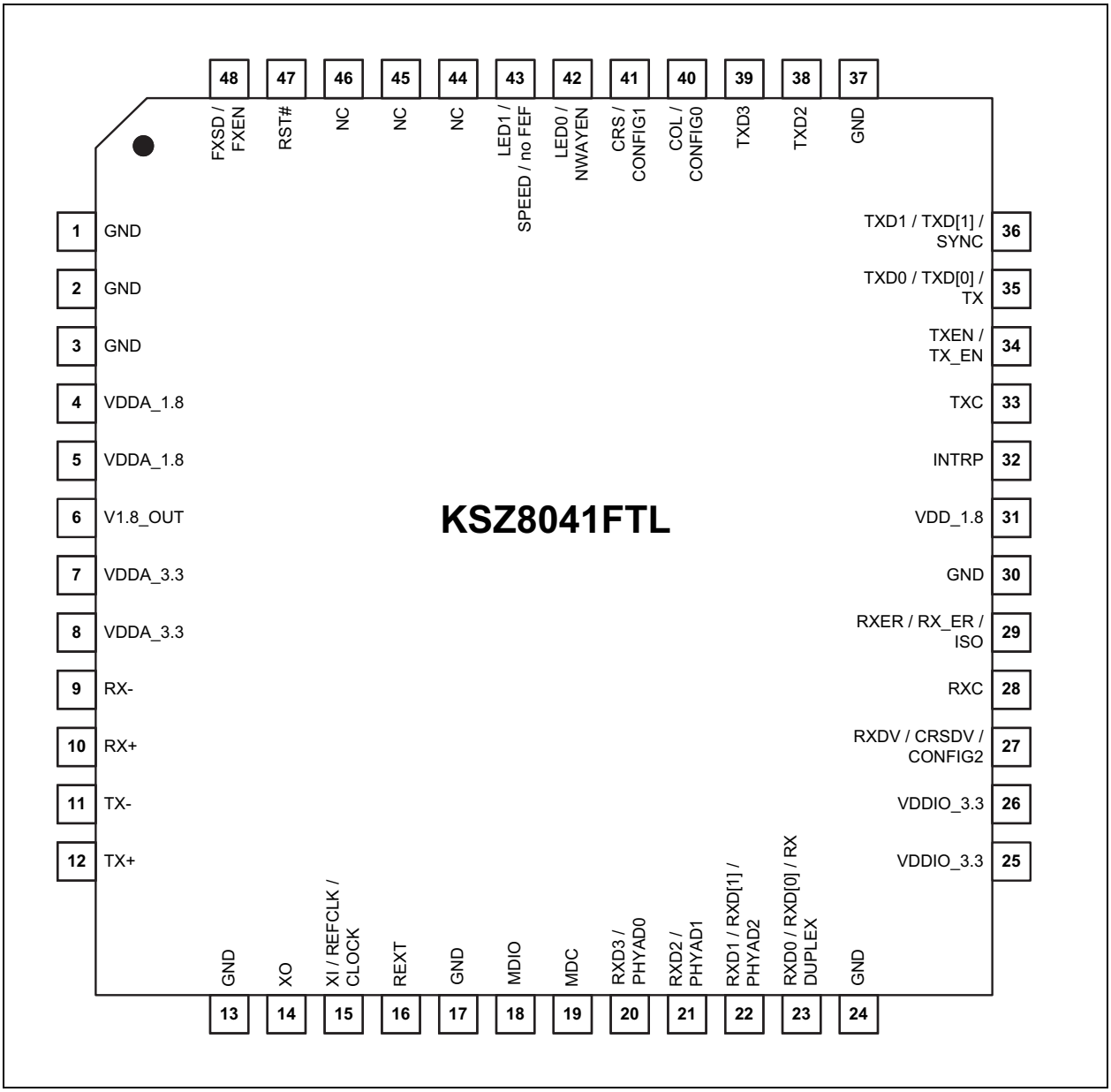


TABLE 2-1: SIGNALS FOR KSZ8041TL/FTL

Pin Number	Pin Name	Type (Note 2-1)	Description
1	GND	GND	Ground
2	GND	GND	Ground
3	GND	GND	Ground
4	VDDA_1.8	P	1.8V analog V_{DD}
5	VDDA_1.8	P	1.8V analog V_{DD}
6	V1.8_OUT	P	1.8V output voltage from chip
7	VDDA_3.3	P	3.3V analog V_{DD}
8	VDDA_3.3	P	3.3V analog V_{DD}
9	RX–	I/O	Physical receive or transmit signal (– differential)
10	RX+	I/O	Physical receive or transmit signal (+ differential)
11	TX–	I/O	Physical transmit or receive signal (– differential)
12	TX+	I/O	Physical transmit or receive signal (+ differential)
13	GND	GND	Ground
14	XO	O	Crystal feedback This pin is used only in MII mode when a 25 MHz crystal is used. This pin is a no connect if oscillator or external clock source is used, or if RMII mode or SMII mode is selected.
15	XI/REFCLK/ CLOCK	I	Crystal/Oscillator/External Clock Input MII Mode: 25 MHz ±50 ppm (crystal, oscillator, or external clock) RMII Mode: 50 MHz ±50 ppm (oscillator, or external clock only) SMII Mode: 125 MHz ±100 ppm (oscillator, or external clock only)
16	REXT	I/O	Set physical transmit output current Connect a 6.49 kΩ resistor in parallel with a 100 pF capacitor to ground on this pin. See KSZ8041TL-FTL reference schematics.
17	GND	GND	Ground
18	MDIO	I/O	Management Interface (MII) Data I/O This pin requires an external 4.7 kΩ pull-up resistor.
19	MDC	I	Management Interface (MII) Clock Input This pin is synchronous to the MDIO data interface.
20	RXD3/ PHYAD0	Ipu/O	MII Mode: Receive Data Output[3](Note 2-2) Config. Mode: The pull-up/pull-down value is latched as PHYADDR[0] during power-up/reset. See Table 2-2 for details.
21	RXD2/ PHYAD1	Ipd/O	MII Mode: Receive Data Output[2](Note 2-2) Config. Mode: The pull-up/pull-down value is latched as PHYADDR[1] during power-up/reset. See Table 2-2 for details.

TABLE 2-1: SIGNALS FOR KSZ8041TL/FTL (CONTINUED)

Pin Number	Pin Name	Type (Note 2-1)	Description
22	RXD1/ RXD[1]/ PHYAD2	Ipd/O	MII Mode: Receive Data Output[1](Note 2-2) RMII Mode: Receive Data Output[1](Note 2-3) Config. Mode: The pull-up/pull-down value is latched as PHYADDR[2] during power-up/reset. See Table 2-2 for details.
23	RXD0/ RXD[0]/ RX DUPLEX	Ipu/O	MII Mode: Receive Data Output[0](Note 2-2) RMII Mode: Receive Data Output[0](Note 2-3) SMII Mode: Receive Data and Control(Note 2-4) Config. Mode: Latched as DUPLEX (register 0h, bit 8) during power-up/reset. See Table 2-2 for details.
24	GND	GND	Ground
25	VDDIO_3.3	P	3.3V digital V_{DD}
26	VDDIO_3.3	P	3.3V digital V_{DD}
27	RXDV/ CRSDV/ CONFIG2	Ipd/O	MII Mode: Receive Data Valid Output RMII Mode: Carrier Sense/Receive Data Valid Output Config. Mode: The pull-up/pull-down value is latched as CONFIG2 during power-up/reset. See Table 2-2 for details.
28	RXC	O	MII Mode: Receive Clock Output.
29	RXER/ RX_ER/ ISO	Ipd/O	MII Mode: Receive Error Output RMII Mode: Receive Error Output Config. Mode: The pull-up/pull-down value is latched as ISOLATE during power-up/reset. See Table 2-2 for details.
30	GND	GND	Ground
31	VDD_1.8	P	1.8V digital V_{DD}
32	INTRP	Opu	Interrupt Output: Programmable Interrupt Output Register 1Bh is the Interrupt Control/Status Register for programming the interrupt conditions and reading the interrupt status. Register 1Fh bit 9 sets the interrupt output to active-low (default) or active-high.
33	TXC	I/O	MII Mode: Transmit Clock Output MII Back-to-Back Mode: Transmit Clock Input
34	TXEN/ TX_EN	I	MII Mode: Transmit Enable Input RMII Mode: Transmit Enable Input
35	TXD0/ TXD[0]/ TX	I	MII Mode: Transmit Data Input[0](Note 2-5) RMII Mode: Transmit Data Input[0](Note 2-6) SMII Mode: Transmit Data and Control(Note 2-7)
36	TXD1/ TXD[1]/ SYNC	I	MII Mode: Transmit Data Input[1](Note 2-5) RMII Mode: Transmit Data Input[1](Note 2-6) SMII Mode: SYNC Clock Input
37	GND	GND	Ground
38	TXD2	I	MII Mode: Transmit Data Input[2](Note 2-5)
39	TXD3	I	MII Mode: Transmit Data Input[3](Note 2-5)

TABLE 2-1: SIGNALS FOR KSZ8041TL/FTL (CONTINUED)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type (Note 2-1)</th><th>Description</th></tr>
<tr><td>40</td><td>COL/
CONFIG0</td><td>Ipd/O</td><td>MII Mode: Collision Detect Output
Config. Mode: The pull-up/pull-down value is latched as CONFIG0 during power-up/reset. See Table 2-2 for details.</td></tr>
<tr><td>41</td><td>CRS/
CONFIG1</td><td>Ipd/O</td><td>MII Mode: Carrier Sense Output
Config. Mode: The pull-up/pull-down value is latched as CONFIG1 during power-up/reset. See Table 2-2 for details.</td></tr>
<tr><td rowspan="11">42
(TL)</td><td rowspan="11">LED0/
NWAYEN</td><td rowspan="11">Ipu/O</td><td>LED Output: Programmable LED0 Output
Config. Mode: Latched as Auto-Negotiation Enable (register 0h, bit 12) during power-up/reset. See Table 2-2 for details.
The LED0 pin is programmable via register 1Eh bits [15:14], and is defined as follows:</td></tr>
<tr><td>LED Mode = [00]</td></tr>
<tr><td>
<table>
<tr><th>Link/Activity</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No Link</td><td>High</td><td>OFF</td></tr>
<tr><td>Link</td><td>Low</td><td>ON</td></tr>
<tr><td>Activity</td><td>Toggle</td><td>Blinking</td></tr>
</table>
</td></tr>
<tr><td>LED Mode = [01]</td></tr>
<tr><td>
<table>
<tr><th>Link</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No Link</td><td>High</td><td>OFF</td></tr>
<tr><td>Link</td><td>Low</td><td>ON</td></tr>
</table>
</td></tr>
<tr><td>LED Mode = [10]: Reserved</td></tr>
<tr><td>LED Mode = [11]: Reserved</td></tr>
</table>

TABLE 2-1: SIGNALS FOR KSZ8041TL/FTL (CONTINUED)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type (Note 2-1)</th><th>Description</th></tr>
<tr><td rowspan="13">42
(FTL)</td><td rowspan="13">LED0/
NWAYEN</td><td rowspan="13">Ipu/O</td><td colspan="3">LED Output: Programmable LED0 Output
Config. Mode: If copper mode (FXEN=0), latched as Auto-Negotiation Enable (register 0h, bit 12) during power-up/reset. If fiber mode (FXEN=1), this pin configuration is always strapped to disable Auto-Negotiation. See Table 2-2 for details.
The LED0 pin is programmable via register 1Eh bits [15:14], and is defined as follows:</td></tr>
<tr><td colspan="3">LED Mode = [00]</td></tr>
<tr><td>Link/Activity</td><td>Pin State</td><td>LED Definition</td></tr>
<tr><td>No Link</td><td>High</td><td>OFF</td></tr>
<tr><td>Link</td><td>Low</td><td>ON</td></tr>
<tr><td>Activity</td><td>Toggle</td><td>Blinking</td></tr>
<tr><td colspan="3">LED Mode = [01]</td></tr>
<tr><td>Link</td><td>Pin State</td><td>LED Definition</td></tr>
<tr><td>No Link</td><td>High</td><td>OFF</td></tr>
<tr><td>Link</td><td>Low</td><td>ON</td></tr>
<tr><td colspan="3">LED Mode = [10]: Reserved</td></tr>
<tr><td colspan="3">LED Mode = [11]: Reserved</td></tr>
<tr><td rowspan="13">43
(TL)</td><td rowspan="13">LED1/SPEED</td><td rowspan="13">Ipu/O</td><td colspan="3">LED Output: Programmable LED1 Output
Config. Mode: Latched as SPEED (register 0h, bit 13) during power-up/reset. See Table 2-2 for details.
The LED1 pin is programmable via register 1Eh bits [15:14], and is defined as follows:</td></tr>
<tr><td colspan="3">LED mode = [00]</td></tr>
<tr><td>Speed</td><td>Pin State</td><td>LED Definition</td></tr>
<tr><td>10BT</td><td>High</td><td>OFF</td></tr>
<tr><td>100BT</td><td>Low</td><td>ON</td></tr>
<tr><td colspan="3">LED mode = [01]</td></tr>
<tr><td>Activity</td><td>Pin State</td><td>LED Definition</td></tr>
<tr><td>No Activity</td><td>High</td><td>OFF</td></tr>
<tr><td>Activity</td><td>Toggle</td><td>Blinking</td></tr>
<tr><td colspan="3">LED Mode = [10]: Reserved</td></tr>
<tr><td colspan="3">LED Mode = [11]: Reserved</td></tr>
</table>

TABLE 2-1: SIGNALS FOR KSZ8041TL/FTL (CONTINUED)

Pin Number	Pin Name	Type (Note 2-1)	Description
43 (FTL)	LED1/SPEED no FEF	Ipu/O	LED Output: Programmable LED1 Output Config. Mode: If copper mode (FXEN=0), latched as SPEED (register 0h, bit 13) during power-up/reset. If fiber mode (FXEN=1), latched as no FEF (no Far-End Fault) during power-up/reset. See Table 2-2 for details. The LED1 pin is programmable via register 1Eh bits [15:14], and is defined as follows:
			LED mode = [00]
			Speed / **Pin State** / **LED Definition**
			10BT / High / OFF
			100BT / Low / ON
			LED mode = [01]
			Activity / **Pin State** / **LED Definition**
			No Activity / High / OFF
			Activity / Toggle / Blinking
			LED Mode = [10]: Reserved
			LED Mode = [11]: Reserved
44	NC	—	No connect
45	NC	—	No connect
46	NC	—	No connect
47	RST#	I	Chip reset (active-low)
48 (TL)	NC	—	No connect
48 (FTL)	FXSD/FXEN	Ipd	FXSD: Signal Detect for 100BASE-FX fiber mode FXEN: Fiber Enable for 100BASE-FX fiber mode If FXEN=0, fiber mode is disabled. PHY is in copper mode. The default is “0”. See “100BASE-FX Operation” section for details.

Note 2-1 P = power supply
GND = ground
I = input
O = output
I/O = bi-directional
Ipu/O = Input with internal pull-up (40 kΩ ±30%) during power-up/reset; output pin otherwise.
Ipd/O = Input with internal pull-down (40 kΩ ±30%) during power-up/reset; output pin otherwise.
Ipu = Input with internal pull-up. (40 kΩ ±30%)
Ipd = Input with internal pull-down. (40 kΩ ±30%)
Opu = Output with internal pull-up. (40 kΩ ±30%)

Note 2-2 MII Rx Mode: The RXD[3..0] bits are synchronous with RXCLK. When RXDV is asserted, RXD[3..0] presents valid data to MAC through the MII. RXD[3..0] is invalid when RXDV is de-asserted.

Note 2-3 RMII Rx Mode: The RXD[1:0] bits are synchronous with REF_CLK. For each clock period in which CRS_DV is asserted, two bits of recovered data are sent from the PHY.

Note 2-4 SMII Rx Mode: Receive data and control information are sent in 10 bit segments. In 100 MBit mode, each segment represents a new byte of data. In 10 MBit mode, each segment is repeated ten times; therefore, every ten segments represent a new byte of data. The MAC can sample any one of every 10 segments in 10 MBit mode.

Note 2-5 MII Tx Mode: The TXD[3..0] bits are synchronous with TXCLK. When TXEN is asserted, TXD[3..0] presents valid data from the MAC through the MII. TXD[3..0] has no effect when TXEN is de-asserted.

Note 2-6 RMII Tx Mode: The TXD[1:0] bits are synchronous with REF_CLK. For each clock period in which TX_EN is asserted, two bits of data are received by the PHY from the MAC.

Note 2-7 SMII Tx Mode: Transmit data and control information are received in 10 bit segments. In 100 MBit mode, each segment represents a new byte of data. In 10 MBit mode, each segment is repeated ten times; therefore, every ten segments represent a new byte of data. The PHY can sample any one of every 10 segments in 10 MBit mode.

TABLE 2-2: STRAP-IN OPTIONS KSZ8041TL/FTL

Pin Number	Pin Name	Type Note 2-1	Description
22 21 20	PHYAD2 PHYAD1 PHYAD0	Ipd/O Ipd/O Ipu/O	The PHY Address is latched at power-up/reset and is configurable to any value from 1 to 7. The default PHY Address is 00001. PHY Address bits [4:3] are always set to '00'.
27 41 40	CONFIG2 CONFIG1 CONFIG0	Ipd/O Ipd/O Ipd/O	The CONFIG[2:0] strap-in pins are latched at power-up/reset and are defined as follows: **CONFIG[2:0] Mode** 000 MII (default) 001 RMII 010 SMII 011 Reserved - not used 100 MII 100 Mbps Preamble Restore 101 RMII back-to-back 110 MII back-to-back 111 Reserved - not used
29	ISO	Ipd/O	ISOLATE mode Pull-up = Enable Pull-down (default) = Disable During power-up/reset, this pin value is latched into register 0h bit 10.
43 (TL)	SPEED	Ipu/O	SPEED mode Pull-up (default) = 100 Mbps Pull-down = 10 Mbps During power-up/reset, this pin value is latched into register 0h bit 13 as the Speed Select, and also is latched into register 4h (Auto-Negotiation Advertisement) as the Speed capability support.
43 (FTL)	SPEED	Ipu/O	If copper mode (FXEN=0), pin strap-in is SPEED mode. Pull-up (default) = 100 Mbps Pull-down = 10 Mbps During power-up/reset, this pin value is latched into register 0h bit 13 as the Speed Select, and also is latched into register 4h (Auto-Negotiation Advertisement) as the Speed capability support.
	no FEF		If fiber mode (FXEN=1), pin strap-in is no FEF. Pull-up (default) = Enable Far-End Fault Pull-down = Disable Far-End Fault This pin value is latched during power-up/reset.

TABLE 2-2: STRAP-IN OPTIONS KSZ8041TL/FTL (CONTINUED)

Pin Number	Pin Name	Type Note 2-1	Description
23	DUPLEX	Ipu/O	DUPLEX mode Pull-up (default) = Half-Duplex Pull-down = Full-Duplex During power-up/reset, this pin value is latched into register 0h bit 8 as the Duplex Mode.
42 (TL)	NWAYEN	Ipu/O	Nway Auto-Negotiation Enable Pull-up (default) = Enable Auto-Negotiation Pull-down = Disable Auto-Negotiation During power-up/reset, this pin value is latched into register 0h bit 12.
42 (FTL)	NWAYEN	Ipu/O	If copper mode (FXEN=0), pin strap-in is Nway Auto-Negotiation Enable. Pull-up (default) = Enable Auto-Negotiation Pull-down = Disable Auto-Negotiation During power-up/reset, this pin value is latched into register 0h bit 12. If fiber mode (FXEN=1), this pin configuration is always strapped to disable Auto-Negotiation.

Note 2-1 Ipu/O = Input with internal pull-up (40 kΩ ±30%) during power-up/reset; output pin otherwise.
Ipd/O = Input with internal pull-down (40 kΩ ±30%) during power-up/reset; output pin otherwise.

Pin strap-ins are latched during power-up or reset. In some systems, the MAC receive input pins may drive high during power-up or reset, and consequently cause the PHY strap-in pins on the MII/RMII/SMII signals to be latched high. In this case, it is recommended to add 1 kΩ pull-downs on these PHY strap-in pins to ensure the PHY does not strap-in to ISOLATE mode, or is not configured with an incorrect PHY Address.

FIGURE 2-3: KSZ8041MLL 48-PIN TQFP ASSIGNMENT, (TOP VIEW)

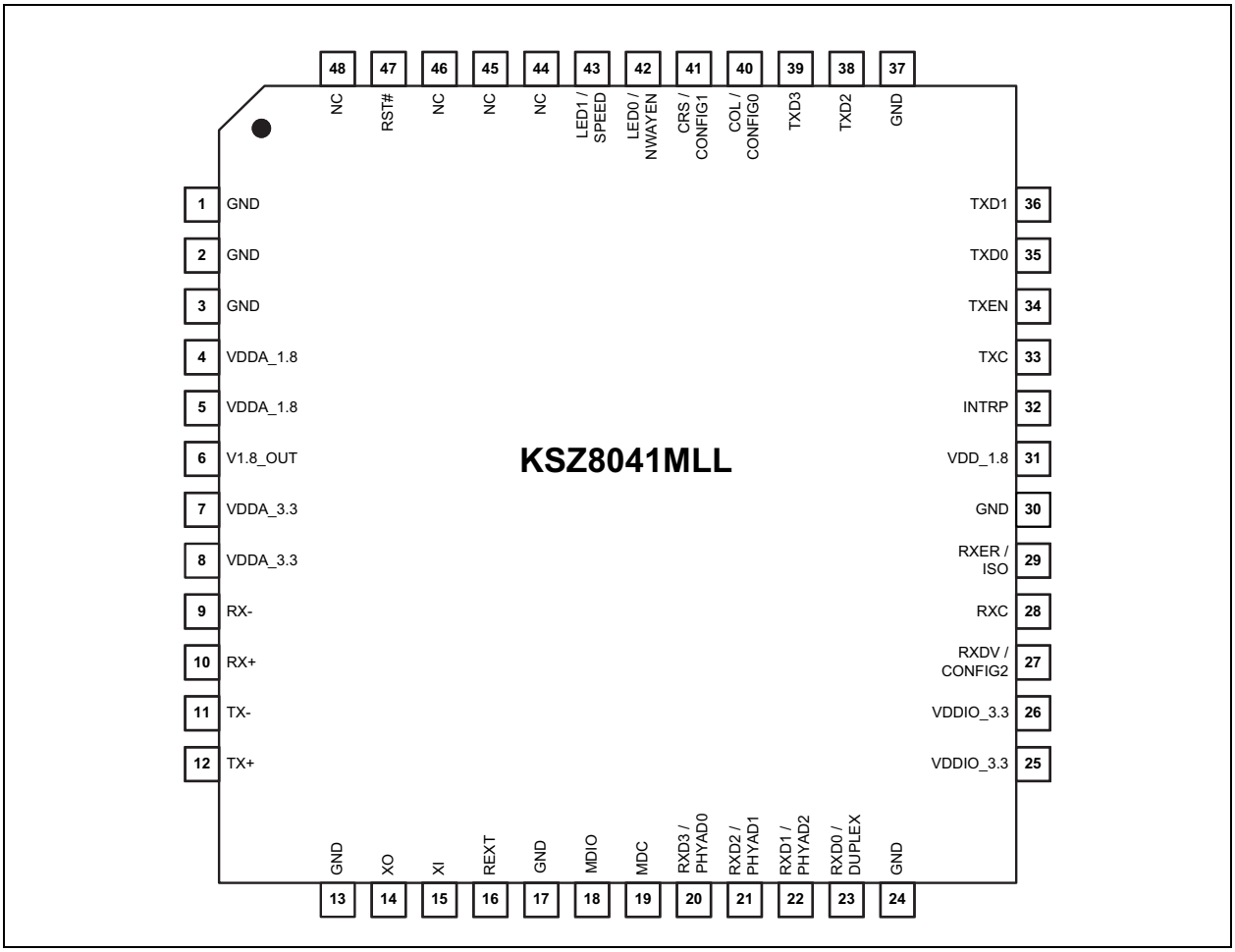


TABLE 2-3: SIGNALS FOR KSZ8041MLL

Pin Number	Pin Name	Type Note 2-1	Description
1	GND	GND	Ground
2	GND	GND	Ground
3	GND	GND	Ground
4	VDDA_1.8	P	1.8V analog V_{DD}
5	VDDA_1.8	P	1.8V analog V_{DD}
6	V1.8_OUT	P	1.8V output voltage from chip
7	VDDA_3.3	P	3.3V analog V_{DD}
8	VDDA_3.3	P	3.3V analog V_{DD}
9	RX–	I/O	Physical receive or transmit signal (– differential)
10	RX+	I/O	Physical receive or transmit signal (+ differential)
11	TX–	I/O	Physical transmit or receive signal (– differential)
12	TX+	I/O	Physical transmit or receive signal (+ differential)
13	GND	GND	Ground

TABLE 2-3: SIGNALS FOR KSZ8041MLL (CONTINUED)

Pin Number	Pin Name	Type Note 2-1	Description
14	XO	O	Crystal feedback This pin is used only when a 25 MHz crystal is used. This pin is a no connect if oscillator or external clock source is used.
15	XI	I	Crystal/Oscillator/External Clock Input 25 MHz ±50 ppm
16	REXT	I/O	Set physical transmit output current Connect a 6.49 kΩ resistor in parallel with a 100 pF capacitor to ground on this pin. See KSZ8041MLL reference schematic.
17	GND	GND	Ground
18	MDIO	I/O	Management Interface (MII) Data I/O This pin requires an external 4.7 kΩ pull-up resistor.
19	MDC	I	Management Interface (MII) Clock Input This pin is synchronous to the MDIO data interface.
20	RXD3/ PHYAD0	Ipu/O	MII Mode: Receive Data Output[3](Note 2-2) Config. Mode: The pull-up/pull-down value is latched as PHYADDR[0] during power-up/reset. See Table 2-4 for details.
21	RXD2/ PHYAD1	Ipd/O	MII Mode: Receive Data Output[2](Note 2-2) Config. Mode: The pull-up/pull-down value is latched as PHYADDR[1] during power-up/reset. See Table 2-4 for details.
22	RXD1/ PHYAD2	Ipd/O	MII Mode: Receive Data Output[1](Note 2-2) Config. Mode: The pull-up/pull-down value is latched as PHYADDR[2] during power-up/reset. See Table 2-4 for details.
23	RXD0/ DUPLEX	Ipu/O	MII Mode: Receive Data Output[0](Note 2-2) Config Mode: Latched as DUPLEX (register 0h, bit 8) during power-up/reset. See Table 2-4 for details.
24	GND	GND	Ground
25	VDDIO_3.3	P	3.3V digital V_{DD}
26	VDDIO_3.3	P	3.3V digital V_{DD}
27	RXDV/ CONFIG2	Ipd/O	MII Mode: Receive Data Valid Output Config. Mode: The pull-up/pull-down value is latched as CONFIG2 during power-up/reset. See Table 2-4 for details.
28	RXC	O	MII Receive Clock Output
29	RXER/ISO	Ipd/O	MII Mode: Receive Error Output Config. Mode: The pull-up/pull-down value is latched as ISOLATE during power-up/reset. See Table 2-4 for details.
30	GND	GND	Ground
31	VDD_1.8	P	1.8V digital V_{DD}
32	INTRP	Opu	Interrupt Output: Programmable Interrupt Output Register 1Bh is the Interrupt Control/Status Register for programming the interrupt conditions and reading the interrupt status. Register 1Fh bit 9 sets the interrupt output to active-low (default) or active-high.
33	TXC	I/O	MII Transmit Clock Output
34	TXEN	I	MII Transmit Enable Input
35	TXD0	I	MII Transmit Data Input[0](Note 2-3)
36	TXD1	I	MII Transmit Data Input[1](Note 2-3)
37	GND	GND	Ground
38	TXD2	I	MII Transmit Data Input[2](Note 2-3)
39	TXD3	I	MII Transmit Data Input[3](Note 2-3)

TABLE 2-3: SIGNALS FOR KSZ8041MLL (CONTINUED)

Pin Number	Pin Name	Type Note 2-1	Description		
40	COL/ CONFIG0	Ipd/O	MII Mode: Collision Detect Output Config. Mode: The pull-up/pull-down value is latched as CONFIG0 during power-up/reset. See Table 2-4 for details.		
41	CRS/ CONFIG1	Ipd/O	MII Mode: Carrier Sense Output Config. Mode: The pull-up/pull-down value is latched as CONFIG1 during power-up/reset. See Table 2-4 for details.		
42	LED0/ NWAYEN	Ipu/O	LED Output: Programmable LED0 Output Config. Mode: Latched as Auto-Negotiation Enable (register 0h, bit 12) during power-up/reset. See Table 2-4 for details. The LED0 pin is programmable via register 1Eh bits [15:14], and is defined as follows:		
			LED Mode = [00]		
			Link/Activity	**Pin State**	**LED Definition**
			No Link	High	OFF
			Link	Low	ON
			Activity	Toggle	Blinking
			LED Mode = [01]		
			Link	**Pin State**	**LED Definition**
			No Link	High	OFF
			Link	Low	ON
			LED Mode = [10]: Reserved		
			LED Mode = [11]: Reserved		
43	LED1/ SPEED	Ipu/O	LED Output: Programmable LED1 Output Config. Mode: Latched as SPEED (register 0h, bit 13) during power-up/reset. See Table 2-4 for details. The LED1 pin is programmable via register 1Eh bits [15:14], and is defined as follows:		
			LED Mode = [00]		
			Speed	**Pin State**	**LED Definition**
			10BT	High	OFF
			100BT	Low	ON
			LED Mode = [01]		
			Activity	**Pin State**	**LED Definition**
			No Activity	High	OFF
			Activity	Toggle	Blinking
			LED Mode = [10]: Reserved		
			LED Mode = [11]: Reserved		
44	NC	—	No connect		
45	NC	—	No connect		
46	NC	—	No connect		
47	RST#	I	Chip reset (active-low)		
48	NC	—	No connect		

Note 2-1 P = power supply
GND = ground
I = input
O = output
I/O = bi-directional

Ipu/O = Input with internal pull-up (40 kΩ ±30%) during power-up/reset; output pin otherwise.
Ipd/O = Input with internal pull-down (40 kΩ ±30%) during power-up/reset; output pin otherwise.
Ipu = Input with internal pull-up. (40 kΩ ±30%)
Ipd = Input with internal pull-down. (40 kΩ ±30%)
Opu = Output with internal pull-up. (40 kΩ ±30%)

Note 2-2 MII Rx Mode: The RXD[3..0] bits are synchronous with RXCLK. When RXDV is asserted, RXD[3..0] presents valid data to MAC through the MII. RXD[3..0] is invalid when RXDV is de-asserted.

Note 2-3 MII Tx Mode: The TXD[3..0] bits are synchronous with TXCLK. When TXEN is asserted, TXD[3..0] presents valid data from the MAC through the MII. TXD[3..0] has no effect when TXEN is de-asserted.

TABLE 2-4: STRAP-IN OPTIONS KSZ8041MLL

Pin Number	Pin Name	Type Note 2-1	Description
22 21 20	PHYAD2 PHYAD1 PHYAD0	Ipd/O Ipd/O Ipu/O	The PHY Address is latched at power-up / reset and is configurable to any value from 1 to 7. The default PHY Address is 00001. PHY Address bits [4:3] are always set to '00'.
27 41 40	CONFIG2 CONFIG1 CONFIG0	Ipd/O Ipd/O Ipd/O	The CONFIG[2:0] strap-in pins are latched at power-up / reset and are defined as follows: **CONFIG[2:0] Mode** 000 MII (default) 001 Reserved - not used 010 Reserved - not used 011 Reserved - not used 100 MII 100 Mbps Preamble Restore 101 Reserved - not used 110 MII Back-to-Back 111 Reserved - not used
29	ISO	Ipd/O	ISOLATE mode Pull-up = Enable Pull-down (default) = Disable During power-up/reset, this pin value is latched into register 0h bit 10.
43	SPEED	Ipu/O	SPEED mode Pull-up (default) = 100 Mbps Pull-down = 10 Mbps During power-up/reset, this pin value is latched into register 0h bit 13 as the Speed Select, and also is latched into register 4h (Auto-Negotiation Advertisement) as the Speed capability support.
23	DUPLEX	Ipu/O	DUPLEX mode Pull-up (default) = Half-Duplex Pull-down = Full-Duplex During power-up/reset, this pin value is latched into register 0h bit 8 as the Duplex Mode.
42	NWAYEN	Ipu/O	Nway Auto-Negotiation Enable Pull-up (default) = Enable Auto-Negotiation Pull-down = Disable Auto-Negotiation During power-up/reset, this pin value is latched into register 0h bit 12.

Note 2-1 Ipu/O = Input with internal pull-up (40 kΩ ±30%) during power-up/reset; output pin otherwise.
Ipd/O = Input with internal pull-down (40 kΩ ±30%) during power-up/reset; output pin otherwise.

Pin strap-ins are latched during power-up or reset. In some systems, the MAC receive input pins may drive high during power-up or reset, and consequently cause the PHY strap-in pins on the MII signals to be latched high. In this case, it is recommended to add 1 kΩ pull-downs on these PHY strap-in pins to ensure the PHY does not strap-in to ISOLATE mode, or is not configured with an incorrect PHY Address.

3.0 FUNCTIONAL DESCRIPTION

The KSZ8041TL is a single 3.3V supply Fast Ethernet transceiver. It is fully compliant with the IEEE 802.3u specification.

On the media side, the KSZ8041TL supports 10BASE-T and 100BASE-TX with HP auto MDI/MDI-X for reliable detection of and correction for straight-through and crossover cables.

The KSZ8041TL offers a choice of MII, RMII, or SMII data interface connection to a MAC processor. The MII management bus option gives the MAC processor complete access to the KSZ8041TL control and status registers. Additionally, an interrupt pin eliminates the need for the processor to poll for PHY status change.

Physical signal transmission and reception are enhanced through the use of patented analog circuitries that make the design more efficient and allow for lower power consumption and smaller chip die size.

The KSZ8041FTL has all the identical rich features of the KSZ8041TL plus 100BASE-FX fiber support.

The KSZ8041MLL is the basic 10BASE-T/100BASE-TX copper version with MII support.

3.1 100BASE-TX Transmit

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125 MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output.

The output current is set by an external 6.49 kΩ 1% resistor for the 1:1 transformer ratio. It has typical rise/fall times of 4 ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot and timing jitter. The wave-shaped 10BASE-T output drivers are also incorporated into the 100BASE-TX drivers.

3.2 100BASE-TX Receive

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based upon comparisons of incoming signal strength against some known cable characteristics, and then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and to improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125 MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII format and provided as the input data to the MAC.

3.3 PLL Clock Synthesizer

The KSZ8041TL/FTL/MLL generates 125 MHz, 25 MHz, and 20 MHz clocks for system timing. In MII mode, internal clocks are generated from an external 25 MHz crystal or oscillator. For the KSZ8041TL/FTL, in RMII and SMII modes, these internal clocks are generated from external 50 MHz and 125 MHz oscillators or system clocks, respectively.

3.4 Scrambler/De-scrambler (100BASE-TX Only)

The purpose of the scrambler is to spread the power spectrum of the signal in order to reduce EMI and baseline wander.

3.5 10BASE-T Transmit

The 10BASE-T drivers are incorporated with the 100BASE-TX drivers to allow for transmission using the same magnetic. The drivers also perform internal wave-shaping and pre-emphasize, and output 10BASE-T signals with a typical amplitude of 2.5V peak. The 10BASE-T signals have harmonic contents that are at least 27 dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

3.6 10BASE-T Receive

On the receive side, input buffer and level detecting squelch circuits are employed. A differential input receiver circuit and a PLL performs the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400 mV or with short pulse widths to prevent noise at the RX+ and RX– inputs from falsely trigger the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8041TL/FTL/MLL decodes a data frame. The receive clock is kept active during idle periods in between data reception.

3.7 SQE and Jabber Function (10BASE-T Only)

In 10BASE-T operation, a short pulse is put out on the COL pin after each frame is transmitted. This SQE Test is required as a test of the 10BASE-T transmit/receive path. If transmit enable (TXEN) is high for more than 20 ms (jabbering), the 10BASE-T transmitter is disabled and COL is asserted high. If TXEN is then driven low for more than 250 ms, the 10BASE-T transmitter is re-enabled and COL is de-asserted (returns to low).

3.8 Auto-Negotiation

The KSZ8041TL/FTL/MLL conforms to the auto-negotiation protocol, defined in Clause 28 of the IEEE 802.3u specification. Auto-negotiation is enabled by either hardware pin strapping (pin 42) or software (register 0h bit 12).

Auto-negotiation allows unshielded twisted pair (UTP) link partners to select the highest common mode of operation. Link partners advertise their capabilities to each other, and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the mode of operation.

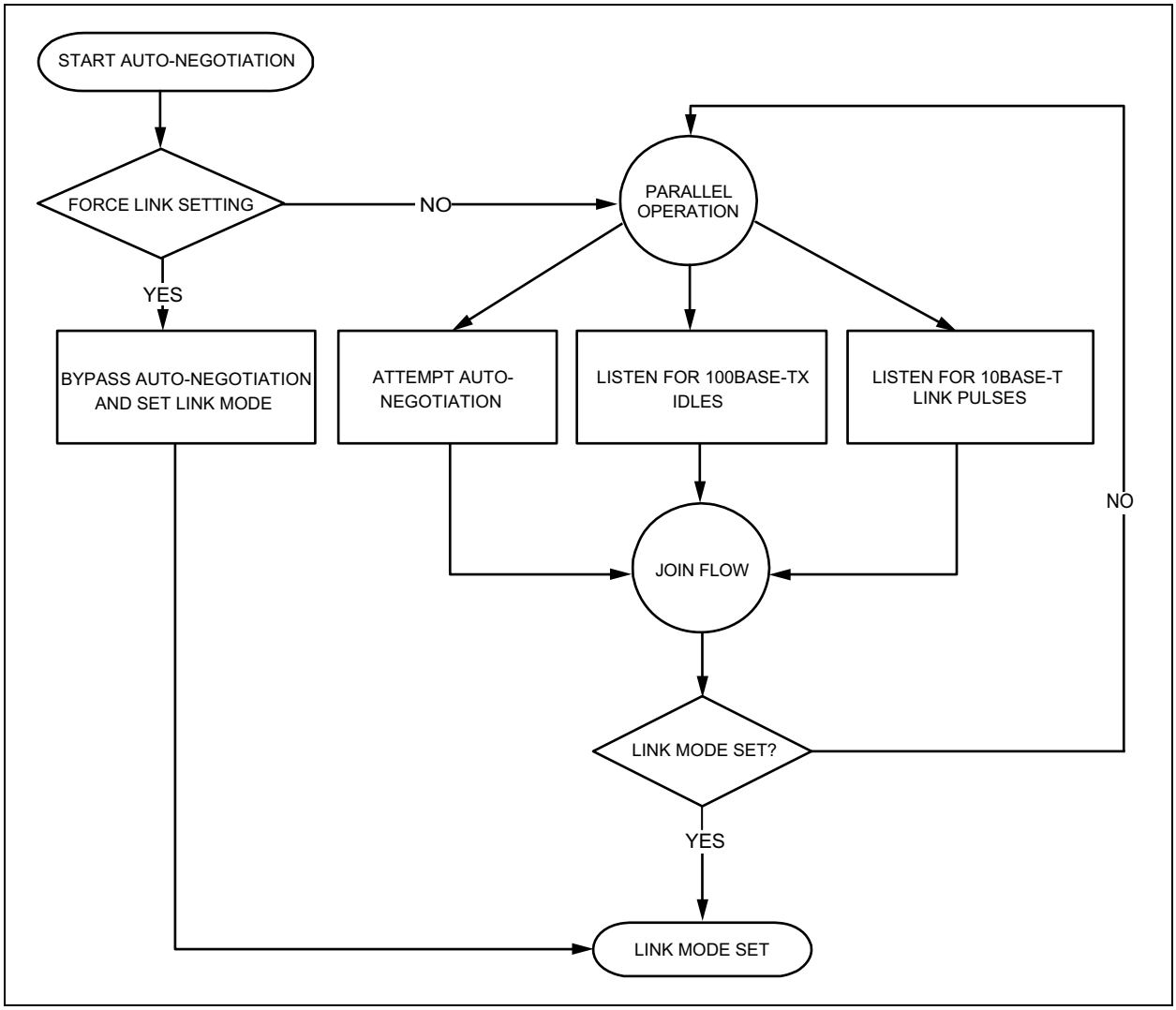
The following list shows the speed and duplex operation mode from highest to lowest.

- Priority 1: 100BASE-TX, full-duplex
- Priority 2: 100BASE-TX, half-duplex
- Priority 3: 10BASE-T, full-duplex
- Priority 4: 10BASE-T, half-duplex

If auto-negotiation is not supported or the KSZ8041TL/FTL/MLL link partner is forced to bypass auto-negotiation, the KSZ8041TL/FTL/MLL sets its operating mode by observing the signal at its receiver. This is known as parallel detection, and allows the KSZ8041TL/FTL/MLL to establish link by listening for a fixed signal protocol in the absence of auto-negotiation advertisement protocol.

The auto-negotiation link up process is shown in the following flow chart.

FIGURE 3-1: AUTO-NEGOTIATION FLOW CHART



3.9 MII Management (MIIM) Interface

The KSZ8041TL/FTL/MLL supports the IEEE 802.3 MII Management Interface, also known as the Management Data Input/Output (MDIO) Interface. This interface allows upper-layer devices to monitor and control the state of the KSZ8041TL/FTL/MLL. An external device with MIIM capability is used to read the PHY status and/or configure the PHY settings. Further details on the MIIM interface can be found in Clause 22.2.4 of the IEEE 802.3 Specification.

The MIIM interface consists of the following:

- A physical connection that incorporates the clock line (MDC) and the data line (MDIO).
- A specific protocol that operates across the aforementioned physical connection that allows a external controller to communicate with one or more PHY devices. Each KSZ8041TL/FTL/MLL device is assigned a unique PHY address between 1 and 7 by its PHYAD[2:0] strapping pins. Also, every KSZ8041TL/FTL/MLL device supports the broadcast PHY address 0, as defined per the IEEE 802.3 Specification, which can be used to read/write to a single KSZ8041TL/FTL/MLL device, or write to multiple KSZ8041TL/FTL/MLL devices simultaneously.
- A set of 16-bit MDIO registers. Register [0:6] are required, and their functions are defined per the IEEE 802.3 Specification. The additional registers are provided for expanded functionality.

The following table shows the MII Management frame format for the KSZ8041TL/FTL/MLL.

TABLE 3-1: MII MANAGEMENT FRAME FORMAT

—	Preamble	Start of Frame	R/W OP Code	PHY Address Bits[4:0]	REG Address Bits[4:0]	TA	Data Bits [15:0]	Idle
Read	32 1's	01	10	00AAA	RRRRR	Z0	DDDDDDDD_DDDDDDDD	Z
Write	32 1's	01	01	00AAA	RRRRR	10	DDDDDDDD_DDDDDDDD	Z

3.10 Interrupt (INTRP)

INTRP (pin 32) is an optional interrupt signal that is used to inform the external controller that there has been a status update to the KSZ8041TL/FTL/MLL PHY register. Bits[15:8] of register 1Bh are the interrupt control bits, and are used to enable and disable the conditions for asserting the INTRP signal. Bits[7:0] of register 1Bh are the interrupt status bits, and are used to indicate which interrupt conditions have occurred. The interrupt status bits are cleared after reading register 1Bh.

Bit 9 of register 1Fh sets the interrupt level to active-high or active-low.

3.11 MII Data Interface

The Media Independent Interface (MII) is specified in Clause 22 of the IEEE 802.3 Specification. It provides a common interface between physical layer and MAC layer devices, and has the following key characteristics:

- Supports 10 Mbps and 100 Mbps data rates.
- Uses a 25 MHz reference clock, sourced by the PHY.
- Provides independent 4-bit wide (nibble) transmit and receive data paths.
- Contains two distinct groups of signals: one for transmission and the other for reception.

By default, the KSZ8041TL/FTL/MLL is configured to MII mode after it is power-up or reset with the following:

- A 25 MHz crystal connected to XI, XO (pins 15, 14), or an external 25 MHz clock source (oscillator) connected to XI.
- CONFIG[2:0] (pins 27, 41, 40) set to '000' (default setting).

3.12 MII Signal Definition

The following table describes the MII signals. Refer to Clause 22 of the IEEE 802.3 Specification for detailed information.

TABLE 3-2: MII SIGNAL DEFINITIONS

MII Signal Name	Direction with Respect to PHY	Direction with Respect to MAC	Description
TXC	Output	Input	Transmit Clock (2.5 MHz for 10 Mbps; 25 MHz for 100 Mbps)
TXEN	Input	Output	Transmit Enable
TXD[3:0]	Input	Output	Transmit Data [3:0]
RXC	Output	Input	Receive Clock (2.5 MHz for 10 Mbps; 25 MHz for 100 Mbps)
RXDV	Output	Input	Receive Data Valid
RXD[3:0]	Output	Input	Receive Data [3:0]
RXER	Output	Input or not required	Receive Error
CRS	Output	Input	Carrier Sense
COL	Output	Input	Collision Detection

3.12.1 TRANSMIT CLOCK (TXC)

TXC is sourced by the PHY. It is a continuous clock that provides the timing reference for TXEN and TXD[3:0].

TXC is 2.5 MHz for 10 Mbps operation and 25 MHz for 100 Mbps operation.

3.12.2 TRANSMIT ENABLE (TXEN)

TXEN indicates the MAC is presenting nibbles on TXD[3:0] for transmission. It is asserted synchronously with the first nibble of the preamble and remains asserted while all nibbles to be transmitted are presented on the MII, and is negated prior to the first TXC following the final nibble of a frame.

TXEN transitions synchronously with respect to TXC.

3.12.3 TRANSMIT DATA [3:0] (TXD[3:0])

TXD[3:0] transitions synchronously with respect to TXC. When TXEN is asserted, TXD[3:0] are accepted for transmission by the PHY. TXD[3:0] is “00” to indicate idle when TXEN is de-asserted. Values other than “00” on TXD[3:0] while TXEN is de-asserted are ignored by the PHY.

3.12.4 RECEIVE CLOCK (RXC)

RXC provides the timing reference for RXDV, RXD[3:0], and RXER.

- In 10 Mbps mode, RXC is recovered from the line while carrier is active. RXC is derived from the PHY’s reference clock when the line is idle, or link is down.
- In 100 Mbps mode, RXC is continuously recovered from the line. If link is down, RXC is derived from the PHY’s reference clock.

RXC is 2.5 MHz for 10 Mbps operation and 25 MHz for 100 Mbps operation.

3.12.5 RECEIVE DATA VALID (RXDV)

RXDV is driven by the PHY to indicate that the PHY is presenting recovered and decoded nibbles on RXD[3:0].

- In 10 Mbps mode, RXDV is asserted with the first nibble of the Start of Frame Delimiter (SFD), “5D”, and remains asserted until the end of the frame.
- In 100 Mbps mode, RXDV is asserted from the first nibble of the preamble to the last nibble of the frame.

RXDV transitions synchronously with respect to RXC.

3.12.6 RECEIVE DATA [3:0] (RXD[3:0])

RXD[3:0] transitions synchronously with respect to RXC. For each clock period in which RXDV is asserted, RXD[3:0] transfers a nibble of recovered data from the PHY.

3.12.7 RECEIVE ERROR (RXER)

RXER is asserted for one or more RXC periods to indicate that a Symbol Error (e.g. a coding error that a PHY is capable of detecting, and that may otherwise be undetectable by the MAC sub-layer) was detected somewhere in the frame presently being transferred from the PHY.

RXER transitions synchronously with respect to RXC. While RXDV is de-asserted, RXER has no effect on the MAC.

3.12.8 CARRIER SENSE (CRS)

CRS is asserted and de-asserted as follows:

- In 10 Mbps mode, CRS assertion is based on the reception of valid preambles. CRS de-assertion is based on the reception of an end-of-frame (EOF) marker.
- In 100 Mbps mode, CRS is asserted when a start-of-stream delimiter, or /J/K symbol pair is detected. CRS is de-asserted when an end-of-stream delimiter, or /T/R symbol pair is detected. Additionally, the PMA layer de-asserts CRS if IDLE symbols are received without /T/R.

3.12.9 COLLISION (COL)

COL is asserted in half-duplex mode whenever the transmitter and receiver are simultaneously active on the line. This is used to inform the MAC that a collision has occurred during its transmission to the PHY.

COL transitions asynchronously with respect to TXC and RXC.

3.13 Reduced MII (RMII) Data Interface (KSZ8041TL/FTL Only)

The Reduced Media Independent Interface (RMII) specifies a low pin count Media Independent Interface (MII). It provides a common interface between physical layer and MAC layer devices, and has the following key characteristics:

- Supports 10 Mbps and 100 Mbps data rates.
- Uses a single 50 MHz reference clock provided by the MAC or the system board.
- Provides independent 2-bit wide (di-bit) transmit and receive data paths.
- Contains two distinct groups of signals: one for transmission and the other for reception.

The KSZ8041TL/FTL is configured in RMII mode after it is power-up or reset with the following:

- A 50 MHz reference clock connected to REFCLK (pin 15).
- CONFIG[2:0] (pins 27, 41, 40) set to '001'.

In RMII mode, unused MII signals, TXD[3:2] (pins 39, 38), are tied to ground.

3.14 RMII Signal Definition (KSZ8041TL/FTL Only)

The following table describes the RMII signals. Refer to RMII Specification for detailed information.

TABLE 3-3: RMII SIGNAL DEFINITIONS

RMII Signal Name	Direction with Respect to PHY	Direction with Respect to MAC	Description
REF_CLK	Input	Input or Output	Synchronous 50 MHz clock reference for receive, transmit and control interface
TX_EN	Input	Output	Transmit Enable
TXD[1:0]	Input	Output	Transmit Data [1:0]
CRS_DV	Output	Input	Carrier Sense/Receive Data Valid
RXD[1:0]	Output	Input	Receive Data [1:0]
RX_ER	Output	Input or not required	Receive Error

3.14.1 REFERENCE CLOCK (REF_CLK)

REF_CLK is sourced by the MAC or system board. It is a continuous 50 MHz clock that provides the timing reference for TX_EN, TXD[1:0], CRS_DV, RXD[1:0], and RX_ER.

3.14.2 TRANSMIT ENABLE (TX_EN)

TX_EN indicates that the MAC is presenting di-bits on TXD[1:0] for transmission. It is asserted synchronously with the first nibble of the preamble and remains asserted while all di-bits to be transmitted are presented on the RMII, and is negated prior to the first REF_CLK following the final di-bit of a frame.

TX_EN transitions synchronously with respect to REF_CLK.

3.14.3 TRANSMIT DATA [1:0] (TXD[1:0])

TXD[1:0] transitions synchronously with respect to REF_CLK. When TX_EN is asserted, TXD[1:0] are accepted for transmission by the PHY. TXD[1:0] is "00" to indicate idle when TX_EN is de-asserted. Values other than "00" on TXD[1:0] while TX_EN is de-asserted are ignored by the PHY.

3.14.4 CARRIER SENSE/RECEIVE DATA VALID (CRS_DV)

CRS_DV is asserted by the PHY when the receive medium is non-idle. It is asserted asynchronously on detection of carrier. This is when squelch is passed in 10 Mbps mode, and when two non-contiguous zeroes in 10 bits are detected in 100 Mbps mode. Loss of carrier results in the de-assertion of CRS_DV.

So long as carrier detection criteria are met, CRS_DV remains asserted continuously from the first recovered di-bit of the frame through the final recovered di-bit, and it is negated prior to the first REF_CLK that follows the final di-bit. The data on RXD[1:0] is considered valid once CRS_DV is asserted. However, since the assertion of CRS_DV is asynchronous relative to REF_CLK, the data on RXD[1:0] is "00" until proper receive signal decoding takes place.

3.14.5 RECEIVE DATA [1:0] (RXD[1:0])

RXD[1:0] transitions synchronously to REF_CLK. For each clock period in which CRS_DV is asserted, RXD[1:0] transfers two bits of recovered data from the PHY. RXD[1:0] is "00" to indicate idle when CRS_DV is de-asserted. Values other than "00" on RXD[1:0] while CRS_DV is de-asserted are ignored by the MAC.

3.14.6 RECEIVE ERROR (RX_ER)

RX_ER is asserted for one or more REF_CLK periods to indicate that a Symbol Error (e.g. a coding error that a PHY is capable of detecting, and that may otherwise be undetectable by the MAC sub-layer) was detected somewhere in the frame presently being transferred from the PHY.

RX_ER transitions synchronously with respect to REF_CLK. While CRS_DV is de-asserted, RX_ER has no effect on the MAC.

3.14.7 COLLISION DETECTION

The MAC regenerates the COL signal of the MII from TX_EN and CRS_DV.

3.15 Serial MII (SMII) Data Interface (KSZ8041TL/FTL Only)

The Serial Media Independent Interface (SMII) is the lowest pin count Media Independent Interface (MII). It provides a common interface between physical layer and MAC layer devices, and has the following key characteristics:

- Supports 10 Mbps and 100 Mbps data rates.
- Uses 125 MHz reference clock provided by the MAC or the system board.
- Uses 12.5 MHz sync pulse provided by the MAC.
- Provides independent single-bit wide transmit and receive data paths for data and control information.

The KSZ8041TL/FTL is configured in SMII mode after it is power-up or reset with the following:

- A 125 MHz reference clock connected to CLOCK (pin 15).
- A 12.5 MHz sync pulse connected to SYNC (pin 36).
- CONFIG[2:0] (pins 27, 41, 40) set to ‘010’.

In SMII mode, unused MII signals, TXD[3:2] (pins 39, 38), are tied to ground.

3.16 SMII Signal Definition (KSZ8041TL/FTL Only)

The following table describes the SMII signals. Refer to SMII Specification for detailed information.

TABLE 3-4: SMII SIGNAL DESCRIPTION

SMII Signal Name	Direction with Respect to PHY	Direction with Respect to MAC	Description
CLOCK	Input	Input or Output	125 MHz clock reference for receive and transmit data and control
SYNC	Input	Output	12.5 MHz sync pulse from MAC
TX	Input	Output	Transmit Data and Control
RX	Output	Input	Receive Data and Control

3.16.1 CLOCK REFERENCE (CLOCK)

CLOCK is sourced by the MAC or system board. It is a continuous 125 MHz clock that provides the timing reference for SYNC, TX, and RX.

3.16.2 SYNC PULSE (SYNC)

SYNC is a 12.5 MHz synchronized pulse derived from CLOCK by the MAC. It is used to indicate the segment boundary for each transmit data/control segment, or receive data/control segment. Each segment is comprised of ten bits.

SYNC is generated continuously by the MAC at every ten cycles of CLOCK.

3.16.3 TRANSMIT DATA AND CONTROL (TX)

TX provides transmit data and control information from MAC-to-PHY in 10-bit segments.

- In 10 Mbps mode, each segment is repeated ten times. Therefore, every ten segments represent a new byte of data. The PHY can sample any one of every ten segments.
- In 100 Mbps mode, each segment represents a new byte of data.

FIGURE 3-2: SMII TRANSMIT DATA/CONTROL SEGMENT

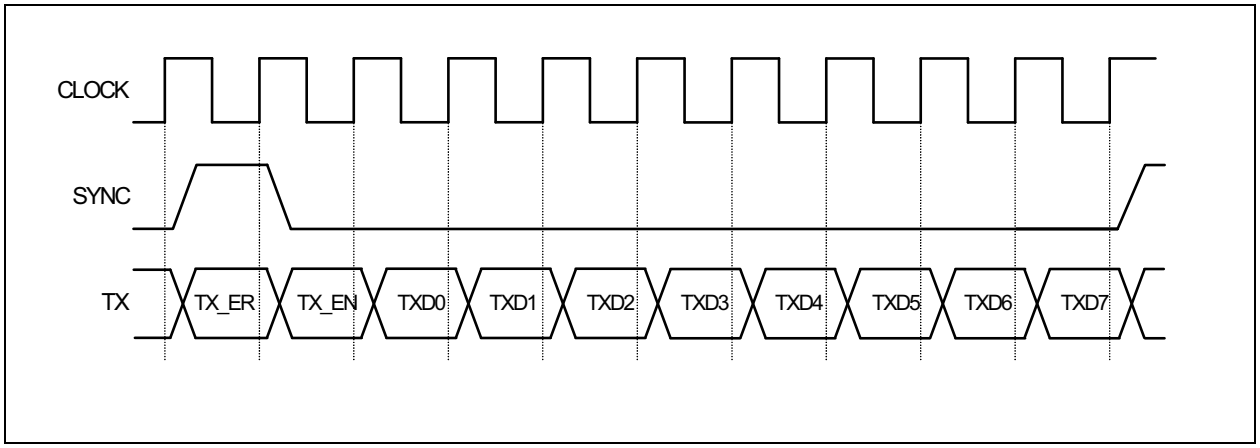


TABLE 3-5: SMII TX BIT DESCRIPTION

SMII TX Bit	Description
TX_ER	Transmit Error
TX_EN	Transmit Enable
TXD[0:7]	Encoded Data See Table 3-6.

TABLE 3-6: SMII TXD[0:7] ENCODING TABLE

TX_ER	TX_EN	TXD0	TXD1	TXD2	TXD3	TXD4	TXD5	TXD6	TXD7
X	0	Use to force an error in a direct MAC-to-MAC connection	Speed 0=10M 1=100M	Duplex 0=Half 1=Full	Link 0=Down 1=Up	Jabber 0=No 1=Yes	1	1	1
X	1	One Data Byte							

3.16.4 RECEIVE DATA AND CONTROL (RX)

RX provides receive data and control information from PHY-to-MAC in 10-bit segments.

- In 10 Mbps mode, each segment is repeated ten times. Therefore, every ten segments represent a new byte of data. The MAC can sample any one of every ten segments.
- In 100 Mbps mode, each segment represents a new byte of data.

The following figure and tables show the receive data/control format for each segment:

FIGURE 3-3: SMII RECEIVE DATA/CONTROL SEGMENT

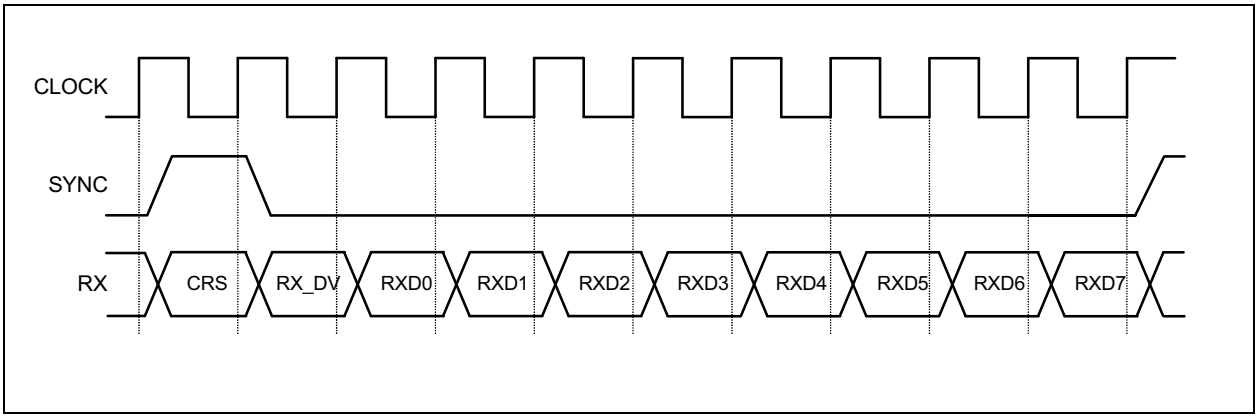


TABLE 3-7: SMII RX BIT DESCRIPTION

SMII RX Bit	Description
CRS	Carrier Sense
RX_DV	Receive Data Valid
RXD[0:7]	Encoded Data See Table 3-8.

TABLE 3-8: SMII RXD[0:7] ENCODING TABLE

CRS	RX_DV	RXD0	RXD1	RXD2	RXD3	RXD4	RXD5	RXD6	RXD7
X	0	RX_ER from previous frame	Speed 0=10M 1=100M	Duplex 0=Half 1=Full	Link 0=Down 1=Up	Jabber 0=No 1=Yes	Upper Nibble 0=Invalid 1=Valid	False Carrier Detected	1
X	1	One Data Byte							

3.16.5 COLLISION DETECTION

Collisions occur when CRS and TX_EN are simultaneously asserted. The MAC regenerates the MII collision signal from CRS and TX_EN.

3.17 HP Auto MDI/MDI-X

HP Auto MDI/MDI-X configuration eliminates the confusion of whether to use a straight cable or a crossover cable between the KSZ8041TL/FTL/MLL and its link partner. This feature allows the KSZ8041TL/FTL/MLL to use either type of cable to connect with a link partner that is in either MDI or MDI-X mode. The auto-sense function detects transmit and receive pairs from the link partner, and then assigns transmit and receive pairs of the KSZ8041TL/FTL/MLL accordingly.

HP Auto MDI/MDI-X is enabled by default. It is disabled by writing a one to register 1F bit 13. MDI and MDI-X mode is selected by register 1F bit 14 if HP Auto MDI/MDI-X is disabled.

An isolation transformer with symmetrical transmit and receive data paths is recommended to support auto MDI/MDI-X.

The IEEE 802.3 Standard defines MDI and MDI-X as follow:

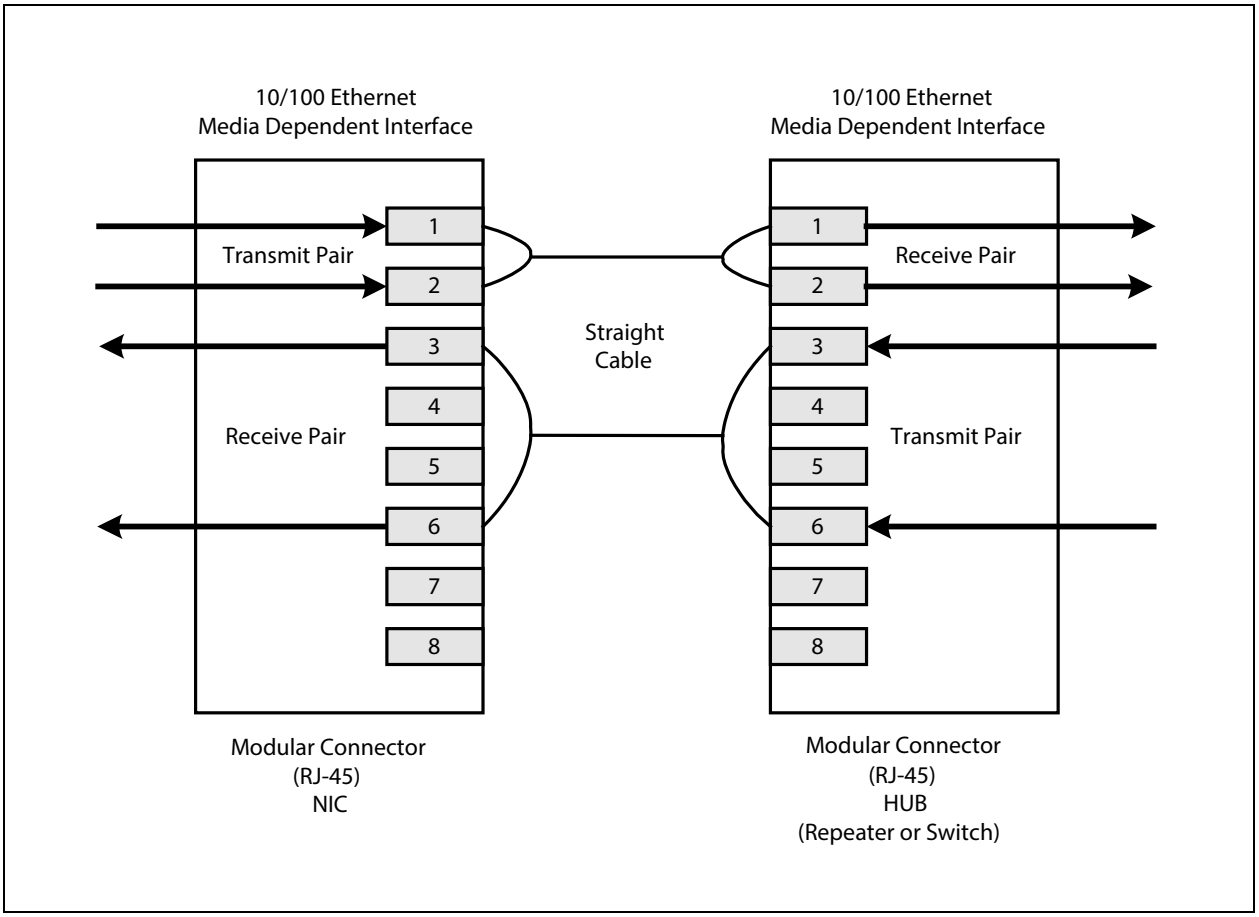
TABLE 3-9: MDI/MDI-X PIN DEFINITION

MDI		MDI-X	
RJ-45 Pin	**Signal**	**RJ-45 Pin**	**Signal**
1	TD+	1	RD+
2	TD–	2	RD–
3	RD+	3	TD+
6	RD–	6	TD–

3.17.1 STRAIGHT CABLE

A straight cable connects an MDI device to an MDI-X device, or an MDI-X device to an MDI device. Figure 3-4 depicts a typical straight cable connection between a network interface card (NIC) and a switch, or hub (MDI-X).

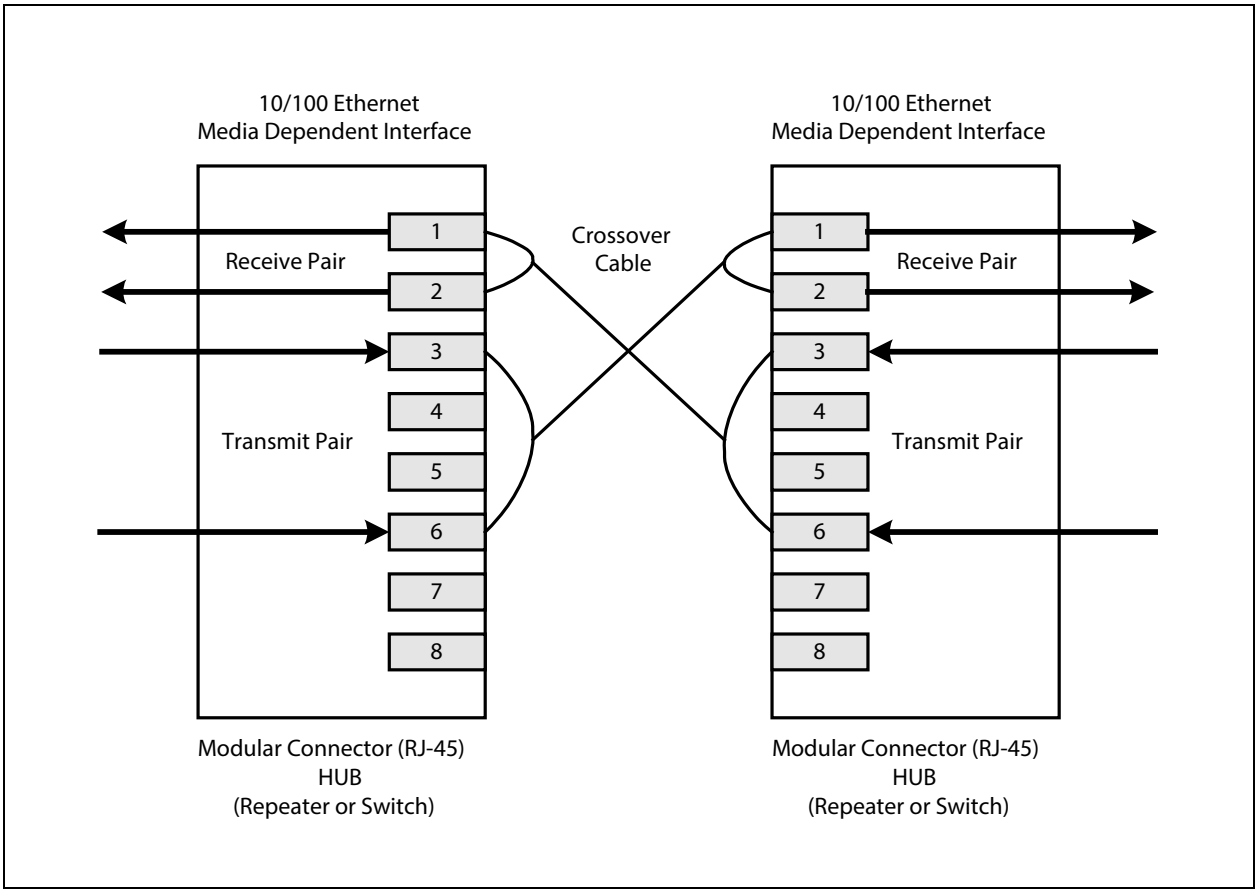
FIGURE 3-4: TYPICAL STRAIGHT CABLE CONNECTION



3.17.2 CROSSOVER CABLE

A crossover cable connects an MDI device to another MDI device, or an MDI-X device to another MDI-X device. Figure 3-5 shows a typical crossover cable connection between two switches or hubs (two MDI-X devices).

FIGURE 3-5: TYPICAL CROSSOVER CABLE CONNECTION



3.18 LinkMD® Cable Diagnostics

The LinkMD® feature utilizes time domain reflectometry (TDR) to analyze the cabling plant for common cabling problems, such as open circuits, short circuits and impedance mismatches.

LinkMD® works by sending a pulse of known amplitude and duration down the MDI and MDI-X pairs, and then analyzing the shape of the reflected signal. Timing the pulse duration gives an indication of the distance to the cabling fault with maximum distance of 200m and accuracy of ±2m. Internal circuitry computes the TDR information and presents it in a user-readable digital format.

Cable diagnostics are only valid for copper connections and do not support fiber optic operation.

3.18.1 ACCESS

LinkMD is initiated by accessing register 1Dh, the LinkMD Control/Status Register, in conjunction with register 1Fh, the PHY Control 2 Register.

3.18.2 USAGE

The following test procedure demonstrates how to use LinkMD for cable diagnostic:

1. Disable auto MDI/MDI-X by writing a ‘1’ to register 1Fh bit 13 to enable manual control over the differential pair used to transmit the LinkMD pulse.
2. Select the differential pair to transmit the LinkMD pulse with register 1Fh bit 14.
3. Start cable diagnostic test by writing a ‘1’ to register 1Dh bit 15. This enable bit is self-clearing.

4. Wait (poll) for register 1Dh bit 15 to return a ‘0’, indicating cable diagnostic test is completed.
5. Read cable diagnostic test results in register 1Dh bits [14:13]. The results are as follows:

00 = Valid test, normal condition

01 = Valid test, open circuit in cable

10 = Valid test, short circuit in cable

11 = Invalid test, cable diagnostic test failed

The ‘11’ case, invalid test, occurs if the KSZ8041TL/FTL/MLL is unable to shut down the link partner. In this instance, the test is not run because it would be impossible for the KSZ8041TL/FTL/MLL to determine if the detected signal is a reflection of the signal generated by the KSZ8041TL/FTL/MLL, or a signal from its link partner.

6. Get distance to fault by multiplying the decimal value in register 1Dh bits [8:0] by a constant of 0.4. The distance, D (expressed in meters), to the cable fault is determined by the following formula:

D (distance to cable fault) = 0.4 x {decimal value of register 1Dh bits [8:0]}

The 0.4 constant may be calibrated for different cable types and cabling conditions, including cables with a velocity of propagation that varies significantly from the norm.

3.19 Power Management

The KSZ8041TL/FTL/MLL offers the following power management modes:

3.19.1 POWER SAVING MODE

This mode is used to reduce power consumption when the cable is unplugged. It is in effect when auto-negotiation mode is enabled, cable is disconnected, and register 1Fh bit 10 is set to 1. Under power saving mode, the KSZ8041TL/FTL/MLL shuts down all transceiver blocks, except for transmitter, energy detect and PLL circuits. Additionally, in MII mode, the RXC clock output is disabled. RXC clock is enabled after the cable is connected and link is established.

Power saving mode is disabled by writing a zero to register 1Fh bit 10.

3.19.2 POWER DOWN MODE

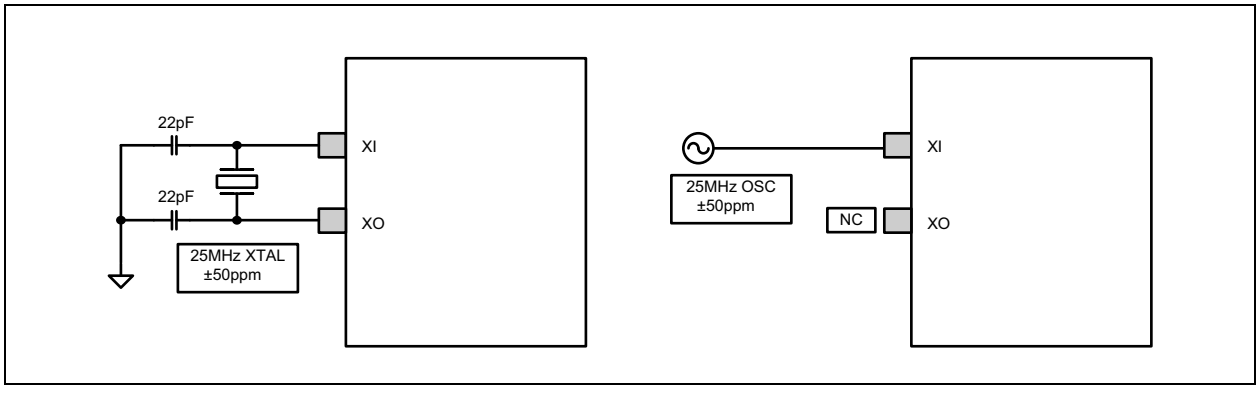
This mode is used to power down the entire KSZ8041TL/FTL/MLL device when it is not in use. Power down mode is enabled by writing a one to register 0h bit 11. In the power down state, the KSZ8041TL/FTL/MLL disables all internal functions, except for the MII management interface.

3.20 Reference Clock Connection Options

A crystal or clock source, such as an oscillator, is used to provide the reference clock for the KSZ8041TL/FTL/MLL.

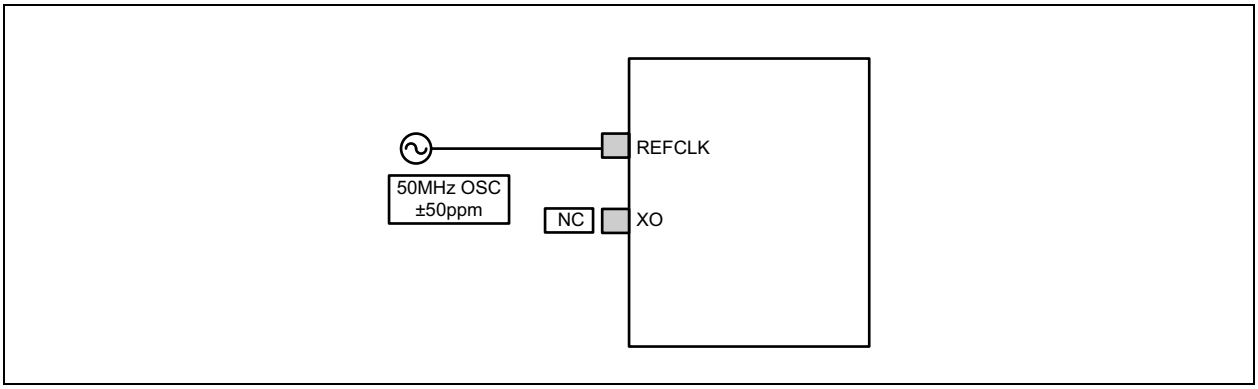
The following figure illustrates how to connect the 25 MHz crystal and oscillator reference clock for MII mode.

FIGURE 3-6: 25 MHZ CRYSTAL/OSCILLATOR REFERENCE CLOCK FOR MII MODE



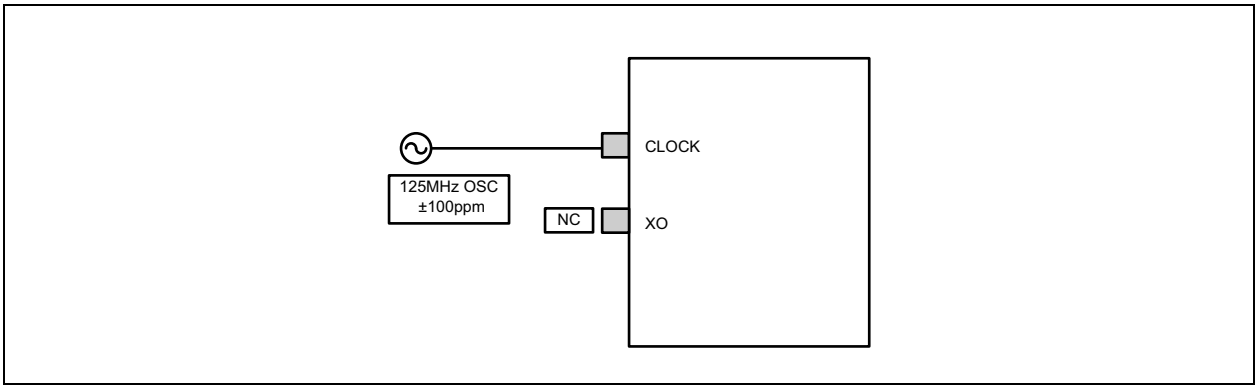
For the KSZ8041TL/FTL, the following figure illustrates how to connect the 50 MHz oscillator reference clock for RMII mode.

FIGURE 3-7: 50 MHZ OSCILLATOR REFERENCE CLOCK FOR RMII MODE



For the KSZ8041TL/FTL, the following figure illustrates how to connect the 125 MHz oscillator reference clock for SMII mode.

FIGURE 3-8: 125 MHZ OSCILLATOR REFERENCE CLOCK FOR SMII MODE



3.21 Reference Circuit for Power and Ground Connections

The KSZ8041TL/FTL/MLL is a single 3.3V supply device with a built-in 1.8V low noise regulator. The power and ground connections are shown in the following figure and table.

FIGURE 3-9: KSZ8041TL/FTL/MLL POWER AND GROUND CONNECTIONS

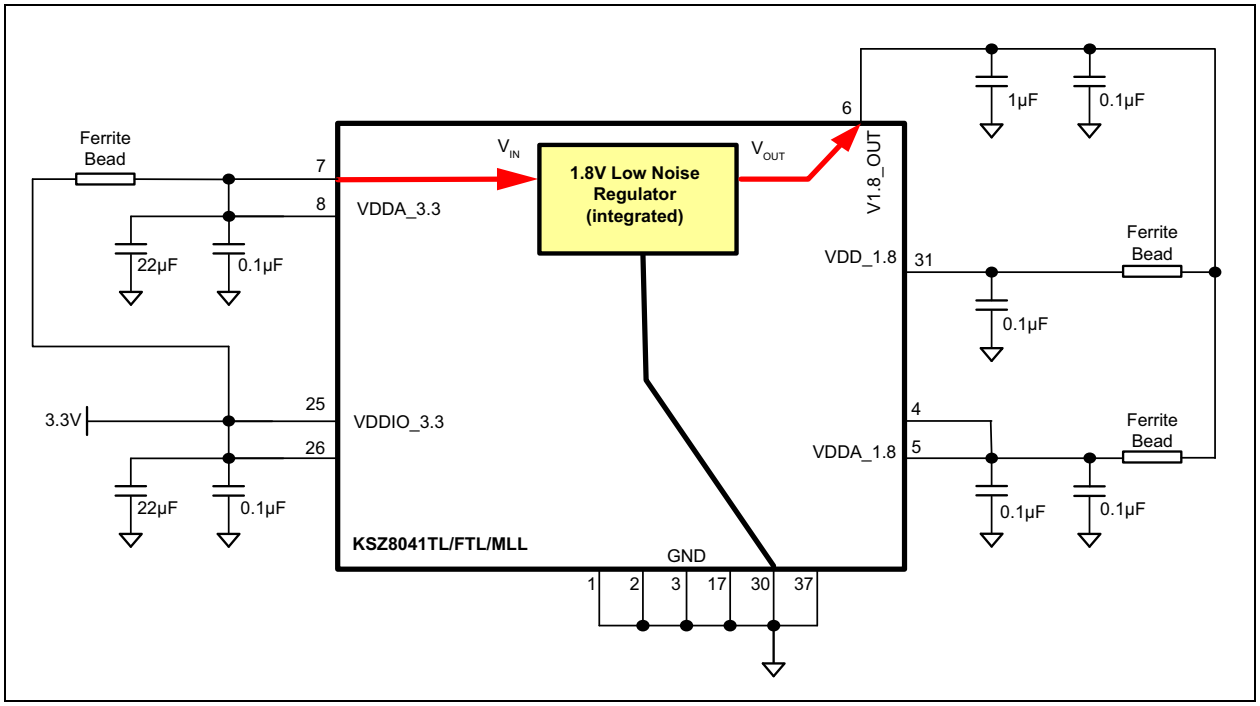


TABLE 3-10: KSZ8041TL/FTL/MLL POWER PIN DESCRIPTION

Power Pin	Pin Number	Pin Type	Description
V1.8_OUT	6	Output	1.8V supply output from KSZ8041TL/FTL/MLL Decouple with 1 µF and 0.1 µF capacitors to ground.
VDD_1.8	31	Input	Connect to V1.8_OUT (pin 6) through ferrite bead. Decouple with 0.1 µF capacitor to ground.
VDDA_1.8	4, 5	Input	Connect to V1.8_OUT (pin 6) through ferrite bead. Decouple with 0.1 µF capacitor on each pin to ground.
VDDIO_3.3	25, 26	Input	Connect to board's 3.3V supply. Decouple with 22 µF and 0.1 µF capacitors to ground.
VDDA_3.3	7, 8	Input	Connect to board's 3.3V supply through ferrite bead. Decouple with 22 µF and 0.1 µF capacitors to ground.

3.22 100BASE-FX Fiber Operation (KSZ8041FTL Only)

100BASE-FX fiber operation is similar to 100BASE-TX copper operation with the differences being that the scrambler/de-scrambler and MLT3 encoder/decoder are bypassed on transmission and reception. In addition, auto-negotiation is bypassed, auto MDI/MDI-X is disabled, and speed is set to 100 Mbps. The duplex can be set to either half or full. Usually, it is set to full-duplex.

3.22.1 FIBER SIGNAL DETECT

In 100BASE-FX operation, FXSD (fiber signal detect), input pin 48, is usually connected to the fiber transceiver SD (signal detect) output pin. 100BASE-FX mode is activated when the FXSD input pin is greater than 1V. When FXSD is between 1V and 1.8V, no fiber signal is detected and a Far-End Fault is generated. When FXSD is over 2.2V, the fiber signal is detected.

100BASE-FX mode and signal detection is summarized in the following table:

TABLE 3-11: COPPER AND FIBER MODE SELECTION

FXSD Input Voltage	Mode
Less than 0.2V	Copper mode
Greater than 1V, but less than 1.8V	Fiber mode No signal detected Far-End Fault generated (if enabled)
Greater than 2.2V	Fiber mode Signal detected

To ensure proper operation, a resistive voltage divider is recommended to adjust the fiber transceiver SD (signal detect) output voltage swing to match the FXSD pin's input voltage threshold.

Alternatively, the Far-End Fault feature can be disabled. In this case, the FXSD input pin is tied high to 3.3V to force 100BASE-FX mode.

3.22.2 FAR-END FAULT

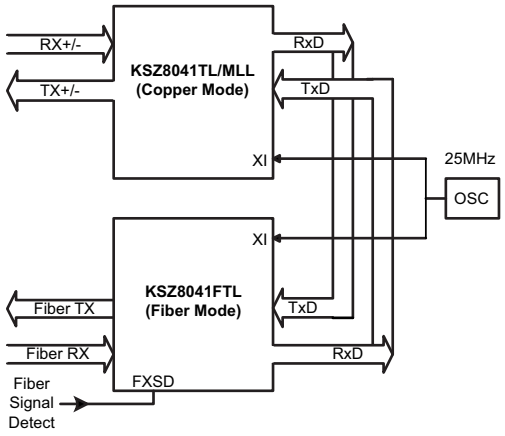
A Far-End Fault (FEF) occurs when the signal detection is logically false on the receive side of the fiber transceiver. The KSZ8041FTL detects a FEF when its FXSD input (pin 48) is between 1V and 1.8V. When a FEF is detected, the KSZ8041FTL signals its fiber link partner that a FEF has occurred by transmitting a repetitive pattern of 84-ones and 1-zero. This pattern is used to inform the fiber link partner that there is a faulty link on its transmit side.

By default, FEF is enabled. FEF is disabled by strapping "no FEF" (pin 43) low. See the Strap-In Options section for detail.

3.23 Back-to-Back Media Converter

A KSZ8041TL/MLL and a KSZ8041FTL can be connected back-to-back to provide a low cost media converter solution. In back-to-back mode, media conversion is between 100BASE-TX copper and 100BASE-FX fiber. On the copper side, link up at 10BASE-T is not allowed, and is blocked during auto-negotiation.

FIGURE 3-10: KSZ8041TL/MLL AND KSZ8041FTL BACK-TO-BACK MEDIA CONVERTER



3.23.1 MII BACK-TO-BACK MODE

In MII Back-to-Back mode, the KSZ8041TL/MLL interfaces with another KSZ8041TL/MLL, or a KSZ8041FTL to provide a complete 100 Mbps repeater or media converter solution. The KSZ8041TL/FTL/MLL devices are configured to MII Back-to-Back mode after they are power-up or reset with the following:

- CONFIG[2:0] (pins 27, 41, 40) set to '110'
- A common 25 MHz reference clock connected to XI (pin 15)
- MII signals connected as shown in the following table.

TABLE 3-12: MII SIGNAL CONNECTION FOR MII BACK-TO-BACK MODE

KSZ8041MLL (100BASE-TX copper) KSZ8041TL (100BASE-TX copper)			KSZ8041MLL (100BASE-TX copper) KSZ8041TL (100BASE-TX copper) KSZ8041FTL (100BASE-FX fiber)		
Pin Name	**Pin Number**	**Pin Type**	**Pin Name**	**Pin Number**	**Pin Type**
RXC	28	Output	TXC	33	Input
RXDV	27	Output	TXEN	34	Input
RXD3	20	Output	TXD3	39	Input
RXD2	21	Output	TXD2	38	Input
RXD1	22	Output	TXD1	36	Input
RXD0	23	Output	TXD0	35	Input
TXC	33	Input	RXC	28	Output
TXEN	34	Input	RXDV	27	Output
TXD3	39	Input	RXD3	20	Output
TXD2	38	Input	RXD2	21	Output
TXD1	36	Input	RXD1	22	Output
TXD0	35	Input	RXD0	23	Output

3.23.2 RMII BACK-TO-BACK MODE (KSZ8041TL/FTL ONLY)

In RMII Back-to-Back mode, the KSZ8041TL interfaces with another KSZ8041TL, or a KSZ8041FTL to provide a complete 100 Mbps repeater or media converter solution. The KSZ8041TL/FTL devices are configured to RMII Back-to-Back mode after they are power-up or reset with the following:

- CONFIG[2:0] (pins 27, 41, 40) set to ‘101’
- A common 50 MHz reference clock connected to REFCLK (pin 15)
- RMII signals connected as shown in the following table.

TABLE 3-13: RMII SIGNAL CONNECTION FOR RMII BACK-TO-BACK MODE

KSZ8041TL (100BASE-TX copper)			KSZ8041TL (100BASE-TX copper) KSZ8041FTL (100BASE-FX fiber)		
Pin Name	**Pin Number**	**Pin Type**	**Pin Name**	**Pin Number**	**Pin Type**
CRSDV	27	Output	TXEN	34	Input
RXD1	22	Output	TXD1	36	Input
RXD0	23	Output	TXD0	35	Input
TXEN	34	Input	CRSDV	27	Output
TXD1	36	Input	RXD1	22	Output
TXD0	35	Input	RXD0	23	Output

RMII Back-to-Back mode provides an option to disable the fiber side when the copper side is down. This, effectively, produces a link fault propagation for media converter applications, such that a copper side link down will automatically disable the fiber side. This KSZ8041TL/FTL feature functions as follows:

- On the KSZ8041TL copper side, RXD2 (pin 21) indicates if there is energy detected at the receive inputs of the copper port. RXD2 outputs a low if there is no energy detected (cable disconnected), and outputs a high if there is energy detected (cable connected).
- The RXD2 output of the KSZ8041TL copper side drives the input of an inverter, and the output of the inverter drives the TXD2 (pin 38) input of the KSZ8041FTL fiber side. The fiber side transmitter is disabled if the TXD2 input is high.

The TXD3 and TXD2 pins should be pulled down with 1K resistors, and RXD3 and RXD2 pins should be left floating, if they are not used.

4.0 REGISTER DESCRIPTIONS

4.1 Register Map

TABLE 4-1: REGISTER MAP

Register Number (Hex)	Description
0h	Basic Control
1h	Basic Status
2h	PHY Identifier 1
3h	PHY Identifier 2
4h	Auto-Negotiation Advertisement
5h	Auto-Negotiation Link Partner Ability
6h	Auto-Negotiation Expansion
7h	Auto-Negotiation Next Page
8h	Link Partner Next Page Ability
9h – 13h	Reserved
14h	MII Control
15h	RXER Counter
16h – 1Ah	Reserved
1Bh	Interrupt Control/Status
1Ch	Reserved
1Dh	LinkMD® Control/Status
1Eh	PHY Control 1
1Fh	PHY Control 2

4.2 Register Descriptions

TABLE 4-2: REGISTER DESCRIPTIONS

Address	Name	Description	Mode Note 4-1	Default
Register 0h – Basic Control				
0.15	Reset	1 = Software reset 0 = Normal operation This bit is self-cleared after a '1' is written to it.	RW/SC	0
0.14	Loopback	1 = Loopback mode 0 = Normal operation	RW	0
0.13	Speed Select (LSB)	1 = 100 Mbps 0 = 10 Mbps This bit is ignored if auto-negotiation is enabled (register 0.12 = 1).	RW	Set by SPEED strapping pin. See Table 2-2 for details.
0.12	Auto-Negotiation Enable	1 = Enable auto-negotiation process 0 = Disable auto-negotiation process If enabled, auto-negotiation result overrides settings in register 0.13 and 0.8.	RW	Set by NWAYEN strapping pin. See Table 2-2 for details.
0.11	Power Down	1 = Power down mode 0 = Normal operation	RW	0

TABLE 4-2: REGISTER DESCRIPTIONS (CONTINUED)

Address	Name	Description	Mode Note 4-1	Default
0.10	Isolate	1 = Electrical isolation of PHY from MII and TX+/ TX– 0 = Normal operation	RW	Set by ISO strapping pin. See Table 2-2 for details.
0.9	Restart Auto-Negotiation	1 = Restart auto-negotiation process 0 = Normal operation. This bit is self-cleared after a ‘1’ is written to it.	RW/SC	0
0.8	Duplex Mode	1 = Full-duplex 0 = Half-duplex	RW	Inverse of DUPLEX strapping pin value. See Table 2-2 for details.
0.7	Collision Test	1 = Enable COL test 0 = Disable COL test	RW	0
0.6:1	Reserved	—	RO	000_000
0.0	Disable Transmitter	0 = Enable transmitter 1 = Disable transmitter	RW	0
Register 1h – Basic Status				
1.15	100BASE-T4	1 = T4 capable 0 = Not T4 capable	RO	0
1.14	100BASE-TX Full-Duplex	1 = Capable of 100 Mbps full-duplex 0 = Not capable of 100 Mbps full-duplex	RO	1
1.13	100BASE-TX Half-Duplex	1 = Capable of 100 Mbps half-duplex 0 = Not capable of 100 Mbps half-duplex	RO	1
1.12	10BASE-T Full-Duplex	1 = Capable of 10 Mbps full-duplex 0 = Not capable of 10 Mbps full-duplex	RO	1
1.11	10BASE-T Half-Duplex	1 = Capable of 10 Mbps half-duplex 0 = Not capable of 10 Mbps half-duplex	RO	1
1.10:7	Reserved	—	RO	0000
1.6	No Preamble	1 = Preamble suppression 0 = Normal preamble	RO	1
1.5	Auto-Negotiation Complete	1 = Auto-negotiation process completed 0 = Auto-negotiation process not completed	RO	0
1.4	Remote Fault	1 = Remote fault 0 = No remote fault	RO/LH	0
1.3	Auto-Negotiation Ability	1 = Capable to perform auto-negotiation 0 = Not capable to perform auto-negotiation	RO	1
1.2	Link Status	1 = Link is up 0 = Link is down	RO/LL	0
1.1	Jabber Detect	1 = Jabber detected 0 = Jabber not detected (default is low)	RO/LH	0
1.0	Extended Capability	1 = Supports extended capabilities registers	RO	1
Register 2h – PHY Identifier 1				
2.15:0	PHY ID Number	Assigned to the 3rd through 18th bits of the Organizationally Unique Identifier (OUI). Kendin Communication’s OUI is 0010A1 (hex).	RO	0022h

TABLE 4-2: REGISTER DESCRIPTIONS (CONTINUED)

Address	Name	Description	Mode Note 4-1	Default
Register 3h – PHY Identifier 2				
3.15:10	PHY ID Number	Assigned to the 19th through 24th bits of the Organizationally Unique Identifier (OUI). Kendin Communication's OUI is 0010A1 (hex).	RO	0001_01
3.9:4	Model Number	Six bit manufacturer's model number.	RO	01_0001
3.3:0	Revision Number	Four bit manufacturer's revision number.	RO	Indicates silicon revision
Register 4h – Auto-Negotiation Advertisement				
4.15	Next Page	1 = Next page capable 0 = No next page capability.	RW	0
4.14	Reserved	—	RO	0
4.13	Remote Fault	1 = Remote fault supported 0 = No remote fault	RW	0
4.12	Reserved	—	RO	0
4.11:10	Pause	[00] = No PAUSE [10] = Asymmetric PAUSE [01] = Symmetric PAUSE [11] = Asymmetric & Symmetric PAUSE	RW	00
4.9	100BASE-T4	1 = T4 capable 0 = No T4 capability	RO	0
4.8	100BASE-TX Full-Duplex	1 = 100 Mbps full-duplex capable 0 = No 100 Mbps full-duplex capability	RW	Set by SPEED strapping pin. See Table 2-2 for details.
4.7	100BASE-TX Half-Duplex	1 = 100 Mbps half-duplex capable 0 = No 100 Mbps half-duplex capability	RW	Set by SPEED strapping pin. See Table 2-2 for details.
4.6	10BASE-T Full-Duplex	1 = 10 Mbps full-duplex capable 0 = No 10 Mbps full-duplex capability	RW	1
4.5	10BASE-T Half-Duplex	1 = 10 Mbps half-duplex capable 0 = No 10 Mbps half-duplex capability	RW	1
4.4:0	Selector Field	[00001] = IEEE 802.3	RW	0_0001
Register 5h – Auto-Negotiation Link Partner Ability				
5.15	Next Page	1 = Next page capable 0 = No next page capability	RO	0
5.14	Acknowledge	1 = Link code word received from partner 0 = Link code word not yet received	RO	0
5.13	Remote Fault	1 = Remote fault detected 0 = No remote fault	RO	0
5.12	Reserved	—	RO	0
5.11:10	Pause	[00] = No PAUSE [10] = Asymmetric PAUSE [01] = Symmetric PAUSE [11] = Asymmetric & Symmetric PAUSE	RO	00
5.9	100BASE-T4	1 = T4 capable 0 = No T4 capability	RO	0

TABLE 4-2: REGISTER DESCRIPTIONS (CONTINUED)

Address	Name	Description	Mode Note 4-1	Default
5.8	100BASE-TX Full-Duplex	1 = 100 Mbps full-duplex capable 0 = No 100 Mbps full-duplex capability	RO	0
5.7	100BASE-TX Half-Duplex	1 = 100 Mbps half-duplex capable 0 = No 100 Mbps half-duplex capability	RO	0
5.6	10BASE-T Full-Duplex	1 = 10 Mbps full-duplex capable 0 = No 10 Mbps full-duplex capability	RO	0
5.5	10BASE-T Half-Duplex	1 = 10 Mbps half-duplex capable 0 = No 10 Mbps half-duplex capability	RO	0
5.4:0	Selector Field	[00001] = IEEE 802.3	RO	0_0001
Register 6h – Auto-Negotiation Expansion				
6.15:5	Reserved	—	RO	0000_0000_000
6.4	Parallel Detection Fault	1 = Fault detected by parallel detection 0 = No fault detected by parallel detection.	RO/LH	0
6.3	Link Partner Next Page Able	1 = Link partner has next page capability 0 = Link partner does not have next page capability	RO	0
6.2	Next Page Able	1 = Local device has next page capability 0 = Local device does not have next page capability	RO	1
6.1	Page Received	1 = New page received 0 = New page not received yet	RO/LH	0
6.0	Link Partner Auto-Negotiation Able	1 = Link partner has auto-negotiation capability 0 = Link partner does not have auto-negotiation capability	RO	0
Register 7h – Auto-Negotiation Next Page				
7.15	Next Page	1 = Additional next page(s) will follow 0 = Last page	RW	0
7.14	Reserved	—	RO	0
7.13	Message Page	1 = Message page 0 = Unformatted page	RW	1
7.12	Acknowledge2	1 = Will comply with message 0 = Cannot comply with message	RW	0
7.11	Toggle	1 = Previous value of the transmitted link code word equaled logic one 0 = Logic zero	RO	0
7.10:0	Message Field	11-bit wide field to encode 2048 messages	RW	000_0000_0001
Register 8h – Link Partner Next Page Ability				
8.15	Next Page	1 = Additional Next Page(s) will follow 0 = Last page	RO	0
8.14	Acknowledge	1 = Successful receipt of link word 0 = No successful receipt of link word	RO	0
8.13	Message Page	1 = Message page 0 = Unformatted page	RO	0

TABLE 4-2: REGISTER DESCRIPTIONS (CONTINUED)

Address	Name	Description	Mode Note 4-1	Default
8.12	Acknowledge2	1 = Able to act on the information 0 = Not able to act on the information	RO	0
8.11	Toggle	1 = Previous value of transmitted link code word equal to logic zero 0 = Previous value of transmitted link code word equal to logic one	RO	0
8.10:0	Message Field	—	RO	000_0000_0000
Register 14h – MII Control				
14.15:8	Reserved	—	RO	0000_0000
14.7	100BASE-TX Preamble Restore	1 = Restore received preamble to MII output (random latency) 0 = Consume 1-byte preamble before sending frame to MII output for fixed latency	RW	0 or 1 (if CONFIG[2:0] = 100) See Table 2-2 for details.
14.6	10BASE-T Preamble Restore	1 = Restore received preamble to MII output 0 = Remove all 7-bytes of preamble before sending frame (starting with SFD) to MII output	RW	0
14.5:0	Reserved	—	RO	00_0001
Register 15h – RXER Counter				
15.15:0	RXER Counter	Receive error counter for Symbol Error frames	RO/SC	0000h
Register 1Bh – Interrupt Control/Status				
1B.15	Jabber Interrupt Enable	1 = Enable Jabber Interrupt 0 = Disable Jabber Interrupt	RW	0
1B.14	Receive Error Interrupt Enable	1 = Enable Receive Error Interrupt 0 = Disable Receive Error Interrupt	RW	0
1B.13	Page Received Interrupt Enable	1 = Enable Page Received Interrupt 0 = Disable Page Received Interrupt	RW	0
1B.12	Parallel Detect Fault Interrupt Enable	1 = Enable Parallel Detect Fault Interrupt 0 = Disable Parallel Detect Fault Interrupt	RW	0
1B.11	Link Partner Acknowledge Interrupt Enable	1 = Enable Link Partner Acknowledge Interrupt 0 = Disable Link Partner Acknowledge Interrupt	RW	0
1B.10	Link Down Interrupt Enable	1 = Enable Link Down Interrupt 0 = Disable Link Down Interrupt	RW	0
1B.9	Remote Fault Interrupt Enable	1 = Enable Remote Fault Interrupt 0 = Disable Remote Fault Interrupt	RW	0

TABLE 4-2: REGISTER DESCRIPTIONS (CONTINUED)

Address	Name	Description	Mode Note 4-1	Default
1B.8	Link Up Interrupt Enable	1 = Enable Link Up Interrupt 0 = Disable Link Up Interrupt	RW	0
1B.7	Jabber Interrupt	1 = Jabber occurred 0 = Jabber did not occur	RO/SC	0
1B.6	Receive Error Interrupt	1 = Receive Error occurred 0 = Receive Error did not occur	RO/SC	0
1B.5	Page Receive Interrupt	1 = Page Receive occurred 0 = Page Receive did not occur	RO/SC	0
1B.4	Parallel Detect Fault Interrupt	1 = Parallel Detect Fault occurred 0 = Parallel Detect Fault did not occur	RO/SC	0
1B.3	Link Partner Acknowl-edge Interrupt	1 = Link Partner Acknowledge occurred 0 = Link Partner Acknowledge did not occur	RO/SC	0
1B.2	Link Down Interrupt	1 = Link Down occurred 0 = Link Down did not occur	RO/SC	0
1B.1	Remote Fault Interrupt	1 = Remote Fault occurred 0 = Remote Fault did not occur	RO/SC	0
1B.0	Link Up Interrupt	1 = Link Up occurred 0 = Link Up did not occur	RO/SC	0
Register 1Dh – LinkMD Control/Status				
1D.15	Cable Diagnostic Test Enable	1 = Enable cable diagnostic test. After test has completed, this bit is self-cleared. 0 = Indicates cable diagnostic test (if enabled) has completed and the status information is valid for read.	RW/SC	0
1D.14:13	Cable Diagnostic Test Result	[00] = normal condition [01] = open condition has been detected in cable [10] = short condition has been detected in cable [11] = cable diagnostic test has failed	RO	00
1D.12:9	Reserved	—	—	0000
1D.8:0	Cable Fault Counter	Distance to fault; it's approximately 0.4m*(Cable Fault Counter value in decimal)	RO	0_0000_0000
Register 1Eh – PHY Control 1				
1E15:14	LED Mode	[00] = LED1: Speed; LED0: Link/Activity [01] = LED1: Activity; LED0: Link [10], [11] = Reserved	RW	00
1E.13	Polarity	0 = Polarity is not reversed 1 = Polarity is reversed	RO	—
1E.12	Far-End Fault Detect	0 = Far-End Fault not detected 1 = Far-End Fault detected This bit applies to KSZ8041FTL fiber only.	RO	0
1E.11	MDI/MDI-X State	0 = MDI 1 = MDI-X	RO	—
1E.10:8	Reserved	—	—	—

TABLE 4-2: REGISTER DESCRIPTIONS (CONTINUED)

Address	Name	Description	Mode Note 4-1	Default
1E.7	Remote Loopback	0 = Normal mode 1 = Remote (analog) loopback is enable	RW	0
1E.6:0	Reserved	—	—	—
Register 1Fh – PHY Control 2				
1F.15	HP_MDIX	0 = Microchip Auto MDI/MDI-X mode 1 = HP Auto MDI/MDI-X mode	RW	1
1F.14	MDI/MDI-X Select	When Auto MDI/MDI-X is disabled, 0 = MDI Mode Transmit on TX+/- (pins 12,11) and Receive on RX+/- (pins 10,9) 1 = MDI-X Mode Transmit on RX+/- (pins 10,9) and Receive on TX+/- (pins 12,11)	RW	0
1F.13	Pairswap Disable	1 = Disable auto MDI/MDI-X 0 = Enable auto MDI/MDI-X	RW	0
1F.12	Energy Detect	1 = Presence of signal on RX+/- analog wire pair 0 = No signal detected on RX+/-	RO	0
1F.11	Force Link	1 = Force link pass 0 = Normal link operation This bit bypasses the control logic and allows transmitter to send pattern even if there is no link.	RW	0
1F.10	Power Saving	1 = Enable power saving 0 = Disable power saving If power saving mode is enabled and the cable is disconnected, the RXC clock output (in MII mode) is disabled. RXC clock is enabled after the cable is connected and link is established.	RW	0
1F.9	Interrupt Level	1 = Interrupt pin active-high 0 = Interrupt pin active-low	RW	0
1F.8	Enable Jabber	1 = Enable jabber counter 0 = Disable jabber counter	RW	1
1F.7	Auto-Negotiation Complete	1 = Auto-negotiation process completed 0 = Auto-negotiation process not completed	RO	0
1F.6	Enable Pause (Flow Control)	1 = Flow control capable 0 = No flow control capability	RO	0
1F.5	PHY Isolate	1 = PHY in isolate mode 0 = PHY in normal operation	RO	0
1F.4:2	Operation Mode Indication	[000] = Still in auto-negotiation [001] = 10BASE-T half-duplex [010] = 100BASE-TX half-duplex [011] = Reserved [101] = 10BASE-T full-duplex [110] = 100BASE-TX full-duplex [111] = Reserved	RO	000
1F.1	Enable SQE Test	1 = Enable SQE test 0 = Disable SQE test	RW	0
1F.0	Disable Data Scrambling	1 = Disable scrambler 0 = Enable scrambler	RW	0

Note 4-1 RW = Read/Write; RO = Read Only; SC = Self-Cleared; LH = Latch High; LL = Latch Low

5.0 OPERATIONAL CHARACTERISTICS

5.1 Absolute Maximum Ratings*

Supply Voltage ($V_{DD\_1.8}$, $V_{DDA\_1.8}$, $V_{1.8\_OUT}$) ..... –0.5V to +2.4V

Supply Voltage ($V_{DDIO\_3.3}$, $V_{DDA\_3.3}$) ..... –0.5V to +4.0V

Input Voltage (All Inputs) ..... –0.5V to +4.0V

Output Voltage (All Outputs) ..... –0.5V to +4.0V

Lead Temperature (soldering, 10s) ..... +260°C

Storage Temperature (T_S) ..... –55°C to +150°C

*Exceeding the absolute maximum rating may damage the device. Stresses greater than the absolute maximum rating may cause permanent damage to the device. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

5.2 Operating Ratings**

Supply Voltage ($V_{DDIO\_3.3}$, $V_{DDA\_3.3}$) ..... +3.135V to +3.465V

Ambient Operating Temperature (T_A)

(Commercial) ..... 0°C to +70°C

(Industrial) ..... –40°C to +85°C

Maximum Junction Temperature (T_J) ..... +125°C

Thermal Resistance

Junction-to-Ambient (Θ_{JA}) ..... +69.64°C/W

Junction-to-Case (Θ_{JC}) ..... +15°C/W

**The device is not guaranteed to function outside its operating ratings.

Note:	Do not drive input signals without power supplied to the device.

6.0 ELECTRICAL CHARACTERISTICS

T_A = 25°C. Specification is for packaged product only.

TABLE 6-1: ELECTRICAL CHARACTERISTICS

Parameters	Symbol	Min.	Typ.	Max.	Units	Note
Supply Current (Note 6-1)						
100BASE-TX	I_{DD1}	—	53.0	58.3	mA	Chip only (no transformer); Full-duplex traffic @ 100% utilization
10BASE-T	I_{DD2}	—	38.0	41.8	mA	Chip only (no transformer); Full-duplex traffic @ 100% utilization
Power Saving Mode	I_{DD3}	—	32.0	35.2	mA	Ethernet cable disconnected (reg. 1F.10 = 1)
Power Down Mode	I_{DD4}	—	4.0	4.4	mA	Software power down (reg. 0.11 = 1)
CMOS Inputs						
Input High Voltage	V_{IH}	2.0	—	—	V	—
Input Low Voltage	V_{IL}	—	—	0.8	V	—
Input Current	I_{IN}	—	–10	10	µA	V_{IN} = GND ~ V_{DDIO}
CMOS Outputs						
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH} = –4 mA
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 4 mA
Output Tri-State Leakage	$\|I_{OZ}\|$	—	—	10	µA	—
LED Outputs						
Output Drive Current	I_{LED}	—	8	—	mA	Each LED pin (LED0, LED1)
100BASE-TX Transmit (measured differentially after 1:1 transformer)						
Peak Differential Output Voltage	V_O	0.95	—	1.05	V	100Ω termination across differential output
Output Voltage Imbalance	V_{IMB}	—	—	2	%	100Ω termination across differential output
Rise/Fall Time	t_r/t_f	3	—	5	ns	—
Rise/Fall Time Imbalance	—	0	—	0.5	ns	—
Duty Cycle Distortion	—	—	—	±0.25	ns	—
Overshoot	—	—	—	5	%	—
Reference Voltage of I_{SET}	V_{SET}	—	0.65	—	V	—
Output Jitter	—	—	0.7	1.4	ns	Peak-to-Peak
10BASE-T Transmit (measured differentially after 1:1 transformer)						
Peak Differential Output Voltage	V_P	2.2	—	2.8	V	100Ω termination across differential output
Jitter Added	—	—	—	3.5	ns	Peak-to-Peak
Rise/Fall Time	t_r/t_f	—	25	—	ns	—
10BASE-T Receive						
Squelch Threshold	V_{SQ}	—	400	—	mV	5 MHz square wave

Note 6-1 Current consumption is for the single 3.3V supply KSZ8041TL/FTL/MLL device only, and includes the 1.8V supply voltage ($V_{DD\_1.8}$, $V_{DDA\_1.8}$, $V_{1.8\_OUT}$) that is provided by the KSZ8041TL/FTL/MLL. The PHY port's transformer consumes an additional 45 mA @ 3.3V for 100BASE-TX and 70 mA @ 3.3V for 10BASE-T.

7.0 TIMING SPECIFICATIONS

7.1 MII SQE Timing (10BASE-T)

FIGURE 7-1: MII SQE TIMING (10BASE-T)

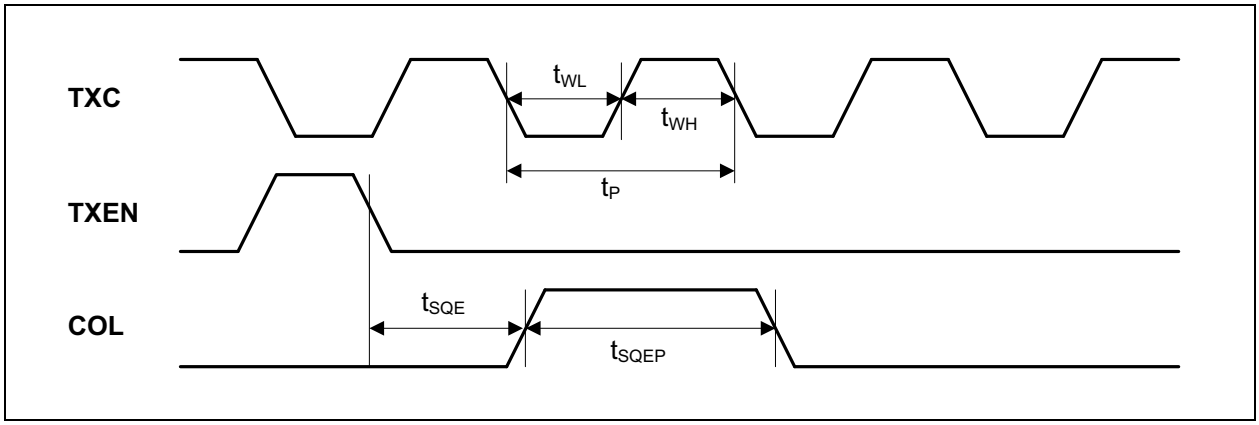


TABLE 7-1: MII SQE TIMING (10BASE-T) PARAMETERS

Symbol	Parameter	Min.	Typ.	Max.	Units
t_P	TXC period	—	400	—	ns
t_{WL}	TXC pulse width low	—	200	—	ns
t_{WH}	TXC pulse width high	—	200	—	ns
t_{SQE}	COL (SQE) delay after TXEN de-asserted	—	2.5	—	µs
t_{SQEP}	COL (SQE) pulse duration	—	1.0	—	µs

7.2 MII Transmit Timing (10BASE-T)

FIGURE 7-2: MII TRANSMIT TIMING (10BASE-T)

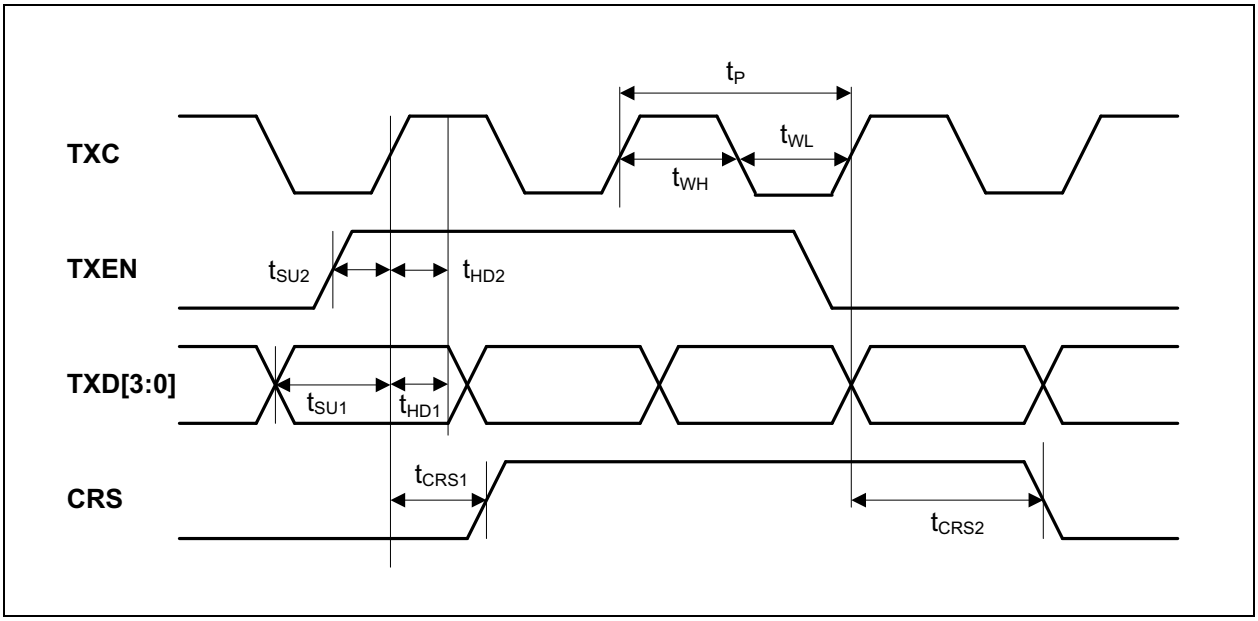


TABLE 7-2: MII TRANSMIT TIMING (10BASE-T) PARAMETERS

Symbol	Parameter	Min.	Typ.	Max.	Units
t_P	TXC period	—	400	—	
t_{WL}	TXC pulse width low	—	200	—	
t_{WH}	TXC pulse width high	—	200	—	
t_{SU1}	TXD[3:0] setup to rising edge of TXC	10	—	—	
t_{SU2}	TXEN setup to rising edge of TXC	10	—	—	
t_{HD1}	TXD[3:0] hold from rising edge of TXC	0	—	—	
t_{HD2}	TXEN hold from rising edge of TXC	0	—	—	
t_{CRS1}	TXEN high to CRS asserted latency	—	160	—	
t_{CRS2}	TXEN low to CRS de-asserted latency	—	510	—	

7.3 MII Receive Timing (10BASE-T)

FIGURE 7-3: MII RECEIVE TIMING (10BASE-T)

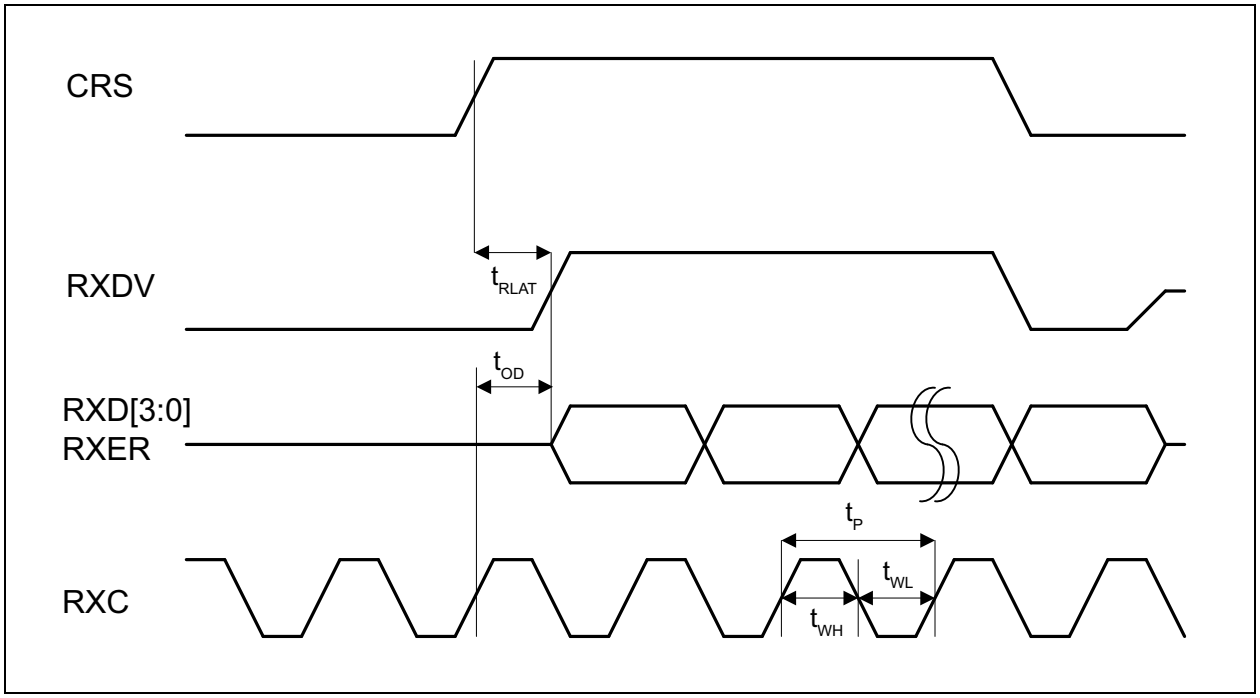


TABLE 7-3: MII RECEIVE TIMING (10BASE-T) PARAMETERS

Parameter	Description	Min.	Typ.	Max.	Units
t_P	RXC period	—	400	—	ns
t_{WL}	RXC pulse width low	—	200	—	ns
t_{WH}	RXC pulse width high	—	200	—	ns
t_{OD}	(RXD[3:0], RXER, RXDV) output delay from rising edge of RXC	182	—	225	ns
t_{RLAT}	CRS to (RXD[3:0], RXER, RXDV) latency	—	6.5	—	µs

7.4 MII Transmit Timing (100BASE-TX)

FIGURE 7-4: MII TRANSMIT TIMING (100BASE-TX)

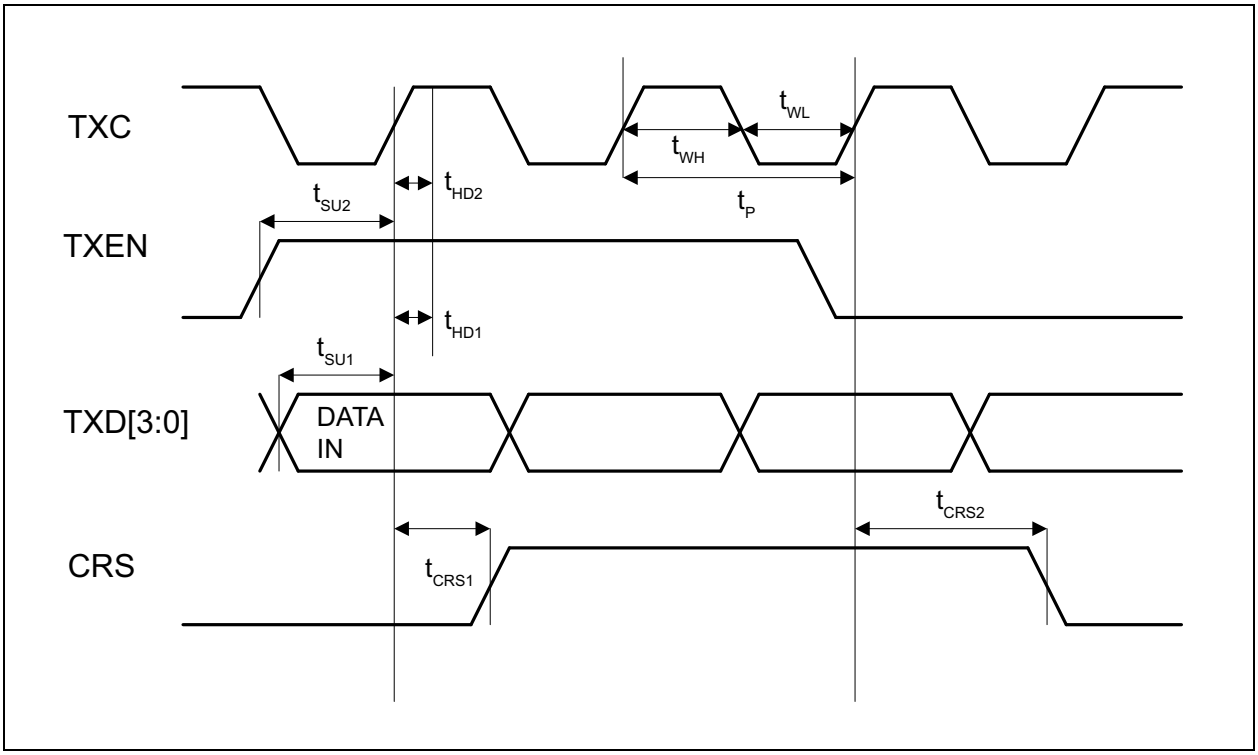


TABLE 7-4: MII TRANSMIT TIMING (100BASE-TX) PARAMETERS

Parameter	Description	Min.	Typ.	Max.	Units
t_P	TXC period	—	40	—	ns
t_{WL}	TXC pulse width low	—	20	—	ns
t_{WH}	TXC pulse width high	—	20	—	ns
t_{SU1}	TXD[3:0] setup to rising edge of TXC	10	—	—	ns
t_{SU2}	TXEN setup to rising edge of TXC	10	—	—	ns
t_{HD1}	TXD[3:0] hold from rising edge of TXC	0	—	—	ns
t_{HD2}	TXEN hold from rising edge of TXC	0	—	—	ns
t_{CRS1}	TXEN high to CRS asserted latency	—	34	—	ns
t_{CRS2}	TXEN low to CRS de-asserted latency	—	33	—	ns

7.5 MII Receive Timing (100BASE-TX)

FIGURE 7-5: MII RECEIVE TIMING (100BASE-TX)

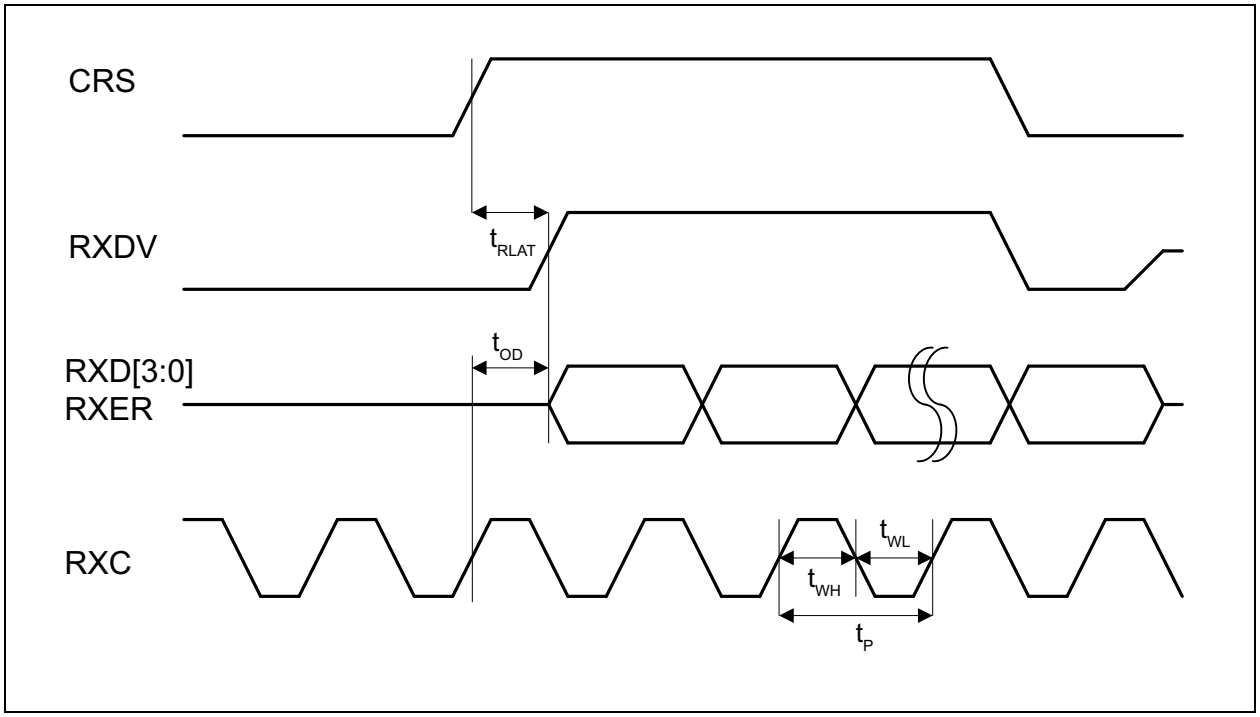


TABLE 7-5: MII RECEIVE TIMING (100BASE-TX) PARAMETERS

Parameter	Description	Min.	Typ.	Max.	Units
t_P	RXC period	—	40	—	ns
t_{WL}	RXC pulse width low	—	20	—	ns
t_{WH}	RXC pulse width high	—	20	—	ns
t_{OD}	(RXD[3:0], RXER, RXDV) output delay from rising edge of RXC	19	—	25	ns
t_{RLAT}	CRS to RXDV latency	—	140	—	ns
	CRS to RXD[3:0] latency	—	52	—	ns
	CRS to RXER latency	—	60	—	ns

7.6 RMII Timing

FIGURE 7-6: RMII TIMING – DATA RECEIVED FROM RMII

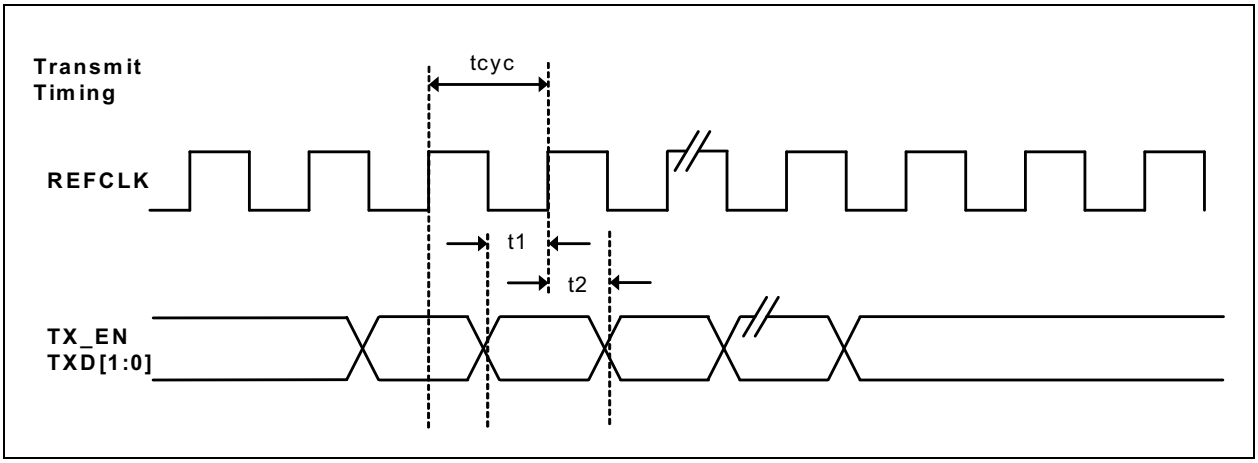


FIGURE 7-7: RMII TIMING – DATA INPUT TO RMII

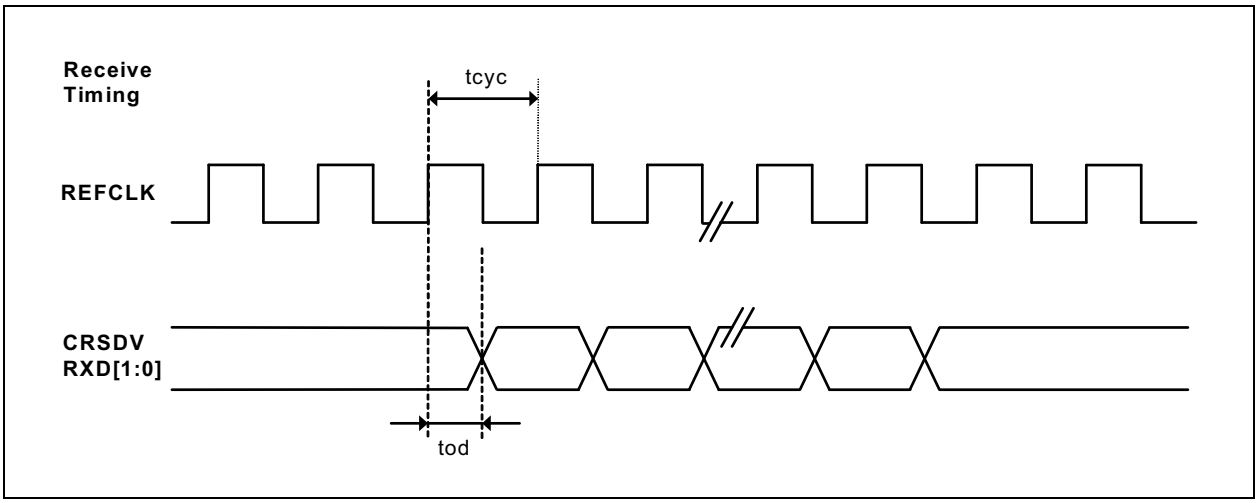


TABLE 7-6: RMII TIMING PARAMETERS

Parameter	Description	Min.	Typ.	Max.	Units
t_{CYC}	Clock cycle	—	20	—	ns
t_1	Setup time	4	—	—	ns
t_2	Hold time	2	—	—	ns
t_{OD}	Output delay	3	—	9	ns

7.7 SMII Timing

FIGURE 7-8: SMII TIMING – DATA RECEIVED FROM SMII

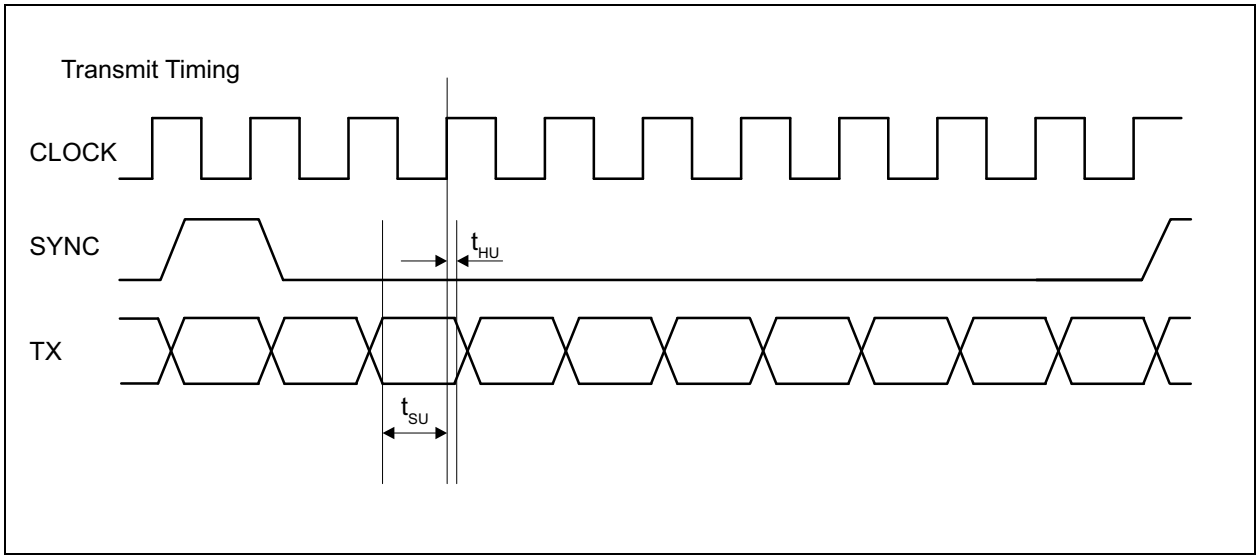


FIGURE 7-9: SMII TIMING – DATA INPUT TO SMII

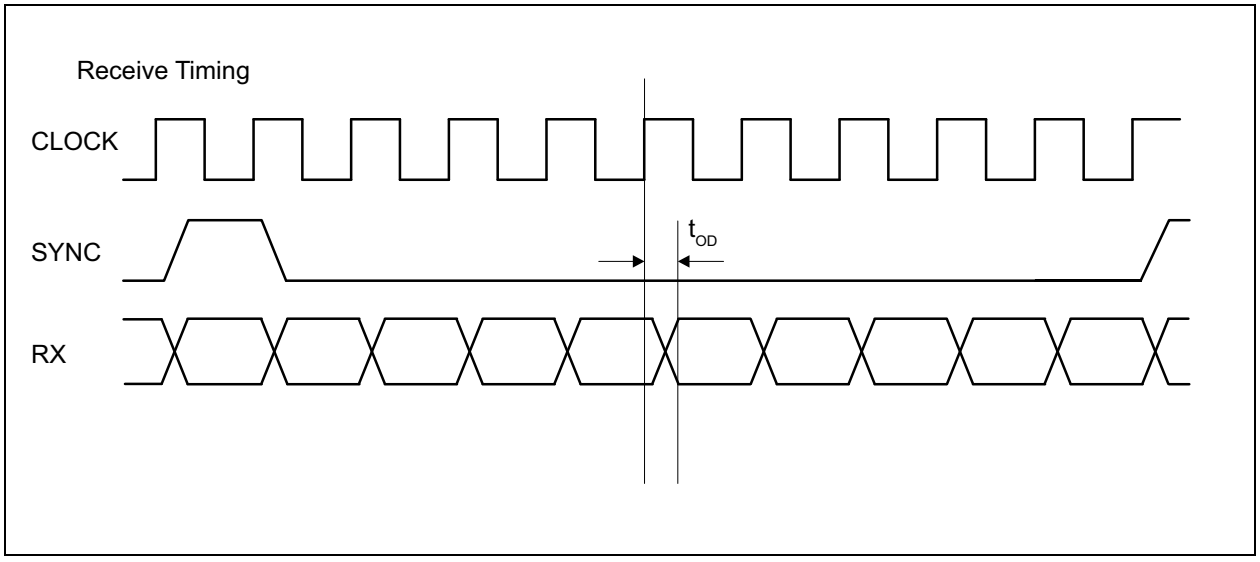


TABLE 7-7: SMII TIMING PARAMETERS

Parameter	Description	Min.	Typ.	Max.	Units
t_{SU}	Setup time	1.5	—	—	ns
t_{HD}	Hold time	1.0	—	—	ns
t_{OD}	Output delay	4.0	—	5.0	ns

7.8 Auto-Negotiation Timing

FIGURE 7-10: AUTO-NEGOTIATION FAST LINK PULSE (FLP) TIMING

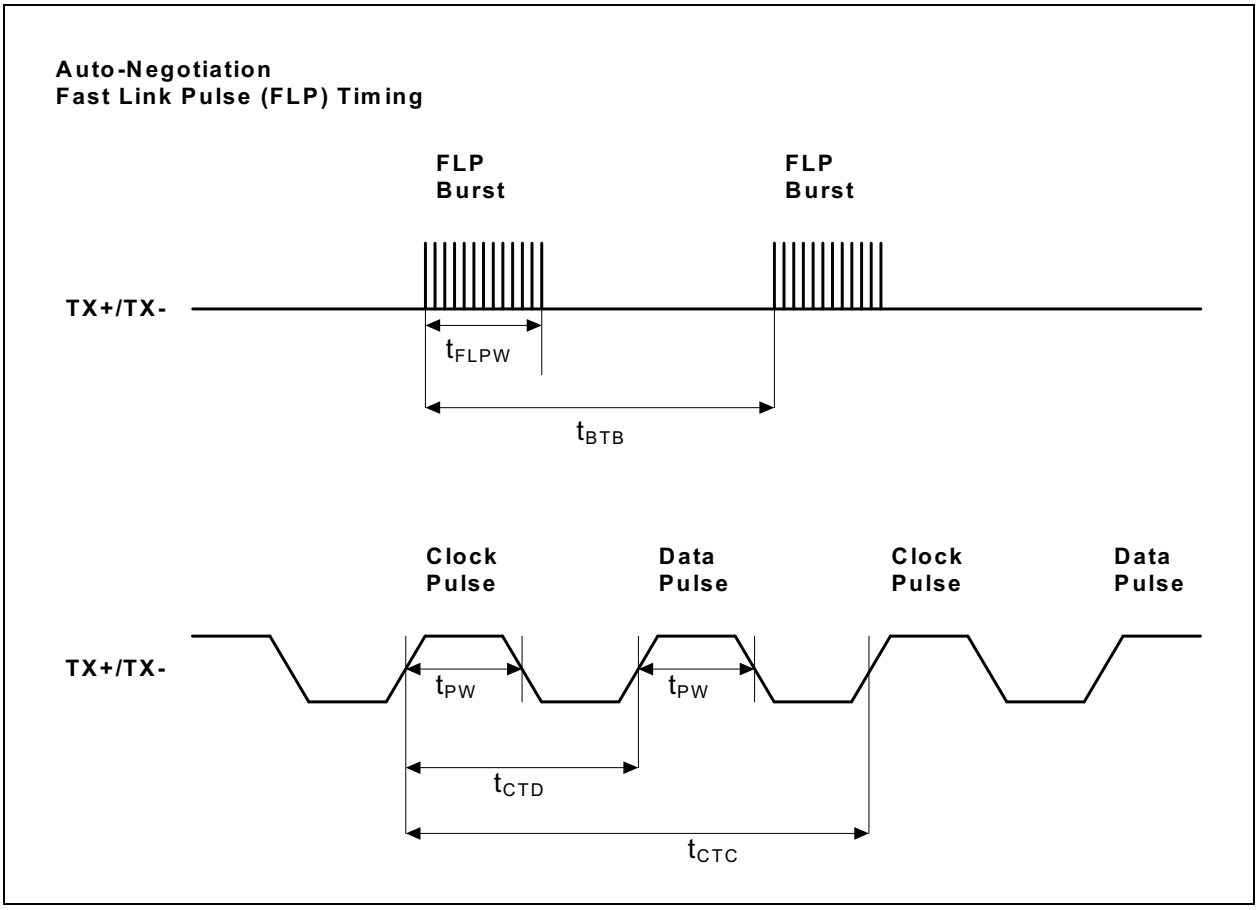


TABLE 7-8: AUTO-NEGOTIATION FAST LINK PULSE TIMING PARAMETERS

Parameter	Description	Min.	Typ.	Max.	Units
t_{BTB}	FLP Burst to FLP Burst	8	16	24	ms
t_{FLPW}	FLP Burst Width	—	2	—	ms
t_{PW}	Clock/Data Pulse Width	—	100	—	ns
t_{CTD}	Clock Pulse to Data Pulse	55.5	64	69.5	µs
t_{CTC}	Clock Pulse to Clock Pulse	111	128	139	µs
—	Number of Clock/Data Pulses per FLP Burst	17	—	33	—

7.9 MDC/MDIO Timing

FIGURE 7-11: MDC/MDIO TIMING

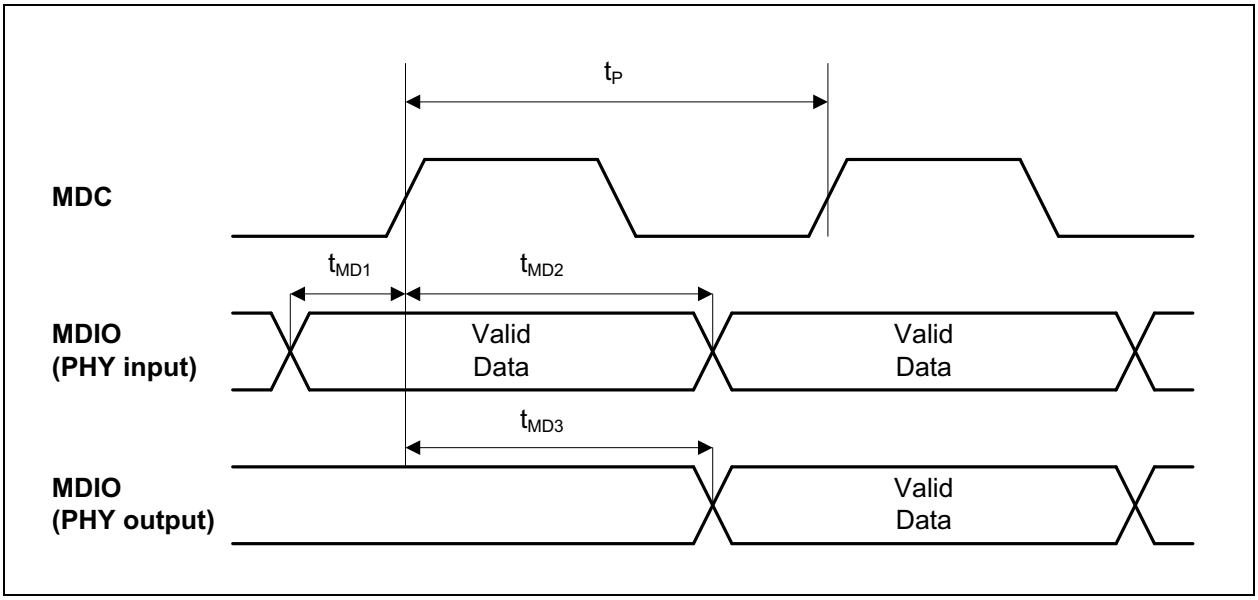


TABLE 7-9: MDC/MDIO TIMING PARAMETERS

Parameter	Description	Min.	Typ.	Max.	Units
t_P	MDC period	—	400	—	ns
t_{MD1}	MDIO (PHY input) setup to rising edge of MDC	10	—	—	ns
t_{MD2}	MDIO (PHY input) hold from rising edge of MDC	4	—	—	ns
t_{MD3}	MDIO (PHY output) delay from rising edge of MDC	—	222	—	ns

7.10 Reset Timing

The KSZ8041TL/FTL/MLL reset timing requirement is summarized in the following figure and table.

FIGURE 7-12: RESET TIMING

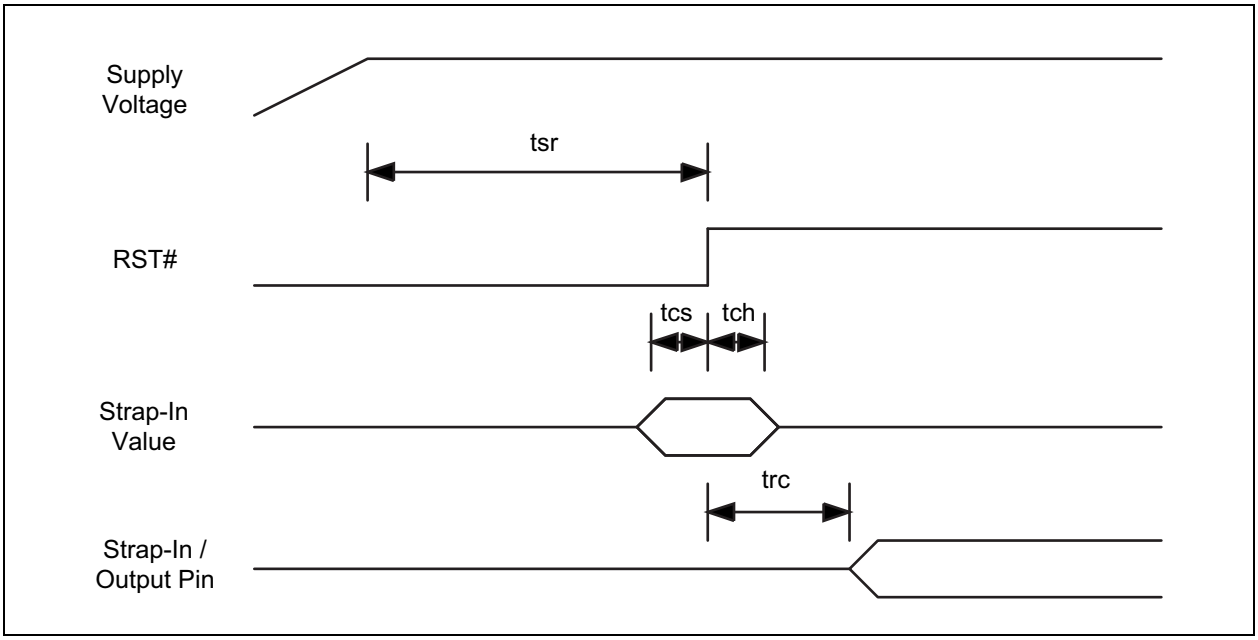


TABLE 7-10: RESET TIMING PARAMETERS

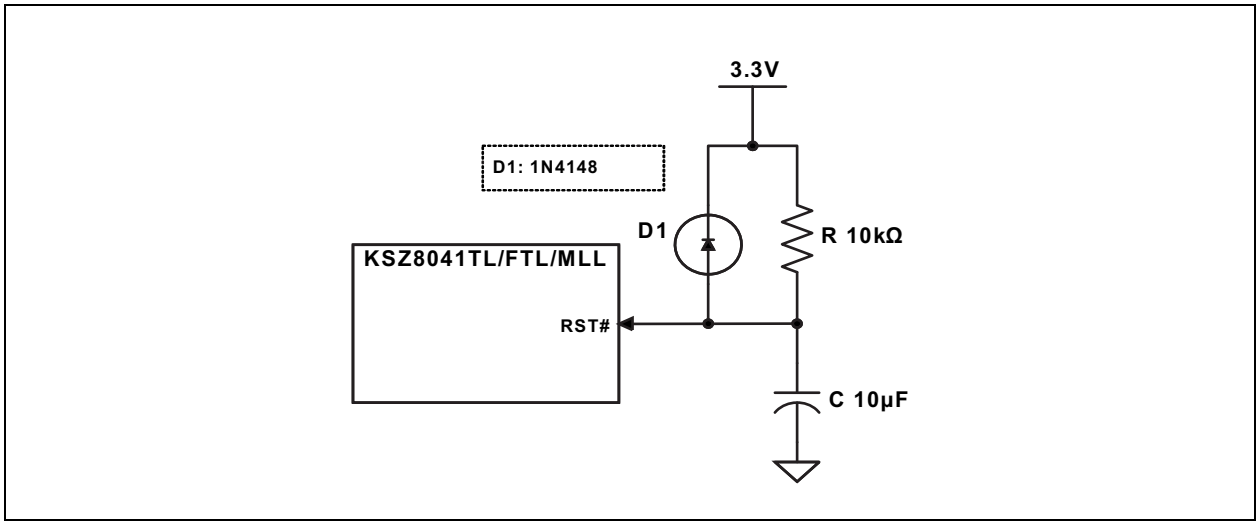
Parameter	Description	Min.	Typ.	Max.	Units
t_{SR}	Stable supply voltage to reset high	10	—	—	ms
t_{CS}	Configuration setup time	5	—	—	ns
t_{CH}	Configuration hold time	5	—	—	ns
t_{RC}	Reset to strap-in pin output	6	—	—	ns

After the de-assertion of reset, it is recommended to wait a minimum of 100 µs before starting programming on the MIIM (MDC/MDIO) Interface.

7.11 Reset Circuit

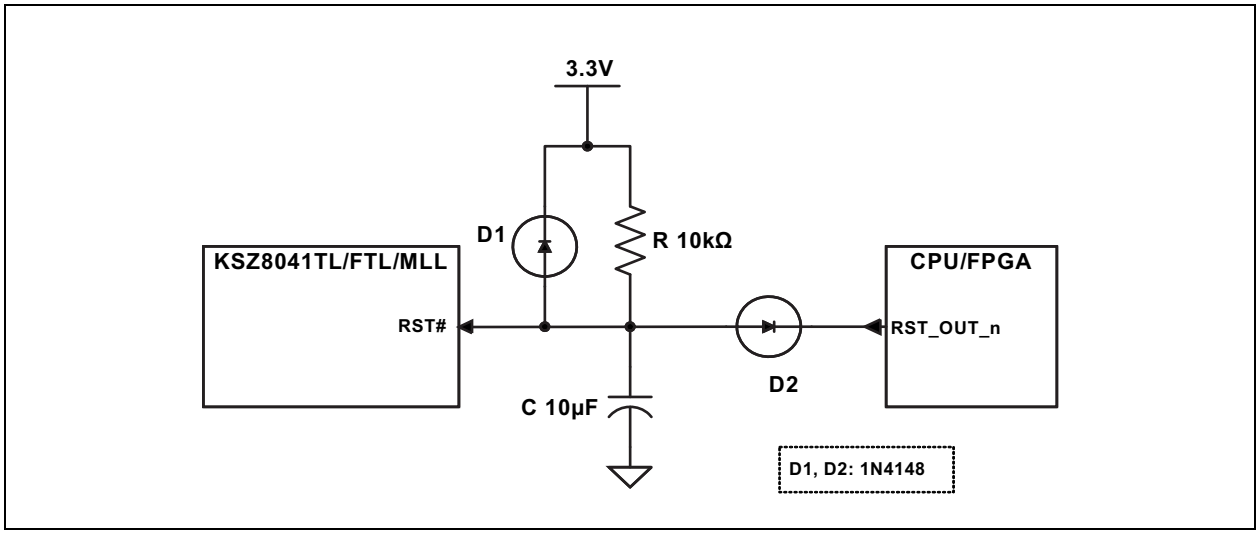
The following reset circuit is recommended for powering up the KSZ8041TL/FTL/MLL if reset is triggered by the power supply.

FIGURE 7-13: RECOMMENDED RESET CIRCUIT



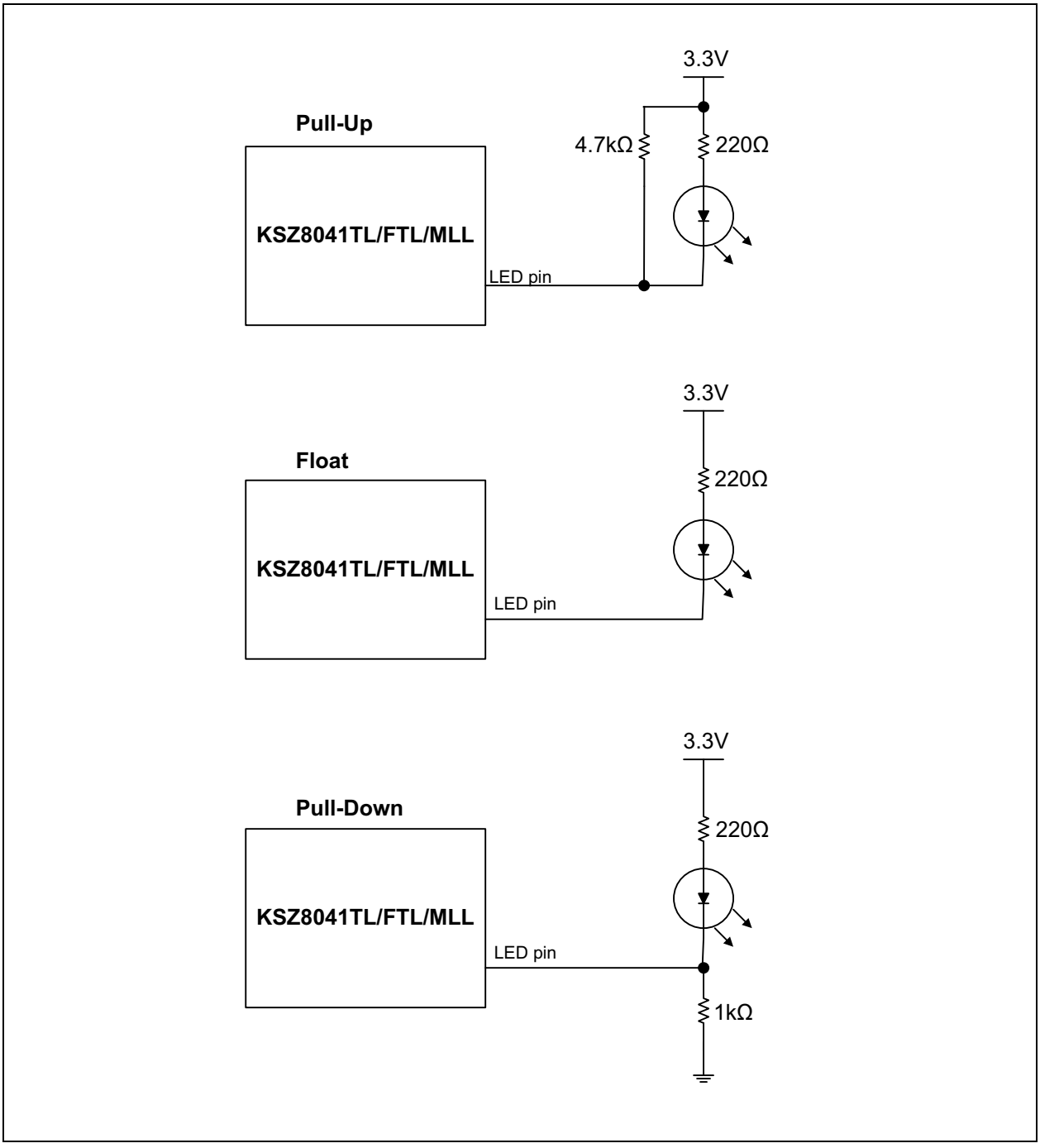
The following reset circuit is recommended for applications where reset is driven by another device (e.g., CPU or FPGA). At power-on-reset, R, C and D1 provide the necessary ramp rise time to reset the KSZ8041TL/FTL/MLL device. The RST_OUT_n from CPU/FPGA provides the warm reset after power up.

FIGURE 7-14: RECOMMENDED RESET CIRCUIT FOR INTERFACING WITH CPU/FPGA RESET OUTPUT



The following figure shows the reference circuits for pull-up, float and pull-down on the LED1 and LED0 strap-in pins.

FIGURE 7-15: REFERENCE CIRCUITS FOR LED STRAPPING PINS



8.0 SELECTION OF ISOLATION TRANSFORMERS

A 1:1 isolation transformer is required at the line interface. An isolation transformer with integrated common-mode choke is recommended for exceeding FCC requirements.

Table 8-1 lists recommended transformer characteristics.

TABLE 8-1: TRANSFORMER SELECTION CRITERIA

Parameter	Value	Test Conditions
Turns Ratio	1 CT:1 CT	—
Open-Circuit Inductance (min.)	350 µH	100 mV, 100 kHz, 8 mA
Leakage Inductance (max.)	0.4 µH	1 MHz (min.)
Interwinding Capacitance (max.)	12 pF	—
D.C. Resistance (max.)	0.9Ω	—
Insertion Loss (max.)	–1.0 dB	0 MHz to 65 MHz
HIPOT (min.)	1500 V_{RMS}	—

TABLE 8-2: QUALIFIED SINGLE-PORT MAGNETICS

Manufacturer	Part Number	Auto MDI-X
Bel Fuse	S558-5999-U7	Yes
Bel Fuse (Mag Jack)	SI-46001	Yes
Bel Fuse (Mag Jack)	SI-50170	Yes
Delta	LF8505	Yes
LanKom	LF-H41S	Yes
Pulse	H1102	Yes
Pulse (low cost)	H1260	Yes
Transpower	HB726	
TDK (Mag Jack)	TLA-6T718	

TABLE 8-3: TYPICAL REFERENCE CRYSTAL CHARACTERISTICS

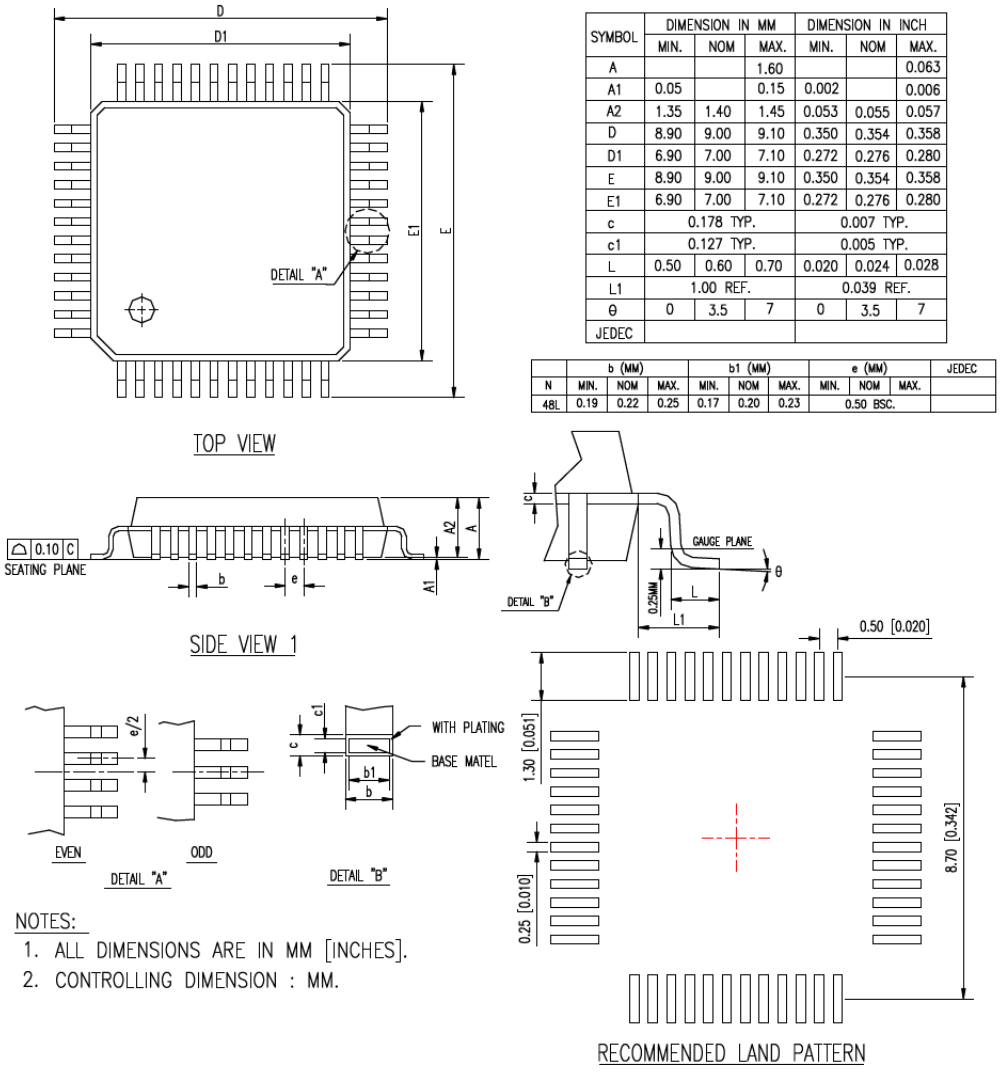
Characteristic	Value
Frequency	25 MHz
Frequency Tolerance (max.)	±50 ppm
Load Capacitance (max.)	20 pF
Series Resistance	40Ω

9.0 PACKAGE OUTLINE

FIGURE 9-1: 48-LEAD LQFP 7 MM X 7 MM PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

TITLE
48 LEAD LQFP 7x7mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	LQFP7x7-48LD-PL-1	UNIT	MM [INCHES]



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	8.90	9.00	9.10	0.350	0.354	0.358
D1	6.90	7.00	7.10	0.272	0.276	0.280
E	8.90	9.00	9.10	0.350	0.354	0.358
E1	6.90	7.00	7.10	0.272	0.276	0.280
c	0.178 TYP.			0.007 TYP.		
c1	0.127 TYP.			0.005 TYP.		
L	0.50	0.60	0.70	0.020	0.024	0.028
L1	1.00 REF.			0.039 REF.		
θ	0	3.5	7	0	3.5	7
JEDEC						

	b (MM)			b1 (MM)			e (MM)			JEDEC
N	MIN.	NOM	MAX.	MIN.	NOM	MAX.	MIN.	NOM	MAX.	
48L	0.19	0.22	0.25	0.17	0.20	0.23	0.50 BSC.			

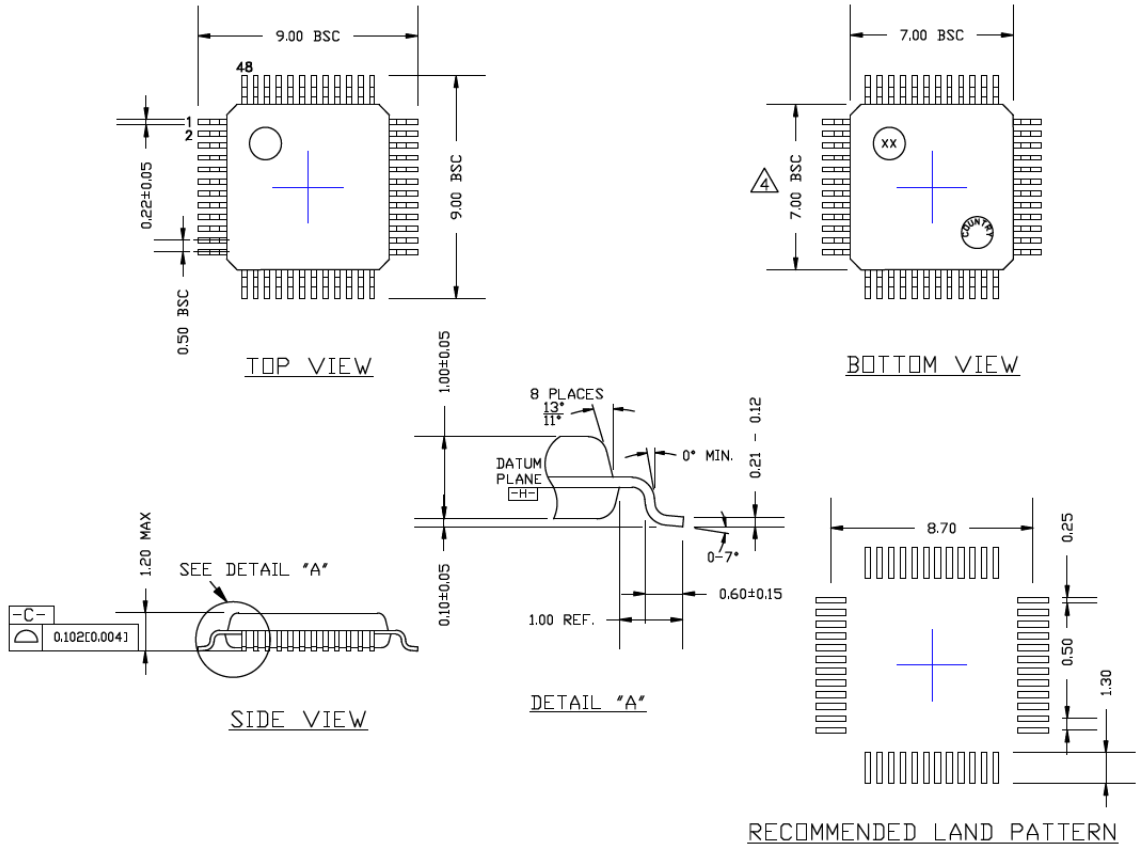
NOTES:
1. ALL DIMENSIONS ARE IN MM [INCHES].
2. CONTROLLING DIMENSION : MM.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

FIGURE 9-2: 48-LEAD TQFP 7 MM X 7 MM PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

TITLE
48 LEAD TQFP 7x7mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	TQFP7x7-48LD-PL-1	UNIT	MM



NOTES :
1. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.254MM.
2. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
3. PACKAGE TOP MOLD DIMENSIONS ARE SMALLER THAN BOTTOM
4. MOLD DIMENSIONS AND TOP OF PACKAGE WILL NOT OVERHANG BOTTOM OF PACKAGE.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00002436B (10-04-17)	Section 5.0, Operational Characteristics	Moved Maximum Junction Temperature information from Section 5.1, Absolute Maximum Ratings* to Section 5.2, Operating Ratings** for consistency with previous releases.
Rev. A (7-11-17)	—	Converted Micrel data sheet KSZ8041TL/FTL/MLL to Microchip DS00002436B. Minor text changes throughout.

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PART NO.	X	X	X	X	—	XX
Device	Interface	Package	Power Option	Temperature		Media Type

Device:	KSZ8041
Interface:	M = MII Interface <blank> = MII/RMII Interface F = MII/RMII Interface with 100BASE-FX Fiber
Package:	L = 48-Lead LQFP T = 48-Lead TQFP
Power Option:	L = Integrated LDO/LDO Controller/Regulator
Temperature:	<blank> = 0°C to +70°C (Commercial) I = –40°C to +85°C (Industrial)
Media Type:	<blank> = 250/Tray TR = 1,000/Reel S = Serial MII Interface, 250/Tray, Commercial Temp. Only, KSZ8041TL/FTL Only

Examples:

a) KSZ8041MLL:	MII Interface, 48-Lead LQFP, Integrated LDO, Commercial Temperature, 250/Tray
b) KSZ8041MLLI:	MII Interface, 48-Lead LQFP, Integrated LDO, Industrial Temperature, 250/Tray
c) KSZ8041MLL-TR:	MII Interface, 48-Lead LQFP, Integrated LDO, Commercial Temperature, 1,000/Reel
d) KSZ8041MLLI-TR:	MII Interface, 48-Lead LQFP, Integrated LDO, Industrial Temperature, 1,000/Reel
e) KSZ8041TL:	MII/RMII Interface, 48-Lead TQFP, Integrated LDO, Commercial Temperature, 250/Tray
f) KSZ8041TLI-S:	Serial MII Interface, 48-Lead TQFP, Integrated LDO, Industrial Temperature, 250/Tray
g) KSZ8041FTL-TR:	MII/RMII Interface with 100BASE-TX Fiber, 48-Lead TQFP, Integrated LDO, Commercial Temperature, 1,000/Reel
h) KSZ8041FTLI:	MII/RMII Interface with 100BASE-TX Fiber, 48-Lead TQFP, Integrated LDO, Industrial Temperature, 250/Tray
i) KSZ8041TL-TR:	MII/RMII Interface, 48-Lead TQFP, Integrated LDO, Commercial Temperature, 1,000/Reel
j) KSZ8041FTL-S:	Serial MII Interface, 48-Lead TQFP, Integrated LDO, Commercial Temperature, 250/Tray
k) KSZ8041TLI:	MII/RMII Interface, 48-Lead TQFP, Integrated LDO, Industrial Temperature, 250/Tray
l) KSZ8041FTL:	MII/RMII Interface with 100BASE-TX Fiber, 48-Lead TQFP, Integrated LDO, Commercial Temperature, 250/Tray

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