General Description

The MDRA1A16FI is a 16-bit, 80 MS/s analog-to-digital converter (ADC). The sampling rate as high as 95 MS/s can be achieved in an optional boost mode. If a lower speed operation is of interest the ADC power consumption can be considerably reduced without degrading the performance up to 55 MS/s.

A differential pipelined architecture with integrated output error digital correction logic provides 16-bit accuracy and guarantees no missing codes over the full operating temperature range.

A differential clock input with a selectable internal 1-to-8 divide ratio controls all internal conversion cycles. An optional duty cycle stabilizer compensates for wide variations of the input clock duty cycle.

The ADC output data format is either parallel CMOS or LVDS (DDR). A data output clock is provided to ensure proper latch timing with receiving logic. Any CMOS levels between 1.8 V and 3.3 V are supported.

Applications

- Communications and Cellular Base Stations
- Software Defined Radios
- Medical Imaging
- Radar and Ultrasound Equipment
- High-Performance Data Acquisition

Features

- 95 MS/s in optional boost mode and 55 MS/s in reduced power mode
- SNR 75 dBFS @ 10 MHz up to 95 MS/s, and 76.9 dBFS with external voltage reference 1.25 V
- SFDR 96 dBc @ 10 MHz and 80 MS/s
- IMD3 -92 dBc @ 75 MHz and 95 MS/s at -7 dBFS
- Power dissipation 0.55 W @ 80 MS/s, and 0.34 W @ 55 MS/s in reduced power mode
- Noise spectral density -154 dBFS/Hz at 80 MS/s
- Differential analog inputs with 693 MHz bandwidth
- Operation from a single 1.8 V power supply
- No time-interleaving or foreground calibration
- Flexible analog input range: 1 V p-p to 2 V p-p (up to 2.5 V p-p with external voltage reference)
- Programmable internal ADC voltage reference
- CMOS 1.8 – 3.3 V or LVDS output
- Serial port interface
- ADC clock duty cycle stabilizer
- Integer 1-to-8 input clock divider
- Temperature range of -40°C to +85°C
- 48-Pin (7mm x 7mm) QFN Package with an exposed pad

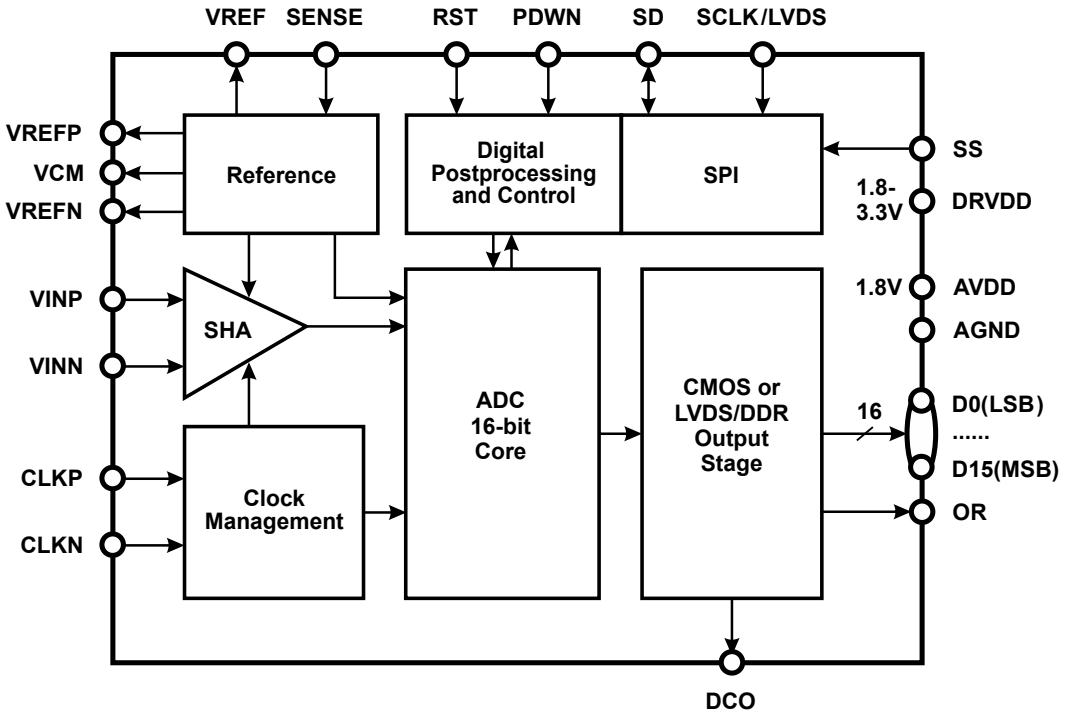

Figure 1 – Functional Block Diagram

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Specifications

ADC DC Specifications

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = -1.0 dBFS differential input, 1.0 V internal reference, DCS disabled, Divide-by-1 Input Clock Mode, unless otherwise noted[1].

Table 1. Default Mode (80 MS/s) DC Specification

Parameter	Min	Typ	Max	Temp	Unit
RESOLUTION	16			Full	Bits
ACCURACY					
No Missing Codes		Guaranteed		Full	
Offset Error	-0.25	-0.02	+0.25	Full	% FSR
Gain Error	-8		+8	Full	% FSR
Differential Nonlinearity (DNL)	-1.0		+1.2	Full	LSB
	-0.8		+0.6	25°C	LSB
Integral Nonlinearity (INL)	-5.0		+5.0	Full	LSB
		±3.0		25°C	LSB
INTERNAL VOLTAGE REFERENCE					
Output Voltage at the VREF pin (1 V Mode)	0.95	0.998	1.05	Full	V
Output Voltage at the VREF pin (0.5 V Mode)	0.47	0.495	0.53	Full	V
Load Regulation at 1.0 mA		1.6		25°C	mV
INPUT REFFERED NOISE					
VREF = 1.0 V		3.9		25°C	LSB rms
External VREF = 1.25 V		3.1		25°C	LSB rms
ANALOG INPUT					
Input Span, VREF = 1.0 V		2		Full	V p-p
Input Capacitance[2]		14		25°C	pF
Input Common-Mode Voltage		0.9		Full	V

[1] Full temperature range in the table means also that AVDD is within 1.7-1.9V, DRVDD is within 1.62-1.98V (CMOS) or 1.7-1.9V (LVDS)
[2] Input capacitance refers to the effective capacitance between one differential input pin and AGND

Parameter	Min	Typ	Max	Temp	Unit
POWER SUPPLIES					
Supply Voltage					
AVDD	1.7	1.8	1.9	Full	V
DRVDD					
LVDS Output Mode	1.7	1.8	1.9	Full	V
CMOS Output Mode[3]	1.62	1.8	3.6	Full	V
Supply Current					
IAVDD[4]		303	330	Full	mA
IDRVDD[4]					
1.8V LVDS ANSI		40	50	Full	mA
1.8V CMOS		16	22	Full	mA
3.3V CMOS		31	36	Full	mA
POWER CONSUMPTION					
DC Input		547		25°C	mW
Sine Wave Input[4]					
DRVDD = 1.8 V					
CMOS Output Mode		574		25°C	mW
LVDS Output Mode		617		25°C	mW
Power-Down Power		0.06[5]		25°C	mW

[3] For DRVDD above 1.98V the ADC's dynamic performance may degrade (refer to section "Digital Output Modes")
[4] Measured with a -1 dBFS, 10 MHz sine wave, and approximately 4.2 pF loading on each output bit
[5] The input clock is not applied

Table 2. Reduced Power and Boost Mode DC Specification

Parameter	RP MODE Min	RP MODE Typ	RP MODE Max	BOOST MODE Min	BOOST MODE Typ	BOOST MODE Max	Temp	Unit
RESOLUTION	16			16			Full	Bits
ACCURACY								
No Missing Codes		Guaranteed			Guaranteed		Full	
Differential Nonlinearity (DNL)	-1.0		1.5	-1.0		1.5	Full	LSB
	-0.75		0.4	-0.8		0.6	25°C	LSB
Integral Nonlinearity (INL)	-4.5		4.5	-8.0		8.0	Full	LSB
		±2.3			±3.2		25°C	LSB
INPUT REFFERED NOISE								
VREF = 1.0 V		3.9			3.9		25°C	LSB rms
External VREF = 1.25 V		3.2			3.1		25°C	LSB rms
POWER SUPPLIES								
Supply Voltage								
AVDD	1.7	1.8	1.9	1.7	1.8	1.9	Full	V
DRVDD								
LVDS Output Mode	1.7	1.8	1.9	1.7	1.8	1.9	Full	V
CMOS Output Mode[3]	1.62	1.8	3.6	1.62	1.8	3.6	Full	V
Supply Current								
IAVDD[4]		190	210		341	365	Full	mA
IDRVDD[4]								
1.8V LVDS ANSI		39	50		41	50	Full	mA
1.8V CMOS		12	15		18	25	Full	mA
3.3V CMOS		22	30		35	45	Full	mA
POWER CONSUMPTION								
DC Input		344			617		25°C	mW
Sine Wave Input[4]								
DRVDD = 1.8 V								
CMOS Output Mode		364			646		25°C	mW
LVDS Output Mode		412			688		25°C	mW
Power-Down Power		0.06[5]			0.06[5]		25°C	mW

ADC AC Specifications

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = -1.0 dBFS differential input, 1.0 V internal reference, DCS disabled, Divide-by-1 Input Clock Mode, unless otherwise noted[1].

Table 3. Default Mode (80 MS/s) AC Specification

Parameter	Min	Typ	Max	Temp	Unit
SIGNAL-TO-NOISE-RATIO (SNR)					
f_{IN} = 10 MHz					
VREF = 1.0 V		75.0		25°C	dBFS
	74.0			Full	dBFS
External VREF = 1.25 V		76.8		25°C	dBFS
	76.0			Full	dBFS
f_{IN} = 75 MHz					
VREF = 1.0 V		73.0		25°C	dBFS
	71.4			Full	dBFS
External VREF = 1.25 V		74.0		25°C	dBFS
	72.2			Full	dBFS
f_{IN} = 140 MHz		70.1		25°C	dBFS
SIGNAL-TO-NOISE-AND-DISTORTION (SNDR)					
f_{IN} = 10 MHz					
VREF = 1.0 V		74.9		25°C	dBFS
	73.8			Full	dBFS
External VREF = 1.25 V		76.7		25°C	dBFS
	75.8			Full	dBFS
f_{IN} = 75 MHz					
VREF = 1.0 V		72.5		25°C	dBFS
	70.0			Full	dBFS
External VREF = 1.25 V		72.6			
	70.5			Full	dBFS
f_{IN} = 140 MHz		67.5		25°C	dBFS
EFFECTIVE NUMBER OF BITS (ENOB)					
f_{IN} = 10 MHz		12.1		25°C	Bits
f_{IN} = 75 MHz		11.8		25°C	Bits
f_{IN} = 140 MHz		10.9		25°C	Bits

Parameter	Min	Typ	Max	Temp	Unit
SPURIOUS-FREE DYNAMIC RANGE (SFDR)					
f_{IN} = 10 MHz					
VREF = 1.0 V		96		25°C	dBc
	87			Full	dBc
External VREF = 1.25 V		92		25°C	dBc
	85			Full	dBc
f_{IN} = 75 MHz					
VREF = 1.0 V		82		25°C	dBc
	76			Full	dBc
External VREF = 1.25 V		77		25°C	dBc
	72			Full	dBc
f_{IN} = 140 MHz		71		25°C	dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)					
AIN at -23 dBFS					
f_{IN} = 10 MHz		94		25°C	dBFS
f_{IN} = 75 MHz		94		25°C	dBFS
f_{IN} = 140 MHz		92		25°C	dBFS
WORST SECOND OR THIRD HARMONIC					
f_{IN} = 10 MHz		-96		25°C	dBc
f_{IN} = 75 MHz		-83		25°C	dBc
f_{IN} = 140 MHz		-71		25°C	dBc
WORST OTHER (HARMONIC OR SPUR)					
f_{IN} = 10 MHz		-102		25°C	dBc
f_{IN} = 75 MHz		-93		25°C	dBc
f_{IN} = 140 MHz		-94		25°C	dBc
NOISE SPECTRAL DENSITY (NSD)					
f_{IN} = 10 MHz					
VREF = 1.0 V		-154		25°C	dBFS/Hz
External VREF = 1.25 V		-156		25°C	dBFS/Hz

Parameter	Min	Typ	Max	Temp	Unit
TWO-TONE SFDR					
f_{IN} = 9.5 MHz (-7 dBFS), 10.5 MHz (-7 dBFS)		91		25°C	dBc
f_{IN} = 73.7 MHz (-7 dBFS), 76.3 MHz (-7 dBFS)		84		25°C	dBc
f_{IN} = 104.1 MHz (-7 dBFS), 106.1 MHz (-7 dBFS)		74		25°C	dBc
INTERMODULATION DISTORTION					
Third Order (IMD3)					
f_{IN} = 9.5 MHz (-7 dBFS), 10.5 MHz (-7 dBFS)		-92		25°C	dBc
f_{IN} = 73.7 MHz (-7 dBFS), 76.3 MHz (-7 dBFS)		-84		25°C	dBc
f_{IN} = 104.1 MHz (-7 dBFS), 106.1 MHz (-7 dBFS)		-74		25°C	dBc
Second Order (IMD2)					
f_{IN} = 9.5 MHz (-7 dBFS), 10.5 MHz (-7 dBFS)		-91		25°C	dBc
f_{IN} = 73.7 MHz (-7 dBFS), 76.3 MHz (-7 dBFS)		-90		25°C	dBc
f_{IN} = 104.1 MHz (-7 dBFS), 106.1 MHz (-7 dBFS)		-77		25°C	dBc
FULL POWER INPUT BANDWIDTH		693		25°C	MHz

Table 4. Reduced Power and Boost Mode AC Specification

Parameter	RP MODE Min	RP MODE Typ	RP MODE Max	BOOST MODE Min	BOOST MODE Typ	BOOST MODE Max	Temp	Unit
SIGNAL-TO-NOISE-RATIO (SNR)								
f_{IN} = 10 MHz								
VREF = 1.0 V		75.2			75.0		25°C	dBFS
	74.0			74.0			Full	dBFS
External VREF = 1.25 V		77.2			76.9		25°C	dBFS
	76.0			76.0			Full	dBFS
f_{IN} = 75 MHz								
VREF = 1.0 V		73.1			73.1		25°C	dBFS
	71.4			71.4			Full	dBFS
External VREF = 1.25 V		74.4			74.3		25°C	dBFS
	72.2			72.2			Full	dBFS
f_{IN} = 140 MHz		70.2			70.4		25°C	dBFS
SIGNAL-TO-NOISE-AND-DISTORTION (SNDR)								
f_{IN} = 10 MHz								
VREF = 1.0 V		75.1			74.8		25°C	dBFS
	73.8			73.8			Full	dBFS
External VREF = 1.25 V		76.9			76.5		25°C	dBFS
	75.8			75.8			Full	dBFS
f_{IN} = 75 MHz								
VREF = 1.0 V		72.3			72.6		25°C	dBFS
	70.0			70.6			Full	dBFS
External VREF = 1.25 V		72.5			72.8			
	70.5			70.6			Full	dBFS
f_{IN} = 140 MHz		68.1			67.4		25°C	dBFS
EFFECTIVE NUMBER OF BITS (ENOB)								
f_{IN} = 10 MHz		12.2			12.1		25°C	Bits
f_{IN} = 75 MHz		11.7			11.8		25°C	Bits
f_{IN} = 140 MHz		11.0			10.9		25°C	Bits

Parameter	RP MODE Min	RP MODE Typ	RP MODE Max	BOOST MODE Min	BOOST MODE Typ	BOOST MODE Max	Temp	Unit
SPURIOUS-FREE DYNAMIC RANGE (SFDR)								
f_{IN} = 10 MHz								
VREF = 1.0 V		94			86		25°C	dBc
	88			84			Full	dBc
External VREF = 1.25 V		91			92		25°C	dBc
	85			84			Full	dBc
f_{IN} = 75 MHz								
VREF = 1.0 V		81			85		25°C	dBc
	76			75			Full	dBc
External VREF = 1.25 V		78			80		25°C	dBc
	73			72			Full	dBc
f_{IN} = 140 MHz		72			70		25°C	dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)								
AIN at -23 dBFS								
f_{IN} = 10 MHz		98			96		25°C	dBFS
f_{IN} = 75 MHz		102			96		25°C	dBFS
f_{IN} = 140 MHz		97			102		25°C	dBFS
WORST SECOND OR THIRD HARMONIC								
f_{IN} = 10 MHz		-94			-86		25°C	dBc
f_{IN} = 75 MHz		-81			-85		25°C	dBc
f_{IN} = 140 MHz		-72			-70		25°C	dBc
WORST OTHER (HARMONIC OR SPUR)								
f_{IN} = 10 MHz		-99			-98		25°C	dBc
f_{IN} = 75 MHz		-93			-94		25°C	dBc
f_{IN} = 140 MHz		-95			-92		25°C	dBc
NOISE SPECTRAL DENSITY (NSD)								
f_{IN} = 10 MHz								
VREF = 1.0 V		-152			-155		25°C	dBFS/ Hz
External VREF = 1.25 V		-154			-157		25°C	dBFS/ Hz

Parameter	RP MODE Min	RP MODE Typ	RP MODE Max	BOOST MODE Min	BOOST MODE Typ	BOOST MODE Max	Temp	Unit
TWO-TONE SFDR								
f_{IN} = 9.5 MHz (-7 dBFS), 10.5 MHz (-7 dBFS)		94			90		25°C	dBc
f_{IN} = 73.7 MHz (-7 dBFS), 76.3 MHz (-7 dBFS)		82			87		25°C	dBc
f_{IN} = 104.1 MHz (-7 dBFS), 106.1 MHz (-7 dBFS)		78			83		25°C	dBc
INTERMODULATION DISTORTION								
Third Order (IMD3)								
f_{IN} = 9.5 MHz (-7 dBFS), 10.5 MHz (-7 dBFS)		-98			-90		25°C	dBc
f_{IN} = 73.7 MHz (-7 dBFS), 76.3 MHz (-7 dBFS)		-86			-92		25°C	dBc
f_{IN} = 104.1 MHz (-7 dBFS), 106.1 MHz (-7 dBFS)		-82			-76		25°C	dBc
Second Order (IMD2)								
f_{IN} = 9.5 MHz (-7 dBFS), 10.5 MHz (-7 dBFS)		-94			-91		25°C	dBc
f_{IN} = 73.7 MHz (-7 dBFS), 76.3 MHz (-7 dBFS)		-82			-87		25°C	dBc
f_{IN} = 104.1 MHz (-7 dBFS), 106.1 MHz (-7 dBFS)		-78			-80		25°C	dBc
FULL POWER INPUT BANDWIDTH		698			698		25°C	MHz

Digital Specifications

AVDD, DRVDD within available range, maximum sampling rate, VIN = -1.0 dBFS differential input, 1.0 V internal reference, DCS disabled, Divide-by-1 Input Clock Mode, unless otherwise noted[1].

Table 5.

Parameter	Min	Typ	Max	Temp	Unit
DIFFERENTIAL CLOCK INPUTS (CLKP, CLKN)					
Logic Compliance		CMOS/LVDS/LVPECL			
Internal Common-Mode Bias		0.9		Full	V
Differential Input Voltage	0.4	0.8	3.6	Full	V p-p
Input Voltage Range	AGND		AVDD	Full	V
LOGIC PINS (RST, SCLK/LVDS, SS, SD)					
High Level Input Voltage (1.8 V / 3.3 V CMOS)	1.4 / 2.5		DRVDD	Full	V
Low Level Input Voltage	0		0.25	Full	V
High Level Input Current			4	Full	µA
Low Level Input Current	-4			Full	µA
High Level Output Voltage[6]					
1.8 V CMOS	1.5			Full	V
3.3 V CMOS	2.7			Full	V
Low Level Output Voltage[7]			0.1	Full	V
LOGIC INPUT (PWDN)[8]					
High Level Input Voltage (1.8 V / 3.3 V CMOS)	1.4 / 2.5		DRVDD	Full	V
Low Level Input Voltage	0		0.25	Full	V
High Level Input Current	4		15	Full	µA
Low Level Input Current	-4			Full	µA
High Level Output Voltage[6]					
1.8 V CMOS	1.5			Full	V
3.3 V CMOS	2.7			Full	V
Low Level Output Voltage[7]			0.1	Full	V

[6] At 1.0 mA load current
[7] At -1.0 mA load current
[8] Pull-down

Parameter	Min	Typ	Max	Temp	Unit
DIGITAL OUTPUTS					
1.8 V CMOS Mode					
High Level Output Voltage[7]	1.5			Full	V
Low Level Output Voltage[8]			0.1	Full	V
3.3 V CMOS Mode					
High Level Output Voltage[7]	2.7			Full	V
Low Level Output Voltage[8]			0.1	Full	V
LVDS ANSI Mode					
Differential Output Voltage	250		400	Full	mV
Output Offset Voltage	1.1		1.4	Full	V
LVDS Reduced Swing Mode					
Differential Output Voltage	150		250	Full	mV
Output Offset Voltage	1.1		1.4	Full	V

Switching Specifications

-1.0 dBFS differential input, 1.0 V internal reference, DCS disabled, Divide-by-1 Input Clock Mode, unless otherwise noted.

Table 6. Default Mode (80 MS/s) Switching Specification

Parameter	Min	Typ	Max	Temp	Unit
CLOCK INPUT PARAMETERS					
Input Clock Rate			480	Full	MHz
Conversion Rate[9]					
DCS Disabled	10		80	Full	MS/s
DCS Enabled	20		80	Full	MS/s
CLK Period – Divide-by-1 Mode (t_{clk})	12.5			Full	ns
CLK Pulse Width High – Divide-by-1 Mode					
DCS Disabled	6.1	6.25	6.4	Full	ns
DCS Enabled	4.38		6.75	Full	ns
CLK Pulse Width High – Divide-by-2 Mode, Divide-by-4 Mode, Divide-by-6 Mode, Divide-by-8 Mode, DSC Enabled or DCS Disabled	4.38		6.75	Full	ns
Aperture Delay[10]		1.4		25°C	ns
Aperture Uncertainty (Jitter)					
Divide-by-1 Mode, DCS Disabled		0.32		25°C	ps rms
Divide-by-1 Mode, DCS Enabled		0.34		25°C	ps rms
Divide-by-2,3,4,5,6,7,8 Mode, DCS Disabled		0.33		25°C	ps rms
Divide-by-3,5,7 Mode, DCS Enabled		0.38		25°C	ps rms
DATA OUTPUT PARAMETERS					
CMOS Mode					
Data Propagation Delay (t_{PD})	8.4		8.7	25°C	ns
DCO Propagation Delay (t_{DCO})		8.9		25°C	ns
DCO to Data Skew (t_{SKEW})	-0.5		-0.2	25°C	ns
Pipeline Delay (Latency)		11		Full	Cycles
LVDS Mode					
Data Propagation Delay (t_{PD})	8.0		8.3	25°C	ns
DCO Propagation Delay (t_{DCO})		8.3		25°C	ns
DCO to Data Skew (t_{SKEW})	-0.3		0	25°C	ns
Pipeline Delay (Latency)		11.5		Full	Cycles

[9] Conversion rate is the clock rate after the divider
[10] Measured with sine full-scale 80 MHz input clock

Table 7. Reduced Power and Boost Mode Switching Specification

Parameter	RP MODE			BOOST MODE			Temp	Unit
	Min	Typ	Max	Min	Typ	Max		
CLOCK INPUT PARAMETERS								
Input Clock Rate			480			480	Full	MHz
Conversion Rate[9]								
DCS Disabled	10		55	10		95	Full	MS/s
DCS Enabled	20		55	20		95	Full	MS/s
Aperture Uncertainty (Jitter)		0.32			0.32		25°C	ps rms

Timing Specifications

Table 8.

Parameter	Min	Typ	Max	Temp	Unit
SPI TIMING REQUIREMENTS					
Setup time between the data and the rising edge of SCLK/LVDS (t_{DS})	$4t_{clk}$			Full	ns
Hold time between the data and the rising edge of SCLK/LVDS (t_{DH})	$4t_{clk}$			Full	ns
Period of the SCLK/LVDS (t_{SCLK})	$10t_{clk}$			Full	ns
Setup time between SS and SCLK/LVDS (t_S)	$4t_{clk}$			Full	ns
Hold time between SS and SCLK/LVDS (t_H)	$4t_{clk}$			Full	ns
SCLK/LVDS pulse width high (t_{HIGH})	$2t_{clk}$			Full	ns
SCLK/LVDS pulse width low (t_{LOW})	$2t_{clk}$			Full	ns
Time required for the SD pin to switch from an input to an output relative to the SCLK/LVDS falling edge	1			Full	ns
Time required for the SD pin to switch from an output to an input relative to the SCLK/LVDS falling edge	1			Full	ns

Absolute Maximum Ratings

Table 9 – Absolute Maximum Ratings

Parameter	Rating
Electrical	
AVDD to AGND	-0.3V to +2.0 V
DRVDD to AGND	-0.3V to +3.6 V
VINP, VINN to AGND	-0.3V to +2.0 V
CLKP, CLKN to AGND	-0.3V to +2.0 V
VREF, VREFP, VREFN to AGND	-0.3V to +2.0 V
VCM to AGND	-0.3V to +2.0 V
RBIAS to AGND	-0.3V to +2.0 V
SENSE to AGND	-0.3V to +2.0 V
RST, PWDN, SCLK/LVDS, SS, SD to AGND	-0.3V to +3.6 V
D0 through D15 to AGND	-0.3V to +3.6 V
DCO to AGND	-0.3V to +3.6 V
Environmental	
Operating Temperature Range (Ambient)	-40°C to +85°C
Maximum Junction Temperature Under Bias	150°C
Storage Temperature Range	-65°C to +150°C
Electrostatic Discharge	
Maximum Stress (by Human Body Model)	2 kV

Typical Performance Characteristics

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sampling rate, 1.0 V internal reference, DCS disabled, 2 V p-p differential input, VIN = -1.0 dBFS, Divide-by-1 Input Clock Mode, 32k sample, T_A = 25°C, CMOS output mode, unless otherwise noted.

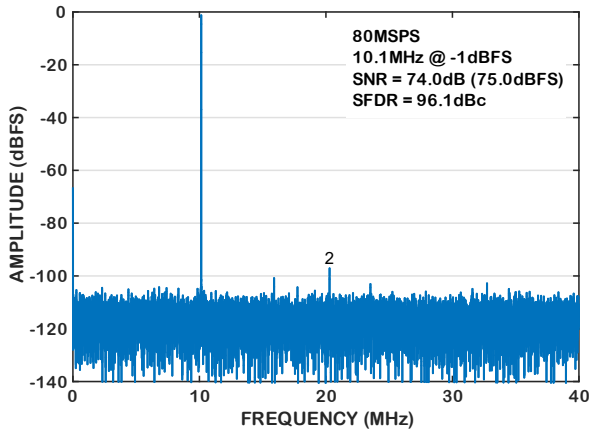

Figure 2 – Single-Tone FFT with f_{IN} = 10.1 MHz

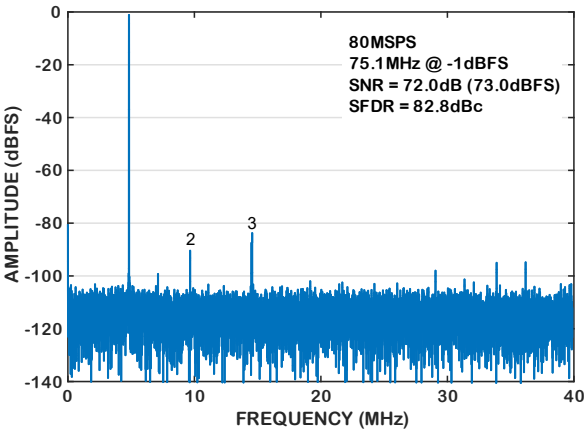

Figure 5 – Single-Tone FFT with f_{IN} = 75.1 MHz

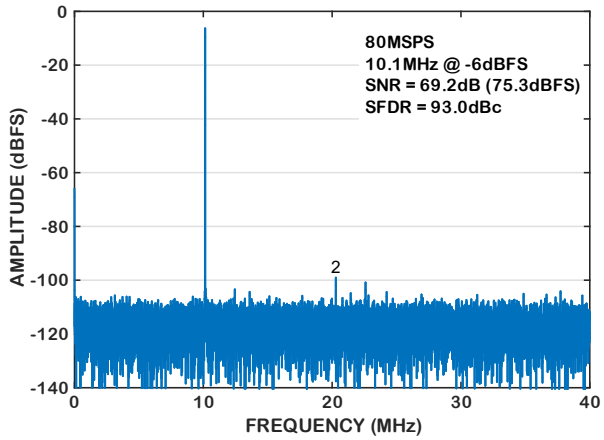

Figure 3 – Single-Tone FFT with f_{IN} = 10.1 MHz and -6 dBFS

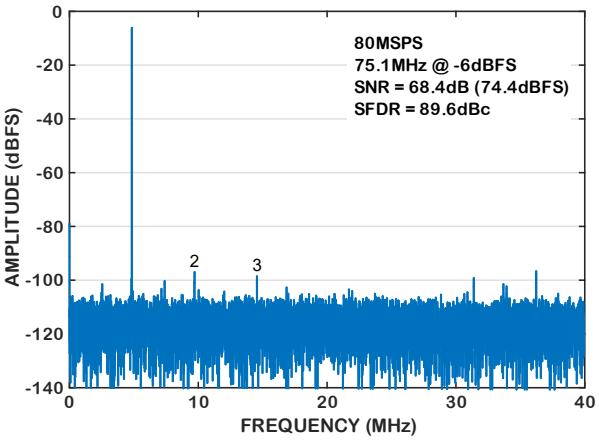

Figure 6 – Single-Tone FFT with f_{IN} = 75.1 MHz and -6 dBFS

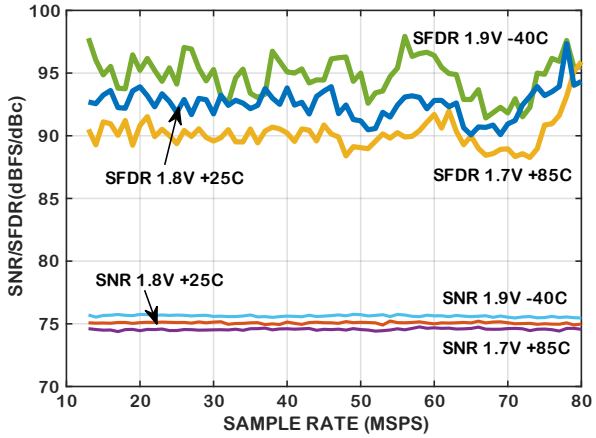

Figure 4 – Single-Tone SNR/SFDR vs. Sample Rate (f_S), Temperature, and AVDD with f_{IN} = 10.1 MHz

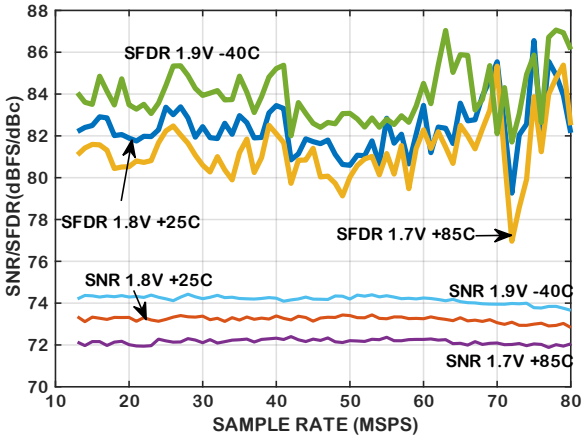

Figure 7 – Single-Tone SNR/SFDR vs. Sample Rate (f_S), Temperature, and AVDD with f_{IN} = 75.1 MHz

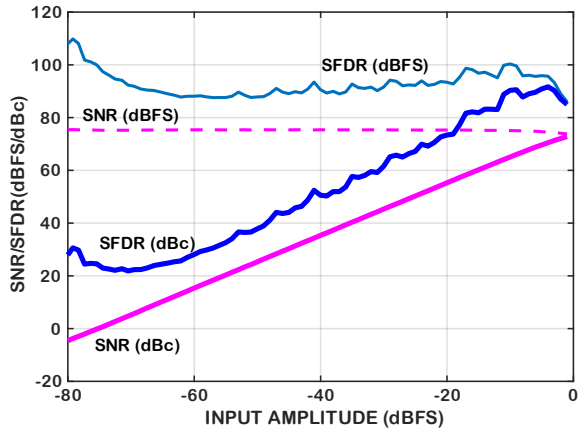

Figure 8 – Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 50.1 MHz

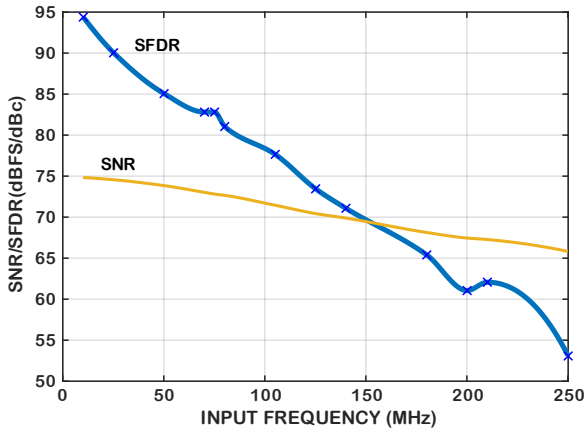

Figure 11 – Single-Tone SNR/SFDR vs. Input Frequency (f_{IN})

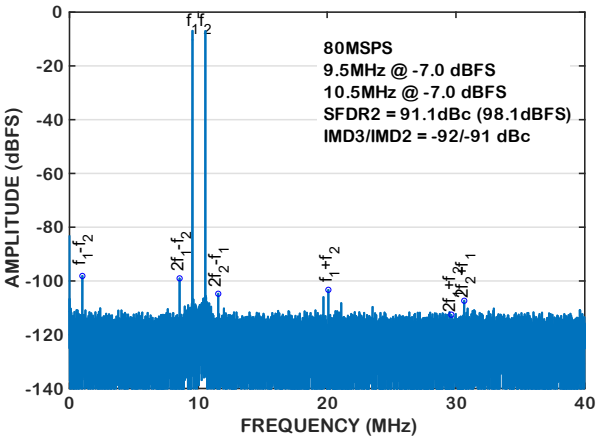

Figure 9 – Two-Tone FFT with f_{IN1} = 9.5 MHz and with f_{IN2} = 10.5 MHz (128k sample)

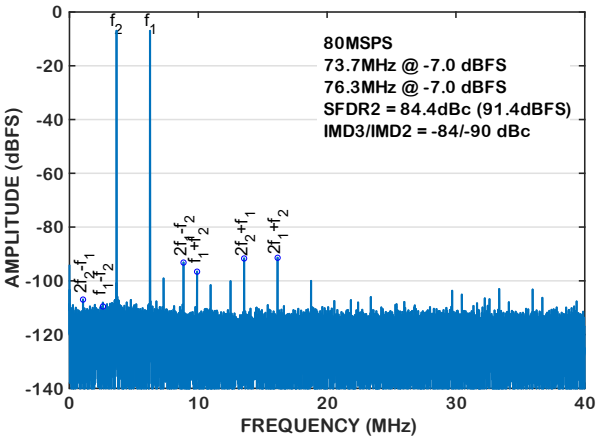

Figure 12 – Two-Tone FFT with f_{IN1} = 73.7 MHz and with f_{IN2} = 76.3 MHz (128k sample)

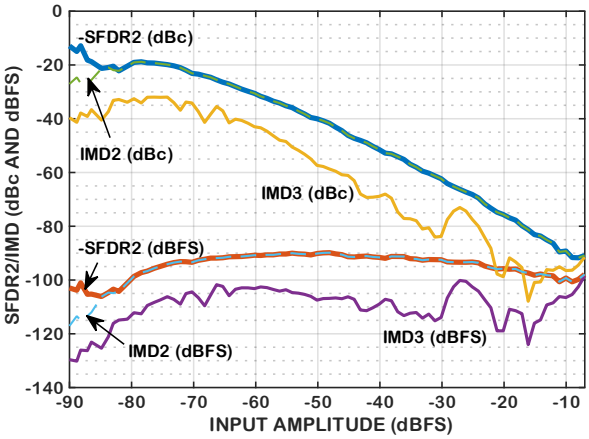

Figure 10 – Two-Tone SFDR/IMD3/IMD2 vs. Input Amplitude (A_{IN}) with f_{IN1} = 9.5 MHz and with f_{IN2} = 10.5 MHz

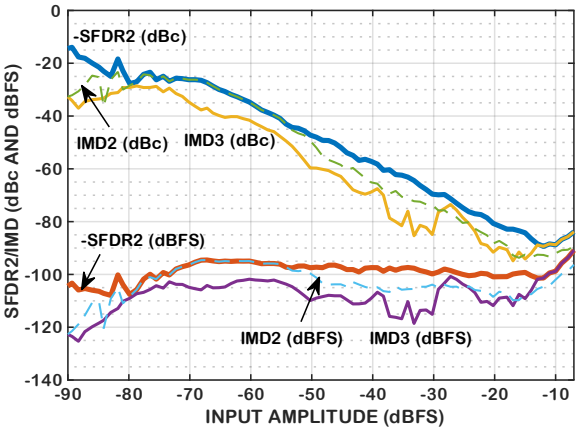

Figure 13 – Two-Tone SFDR/IMD3/IMD2 vs. Input Amplitude (A_{IN}) with f_{IN1} = 73.7 MHz and with f_{IN2} = 76.3 MHz

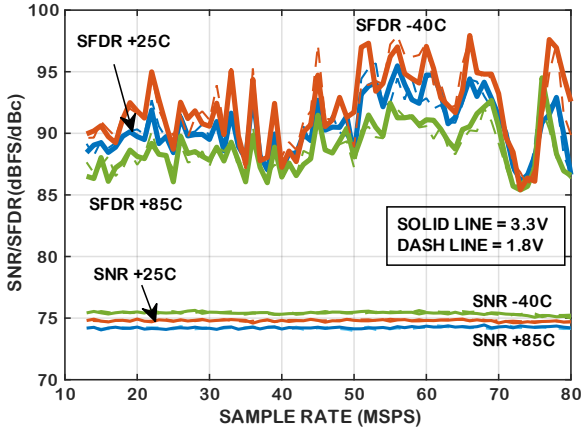

Figure 14 – Single-Tone SNR/SFDR vs. Sample Rate (f_S), Temperature, and DRVDD with f_{IN} = 25.1 MHz

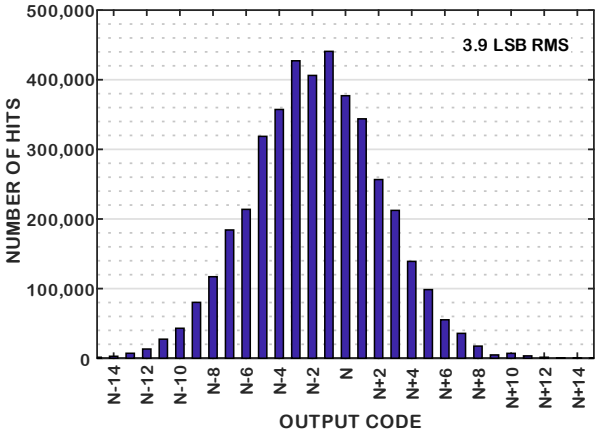

Figure 17 – Grounded Input Histogram

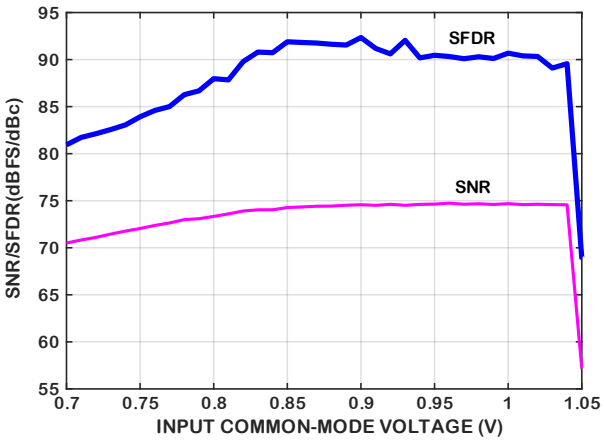

Figure 15 – SNR/SFDR vs. Input Common Mode (VCM) with f_{IN} = 25.1 MHz

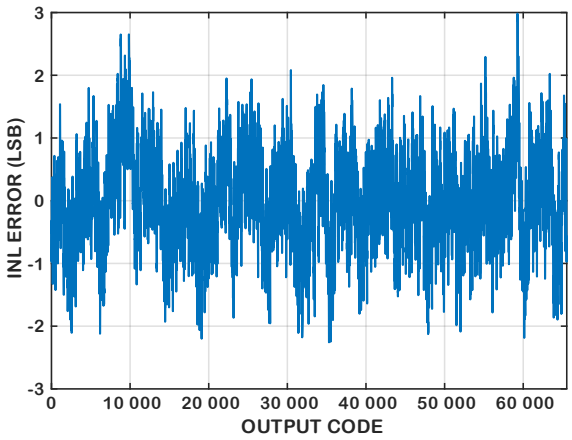

Figure 18 – INL with f_{IN} = 10.1 MHz

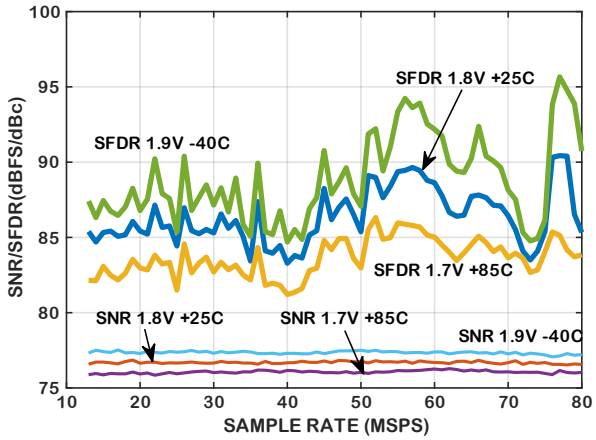

Figure 16 – SNR/SFDR vs. Sample Rate (f_S) and Temperature with f_{IN} = 25.1 MHz and External Reference Voltage (VREF) 1.25 V

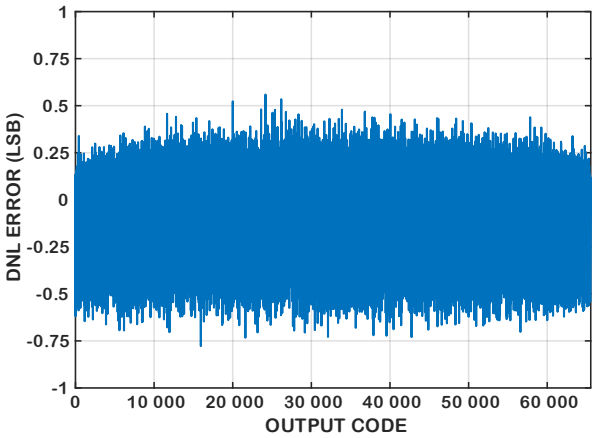

Figure 19 – DNL with f_{IN} = 10.1 MHz

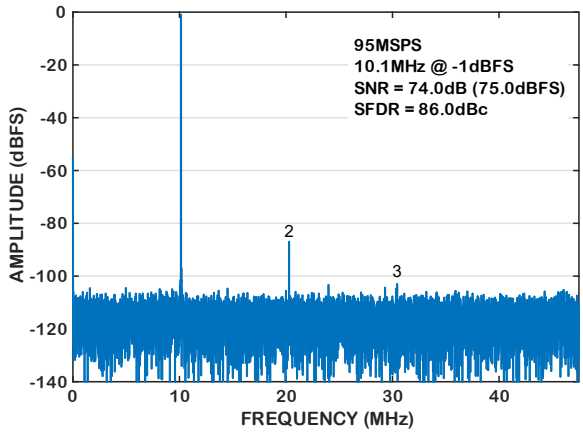

Figure 20 – Single-Tone FFT with f_{IN} = 10.1 MHz in Boost Mode

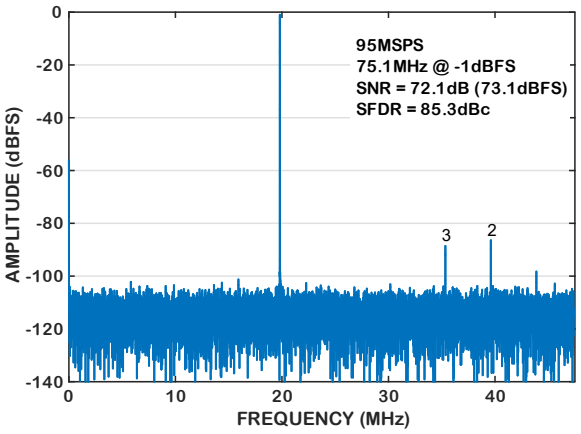

Figure 23 – Single-Tone FFT with f_{IN} = 75.1 MHz in Boost Mode

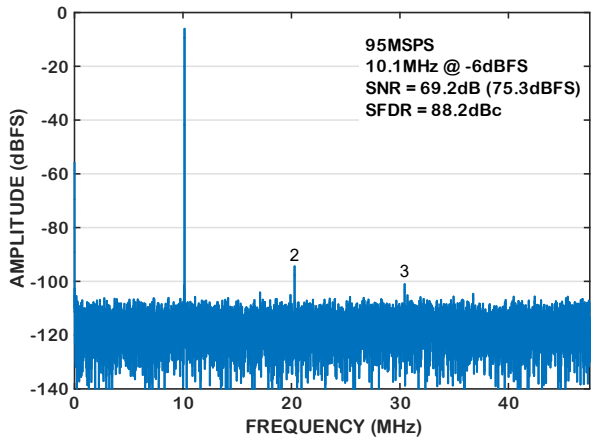

Figure 21 – Single-Tone FFT with f_{IN} = 10.1 MHz and -6 dBFS in Boost Mode

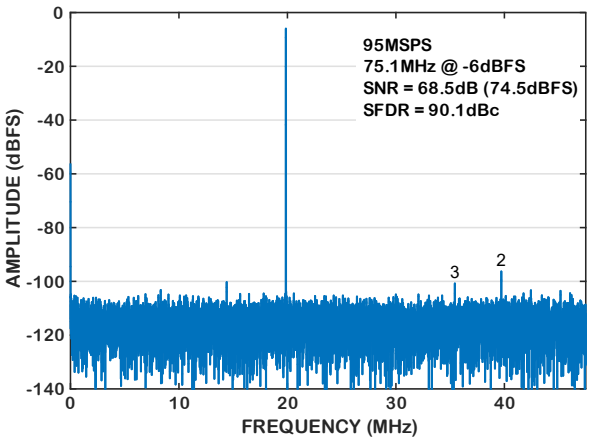

Figure 24 – Single-Tone FFT with f_{IN} = 75.1 MHz and -6 dBFS in Boost Mode

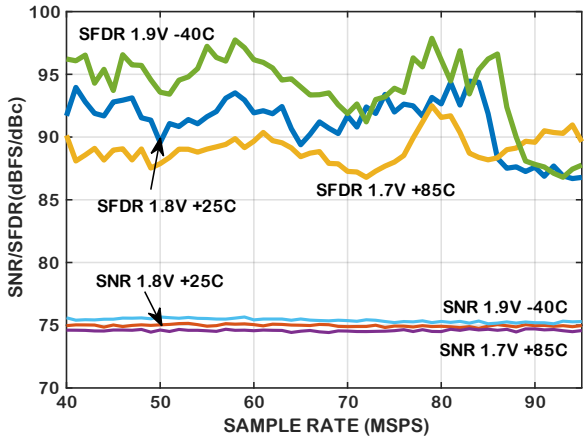

Figure 22 – Single-Tone SNR/SFDR vs. Sample Rate (f_S), Temperature, and AVDD with f_{IN} = 10.1 MHz in Boost Mode

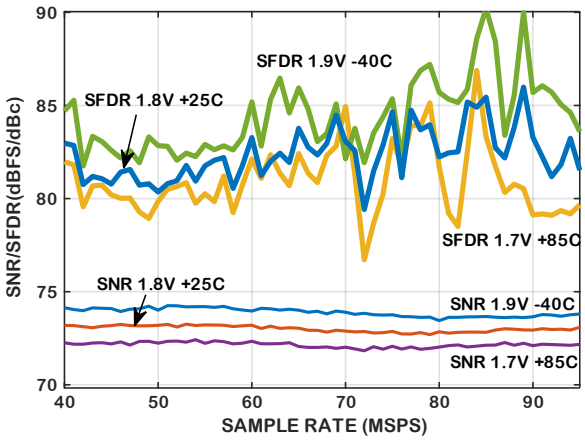

Figure 25 – Single-Tone SNR/SFDR vs. Sample Rate (f_S), Temperature, and AVDD with f_{IN} = 75.1 MHz in Boost Mode

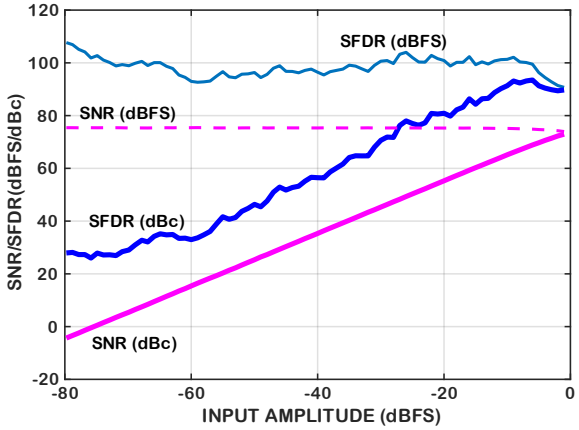

Figure 26 – Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 50.1 MHz in Boost Mode

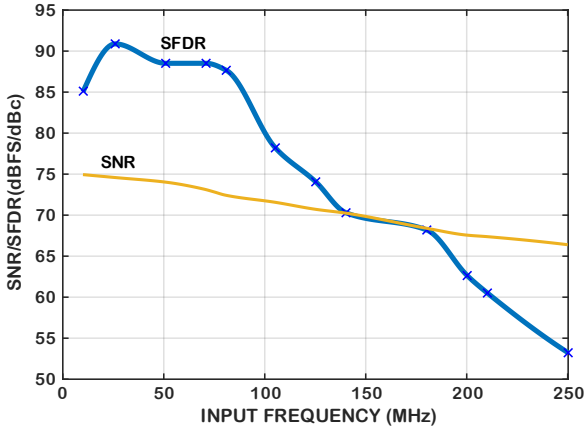

Figure 29 – Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}) in Boost Mode

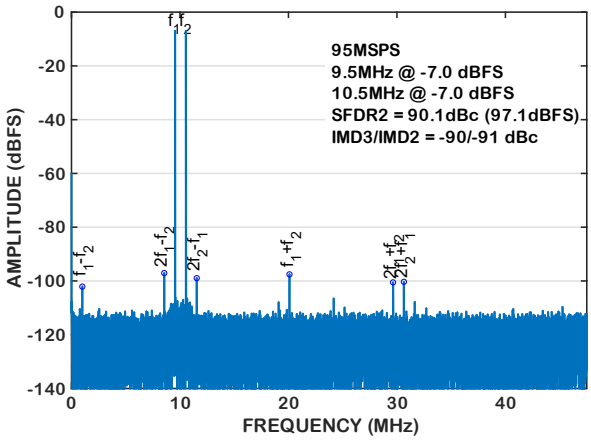

Figure 27 – Two-Tone FFT with f_{IN1} = 9.5 MHz and with f_{IN2} = 10.5 MHz in Boost Mode Mode (128k sample)

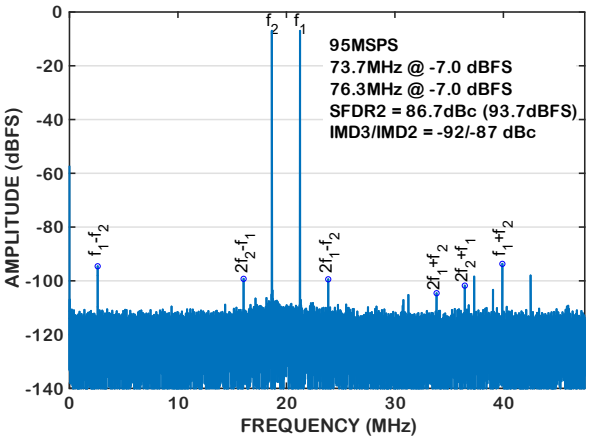

Figure 30 – Two-Tone FFT with f_{IN1} = 73.7 MHz and with f_{IN2} = 76.3 MHz in Boost Mode (128k sample)

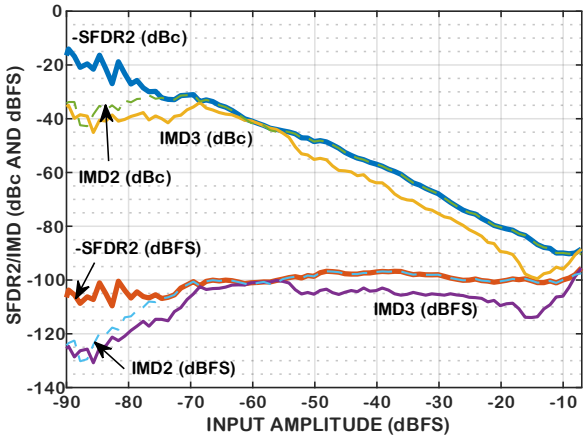

Figure 28 – Two-Tone SFDR/IMD3/IMD2 vs. Input Amplitude (A_{IN}) with f_{IN1} = 9.5 MHz and with f_{IN2} = 10.5 MHz in Boost Mode

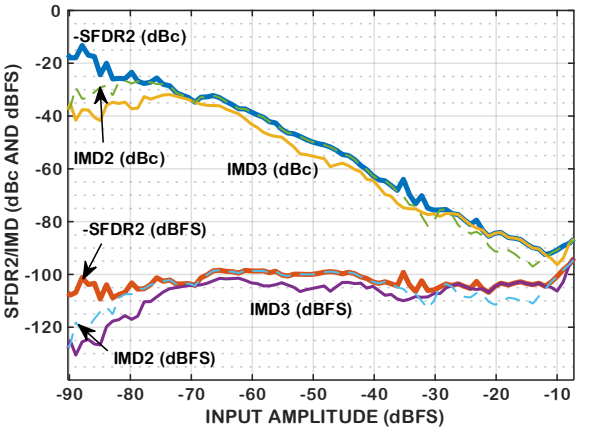

Figure 31 – Two-Tone SFDR/IMD3/IMD2 vs. Input Amplitude (A_{IN}) with f_{IN1} = 73.7 MHz and with f_{IN2} = 76.3 MHz in Boost Mode

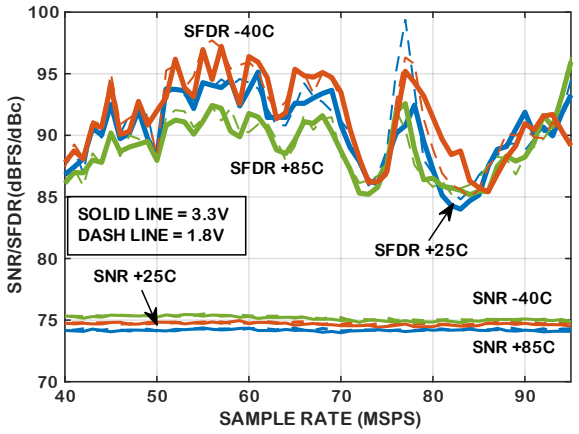

Figure 32 – Single-Tone SNR/SFDR vs. Sample Rate (f_S), Temperature, and DRVDD with f_{IN} = 25.1 MHz in Boost Mode

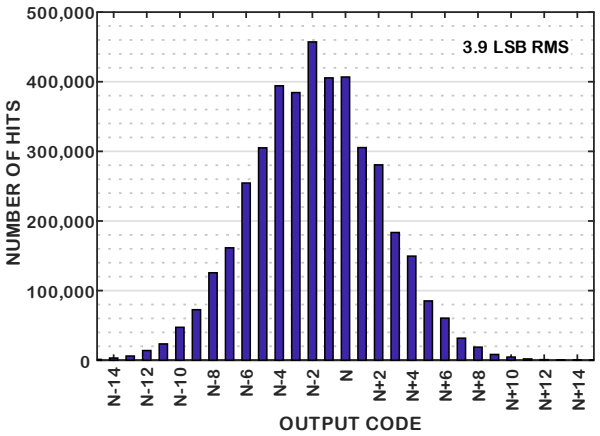

Figure 35 – Grounded Input Histogram in Boost Mode

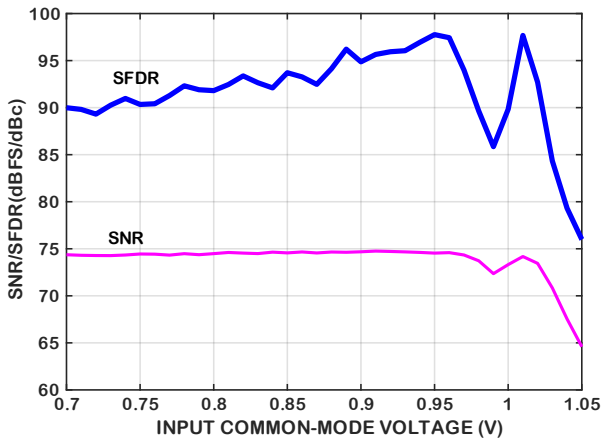

Figure 33 – SNR/SFDR vs. Input Common Mode (VCM) with f_{IN} = 25.1 MHz in Boost Mode

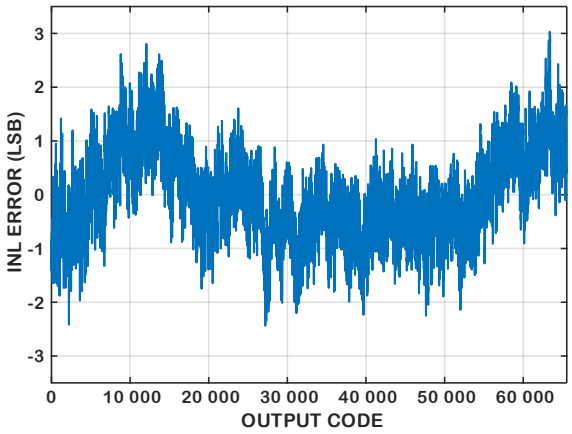

Figure 36 – INL with f_{IN} = 10.1 MHz in Boost Mode

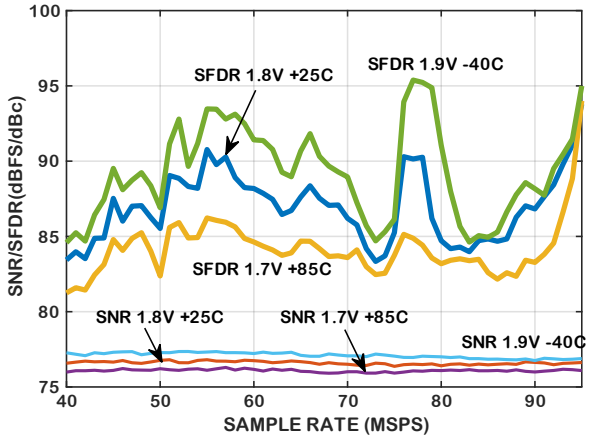

Figure 34 – SNR/SFDR vs. Sample Rate (f_S) and Temperature with f_{IN} = 25.1 MHz and External Reference Voltage (VREF) 1.25 V in Boost Mode

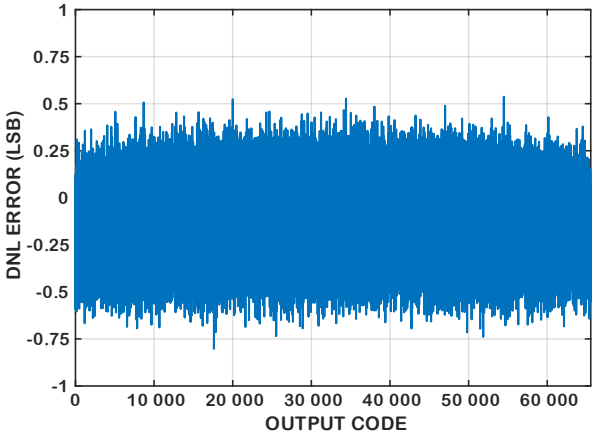

Figure 37 – DNL with f_{IN} = 10.1 MHz in Boost Mode

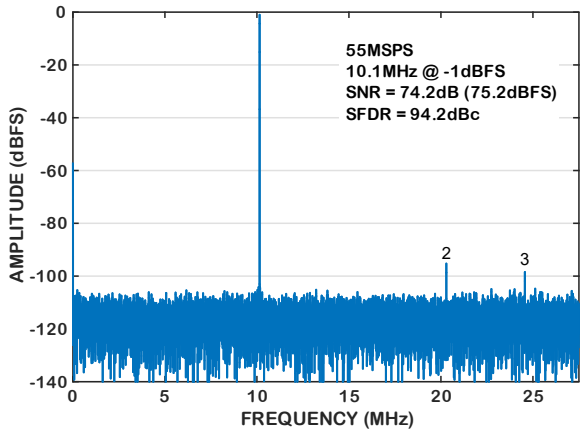

Figure 38 – Single-Tone FFT with f_{IN} = 10.1 MHz in RP Mode

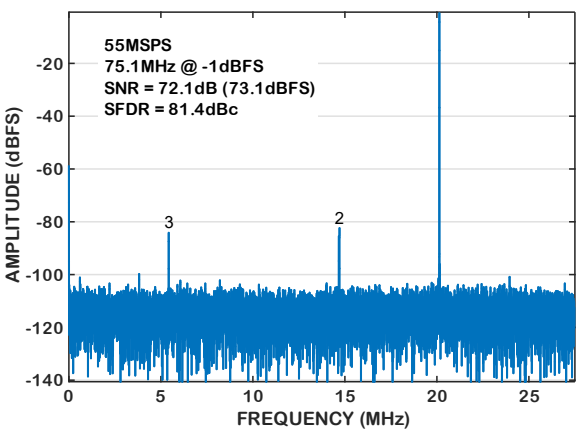

Figure 41 – Single-Tone FFT with f_{IN} = 75.1 MHz in RP Mode

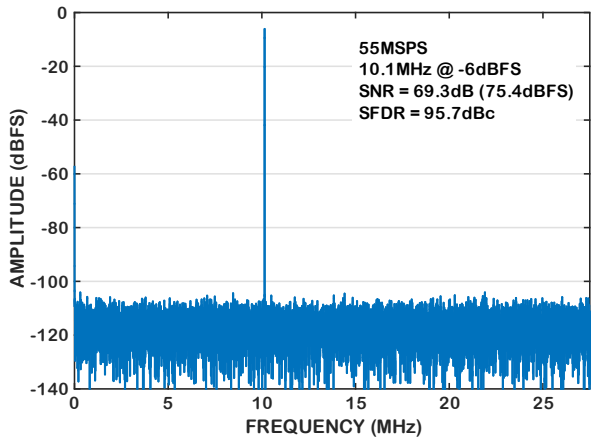

Figure 39 – Single-Tone FFT with f_{IN} = 10.1 MHz and -6 dBFS in RP Mode

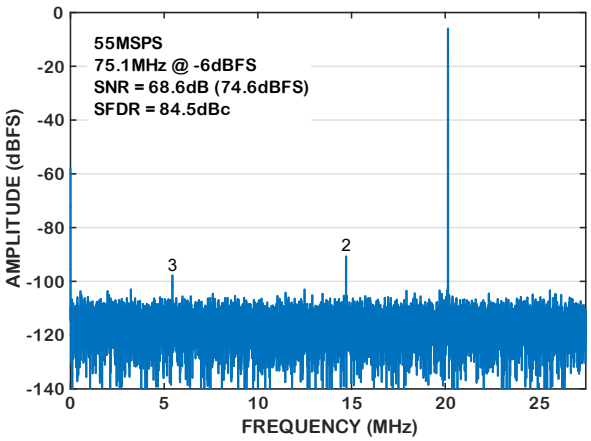

Figure 42 – Single-Tone FFT with f_{IN} = 75.1 MHz and -6 dBFS in RP Mode

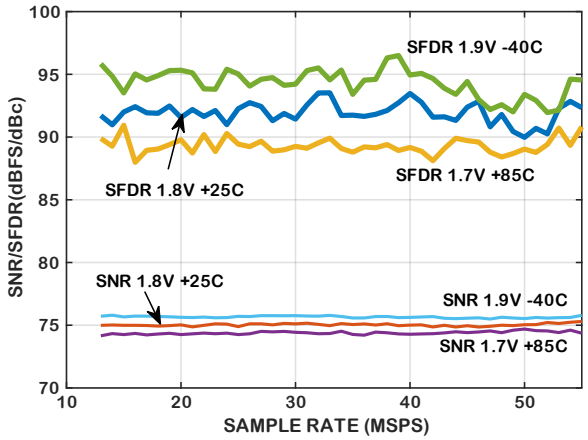

Figure 40 – Single-Tone SNR/SFDR vs. Sample Rate (f_S), Temperature, and AVDD with f_{IN} = 10.1 MHz in RP Mode

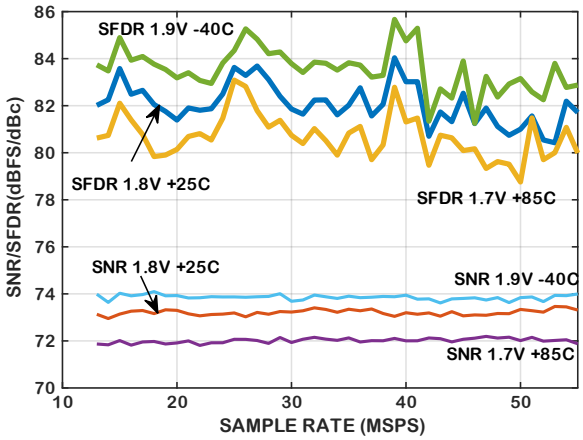

Figure 43 – Single-Tone SNR/SFDR vs. Sample Rate (f_S), Temperature, and AVDD with f_{IN} = 75.1 MHz in RP Mode

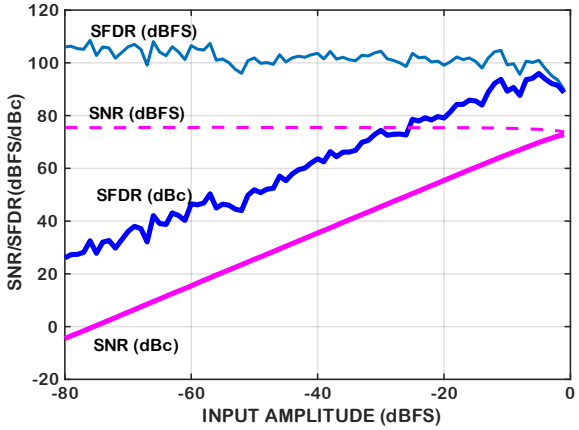

Figure 44 – Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 50.1 MHz in RP Mode

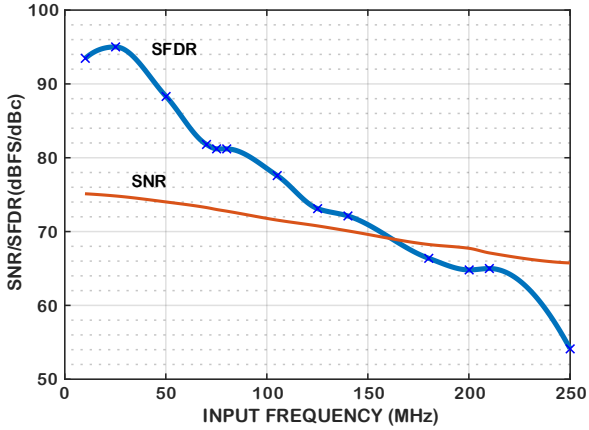

Figure 47 – Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}) in RP Mode

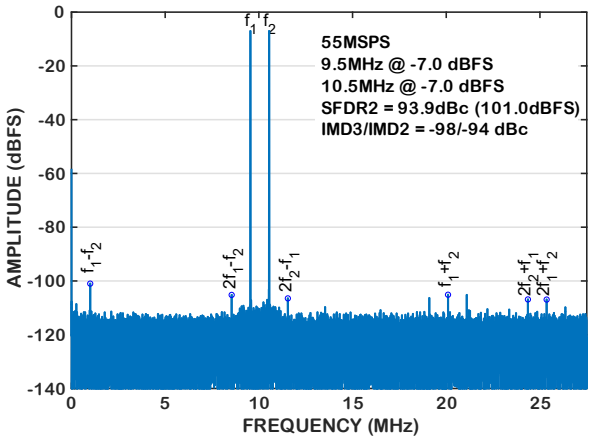

Figure 45 – Two-Tone FFT with f_{IN1} = 9.5 MHz and with f_{IN2} = 10.5 MHz in RP Mode (128k sample)

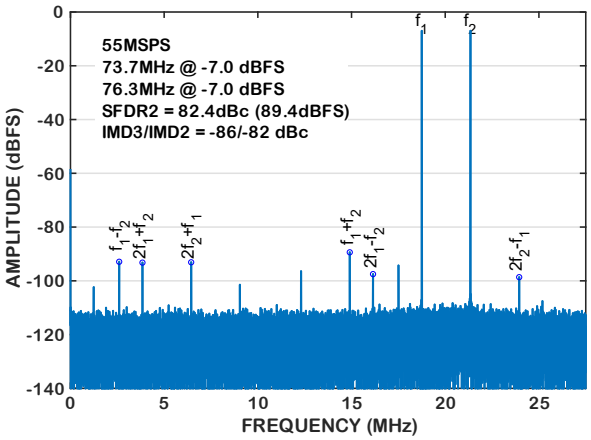

Figure 48 – Two-Tone FFT with f_{IN1} = 73.7 MHz and with f_{IN2} = 76.3 MHz in RP Mode (128k sample)

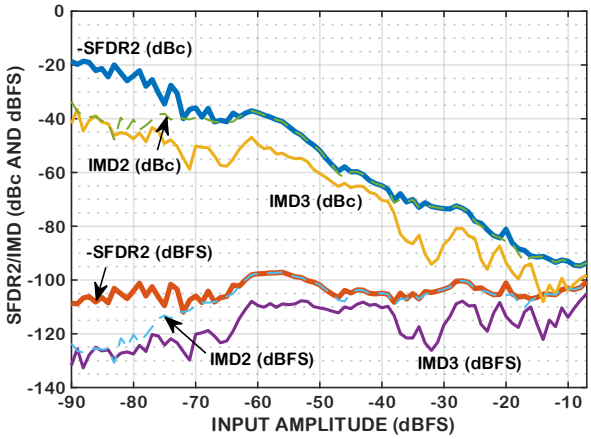

Figure 46 – Two-Tone SFDR/IMD3/IMD2 vs. Input Amplitude (A_{IN}) with f_{IN1} = 9.5 MHz and with f_{IN2} = 10.5 MHz in RP Mode

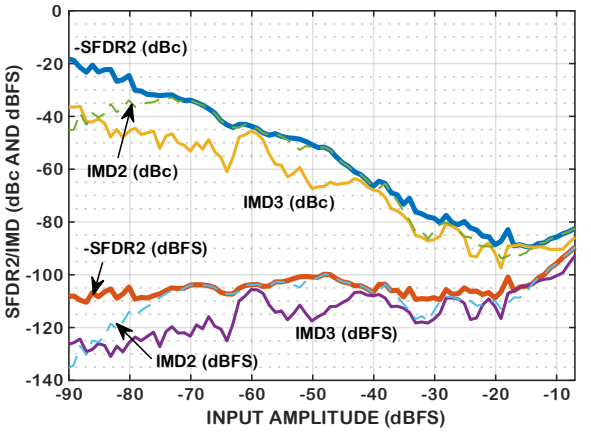

Figure 49 – Two-Tone SFDR/IMD3/IMD2 vs. Input Amplitude (A_{IN}) with f_{IN1} = 73.7 MHz and with f_{IN2} = 76.3 MHz in RP Mode

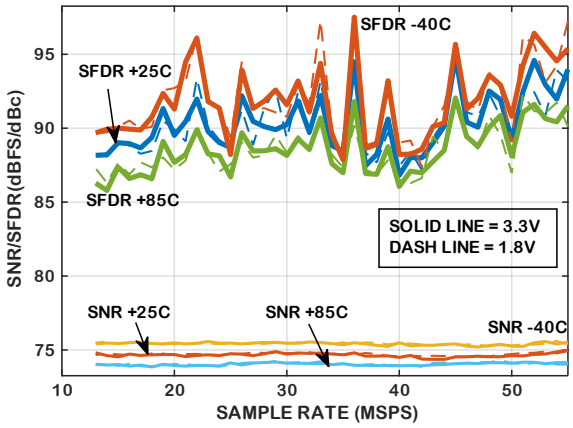

Figure 50 – Single-Tone SNR/SFDR vs. Sample Rate (f_S), Temperature, and DRVDD with f_{IN} = 25.1 MHz in RP Mode

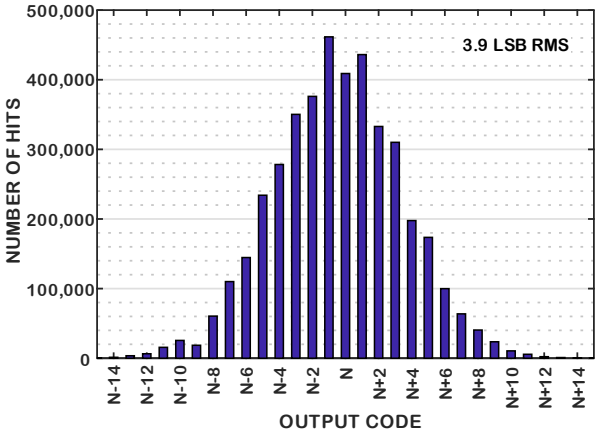

Figure 53 – Grounded Input Histogram in RP Mode

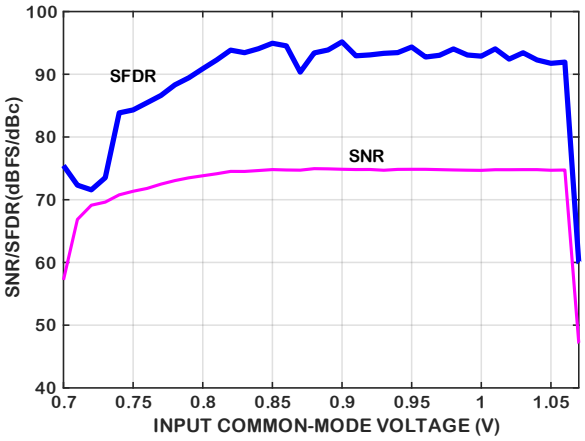

Figure 51 – SNR/SFDR vs. Input Common Mode (VCM) with f_{IN} = 25.1 MHz in RP Mode

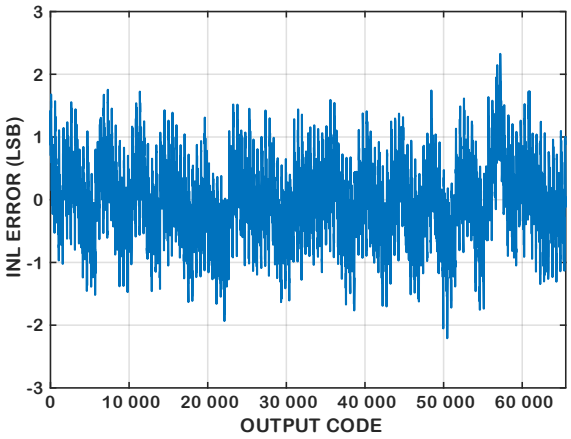

Figure 54 – INL with f_{IN} = 10.1 MHz in RP Mode

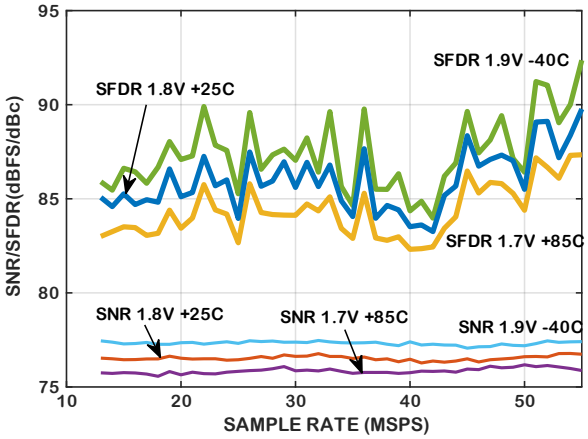

Figure 52 – SNR/SFDR vs. Sample Rate (f_S) and Temperature with f_{IN} = 25.1 MHz and External Reference Voltage (VREF) 1.25 V in RP Mode

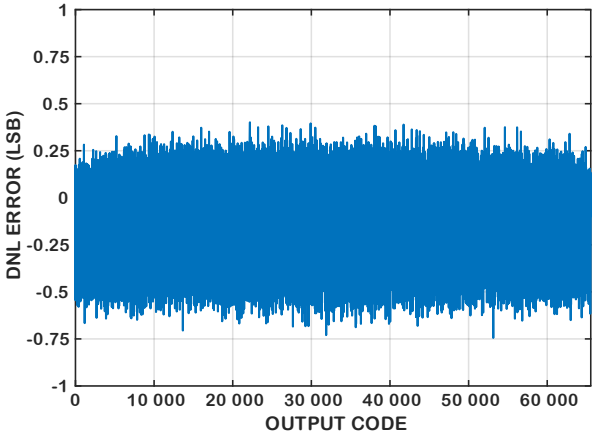

Figure 55 – DNL with f_{IN} = 10.1 MHz in RP Mode

Pin Configuration and Function Description

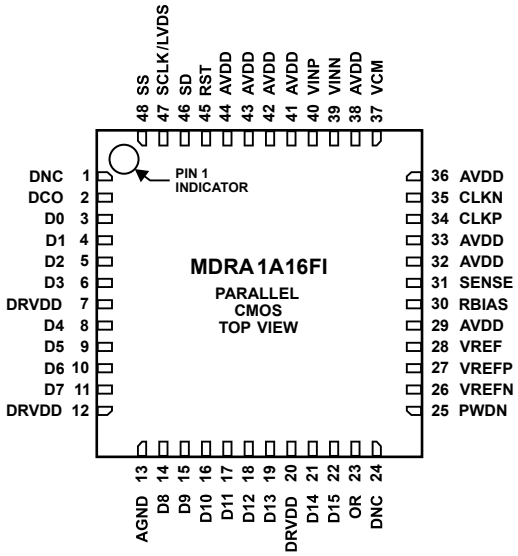

Figure 56 – VQFN48L Parallel CMOS Pin Configuration (Top View)

Table 10 – Pin Function Descriptions in Parallel CMOS Mode

Pin No.	Symbol	Type	Pin description
POWER SUPPLIES			
29, 32, 33, 36, 38, 41 – 44	AVDD	Supply	Analog Power Supply (1.8 V Nominal)
13	AGND	Ground	Analog Ground
0	AGND	Ground	Analog Ground. The exposed thermal pad on the bottom of the package provides the analog ground for the input. The exposed pad must be connected to ground for proper operation
7, 12, 20	DRVDD	Supply	Digital Output Driver Supply (1.8 - 3.3 V)
ANALOG PINS			
40	VINP	Input	Differential Non-inverting Analog Input (+)
39	VINN	Input	Differential Inverting Analog Input (-)
30	RBIAS	Input	External Reference Bias Resistor (12.1kΩ in Default/Boost Mode and 24kΩ in RP Mode)
28	VREF	Input/ Output	Voltage Reference Input/Output
27	VREFP	Output	Internal Upper Reference Voltage (to be filtered externally)
26	VREFN	Output	Internal Lower Reference Voltage (to be filtered externally)
37	VCM	Output	Common-Mode Level Bias Output for Analog Inputs
31	SENSE	Input	Voltage Reference Mode Selection
34	CLKP	Input	ADC Clock Input - Non-inverting
35	CLKN	Input	ADC Clock Input - Inverting

Pin No.	Symbol	Type	Pin description
DIGITAL INPUTS			
45	RST	Input	ADC Reset (“0” – reset; “1” – normal operation)
46	SD	Input	SPI Serial Data I/O (if SPI is disabled – “0”)
47	SCLK/LVDS	Input	ADC Output Mode (“1” – LVDS; “0” – CMOS). In SPI mode: SPI Serial Clock
48	SS	Input	SPI Chip Select (Active Low, if SPI is disabled – “1”)
25	PDWN	Input	Power-Down Input (“1”- power down; “0” – normal operation)
DIGITAL OUTPUTS			
22	D15	Output	CMOS Output Data (MSB)
21	D14	Output	CMOS Output Data
19	D13	Output	CMOS Output Data
18	D12	Output	CMOS Output Data
17	D11	Output	CMOS Output Data
16	D10	Output	CMOS Output Data
15	D9	Output	CMOS Output Data
14	D8	Output	CMOS Output Data
11	D7	Output	CMOS Output Data
10	D6	Output	CMOS Output Data
9	D5	Output	CMOS Output Data
8	D4	Output	CMOS Output Data
6	D3	Output	CMOS Output Data
5	D2	Output	CMOS Output Data
4	D1	Output	CMOS Output Data
3	D0	Output	CMOS Output Data (LSB)
23	OR	Output	Overrange Output
2	DCO	Output	Data Clock Output
UNUSED PINS			
1, 24	DNC		Do not connect

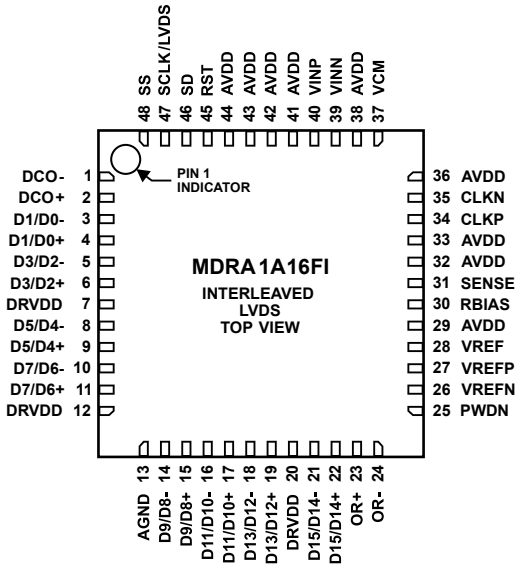

Figure 57 – VQFN48L Interleaved Parallel LVDS Pin Configuration (Top View)

Table 11 – Pin Function Description in Interleaved Parallel LVDS Mode

Pin No.	Symbol	Type	Pin description
POWER SUPPLIES			
29, 32, 33, 36, 38, 41 – 44	AVDD	Supply	Analog Power Supply (1.8 V Nominal)
13	AGND	Ground	Analog Ground
0	AGND	Ground	Analog Ground. The exposed thermal pad on the bottom of the package provides the analog ground for the input. The exposed pad must be connected to ground for proper operation
7, 12, 20	DRVDD	Supply	Digital Output Driver Supply (1.8 - 3.3 V)
ANALOG PINS			
40	VINP	Input	Differential Non-inverting Analog Input (+)
39	VINN	Input	Differential Inverting Analog Input (-)
30	RBIAS	Input	External Reference Bias Resistor (12.1kΩ in Default/Boost Mode; 24kΩ in RP Mode)
28	VREF	Input/ Output	Voltage Reference Input/Output
27	VREFP	Output	Internal Upper Reference Voltage (to be filtered externally)
26	VREFN	Output	Internal Lower Reference Voltage (to be filtered externally)
37	VCM	Output	Common-Mode Level Bias Output for Analog Inputs
31	SENSE	Input	Voltage Reference Mode Selection
34	CLKP	Input	ADC Clock Input - Non-inverting
35	CLKN	Input	ADC Clock Input - Inverting

Pin No.	Symbol	Type	Pin description
DIGITAL INPUTS			
45	RST	Input	ADC Reset (“0” – reset; “1” – normal operation)
46	SD	Input	SPI Serial Data I/O (if SPI is disabled – “0”)
47	SCLK/LVDS	Input	ADC Output Mode (“1” – LVDS; “0” – CMOS). In SPI mode: SPI Serial Clock
48	SS	Input	SPI Chip Select (Active Low, if SPI is disabled – “1”)
25	PDWN	Input	Power-Down Input (“1”- power down; “0” – normal operation)
DIGITAL OUTPUTS			
22	D15/D14+	Output	LVDS Output Data Bit 15/14 (MSB) - True
21	D15/D14-	Output	LVDS Output Data Bit 15/14 (MSB) - Complement
19	D13/D12+	Output	LVDS Output Data Bit 13/12 - True
18	D13/D12-	Output	LVDS Output Data Bit 13/12 - Complement
17	D11/D10+	Output	LVDS Output Data Bit 11/10 - True
16	D11/D10-	Output	LVDS Output Data Bit 11/10 - Complement
15	D9/D8+	Output	LVDS Output Data Bit 9/8 - True
14	D9/D8-	Output	LVDS Output Data Bit 9/8 - Complement
11	D7/D6+	Output	LVDS Output Data Bit 7/6 - True
10	D7/D6-	Output	LVDS Output Data Bit 7/6 - Complement
9	D5/D4+	Output	LVDS Output Data Bit 5/4 - True
8	D5/D4-	Output	LVDS Output Data Bit 5/4 - Complement
6	D3/D2+	Output	LVDS Output Data Bit 3/2 - True
5	D3/D2-	Output	LVDS Output Data Bit 3/2 - Complement
4	D1/D0+	Output	LVDS Output Data Bit 1/0 (LSB) - True
3	D1/D0-	Output	LVDS Output Data Bit 1/0 (LSB) - Complement
23	OR+	Output	LVDS Overrange Output - True
24	OR-	Output	LVDS Overrange Output - Compliment
2	DCO+	Output	LVDS Data Clock Output - True
1	DCO-	Output	LVDS Data Clock Output - Compliment

Functional Description

IC Architecture

The device is a 16-bit pipeline analog-to-digital converter (ADC) with sampling frequency of 80 MS/s. Figure 1 shows its block diagram.

Input analog differential signal is supplied via VINP/VINN pins to an input sample and hold circuit and then it is processed by the core of 16-bit ADC. Sampling moment corresponds to CLKP switching from high to low with aperture delay t_A.

A digital post-processing system corrects nonidealities of analog blocks and generates output data. The user can select the encoding of output data and also program IC operating mode through the SPI port.

A differential clock input signal is supplied via CLKP/CLKN pins to internal clock circuit, which includes a duty cycle stabilizer and an integrated input clock divider.

The ADC output data format is either parallel CMOS or LVDS/DDR. A data output clock is provided to ensure proper latch timing with receiving logic.

An integrated voltage reference allows using both internal and external reference voltage VREF, which defines the ADC input voltage scale. The user can program VREF by means of external adjusting resistors or through the SPI port. The voltage, which can be used as a common-mode level of the input signal is set by the VCM pin.

The converter operates at 1.8 V. A separate voltage from 1.8 V to 3.3 V can be used for the output interface (LVDS mode supports only 1.8 V) and SPI. In shutdown mode output buffers are switched to high-impedance state.

Figure 58 and Figure 59 show a typical connection diagrams in CMOS and LVDS output modes.

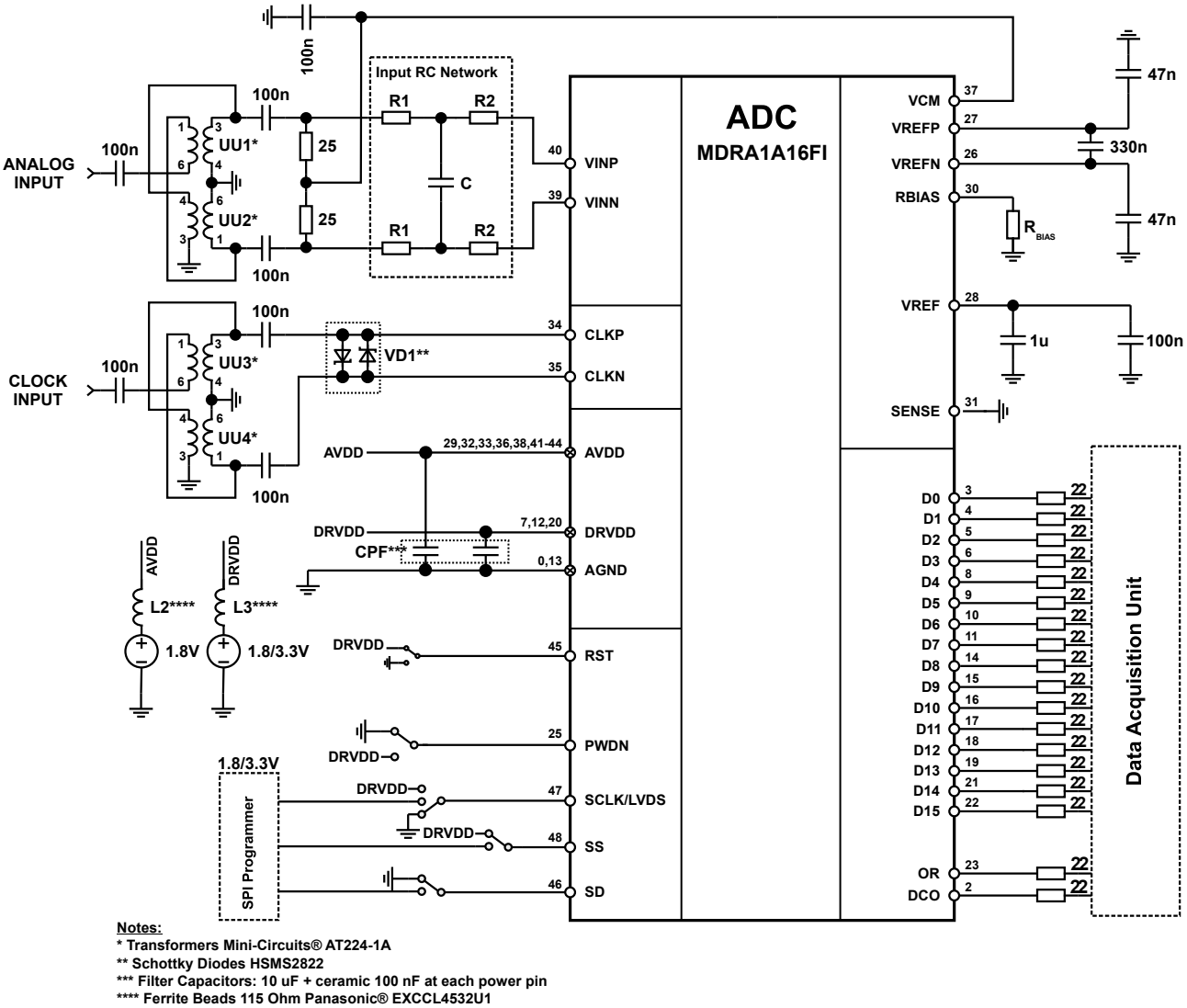

Figure 58 – Typical Connection Diagram, CMOS Output Mode

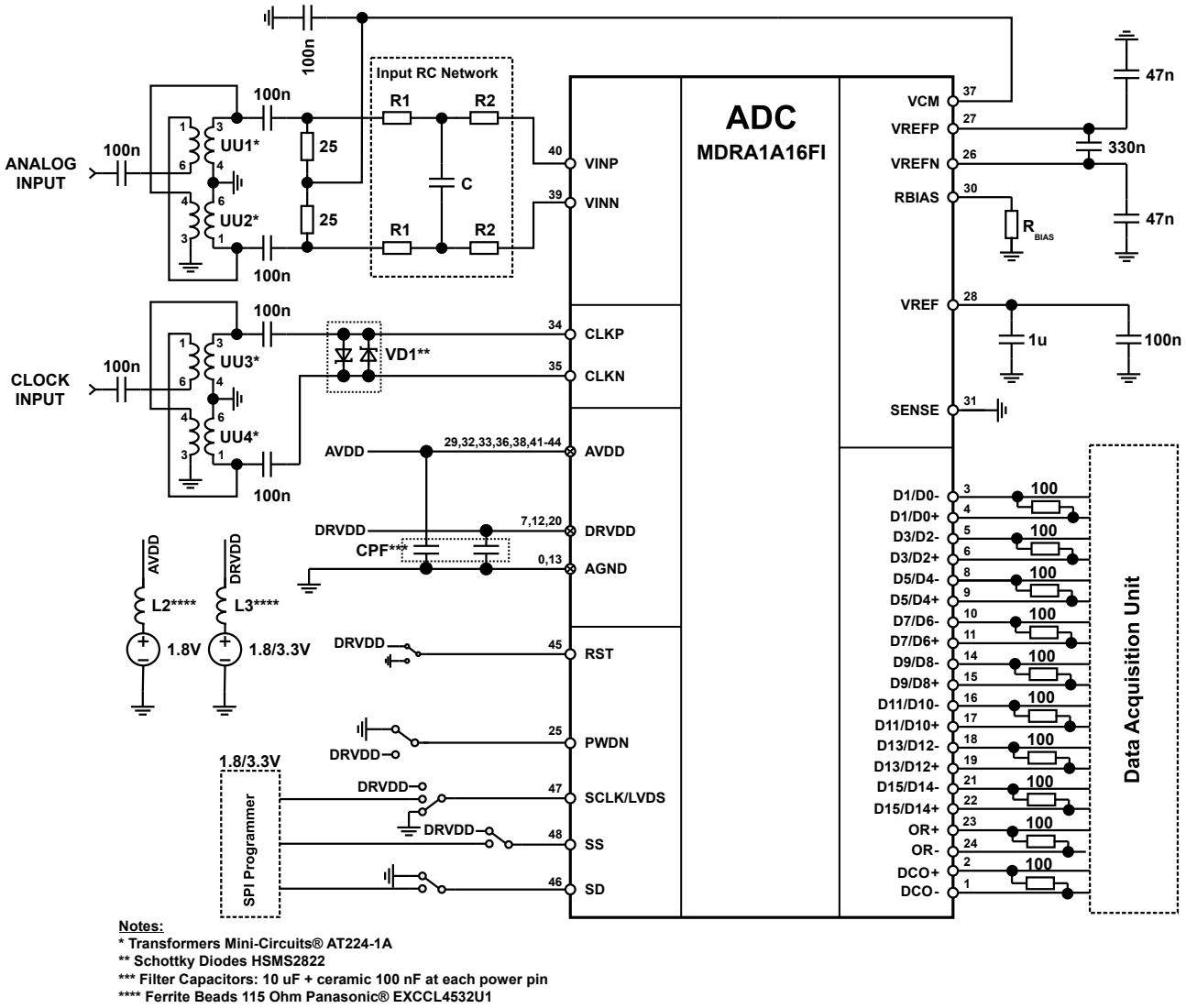

Figure 59 – Typical Connection Diagram, LVDS Output Mode

Analog Input Considerations

A simplified equivalent circuit of the ADC input is shown in Figure 60. This figure represents: internal parasitic elements, ESD protection circuits and parasitic elements of the package.

The ADC input sample-and-hold circuit designed on switching capacitors and optimized to operate with a differential input signal. The clock signal closes and opens an input analog switch, which toggle the input network to sample and hold phases, one after another. When the stage is in sample mode, the signal source's output resistance should be small enough, because charging the sampling capacitors and settling should take less than a half of a clock cycle.

A small resistor in series with each input and a shunt capacitor should help to reduce peak transient currents and isolate the drive circuitry from the sample-and-hold switching. The resulting RC network forms a low pass filter. An example of differential double balun coupling for input configuration is shown in Figure 59. The recommended RC network values is provided in Table 12. However, these values are dependent on the input signal and should be used as a starting guide.

The best dynamic performance of the ADC is achieved when the source impedances driving VINP/VINN are matched, and the differential inputs are properly balanced.

Table 12 – Example of Input RC Network

Frequency Range (MHz)	R1 Series (Ω Each)	C Differential (pF)	R2 Series (Ω Each)
0 to 100	15	18	15
100 to 250	10	8.2	15

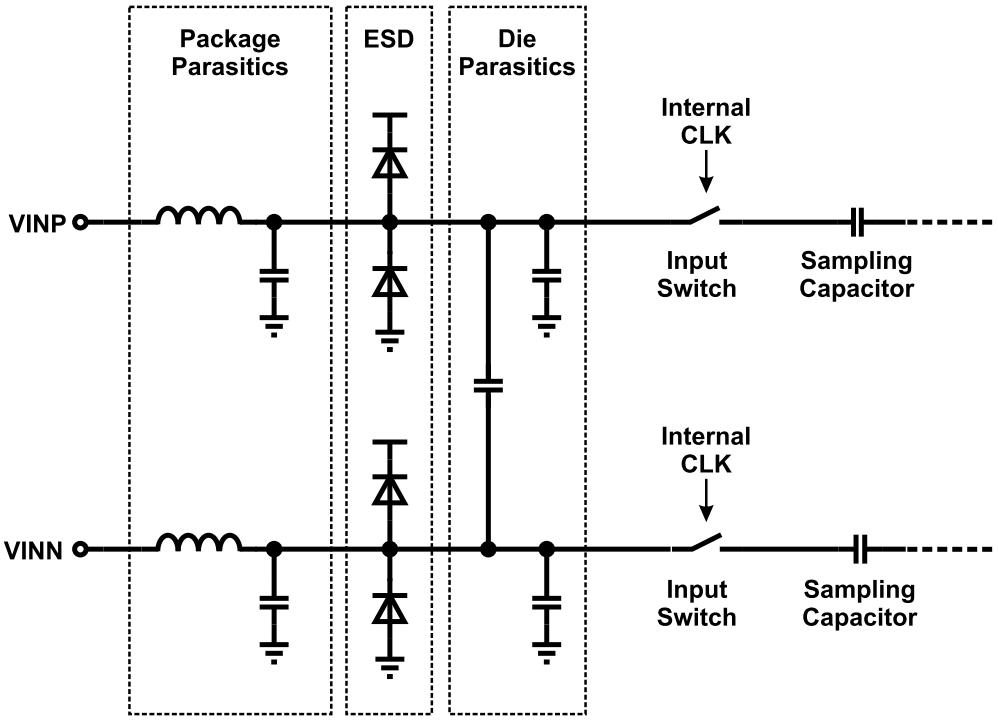

Figure 60 – Equivalent Analog Input Circuit

Input Common-Mode

The analog inputs are not internally DC biased, so this bias should be provided by the user externally. The best ADC performance is achieved when the common-mode level of the differential inputs is equal to ½VDDA, however the IC operates with reasonable characteristics in a wider common-mode level range.

An integrated voltage source provides a voltage which is recommended to be used as an input common-mode level. This voltage is available at VCM pin (see Figure 61) and should be filtered by means of 0.1 μF capacitor.

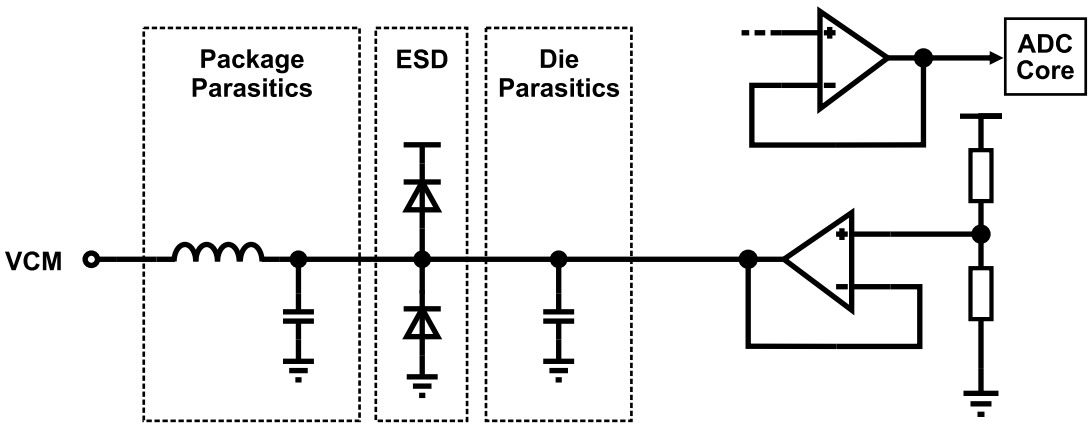

Figure 61 – Equivalent VCM Circuit

Voltage Reference

The device contains an internal voltage reference. The input range (scale) of the ADC can be adjusted by setting the voltage at VREF pin. VREF is set by an internal or external voltage reference, and at the same time it can be programmed by external adjusting resistors or through the SPI port. The ADC input range linearly depends on VREF and could be calculated by the following equation

$$FS = 2 \cdot V_{REF} \quad (1)$$

The VREFP and VREFN pins require external load capacitors to reduce the reference circuit noise.

Internal Reference Connection

A comparator in the select logic (Figure 62) detects the potential at SENSE pin and configures the reference voltage circuit in accordance with Table 14.

If SENSE is grounded, a resistive feedback loop is set up around the reference amplifier to make V_{REF} equal to approximately 1 V (which corresponds to scale 2 Vp-p). In this mode, when SENSE is grounded, the full scale can be adjusted through the SPI port. By setting bits 8 and 7 in register R_CNTRL the user can configure full scale up to 1.25, 1.5 and 1.75 Vp-p in accordance with Table 13.

If external resistors are connected between VREF and SENSE, as shown in Figure 63, then VREF is set according to the following equation:

$$V_{REF} = 0.5 \cdot \left(1 + \frac{R2}{R1}\right) \quad (2)$$

If SENSE pin is connected to VREF, the reference amplifier is switched to a unity feedback mode, and V_{REF} is 0.5 V.

If the internal voltage reference is used to drive multiple ADCs, the load of the other converters on the reference must be considered. Figure 64 shows how the internal reference voltage is affected by loading.

External Reference Connection

The use of an external reference may be necessary to reduce the ADC gain error or improve thermal drift characteristics. Figure 65 shows the typical drift characteristics of the internal reference in 1.0 V mode.

Table 13 – Reference Configuration through the SPI

Code	V_{REF}, V	FS
00	0.625	1.25 V p-p
01	0.75	1.5 V p-p
10	0.875	1.75 V p-p
11	1.0	2.0 V p-p (by default)

When the SENSE pin is tied to AVDD, the internal reference is disabled which allows the user to set V_{REF} by the external source. The current flowing into the VREF pin depends on both the external reference and supply voltages but it is typically within ±0.1 mA.

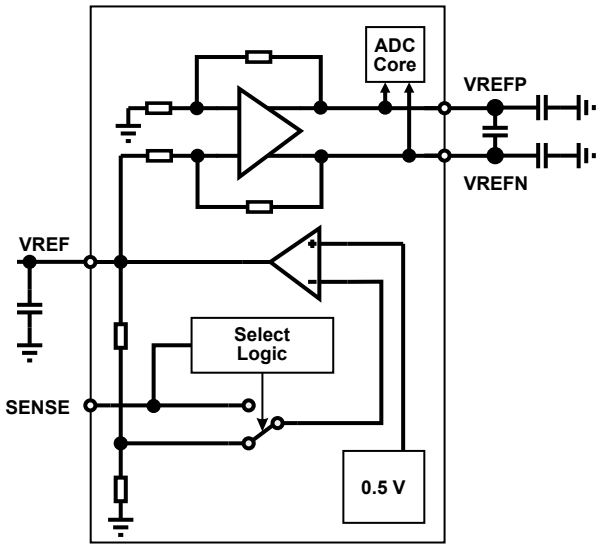

Figure 62 – Internal Reference Configuration

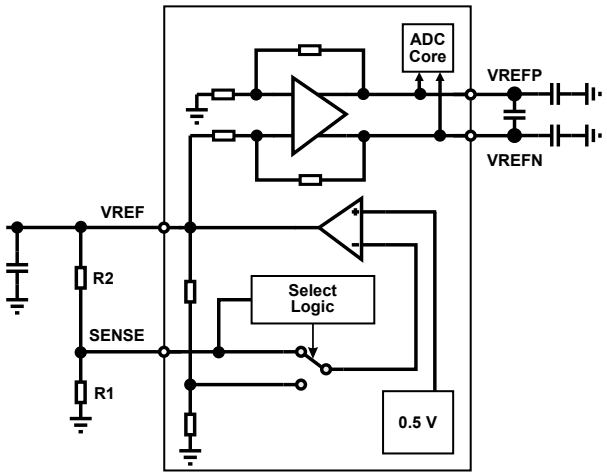

Figure 63 – Programmable Reference Configuration

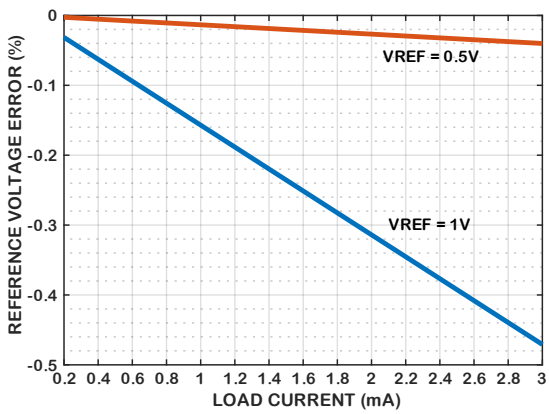

Figure 64 – VREF Accuracy vs. Load

Table 14 – Reference Configuration Summary

Configuration	SENSE Voltage	Resulting V_{REF}, V	ADC scale, V p-p
External	more than V_{DDA} – 0.2	$V_{REF\_external}$	$2V_{REF\_external}$
Internal Fixed	V_{REF}	0.5	1.0
Programmable	between 0.2V and V_{REF}	0.5(1+R2/R1)	$2V_{REF}$
Internal Fixed	less than AGND – 0.2V	1.0	2.0

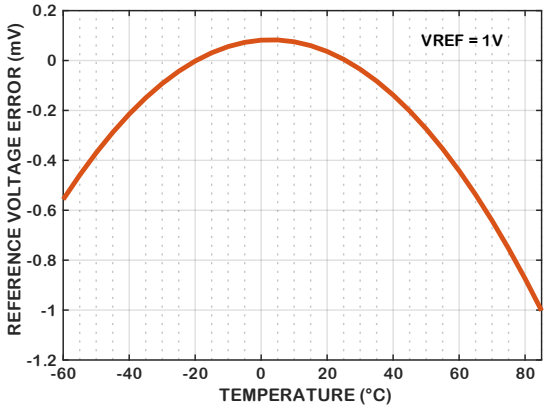

Figure 65 – Typical VREF Drift

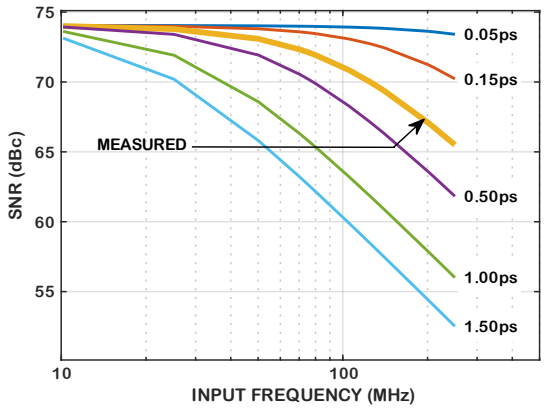

Figure 66 – SNR vs. Input Frequency and Jitter

Input Clock Considerations

For optimal performance it is recommended to clock pins CLKP and CLKN with a differential signal. These pins are DC biased internally and require no external bias (see Figure 67).

The clock input can be CMOS, LVDS, LVPECL or sinusoidal. When selecting signal source its jitter is of the most concern.

Clock Jitter

A high-speed ADC with high resolution is sensitive to the quality of the input clock signal. The degradation of SNR at a given input frequency f_{IN} in relation to the SNR at low frequencies (SNR_{LF}) due to rms aperture jitter of the input clock (t_{JRMS}) can be calculated by

$$SNR_{HF} = -10 \log\left[\left(2\pi f_{IN} \cdot t_{J_{RMS}}\right)^2 + 10^{-\frac{SNR_{LF}}{10}}\right] \quad (3)$$

Undersampling applications are particularly sensitive to jitter, as illustrated in Figure 66.

In addition to the clock own jitter, jitter introduced by the ADC's clock input circuit is also important. The higher clock amplitude and the quicker clock edges are the lower jitter is. Partially this is due to the fact that a circuit operating with steep edges is less sensitive to the power and ground noise.

Since a sinusoidal signal changes more slowly than a rectangular one, the ADC's own jitter is higher when clocked by the sinusoidal signal. It is possible to partially compensate this drawback of the sinusoidal signal by maximizing its amplitude. An amplitude limiter like back-to-back connected Schottky diodes can help to avoid unacceptable voltages at CLKP/CLKN.

The CLKP/CLKN inputs should be considered as analog if an aperture jitter can worsen the ADC dynamic performance. To avoid modulation between the clock signal and digital noise, it is recommended to separate power supplies of clock drivers from the ADC output driver supplies. A circuit based on a low jitter crystal-controlled oscillator makes the best clock source.

Clock Duty Cycle

A typical pipeline ADC uses both clock edges to generate a variety of internal timing signals. That is why it is very sensitive to clock duty cycle. Commonly, a ±2% tolerance of clock duty cycle is required at high sampling speed to maintain dynamic performance characteristics.

If the required clock duty cycle is not provided, the user can use one of the following two methods: turn on the internal duty cycle stabilizer (DCS) or turn on the internal input clock divider with even division ratio.

The DCS retimes the nonsampling (rising) edge of the input clock to provide an internal clock signal with a

nominal 50% duty cycle. Enabling of the DCS does not cancel strict requirements to jitter in the falling edge of the input clock signal. If it is not required, the DCS is recommended to be disabled. At high levels of signal-to-noise ratio (SNR) enabling the DCS can lead to SNR reduction up to 1.2 dB (see Figure 68 and Figure 69).

The DCS may not operate at clock frequencies lower than 20 MHz. The duty cycle control loop has a time constant associated with it, so a wait time of up to 15 μs is required when the clock frequency is changed dynamically. The user can turn on the corrector by writing “1” to bit 6 in register CLK_CTRL.

The DCS typically consumes about 2 mA at 80 MS/s.

Input Clock Divider

The IC contains an input clock frequency divider that allows dividing the input clock by integer values between 2 and 8. In case of even division ratios (2, 4, 6, 8), the duty cycle stabilizer (DCS) is not required because the output of the divider inherently produces a 50% duty cycle. It is not recommended to enable the DCS in these divide modes because it may cause a slight degradation of signal-to-noise ratio.

For other divide ratios (3, 5, and 7) the duty cycle at the divider output is approximately equal to the input clock’s duty cycle. In these modes, if the input clock has a 50% duty cycle, there is no need to turn on the DCS again. However, if a 50% duty cycle clock is not available for any reason, it is required to enable the DCS. Enabling the DCS as well as the Input Clock Divider increases the clock jitter according to Table 6.

The input clock divider can be enabled by selecting a division factor by means of bit 13, 12 and 11 in register CLK_CTRL.

A clock signal with frequency exceeding the maximum of the ADC conversion rate may be applied to the CLKP/CLKN pin. It can be done only if the division factor is *preliminary* set so that the divided clock frequency is within the proper range. The user should first set the required division factor and only then increase the clock frequency. Otherwise, the connection of the external generator with too high frequency to the internal IC circuits can lead to a fault condition.

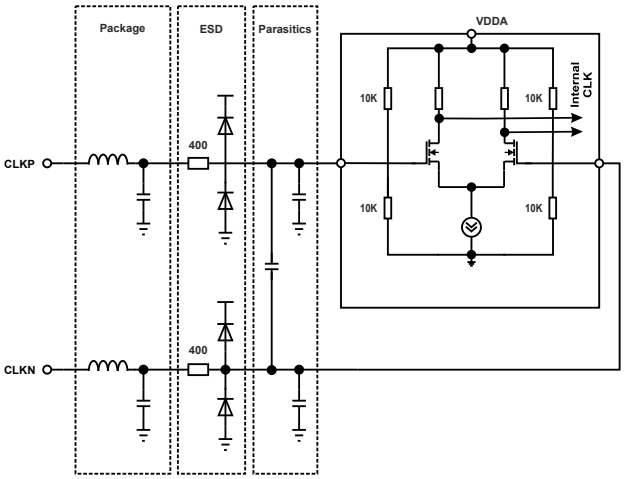

Figure 67 – Equivalent Clock Input Circuit

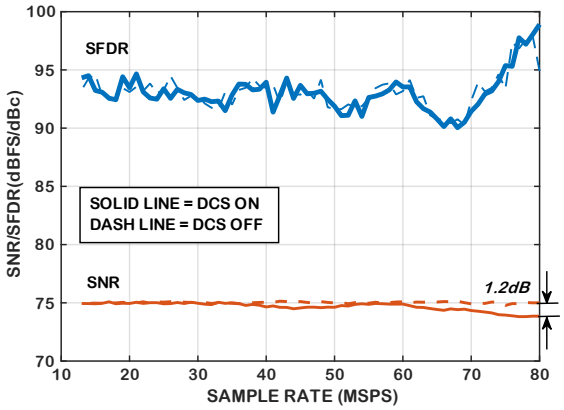

Figure 68 – Typical Single-Tone SNR/SFDR vs. Sample Rate with f_{IN} = 10.1 MHz when the Duty Cycle Stabilizer is either On or Off

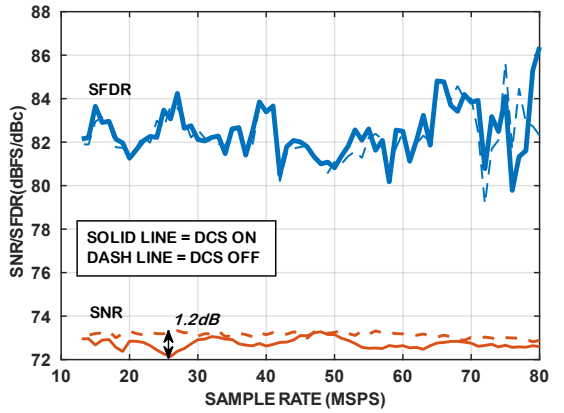

Figure 69 – Typical Single-Tone SNR/SFDR vs. Sample Rate with f_{IN} = 75.1 MHz when the Duty Cycle Stabilizer is either On or Off

Boost and RP Modes

The maximum sample rate of this ADC can be increased up to 95 MS/s while keeping the dynamic performance nearly the same. This improvement is available at the expense of more power consumption and can be achieved by toggling to Boost mode.

On the contrary, a considerable amount of power can be saved, if the ADC operates at sampling frequencies lower than 55 MS/s. For such applications it is recommended to use the ADC in Reduced Power (RP) mode. As well as in Boost mode both the AC and DC performance in RP mode don't degrade in comparison with the default 80 MS/s mode.

To look up the performance details in these modes please see Specifications and Typical Performance Characteristics.

Toggling between default and Boost mode is available via the SPI by programming registers 0x53-0x56. To choose RP mode the value of the external RBIAS resistor should be changed from 12.1 to 24 ±1% kOhm. All the configurations are summarized at Table 15.

Table 15 – Default/Boost/RP Mode Configuration

Register / RBIAS	Default	Boost	RP
0x53	0x0003	0x00DB	0x0003
0x54	0x0027	0x3627	0x0027
0x55	0x0067	0x0127	0x0067
0x56	0x0027	0x4027	0x0027
R_{BIAS}	12.1kΩ	12.1kΩ	24kΩ

Power Consumption and Power Modes

As shown in Figure 70 - Figure 72, the power dissipated by the IC is proportional to its sample rate. In CMOS output mode, the current of the digital drivers is defined by their strength and the load on each output bit (C_L). The maximum current at DRVDD pin can be approximately calculated as

$$I_{Q_{DRVDD}} = V_{DRVDD} \cdot C_L \cdot F_S \cdot N, \qquad (4)$$

where N is the number of output bits plus one DCO.

The power consumption reaches its maximum when every output bit switches on every clock cycle. For example, if a rectangular signal is applied to the ADC input with the Nyquist frequency of $F_S/2$. In practice, the DRVDD current is defined by the average number of output bits switching, which depends on the sample rate and the characteristics of the analog input signal.

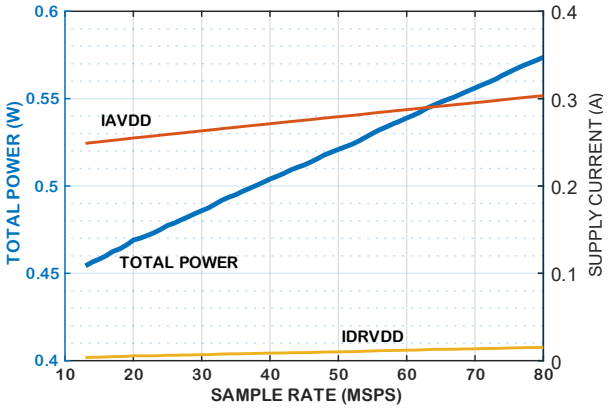

Figure 70 – Power and Current vs. Sample Rate

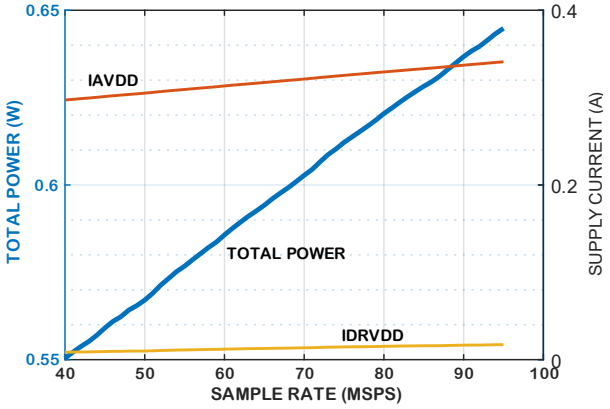

Figure 71 – Power and Current vs. Sample Rate in Boost Mode

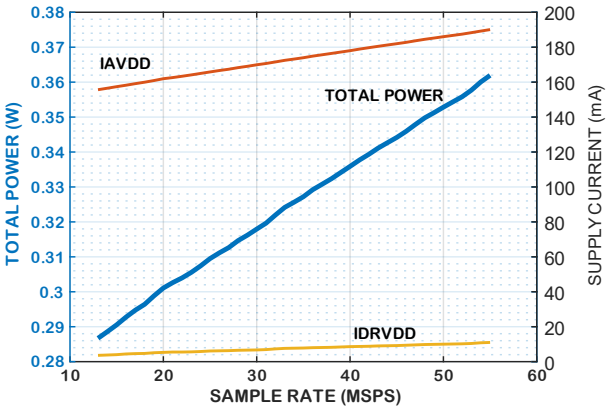

Figure 72 – Power and Current vs. Sample Rate in RP Mode

Output Driver Power

Decreasing the load capacitance leads to reduction of power consumption and also improves SNR, because the noise caused by peak charge currents is decreasing. The same effect is achieved if the output drivers' supply voltage is reduced or they are less powerful. To trim the output digital buffer's power the user can program bit 4, 3 and 1 in register R_CNTRL.

It is recommended to set the lowest power of output drivers, unless it leads to faults while receiving the output data. (Refer to section "Digital Output"). Table 16 shows available configurations of output drivers' power. The greater number of "+" signs the more powerful the drivers are, and on the contrary, '-' sign means lower power relative to its nominal value ("0").

In the LVDS output mode the output interface's power consumption depends weakly on the conversion rate.

Table 16 – Configuration of Output Driver Power in CMOS Output Mode

o_conf (R_CNTRL[1])	od_load (R_CNTRL[4:3])	Output Driver Power mode ("+" – more, "-" – less powerful)
0	00	0 - (the "weakest" driver)
0	01	0 0 (default)
0	10	0 +
0	11	0 ++
1	00	+ -
1	01	+ 0
1	10	+ +
1	11	+ ++ (the most powerful driver)

IC Power Modes

There are three power modes: normal, power-down and standby mode.

Switching from normal (default) to power-down mode can be done either by asserting the PDWN pin high or by writing "01" to register PWR_CTRL. During power-down all the ADC internal blocks including the core, reference circuits, and the input clock buffer are shut down. The external capacitors connected to the VREFP and VREFN pins discharged when entering power-down mode, so they must be recharged when returning to normal operation. It usually takes about 300 µs to recharge these capacitors. In standby mode the internal reference circuitry keeps powered, so faster wake-up times are available (about 100 µs). To choose standby mode write "10" to register PWR_CTRL.

Switching to normal operating mode from power-down or standby mode through the SPI port is not possible because the SPI is not available in these modes. The SPI port is only available if PDWN = "0", otherwise the IC is powered-down.

In shutdown mode the digital output drivers are switched to high-impedance state.

The ADC can be powered-down without applying the input clock. If the PWDN pin is asserted high, the ADC will automatically be placed in power-down mode. During normal operation the PWDN pin may be left disconnected, because there is an internal resistor of 250 kOhm to pull-down the PWDN pin.

Digital Outputs

Digital Output Modes

The ADC output drivers can be configured to interface with either CMOS or LVDS data receiving circuits.

The output data mode can be selected in two ways. Without the SPI it can be done by keeping the voltage at the SCLK/LVDS pin constant during an initialization cycle. The initialization cycle is a time period of 16 clocks after the IC having been reset (for more information please refer to section "Serial Port Interface (SPI)"). If during this initialization time period the SCLK/LVDS pin is tied low, the IC will switch to CMOS output mode. And on the contrary, if the SCLK/LVDS pin is set high during the initialization, the ADC will work in LVDS mode. After the end of the initialization cycle the SCLK/LVDS pin can be used to program the IC through the SPI port, and that will not influence the selected mode.

Since most users do not switch between CMOS and LVDS modes during operation, it is recommended to set the output mode with the SCLK/LVDS pin in advance to avoid unwanted currents through LVDS termination resistors.

The second way to select an output data mode is to write “0” (CMOS) or “1” (LVDS) to bit 2 in register R_CNTRL. After that control should be handed to this register by writing “1” to bit 15 of register 0x04.

The output data drivers can interface with 1.8 V – 3.3 V CMOS logic families. For operation with a particular interface no special configuration is required. It is enough to power the needed supply voltage to the DRVDD pins. It is also recommended to trim the output drivers’ power (see section “Power Consumption and Power Modes”) in order to minimize current glitches on the supplies.

Applications requiring the ADC to drive large capacitive loads may require external buffers or latches. In CMOS mode, the user should take into account that the ADC’s dynamic performance can be a little lower at 3.3 V then at 1.8 V or LVDS mode (see Figure 14). Besides, a higher load capacitance leads to a stronger degradation of the performance in CMOS output mode. The recommended load including the capacitance of the PCB and the digital data receiver’s input is about 4.5 pF.

In LVDS output mode the DRVDD voltage can only be 1.8 V. Output drive levels can be selected either ANSI LVDS or reduced swing LVDS mode (RS). To select the mode via the SPI port, write to bit 1 of register R_CNTRL “0” (ANSI default) or “1” (RS). The reduced swing LVDS mode lowers the DRVDD current and reduces power consumption.

The digital output pins can be switched to a high impedance state. The three-state mode is enabled via the SPI port by writing “0” to register BUF_CONTROL (0x4B). By programming this register’s separate bits, OR signal or DCO signal can be switched to the high-impedance state. Disabling the digital output in this way is not intended for rapid access to the data bus. The output data recovery time can reach 1 µs.

A constant value can be set to any of the output bits using registers OUT_AND (0x4C) and OUT_OR (0x4D) which apply a mask to ADC’s output data according to the scheme of Figure 73.

For example, to switch bit 15 of output code (D15) to “1”, it is required to set bit 15 of register OUT_AND to “1”, and write “1” to bit 15 of register OUT_OR. If D15 is supposed to be constant “0”, it is enough to write “0” to bit 15 of register OUT_AND. Note, that masking of digital data doesn’t have any effect if the sync pattern is applied to the output (see Output Data Synchronization).

Output Data Format

The output data format is selected using bits 6-5 in register R_CTRL. The data format can be selected for either offset binary code (“00”), twos complement (“01”), or gray code (“10”). Table 17 shows an example of encoding. The overflow flag OR indicates that the input signal is out of operating range (see Figure 77).

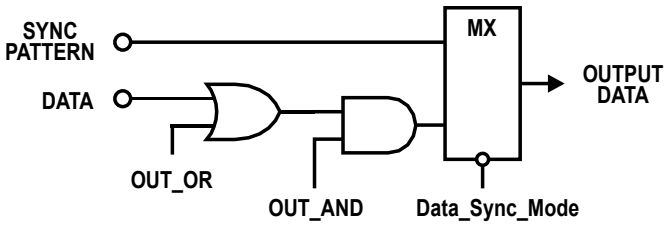

Figure 73 – Masking of Digital Output

Timing

The IC provides latched output data with a pipeline delay of 11 clock cycles (11.5 clock cycles in LVDS mode). Timing diagrams of the ADC operation for both modes are presented in Figure 75 and Figure 76. Data outputs are available one propagation delay t_{PD} after the falling edge of the clock signal.

It is recommended to minimize the length of the output data paths and loads, because long edges can degrade the ADC dynamic performance.

The lowest typical conversion rate of this ADC is 10 MS/s. At sampling rates below 10 MS/s, dynamic performance may degrade. At rates lower than 5 MS/s the ADC does not operate properly.

Data Clock Output

The ADC provides a single data clock output (DCO) pin in CMOS output mode and two differential data clock output pins in LVDS mode. This clock helps the user to capture the output data in an external register.

In CMOS output mode the data outputs are valid on the DCO falling edge. The DCO polarity can be changed by means of bit 0 in register CLK_CTRL.

In LVDS output mode data is output as double data rate with odd numbered output bits (D15, D13, D11, …) transitioning near the falling edge of DCO+/DCO- and the even numbered output bits (D14, D12, D10, …) transitioning near the rising edge of DCO+/DCO-. The data should be captured in an external register by both edges of the differential DCO+/DCO- in this mode.

Output Data Synchronization

The ADC dynamic performance hugely degrades if there is no synchronization of output data flow. In some cases (especially in LVDS mode) the DCO may require shifting in relation to data in order to synchronize the output data and the clock output. DCO delay can be programmed in the range from 0 to 3.4 ns by means of bit 5-1 in register CLK_CTRL. If required, the DCO polarity can be changed.

The user can check if the output data is gathered correctly by a special test mode. In case of writing “1” to bit 10 in register R_CNTRL, a digital test pattern {0x5555 – 0xAAAA – 0x5555 – 0xAAAA - …}, as shown in Figure 74, will be outputted. The user can set its own pattern by registers DATA1 and DATA2. For example, in order to observe data changing each half clock in LVDS mode, the same value as in DATA1 - 0x5555, can be written to DATA2. Detected faults when reading the pattern indicate a desynchronization of the output data and the data clock output (DCO).

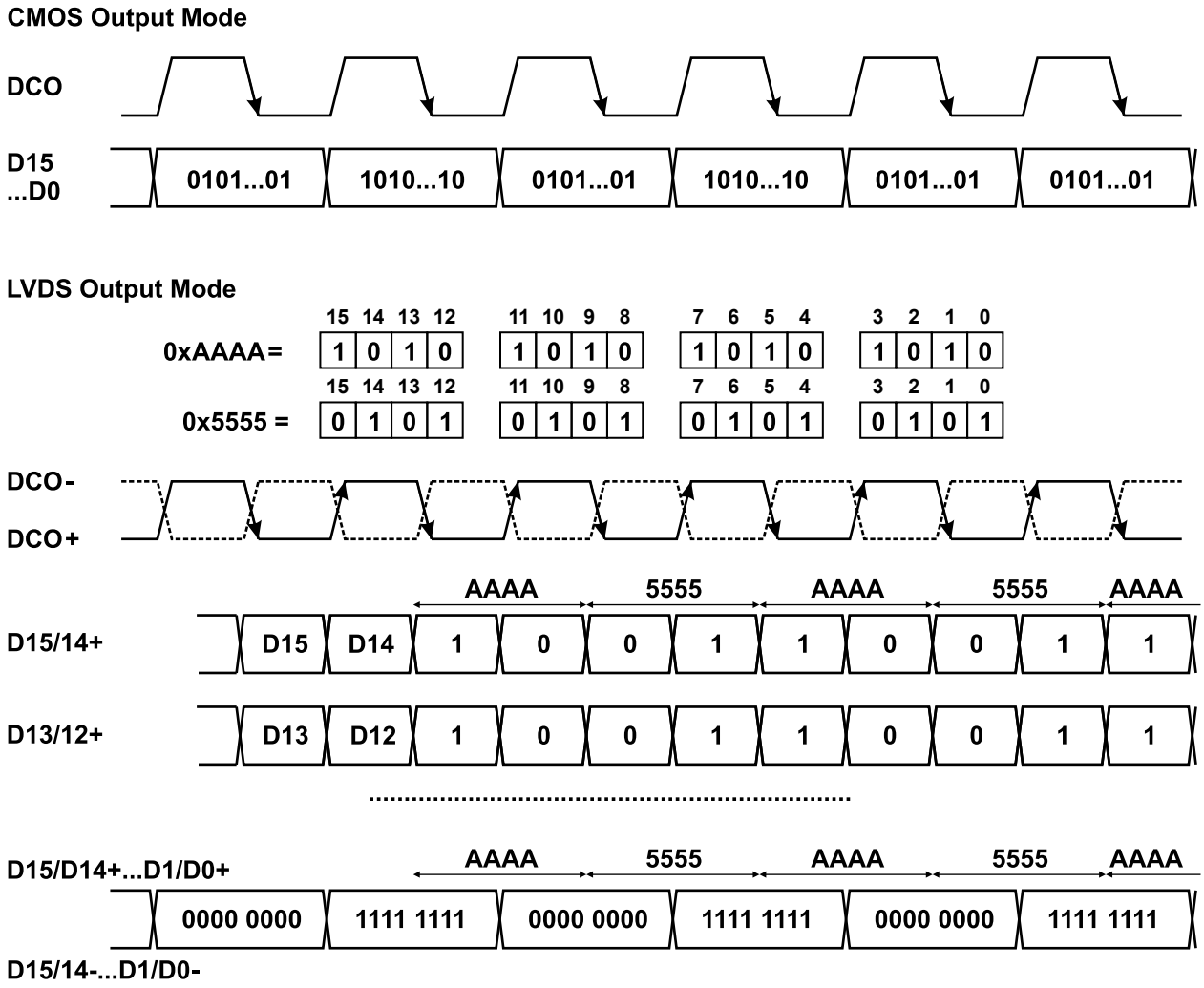

Figure 74 – Digital Output Test Pattern Mode Timing Diagram

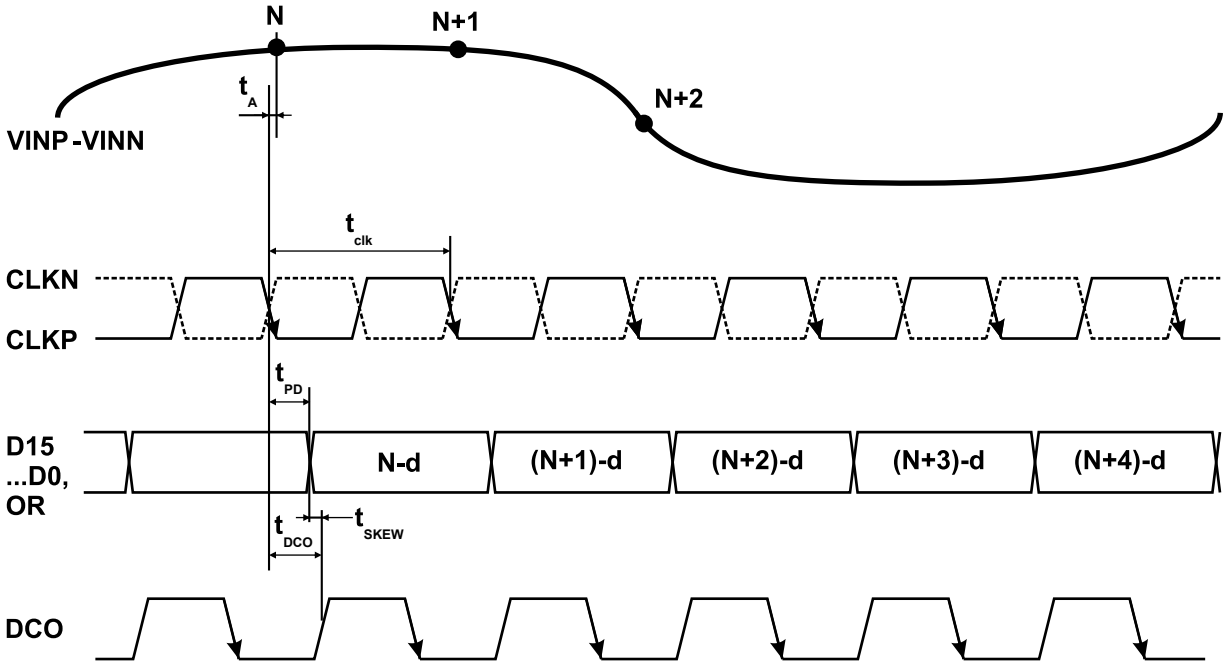

Figure 75 – Timing Diagram of the ADC in CMOS Output Mode

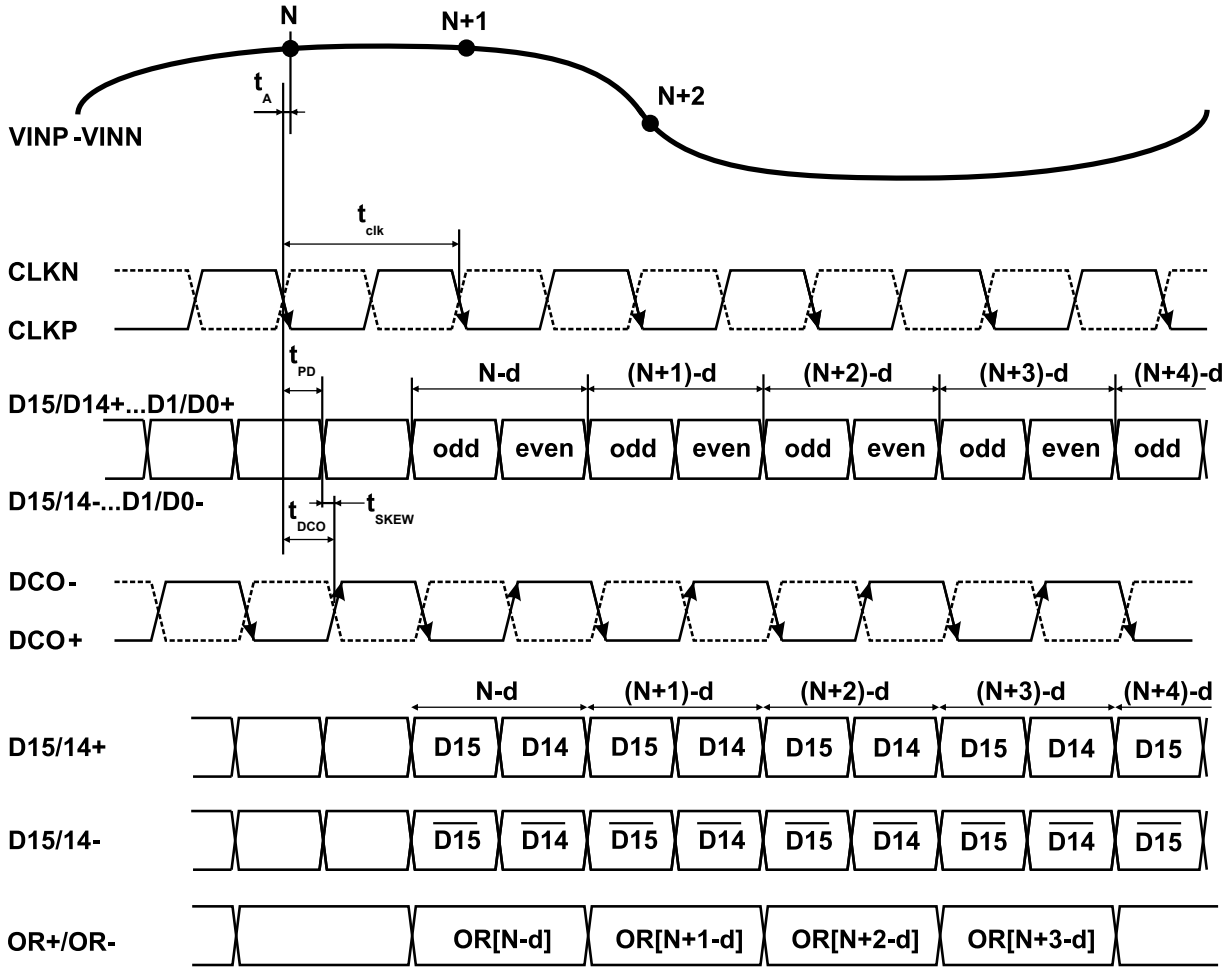

Figure 76 – Timing Diagram of the ADC in LVDS Output Mode

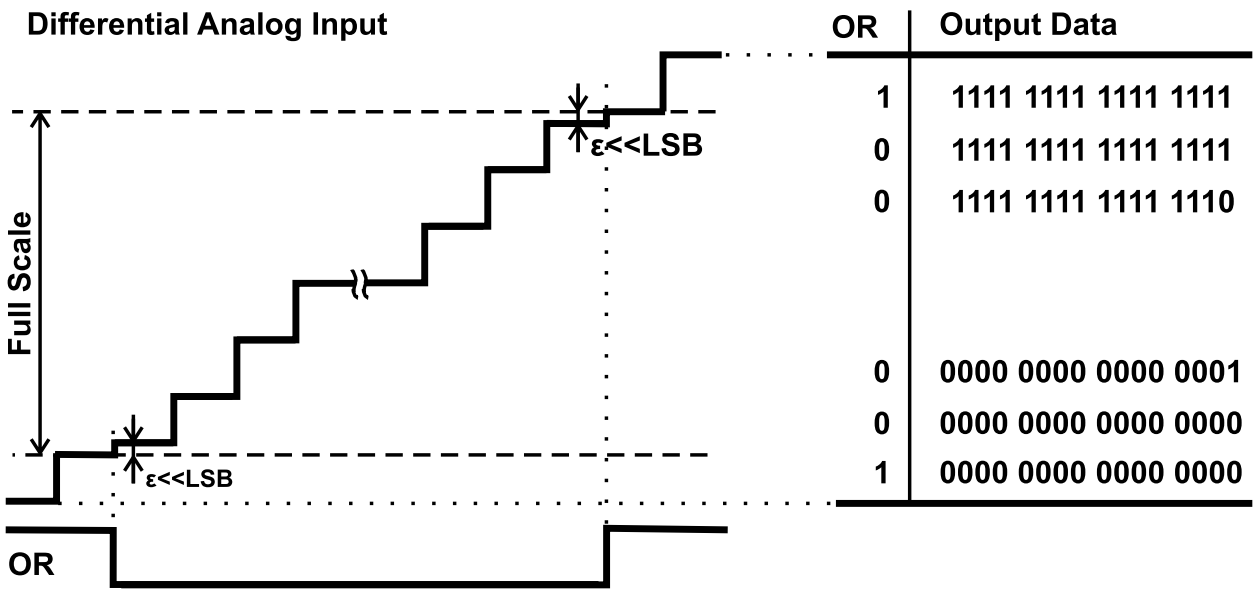

Figure 77 – Overflow Flag (OR)

Table 17 – Output Data Format

V_{INP}-V_{INN}	Offset binary (ODF = 00)	Twos Complement (ODF = 01)	Gray code (ODF = 10)	OR
≤-V_{REF}	0000 0000 0000 0000	1000 0000 0000 0000	0000 0000 0000 0000	1
-V_{REF} + ε[11]	0000 0000 0000 0000	1000 0000 0000 0000	0000 0000 0000 0000	0
-V_{REF} + Δ_{LSB}	0000 0000 0000 0001	1000 0000 0000 0001	0000 0000 0000 0001	0
-V_{REF} + 2Δ_{LSB}	0000 0000 0000 0010	1000 0000 0000 0010	0000 0000 0000 0011	0
-V_{REF} + 3Δ_{LSB}	0000 0000 0000 0011	1000 0000 0000 0011	0000 0000 0000 0010	0
-V_{REF} + 4Δ_{LSB}	0000 0000 0000 0100	1000 0000 0000 0100	0000 0000 0000 0110	0
…	…	…	…	0
-2Δ_{LSB}	0111 1111 1111 1110	1111 1111 1111 1110	0100 0000 0000 0001	0
-Δ_{LSB}	0111 1111 1111 1111	1111 1111 1111 1111	0100 0000 0000 0000	0
0+ ε	1000 0000 0000 0000	0000 0000 0000 0000	1100 0000 0000 0000	0
+Δ_{LSB}	1000 0000 0000 0001	0000 0000 0000 0001	1100 0000 0000 0001	0
+2Δ_{LSB}	1000 0000 0000 0010	0000 0000 0000 0010	1100 0000 0000 0011	0
…	…	…	…	0
+V_{REF} - 4Δ_{LSB}	1111 1111 1111 1011	0111 1111 1111 1011	1000 0000 0000 0110	0
+V_{REF} - 3Δ_{LSB}	1111 1111 1111 1100	0111 1111 1111 1100	1000 0000 0000 0010	0
+V_{REF} - 2Δ_{LSB}	1111 1111 1111 1101	0111 1111 1111 1101	1000 0000 0000 0011	0
+V_{REF} – Δ_{LSB}	1111 1111 1111 1110	0111 1111 1111 1110	1000 0000 0000 0001	0
+V_{REF} - ε	1111 1111 1111 1111	0111 1111 1111 1111	1000 0000 0000 0000	0
≥+V_{REF}	1111 1111 1111 1111	0111 1111 1111 1111	1000 0000 0000 0000	1

[11] ε << Δ_{LSB}, where $\Delta_{LSB} = 2V_{REF}/2^{16}$ – least significant bit

Powering ON and Configuration

Reset and Initialization

In spite of the fact that the ADC has a power-on-reset, for stable operation it is recommended to reset the IC again applying a pulse with zero length of about 0.1 ms to the RST pin after all the external capacitors are charged (including capacitors at the reference voltage pins).

After having reset when the input clock is applied to the CLKP/CLKN pins, the initialization is started and continues for the first 16 clock cycles. During this time period the high level should be maintained at the SS pin. It is also required to set the SCLK/LVDS pin either high or low depending on whether CMOS or LVDS output mode is wanted. Besides the 16 clock cycles for initialization, up to 3000 more clock cycles are required to configure and set up all the internal modes and get the IC ready for operation. It is also recommended to keep the SD pin low during the initialization to make this process as short as possible.

Data Transfer Protocol

Three pins define the SPI port of this ADC: the SD pin, the SCLK/LVDS pin, and the SS pin (see Table 18)

The SCLK/LVDS pin is also used for the ADC initialization and is available only after the 16 first clock cycles. Despite this, it is not recommended to use the SPI earlier than the IC is ready (3000 clocks). Switching the IC to power-down mode by means of PWDN pin before or during the initialization also disables the SPI.

Data transmission through the SPI port is possible only when the clock signal is applied to CLKP/CLKN pins. This is because all signals at the SPI pins are internally re-synchronized to the input clock. The maximum interface frequency is 1/10 of the ADC's clock frequency. Other timing parameters of the SPI are provided in Timing Specifications.

Serial Port Interface (SPI)

The serial port interface (SPI) allows the user to configure the ADC depending on the application. The IC can be configured by programming the registers provided in the Memory Map.

The SPI interface's supply pin is DRVDD, so it can be set at any level between 1.8 V and 3.3 V to enable operation with an SPI bus at these voltages without requiring level translation. The user should also keep in mind that the DRVDD pin defines the digital output levels. The SPI interface is flexible enough to be controlled by either FPGAs or microcontrollers.

The SPI port should not be active during periods when the best dynamic performance of the converter is required. Because the interface signals are typically asynchronous to the ADC clock, noise from these signals can degrade the IC performance. If the SPI bus is used for other devices, it may be necessary to use buffers between the bus and the ADC to prevent these signals from transitioning at the converter inputs during critical sampling moments.

The SPI's controller is always a slave. If the SS signal is high, data is not transmitted. To start the transmission, it is required to switch the SS to the low level, and then transmit data to the SD input synchronously with the SCLK/LVDS (a serial clock) so that the data is valid by the rising edge of SCLK/LVDS (Figure 78). When transmission is completed, it is required to toggle the SS pin high. If the SPI is not used, the SS should be tied high.

The serial frame consists of three bytes (Figure 78, Figure 79). All three bytes are transmitted starting from the least significant bit. The first byte in the frame sets the register's address and transmission direction. The first bit of the first byte indicates whether reading (R/nW="1") or writing (R/nW="0") will be done. In a writing cycle the address byte should be followed by two data bytes. The SD pin works as an input. In a reading cycle, the SD pin changes direction after reading the first address byte, and transmits two data bytes valid for receiving by the SCLK/LVDS rising edge.

Table 18 – Serial Port Interface Pins

Pin	Description
SCLK/LVDS	Serial clock signal which is required to synchronize serial interface writes and reads
SD	Serial data input/output. This bidirectional pin serves as an input or an output, depending on the instruction being sent and the relative position in the timing frame
SS	Interface enable or chip select. An active low enables data receive/transmission

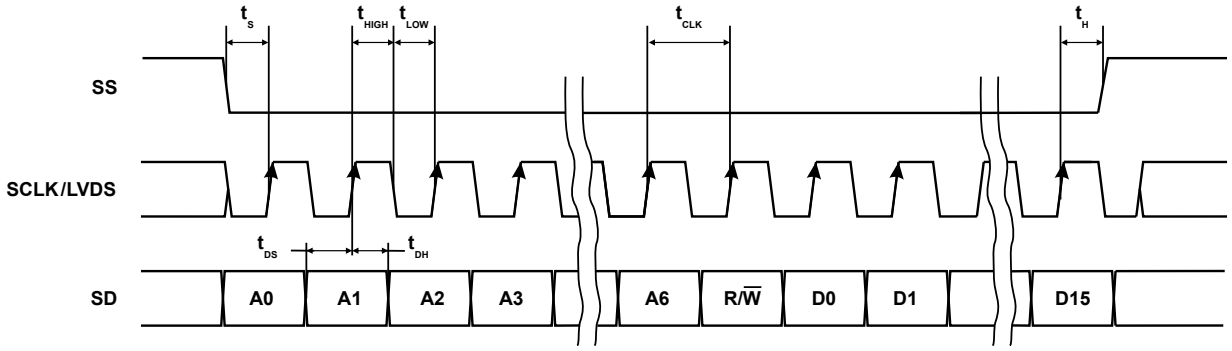

Figure 78 – SPI Timing Diagram

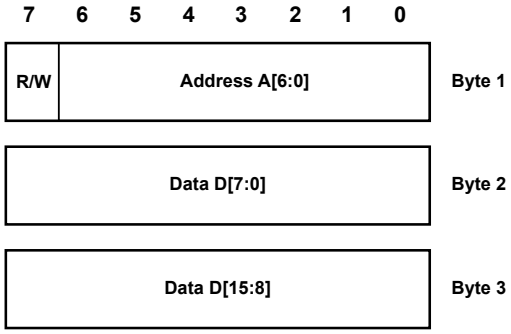

Figure 79 – Serial Frame Format

Configuration without the SPI

In applications that do not interface to the SPI control registers, the SCLK/LVDS pin defines the configuration of the output interface. This pin as well as the PWDN and the RST pin serve as standalone CMOS-compatible control pins. Their CMOS levels correspond to the supply voltage DRVDD. The SS pin should be tied high while the serial interface is disabled. Any change at the SCLK/LVDS matters only during the first 16 clock cycles after reset. Configurations available without the SPI are provided in Table 19.

SPI Accessible Features

Table 20 describes briefly the general features that are accessible via the SPI port.

Memory Map

Each row in the memory map register table has 16-bit location (Table 21). If a location is not filled, it can take any value. There are locations where either “0” or “1” is provided. These are service bits which are responsible for test or unused IC modes. During programming it is not allowed to change the service bits value.

The R_CNTRL(0x01) register is not usual. Some of its bits are used to configure the IC but there are also bits-flags which indicate a current IC status. These bits-flags are not programmable. For example, bit 15, 14, 13 and 0 are service read-only flags. It means that they will not change their value whatever the user writes to them.

The R_CNTRL register has another feature. To take control of its second bit the user should switch a certain multiplexer by writing “1” to bit 15 in register MUX(0x04). This multiplexer is responsible for whether the initial configuration or the configuration via the SPI is used by the ADC. In other words, the R_CNTRL register contains bits which show the active converter configuration and which can be re-program only after reprogramming some other registers. So, if some data is written to the R_CNTRL register and cannot be read back, the following reasons could be:

- Bits-flags have changed,
- Some conditions that allow to change configuration are not met (for example, a multiplexer has not been switched).

There are also the following unfixed problems in the digital part of the IC:

- Two ODF bits of the R_CNTRL register are mixed up after having been read. The IC operates according to the written value.
- The SPI registers are updated “on-fly”, i.e., directly during data transmission
- The user cannot leave power-down or standby mode through the SPI

Table 19 – Mode Selection

Pin	External Voltage	ADC configuration
SCLK/LVDS	DRVDD	LVDS output mode
	AGND	CMOS output mode
PWDN	DRVDD	Power-down mode
	AGND (by default)	Normal operation
RST	DRVDD	Active mode
	AGND	Reset mode

Table 20 – Features Accessible Using the SPI

Feature	Description
Power modes	Allows the user to set either “power-down”, “standby” or “boost” mode
Clock signal	Allows the user to enable the DCS, set the clock divider, and change the input clock phase
Offset	Allows the user to digitally adjust the ADC offset
Test I/O	Allows the user to set known data on output bits
Output Disable	Allows the user completely or separately switch the output bits to high-impedance state
Data Output Mode	Allows the user to set the output mode
Output Delay and Phase	Allows the user to invert DCO, and adjust its delay relative to the data
Reference voltage	Allows the user to set the VREF

Table 21 – Memory map

Addr. (Hex)	Name	Bit 15 (MSB)	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default value (Hex)
0x01	R_CNTRL Interface and reference voltage	Service flag	Service flag	Service flag	0	0	Data_Sync_Mode 0=normal operation 1= a test pattern on output bits	0	vref_select 00=Vref 0.625 01=Vref 0.75 10=Vref 0.875 11=Vref 1.0		Output Data Format 00 = offset binary 01 = twos compliment 10 = Gray code 11 = Gray code		od_load 00 = 2pF 01 = 4pF 10 = 6pF 11 = 8pF		0 = CMOS output mode 1 = LVDS output mode	o_conf. in CMOS: 0=3.3V / 1=1.8V in LVDS: 0=ANSI / 1=RS	Service flag	0x6188
0x04	MUX	LVDS/CMOS mux: which config. to use 0= during initialization 1= programmed by SPI					1	1	1		1		1		11		1	0x7FF
0x44	CORRECTION	Offset (A twos-complement number in the range from -32767 to +32767)																Current value
0x4A	PWR_CTRL Power Mode			0	0	0	0	0	0	1	1	1	1	1	1	Power mode 00 = normal 01 = power-down 10 = standby 11 = normal		0xFC
0x4B	BUF_CONTROL output enable			1	1	EN DNC	EN OR	EN DCN	EN DCO	EN D14 D15	EN D12 D13	EN D10 D11	EN D8 D9	EN D6 D7	EN D4 D5	EN D2 D3	EN D0 D1	0x3FFF
0x4C	OUT_AND	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0xFFFF

Addr. (Hex)	Name	Bit 15 (MSB)	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default value (Hex)
0x4D	OUT_OR	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0
0x4E	CLK_CTRL Input/output Clock			000 = input clock divider disabled 001 = division by 2 010 = division by 3 011 = division by 4 100 = division by 5 101 = division by 6 110 = division by 7 111 = division by 8			00		0 = input clock, no inversion 1 = input clock, inverted		0 = the DCS disabled 1 = the DCS enabled	Data Clock Output delay 00000 = 0 ps 00001 = 95 ps 00010 = 213 ps ... 11110 = 3294 ps 11111 = 3385 ps					DCO polarity 0 = DCO without inversion 1 = DCO with inversion	0
0x53	Boost / RP / Default Mode	0x0003 = Default / RP 0x00DB = Boost																0x0003
0x54		0x0027= Default / RP 0x3627 = Boost																0x0027
0x55		0x0067= Default / RP 0x0127 = Boost																0x0067
0x56		0x0027= Default / RP 0x4027= Boost																0x0027
0x5A	DATA1	The first part of the output test pattern																0x5555
0x5B	DATA2	The second part of the output test pattern																0xAAAA

Outline Dimensions

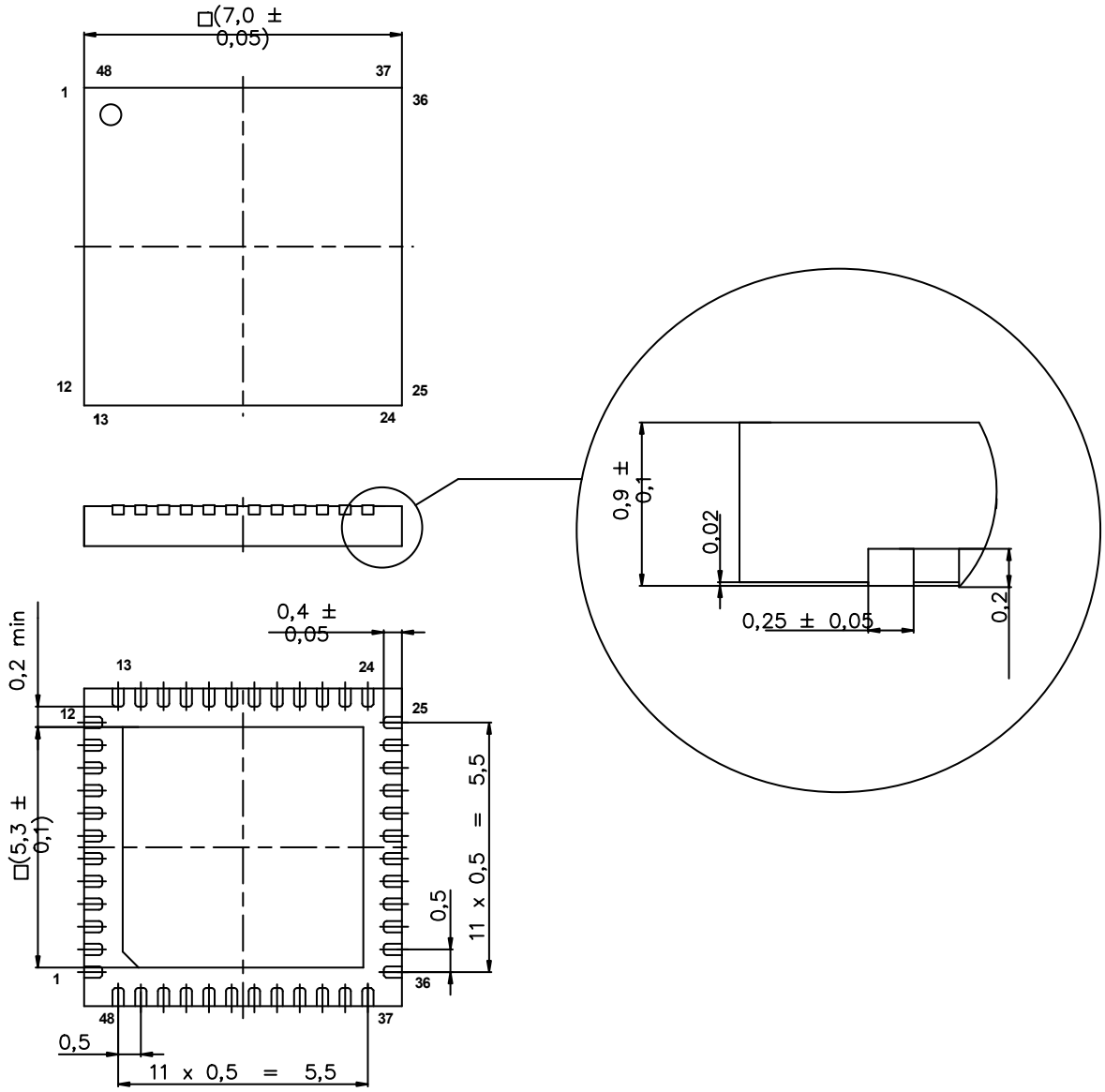

Figure 80 – 48-Pins Quad-Flat No-leads (VQFN48L) Package with an Exposed Pad and 7 mm x 7 mm Body. Dimensions shown in millimeters

Ordering Guide

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