

## Product Overview

The NSI66x1A is a single channel reinforced isolated smart gate driver to drive IGBTs and SiC MOSFETs in many applications. It can source and sink 10A peak current. System robustness is supported by 150kV/us minimum common-mode transient immunity (CMTI).

The NSI66x1A includes crucial protection features such as miller clamp, DESAT, UVLO and soft turn off. UVLO and short circuit fault are reported through separate pins. ASC feature is designed to force output on in emergency, which supports system fault management.

NSI66x1A is suitable for high reliability, power density and efficiency switching power system.

## Key Features

- 5.7kV<sub>RMS</sub> withstand isolation voltage
- SiC MOSFETs and IGBTs up to 2121V<sub>pk</sub>
- Driver side supply voltage: up to 32V with UVLO
- 10A peak source and sink output current
- High CMTI: ±150kV/us
- 200ns fast response time of DESAT
- Monitor status of device on FLT and RDY
- 80ns typical propagation delay
- 400mA soft turn off current
- 30ns maximum pulse width distortion
- Internal miller clamp
- Active short circuit protection
- Operation ambient temperature: -40°C ~125°C
- RoHS & REACH Compliant
- Lead-free component, suitable for lead-free soldering profile: 260°C, MSL2

## Safety Regulatory Approvals

- UL recognition: 5700V<sub>RMS</sub>
- DIN EN IEC 60747-17(VDE 0884-17)
- CSA component notice 5A
- CQC certification per GB4943.1

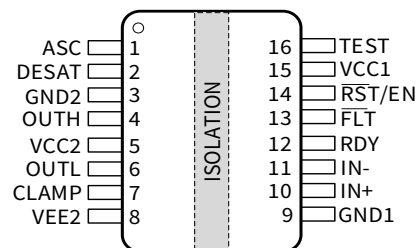
## Applications

- Isolated IGBT/SiC MOSFET gate driver
- On-board Charger and DC/DC Converter for HEV/EVs
- Industrial Motor Drives and Solar Inverters
- UPS and Power Supplies

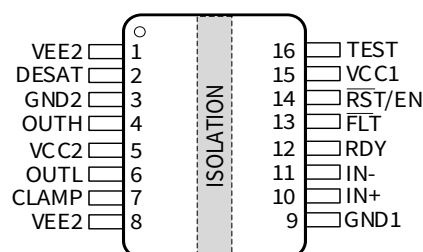
## Device Information

| Part Number     | ASC Feature | Package | Body size      |
|-----------------|-------------|---------|----------------|
| NSI6611ASC-DSWR | Yes         | SOW16   | 10.3×7.5×2.3mm |
| NSI6651ASC-DSWR | No          | SOW16   | 10.3×7.5×2.3mm |
| NSI6651ALC-DSWR | No          | SOW16   | 10.3×7.5×2.3mm |

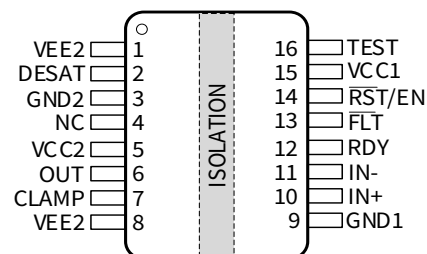
## Functional Block Diagram



NSI6611ASC-DSWR



NSI6651ASC-DSWR



NSI6651ALC-DSWR

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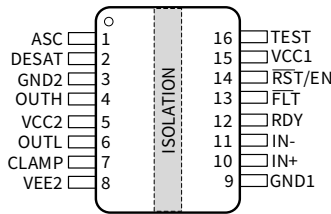
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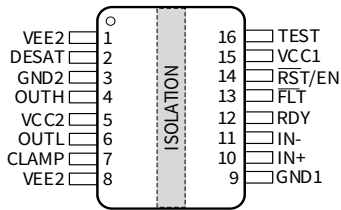
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# 1. Pin Configuration and Functions

NSI6611ASC Top View



NSI6651ASC Top View



NSI6651ALC Top View

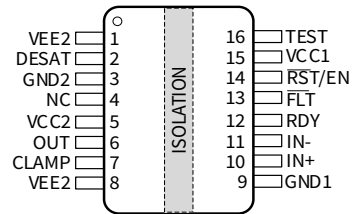


Table 1.1 NSI66x1A Pin Configuration and Description

| SYMBOL           | PIN NO.    |            |            | FUNCTION  |
|------------------|------------|------------|------------|---|
|                  | NSI6611ASC | NSI6651ASC | NSI6651ALC |   |
| ASC              | 1          | /          | /          | Active Short Circuit pin. If ASC is set to high, the OUTH pin will be forced to output high under the emergency         |
| DESAT            | 2          | 2          | 2          | Fast overcurrent and short circuit protection   |
| GND2             | 3          | 3          | 3          | Driver side ground pin  |
| OUTH             | 4          | 4          | /          | Driver source output pin  |
| V <sub>CC2</sub> | 5          | 5          | 5          | Driver side positive supply pin   |
| OUTL             | 6          | 6          | /          | Driver sinks output pin   |
| CLAMP            | 7          | 7          | 7          | Internal active miller clamp to prevent false turn-on   |
| V <sub>EE2</sub> | 8          | 1,8        | 1,8        | Driver side negative supply pin   |
| GND1             | 9          | 9          | 9          | Input-side ground pin   |
| IN+              | 10         | 10         | 10         | Non-inverting gate driver control input   |
| IN-              | 11         | 11         | 11         | Inverting gate driver control input   |
| RDY              | 12         | 12         | 12         | Power good signal. Active low to report under voltage lock  |
| FLT              | 13         | 13         | 13         | Fault output pin. Active low to report overcurrent or short circuit   |
| RST              | 14         | 14         | 14         | Enable the device if this pin is set to high, or reset the fault signal under DESAT condition if this pin is set to low |
| V <sub>CC1</sub> | 15         | 15         | 15         | Input-side power supply   |
| NC               | /          | /          | 4          | No Connection   |
| OUT              | /          | /          | 6          | Driver output pin   |
| Test             | 16         | 16         | 16         | Test mode pin. It is recommended to connect to GND1   |

## 2. Absolute Maximum Ratings

| Parameters                     | Symbol                          | Min           | Max           | Unit |
|--------------------------------|---------------------------------|---------------|---------------|------|
| Driver Side Supply Voltage     | $V_{CC2-V_{EE2}}$               | -0.3          | 35            | V    |
| Driver Side Supply Voltage     | $V_{CC2-GND2}$                  | -0.3          | 35            | V    |
| Driver Side Supply Voltage     | $V_{EE2-GND2}$                  | -17.5         | 0.3           | V    |
| Output Signal Voltage - DC     | $V_{OUTH}, V_{OUTL}, V_{CLAMP}$ | $V_{EE2}-0.3$ | $V_{CC2}$     | V    |
| Operating Junction Temperature | $T_J$                           | -40           | 150           | °C   |
| Storage Temperature            | $T_{stg}$                       | -65           | 150           | °C   |
| Input Side Supply Voltage      | $V_{CC1}$                       | -0.3          | 6             | V    |
| Input Signal Voltage - DC      | $V_{IN+}, V_{IN-}, V_{RST}$     | GND1-0.3      | $V_{CC1}+0.3$ | V    |
| RDY, FLT (Input Side)          | $V_{RDY}, V_{FLT}$              | GND1-0.3      | $V_{CC1}$     | V    |
| FLT and RDY input current      | $I_{FLT}, I_{RDY}$              |               | 20            | mA   |
| DESAT (Driver Side)            | $V_{DESAT}$                     | GND2-0.3      | $V_{CC2}+0.3$ | V    |
| ASC (Driver Side)              | $V_{ASC}$                       | GND2-0.3      | GND2+6        | V    |

## 3. ESD Ratings

|                         |   | Symbol         | Value | Unit |
|-------------------------|---|----------------|-------|------|
| Electrostatic discharge | Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup> | $V_{ESD\_HBM}$ | ±3000 | V    |
|                         | Charged-device model (CDM), per AEC Q100-011            | $V_{ESD\_CDM}$ | ±1500 | V    |

1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 4. Recommended Operating Conditions

| Parameters                                      | Symbol                   | Min                  | Max                  | Unit |
|---|--------------------------|----------------------|----------------------|------|
| Ambient Temperature                             | $T_A$                    | -40                  | 125                  | °C   |
| Input Side Supply Voltage                       | $V_{CC1-GND1}$           | 3                    | 5.5                  | V    |
| Driver Side Supply Voltage                      | $V_{CC2-GND2}$           | 13                   | 32                   | V    |
| Driver Side Supply Voltage                      | $V_{CC2-V_{EE2}}$        | -                    | 32                   | V    |
| ASC (Driver Side)                               | $V_{ASC}$                | GND2                 | GND2+5               | V    |
| $IN+, IN-, \overline{RST}/EN$ (Respect to GND1) | High level input voltage | $0.7 \times V_{CC1}$ | $V_{CC1}$            | V    |
|   | Low level input voltage  | 0                    | $0.3 \times V_{CC1}$ |      |

## 5. Thermal Information

| <i>Parameters</i>                            | <i>Symbol</i>   | <i>SOW16</i> | <i>Unit</i> |
|--|-----------------|--------------|-------------|
| Junction-to-ambient thermal resistance       | $R_{\theta JA}$ | 97.0         | °C/W        |
| Junction-to-top characterization parameter   | $\Psi_{JT}$     | 35.8         | °C/W        |
| Junction-to-board characterization parameter | $\Psi_{JB}$     | 39.0         | °C/W        |
| Junction-to-case(top) thermal resistance     | $R_{JC(top)}$   | 23.3         | °C/W        |

- 1) Standard JESD51-3 Low Effective Thermal Conductivity Test Board (1s) in an environment described in JESD51-2a.
- 2) Standard JESD51-3 Low Effective Thermal Conductivity Test Board (1s) by transient dual interface test method described in JESD51-14.
- 3) Obtained by Simulating in an environment described in JESD51-2a.

## 6. Specifications

### 6.1. DC Electrical Characteristics

All min and max specifications are at  $T_A = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . Typical values are tested at  $V_{CC1} = 3.3\text{V}$  or  $5\text{V}$ ,  $V_{CC2} = 15\text{V}$  or  $30\text{V}$ ,  $V_{EE2} = \text{GND2}$ .

| Parameter                                   | Symbol           | Min  | Typ  | Max  | Unit          | Condition   |
|---|------------------|------|------|------|---------------|---|
| <b>Input Side Supply</b>                    |                  |      |      |      |               |   |
| Input side Supply Quiescent Current         | $I_{CC1}$        | 0.6  | 1.6  | 3.6  | mA            | $V_{CC1} = 5\text{V}$ , OUT=High  |
| $V_{CC1}$ UVLO Rising Threshold             | $V_{CC1\_ON}$    | 2.5  | 2.7  | 2.9  | V             |   |
| $V_{CC1}$ UVLO Falling Threshold            | $V_{CC1\_OFF}$   | 2.3  | 2.5  | 2.7  | V             |   |
| $V_{CC1}$ UVLO Hysteresis                   | $V_{CC1\_HYS}$   |      | 0.2  |      | V             |   |
| $V_{CC1}$ UVLO deglitch time                | $t_{VCC1\_FIL}$  |      | 10   |      | $\mu\text{s}$ | $\overline{\text{IN}}+ = V_{CC1}$ $\overline{\text{IN}}- = \text{GND1}$ |
| $V_{CC1}$ UVLO on delay to output high      | $t_{VCC1H\_OUT}$ |      | 33   |      |               |   |
| $V_{CC1}$ UVLO on delay to output low       | $t_{VCC1L\_OUT}$ |      | 10   |      |               |   |
| $V_{CC1}$ UVLO on delay to RDY high         | $t_{VCC1H\_RDY}$ |      | 38   |      |               |   |
| $V_{CC1}$ UVLO on delay to RDY low          | $t_{VCC1L\_RDY}$ |      | 10   |      |               |   |
| <b>Driver Side Supply</b>                   |                  |      |      |      |               |   |
| Driver side Supply Quiescent Current        | $I_{CC2}$        | 2.5  | 3.3  | 4.3  | mA            | $V_{CC2} = 15\text{V}$ , $V_{EE2} = \text{GND2}$ ,<br>OUT=High          |
| $V_{CC2}$ UVLO Rising Threshold             | $V_{CC2\_ON}$    | 10.5 | 11.2 | 12.8 | V             |   |
| $V_{CC2}$ UVLO Falling Threshold            | $V_{CC2\_OFF}$   | 9.8  | 10.4 | 11.8 | V             |   |
| $V_{CC2}$ UVLO Hysteresis                   | $V_{CC2\_HYS}$   |      | 0.8  |      | V             |   |
| $V_{CC2}$ UVLO deglitch time                | $t_{VCC2\_FIL}$  |      | 5    |      | $\mu\text{s}$ | $\overline{\text{IN}}+ = V_{CC1}$ $\overline{\text{IN}}- = \text{GND1}$ |
| $V_{CC2}$ UVLO on delay to output high      | $t_{VCC2H\_OUT}$ |      | 11   |      |               |   |
| $V_{CC2}$ UVLO on delay to output low       | $t_{VCC2L\_OUT}$ |      | 10   |      |               |   |
| $V_{CC2}$ UVLO on delay to RDY high         | $t_{VCC2H\_RDY}$ |      | 11   |      |               |   |
| $V_{CC2}$ UVLO on delay to RDY low          | $t_{VCC2L\_RDY}$ |      | 14   |      |               |   |
| <b>RDY Reporting</b>                        |                  |      |      |      |               |   |
| $V_{CC2}$ UVLO RDY low minimum holding time | $t_{RDY\_HLD}$   |      |      | 1    | ms            |   |
| Open drain low output voltage               | $V_{RDY\_L}$     |      |      | 0.3  | V             | $I_{\text{SINK\_RDY}} = 5\text{mA}$                                     |
| <b>Input Pin Characteristic</b>             |                  |      |      |      |               |   |
| Logic High Input Threshold (IN+, IN-, RST)  | $V_{INH}$        |      | 2.9  | 3.5  | V             | $V_{CC1} = 5\text{V}$   |
| Logic Low Input Threshold (IN+, IN-, RST)   | $V_{INL}$        | 1.5  | 2.1  |      | V             | $V_{CC1} = 5\text{V}$   |
| Input Hysteresis Voltage (IN+, IN-, RST)    | $V_{hys\_IN}$    |      | 0.8  |      | V             | $V_{CC1} = 5\text{V}$   |
| IN+ Input Current                           | $I_{IN+\_H}$     |      | 90   |      | $\mu\text{A}$ | $V_{IN+} = 5\text{V}$   |

**DC Electrical Characteristics(continued)**

All min and max specifications are at  $T_A = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . Typical values are tested at  $V_{CC1} = 3.3\text{V}$  or  $5\text{V}$ ,  $V_{CC2} = 15\text{V}$  or  $30\text{V}$ ,  $V_{EE2} = \text{GND2}$ .

| Parameter   | Symbol           | Min | Typ             | Max             | Unit          | Condition   |
|---|------------------|-----|-----------------|-----------------|---------------|---|
| IN- Input Current                                   | $I_{IN\_L}$      |     | -90             |                 | $\mu\text{A}$ | $V_{IN} = \text{GND1}$  |
| <b>ASC Pin Characteristic (only for NSI6611ASC)</b> |                  |     |                 |                 |               |   |
| Logic High Input Threshold (ASC)                    | $V_{ASCH}$       | 2.7 | 2.9             | 3.2             | V             |   |
| Logic Low Input Threshold (ASC)                     | $V_{ASCL}$       | 1.3 | 1.5             | 1.7             | V             |   |
| ASC to output rising edge delay                     | $t_{ASC\_r}$     | 390 | 560             | 1100            | ns            |   |
| ASC to output falling edge delay                    | $t_{ASC\_f}$     | 150 | 360             | 480             | ns            |   |
| <b>Enable Pin Characteristic</b>                    |                  |     |                 |                 |               |   |
| RST deglitch filter time for Enable/Shutdown        | $t_{min\_RST}$   | 28  | 40              | 60              | ns            |   |
| <b>Output Pin Characteristic</b>                    |                  |     |                 |                 |               |   |
| High Level Output Voltage                           | $V_{OH}$         |     | $V_{CC2} - 0.6$ |                 | V             | $I_{OUT} = -200\text{mA}$ , $V_{IN+} = \text{High}$ , $V_{IN-} = \text{Low}$                                |
| Low Level Output Voltage                            | $V_{OL}$         |     | 0.1             |                 | V             | $I_{OUT} = 200\text{mA}$ , $V_{IN+} = \text{Low}$ , $V_{IN-} = \text{Low}$                                  |
| Output pull-up resistance                           | $R_{OH}$         |     | 2.2             |                 | $\Omega$      | $I_{OUT} = -0.1\text{A}$ , $V_{IN+} = \text{High}$ , $V_{IN-} = \text{Low}$                                 |
| Output pull-down resistance                         | $R_{OL}$         |     | 0.3             |                 | $\Omega$      | $I_{OUT} = 0.1\text{A}$ , $V_{IN+} = \text{Low}$ , $V_{IN-} = \text{High}$                                  |
| Low Level Clamp Voltage                             | $V_{CLAMP}$      |     | $V_{EE2} + 0.8$ |                 | V             | $I_{CLAMP} = 1\text{A}$ , $V_{IN+} = \text{Low}$ , $V_{IN-} = \text{Low}$                                   |
| High Level Peak Output Current                      | $I_{OUTH}$       |     | 11              |                 | A             | $V_{CC2} = 15\text{V}$ , pulse width $< 10\mu\text{s}$  |
| Low Level Peak Output Current                       | $I_{OUTL}$       |     | 12              |                 | A             |   |
|   |                  |     | 8               |                 | A             | $V_{OUT} = V_{EE2} + 2.5\text{V}$   |
| Clamp Threshold Voltage                             | $V_{CLAMP\_TH}$  | 1.5 | 2               | 2.5             | V             | $V_{CLAMP}$ falling, $V_{IN+} = \text{Low}$ , $V_{IN-} = \text{Low}$  |
| Calmp Delay   | $t_{DCLMP}$      |     | 60              |                 | ns            |   |
| OUT Short Circuit Clamping Voltage                  | $V_{CLP\_OUT}$   |     | $V_{CC2} + 1.1$ | $V_{CC2} + 2$   | V             | $V_{IN+} = \text{High}$ , $V_{IN-} = \text{Low}$ , $I_{OUTL} = 0.5\text{A}$ , pulse width $< 10\mu\text{s}$ |
| CLAMP Short Circuit Clamping Voltage                | $V_{CLP\_CLAMP}$ |     | $V_{CC2} + 1.8$ | $V_{CC2} + 2.5$ | V             | $V_{IN+} = \text{High}$ , $V_{IN-} = \text{Low}$ , $I_{OUTH} = 0.5\text{A}$ , pulse width $< 10\mu\text{s}$ |
|   |                  |     | $V_{CC2} + 0.8$ |                 | V             | $V_{IN+} = \text{High}$ , $V_{IN-} = \text{Low}$ , $I_{CLAMP} = 20\text{mA}$                                |
| OUT Active Pull-Down Voltage                        | $V_{SD\_OUT}$    | 1.5 | 2.3             | 3.1             | V             | $V_{CC2} = \text{OPEN}$ , $I_{OUTL} = 0.1 \times I_{OUTL}(\text{typ})$                                      |

**DC Electrical Characteristics(continued)**

All min and max specifications are at  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ . Typical values are tested at  $V_{CC1} = 3.3\text{V}$  or  $5\text{V}$ ,  $V_{CC2} = 15\text{V}$  or  $30\text{V}$ ,  $V_{EE2} = \text{GND2}$ .

| <b>Parameter</b>                           | <b>Symbol</b>           | <b>Min</b> | <b>Typ</b> | <b>Max</b> | <b>Unit</b>   | <b>Condition</b>                    |
|--|-------------------------|------------|------------|------------|---------------|-------------------------------------|
| <b>Desaturation</b>                        |                         |            |            |            |               |                                     |
| Blanking Capacitor Discharge Current       | $I_{\text{DCHG}}$       | 12         | 14         |            | mA            | $V_{\text{DESAT}} = 6\text{V}$      |
| Blanking Capacitor Charge Current          | $I_{\text{CHG}}$        | 430        | 500        | 600        | $\mu\text{A}$ | $V_{\text{DESAT}} = 2\text{V}$      |
| Detection Threshold                        | $V_{\text{DESAT\_TH}}$  | 8.5        | 9.26       | 9.8        | V             |                                     |
| Leading edge blank time                    | $t_{\text{DESAT\_LEB}}$ |            | 200        |            | ns            |                                     |
| DESAT deglitch filter time                 | $t_{\text{DESAT\_FIL}}$ | 150        | 200        | 265        | ns            |                                     |
| DESAT sense to OUT(L) 90% delay            | $t_{\text{DESAT\_OFF}}$ | 150        | 250        | 300        | ns            |                                     |
| DESAT sense to FLT low delay               | $t_{\text{DESAT\_FLT}}$ | 400        | 650        | 750        | ns            |                                     |
| FLT mute time                              | $t_{\text{FLT\_MUTE}}$  | 0.55       |            | 1          | ms            |                                     |
| RST deglitch filter time for Resetting FLT | $t_{\text{RST\_FIL}}$   | 400        | 600        | 800        | ns            |                                     |
| <b>Soft turn off</b>                       |                         |            |            |            |               |                                     |
| Soft turn off current                      | $I_{\text{STO}}$        | 250        | 400        | 570        | mA            |                                     |
| <b>FLT Reporting</b>                       |                         |            |            |            |               |                                     |
| Open drain low output voltage              | $V_{\text{FLT\_L}}$     |            |            | 0.3        | V             | $I_{\text{SINK\_FLT}} = 5\text{mA}$ |



## 6.2. Switching Electrical Characteristics

Typical values are at  $V_{CC1}=5V$ ,  $V_{CC2}=15V$ ,  $V_{EE2}=GND2$ . All min and max specifications are at  $T_A=-40^{\circ}C$  to  $125^{\circ}C$ ,  $C_L=0.1nF$

| Parameter                                  | Symbol               | Min | Typ | Max | Unit        | Condition        |
|--|----------------------|-----|-----|-----|-------------|------------------|
| Minimum Pulse Width                        | $t_{PWmin\_IN+,IN-}$ | 20  | 40  | 70  | ns          |                  |
| Output Rise Time                           | $t_R$                |     | 56  |     | ns          | $C_{LOAD}=10nF$  |
| Output Fall Time                           | $t_F$                |     | 53  |     | ns          |                  |
| Propagation Delay                          | $t_{pLH\_IN+,IN-}$   | 70  | 80  | 110 | ns          | $C_{LOAD}=0.1nF$ |
|  | $t_{pHL\_IN+,IN-}$   | 70  | 80  | 110 | ns          |                  |
| Pulse Width Distortion $ t_{pHL}-t_{pLH} $ | $t_{PWD}$            |     |     | 30  | ns          |                  |
| Common Mode Transient Immunity             | CMTI                 | 150 |     |     | kV/ $\mu s$ |                  |

### 6.3. Typical Characteristics

V<sub>CC1</sub>= 5V, V<sub>CC2</sub> =15V, V<sub>EE2</sub>=GND2 for NSI66x1A. Output has no load unless otherwise noted.

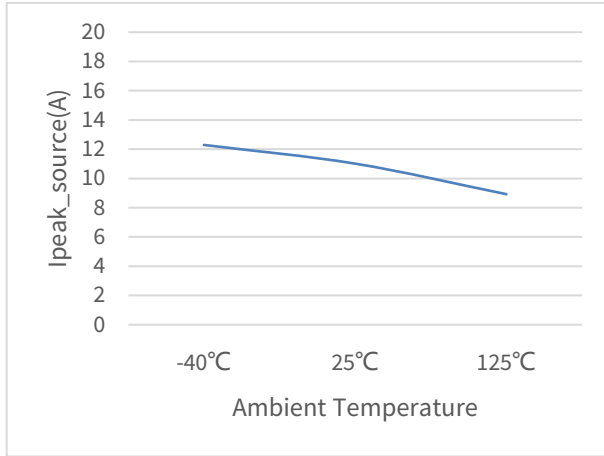


Figure 6.1 I<sub>peak\_source</sub> vs Temperature

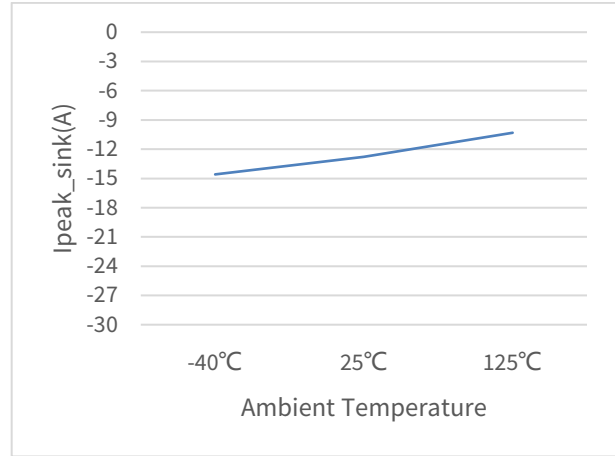


Figure 6.2 I<sub>peak\_sink</sub> vs Temperature

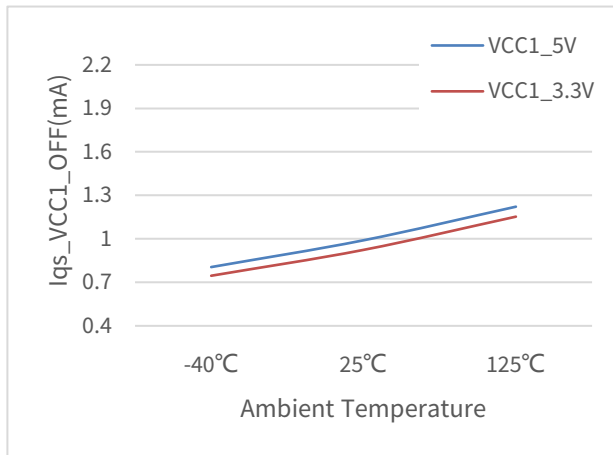


Figure 6.3 I<sub>qs\_VCC1\_OFF</sub> vs Temperature

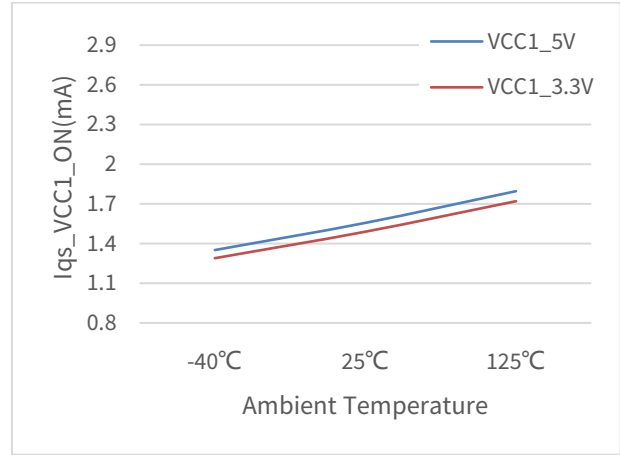


Figure 6.4 I<sub>qs\_VCC1\_ON</sub> vs Temperature

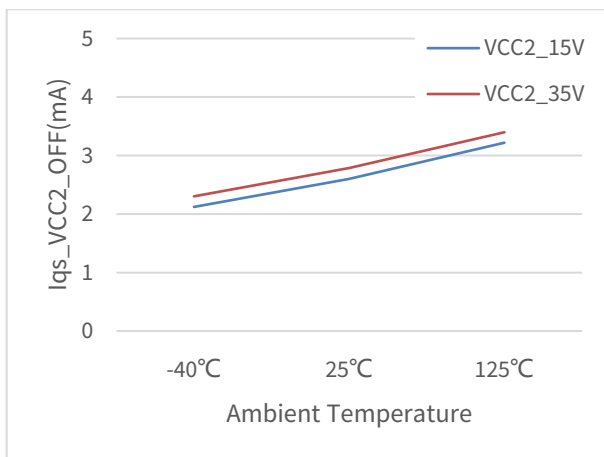


Figure 6.5 I<sub>qs\_VCC2\_OFF</sub> vs Temperature

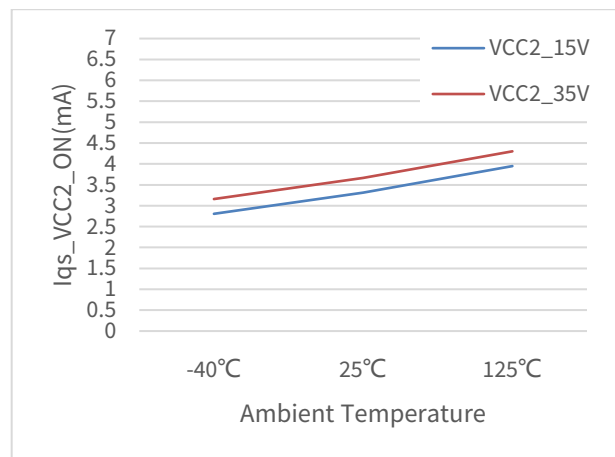


Figure 6.6 I<sub>qs\_VCC2\_ON</sub> vs Temperature

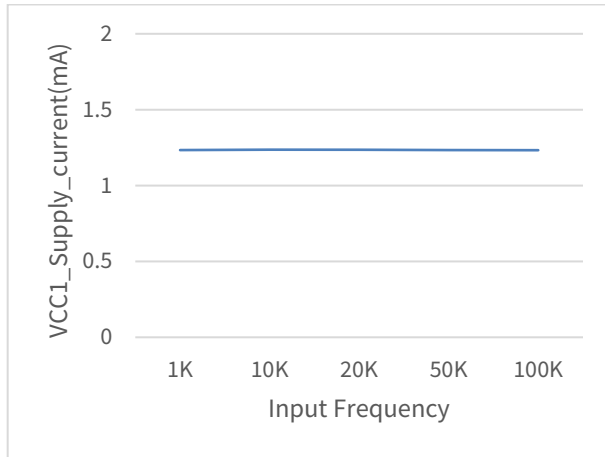


Figure 6.7 V<sub>CC1</sub> Supply current vs Input Frequency

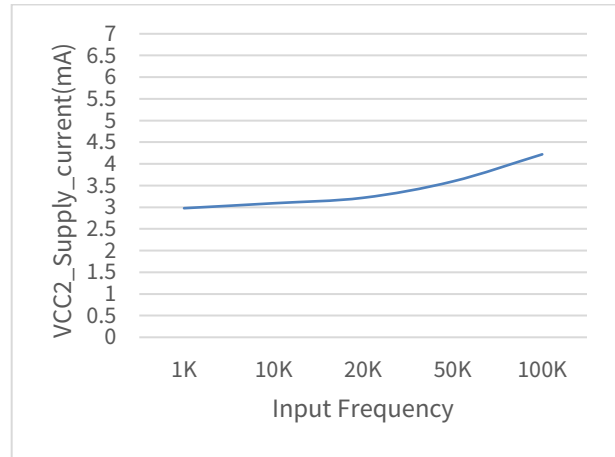


Figure 6.8 V<sub>CC2</sub> Supply current vs Input Frequency

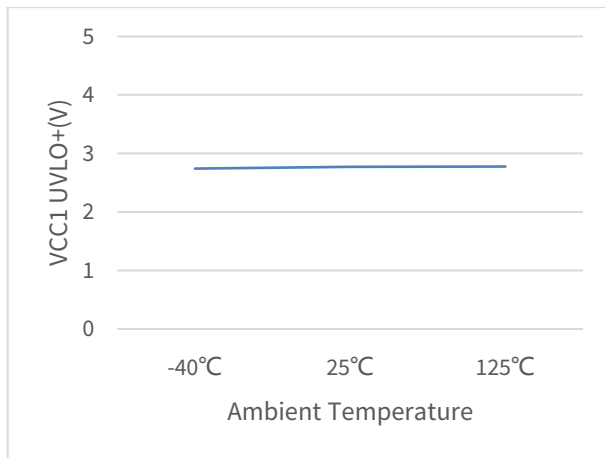


Figure 6.9 V<sub>CC1</sub> UVLO+ vs Temperature

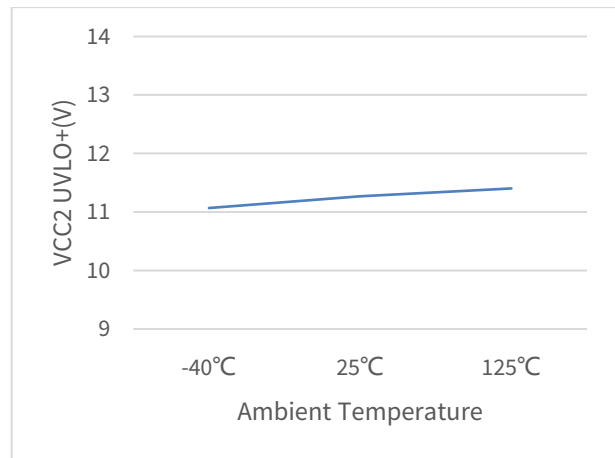


Figure 6.10 V<sub>CC2</sub> UVLO+ vs Temperature

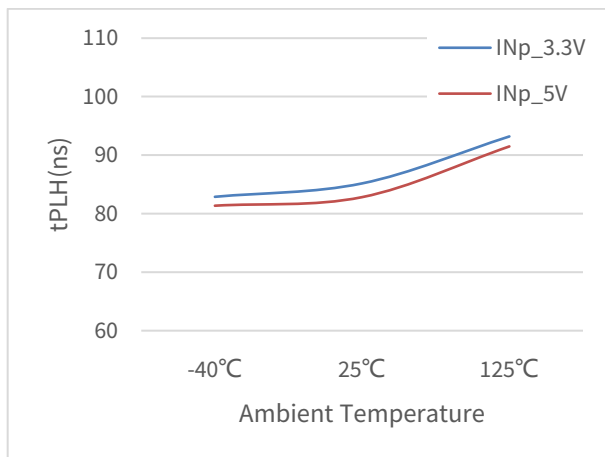


Figure 6.11 t<sub>PLH</sub> vs Temperature

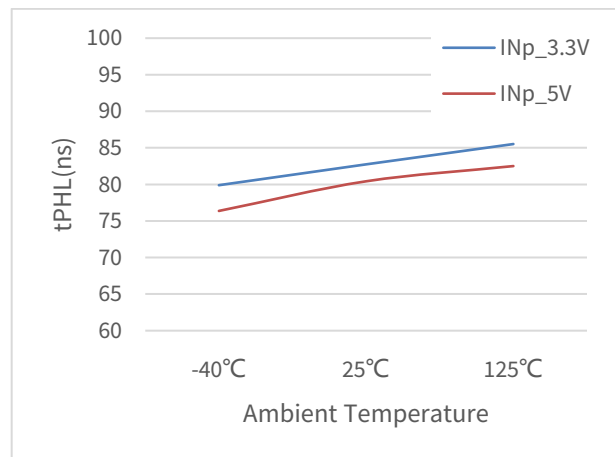


Figure 6.12 t<sub>PHL</sub> vs Temperature

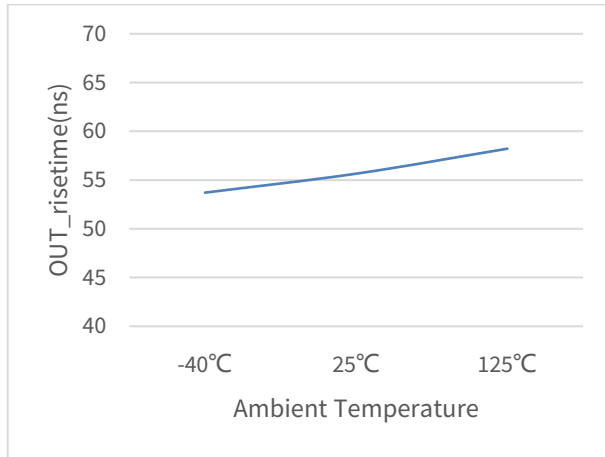


Figure 6.13 OUT\_risetime vs Temperature

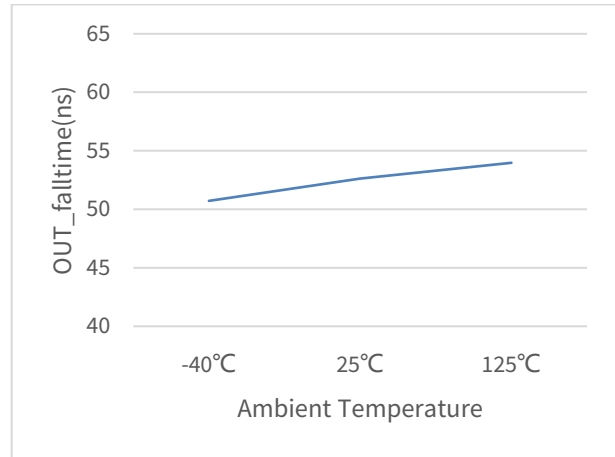


Figure 6.14 OUT\_falltime vs Temperature

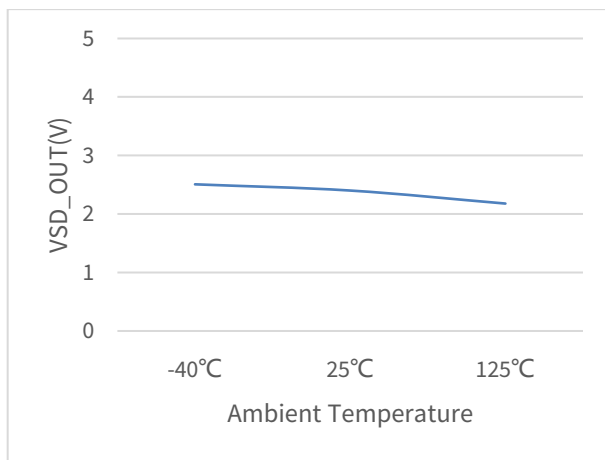


Figure 6.15 VSD\_OUT vs Temperature

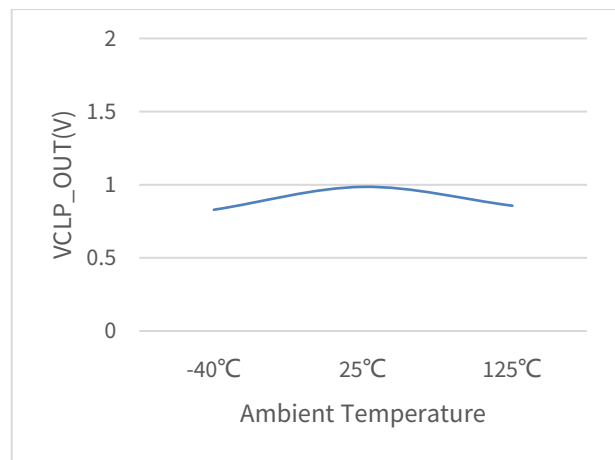


Figure 6.16 VCLP\_OUT vs Temperature

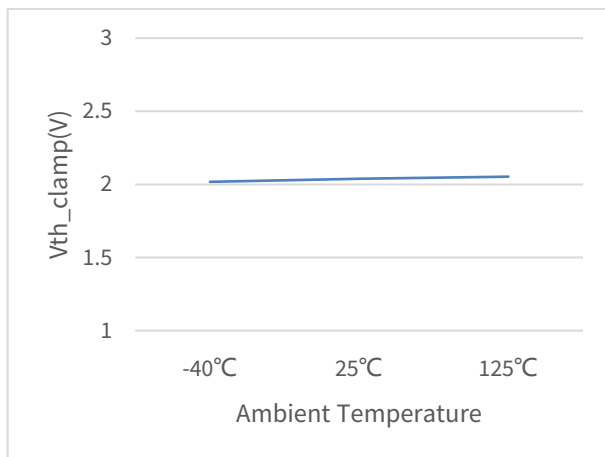


Figure 6.17 Vth\_clamp vs Temperature

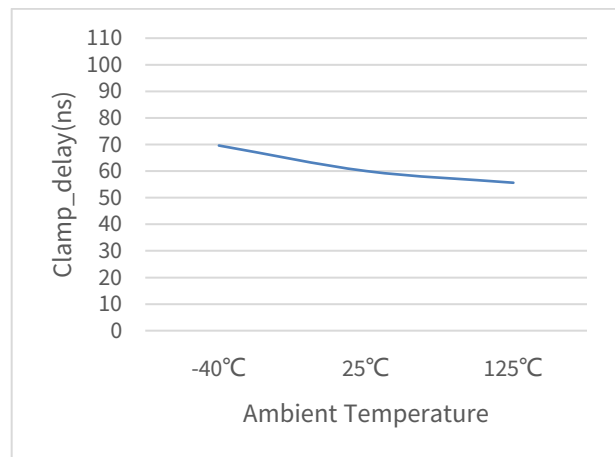


Figure 6.18 Clamp\_delay vs Temperature

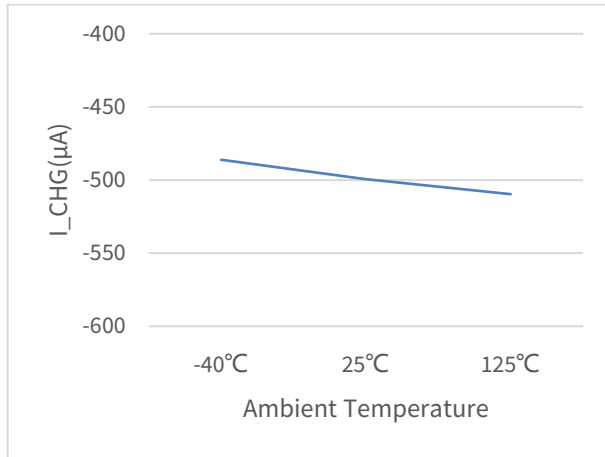


Figure 6.19 I\_CHG vs Temperature

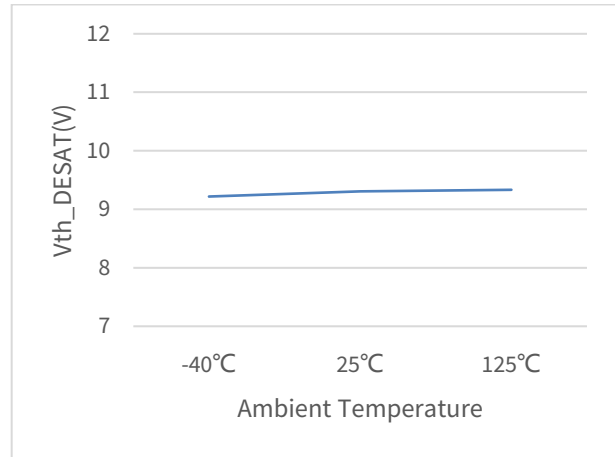


Figure 6.20 DESAT Threshold Voltage vs Temperature

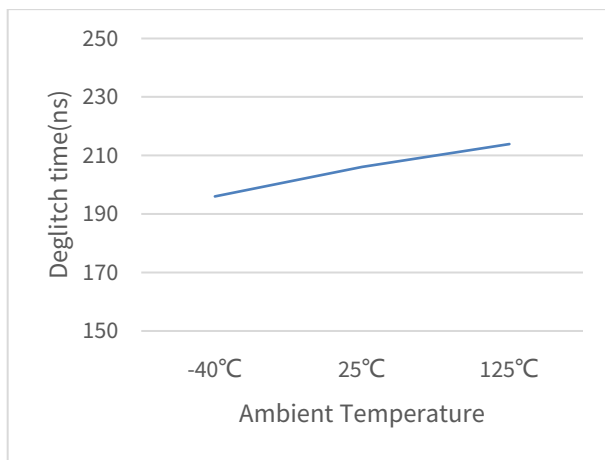


Figure 6.21 Deglitch time vs Temperature

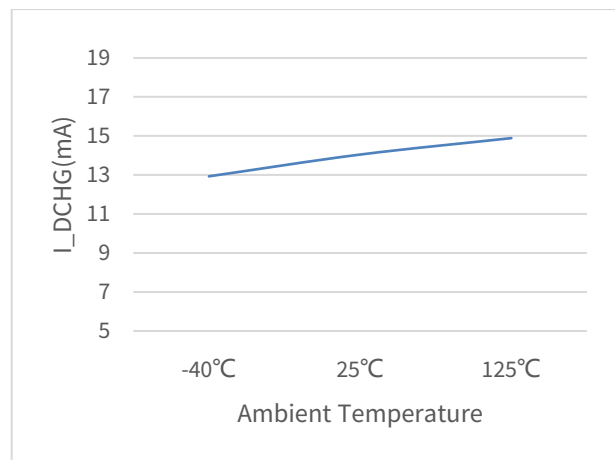


Figure 6.22 I\_DCHG vs Temperature

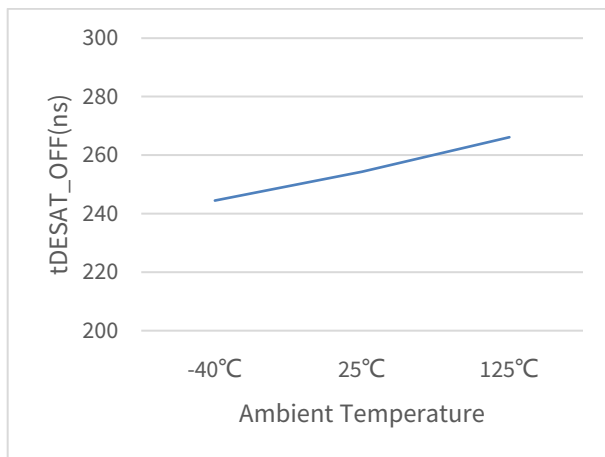


Figure 6.23 t<sub>DESAT\_OFF</sub> vs Temperature

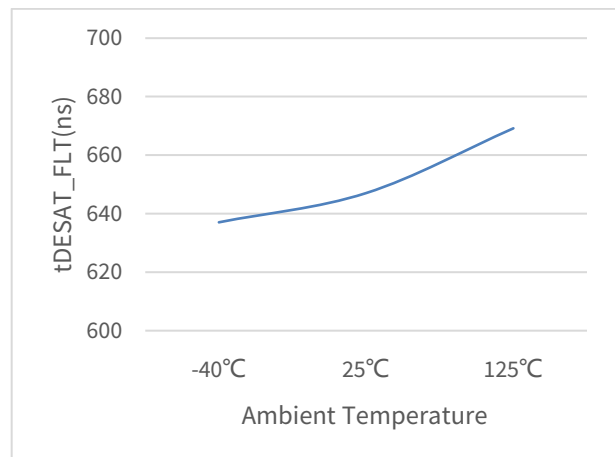


Figure 6.24 t<sub>DESAT\_FLT</sub> vs Temperature

## 7. High Voltage Feature Description

### 7.1. Insulation and Safety Related Specifications

| <i>Parameter</i>                                 | <i>Symbol</i> | <i>SOW16</i> | <i>Unit</i> | <i>Comments</i>                       |
|--|---------------|--------------|-------------|---------------------------------------|
| Minimum External Clearance                       | CLR           | 8.0          | mm          | IEC 60664-1:2007                      |
| Minimum External Creepage                        | CPG           | 8.0          | mm          | IEC 60664-1:2007                      |
| Distance Through Insulation                      | DTI           | 20           | µm          | Minimum internal gap                  |
| Tracking Resistance (Comparative Tracking Index) | CTI           | >600         | V           | DIN EN 60112 (VDE 0303-11); IEC 60112 |
| Material Group                                   |               | I            |             |                                       |

| <i>Description</i>                  | <i>Test Condition</i>                   | <i>Value</i> |
|-------------------------------------|---|--------------|
| Overvoltage Category per IEC60664-1 | For Rated Mains Voltage $\leq$ 150Vrms  | I to IV      |
|                                     | For Rated Mains Voltage $\leq$ 300Vrms  | I to IV      |
|                                     | For Rated Mains Voltage $\leq$ 600Vrms  | I to IV      |
|                                     | For Rated Mains Voltage $\leq$ 1000Vrms | I to III     |
| Climatic Classification             |   | 40/125/21    |
| Pollution Degree per DIN VDE 0110   |   | 2            |

7.2. Insulation Characteristics

| Description                               | Test Condition  | Symbol     | Value      | Unit       |
|---|---|------------|------------|------------|
| Maximum Working Isolation Voltage         | AC voltage (sine wave) Time dependent dielectric breakdown (TDDB)test   | $V_{IOWM}$ | 1500       | $V_{RMS}$  |
|   | DC voltage  |            | 2121       | $V_{DC}$   |
| Maximum Repetitive Peak Isolation Voltage | AC voltage(bipolar)   | $V_{IORM}$ | 2121       | $V_{PEAK}$ |
| Apparent Charge                           | Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}$ , $t_{ini} = 60s$ , $V_{pd}(m)=1.2*V_{IORM}$ , $t_m=10s$ .  | $q_{pd}$   | <5         | pC         |
|   | Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$ , $t_{ini}=60s$ , $V_{pd}(m)=1.6*V_{IORM}$ , $t_m=10s$   |            |            |            |
|   | Method b, routine test (100% production) and preconditioning (type test); $V_{ini}=1.2*V_{IOTM}$ , $t_{ini}=1s$<br>$V_{pd}(m)=1.875*V_{IORM}$ , $t_m=1s$ (method b1) or $V_{pd}(m)=V_{ini}$ , $t_m=t_{ini}$ (method b2) |            |            |            |
| Maximum Transient Isolation Voltage       | $t = 60s$   | $V_{IOTM}$ | 8000       | $V_{PEAK}$ |
| Maximum impulse voltage                   | Tested in air, 1.2/50-us waveform per IEC62368-1  | $V_{IMP}$  | 6250       | $V_{PEAK}$ |
| Maximum Surge Isolation Voltage           | Test method per IEC60065, 1.2/50us waveform, $V_{TEST}=V_{IOSM} \times 1.6$   | $V_{IOSM}$ | 10000      | $V_{PEAK}$ |
| Isolation Resistance                      | $V_{IO} = 500V$ at $T_A = T_S$  | $R_{IO}$   | $>10^9$    | $\Omega$   |
|   | $V_{IO} = 500V$ at $100^\circ C \leq T_A \leq 125^\circ C$  |            | $>10^{11}$ | $\Omega$   |
|   | $V_{IO} = 500V$ , $T_A = 25^\circ C$  |            | $>10^{12}$ | $\Omega$   |
| Isolation Capacitance                     | $f = 1MHz$  | $C_{IO}$   | 0.8        | pF         |
| <b>UL1577</b>                             |   |            |            |            |
| Maximum Withstanding Isolation Voltage    | $V_{TEST} = V_{ISO}$ , $t = 60s$ (qualification);<br>$V_{TEST} = 1.2 \times V_{ISO}$ , $t = 1s$ (100%production)  | $V_{ISO}$  | 5700       | $V_{RMS}$  |

7.3. Safety Limiting Values for SOW16 Package

| Description                      | Test Condition   | Symbol | Value       |      | Unit |
|----------------------------------|--|--------|-------------|------|------|
| Maximum Safety Temperature       |  | $T_s$  | 150         |      | °C   |
| Maximum Safety Power Dissipation | $R_{\theta JA}=97^{\circ}\text{C}/\text{W}$ , $T_J=150^{\circ}\text{C}$ , $V_{CC2}=20\text{V}$ , $V_{EE2}=-5\text{V}$ , $T_A=25^{\circ}\text{C}$ | $P_s$  | Total       | 1288 | mW   |
| Maximum Safety Current           | $R_{\theta JA}=97^{\circ}\text{C}/\text{W}$ , $V_{CC2}=15\text{V}$ , $V_{EE2}=-5\text{V}$ , $T_J=150^{\circ}\text{C}$ , $T_A=25^{\circ}\text{C}$ | $I_s$  | Driver side | 64.4 | mA   |
|                                  | $R_{\theta JA}=97^{\circ}\text{C}/\text{W}$ , $V_{CC2}=20\text{V}$ , $V_{EE2}=-5\text{V}$ , $T_J=150^{\circ}\text{C}$ , $T_A=25^{\circ}\text{C}$ |        | Driver side | 51.5 |      |

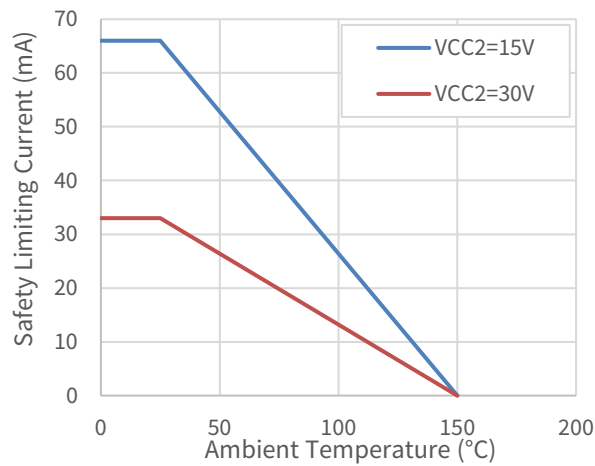


Figure 7.1 Thermal Derating Curve for Limiting Current per DIN VDE V 0884-11 for SOW16 Package

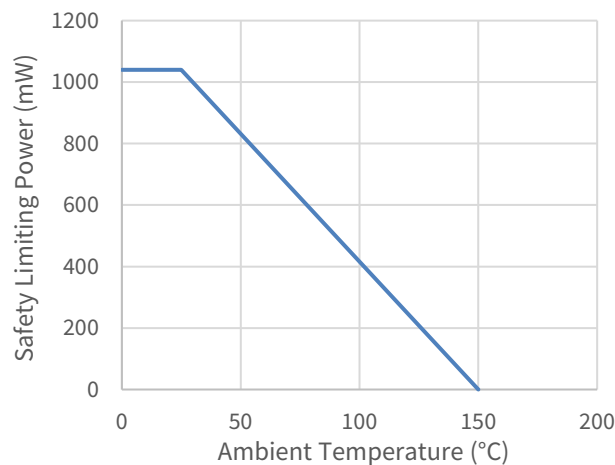


Figure 7.2 Thermal Derating Curve for Limiting Power per DIN VDE V 0884-11 for SOW16 Package



**7.4. Regulatory Information for SOW16 Package**

| <i>UL</i>   |   | <i>VDE</i>   | <i>CQC</i>                      |
|---|---|--|---------------------------------|
| UL 1577 Component Recognition Program                     | Approved under CSA Component Acceptance Notice 5A         | DIN VDE V 0884-17  | Certified according to GB4943.1 |
| Single Protection, 5700V <sub>RMS</sub> Isolation Voltage | Single Protection, 5700V <sub>RMS</sub> Isolation voltage | Reinforced Insulation<br>V <sub>IORM</sub> =2121V <sub>PEAK</sub> ,<br>V <sub>IOTM</sub> =8000V <sub>PEAK</sub> ,<br>V <sub>IOSM</sub> =10000V <sub>PEAK</sub> | Reinforced Insulation           |
| E500602   |   | 40052820   | CQC20001264939                  |

## 8. Function Description

### 8.1. Overview

The NSI66x1A is a high reliable power transistor gate driver. It can source and sink 10A peak current, which is suitable to drive MOSFET, IGBT, or SiC MOSFET. The NSI66x1A is available in SOW16 package, which can support 5700V<sub>RMS</sub> isolation per UL1577. System robustness is supported by 150kV/us minimum common-mode transient immunity (CMTI).

Besides, the NSI66x1A includes crucial protection features such as miller clamp, DESAT short circuit detection and soft turn off. UVLO and short circuit fault are reported through separate pins. ASC feature is designed to force output ON in emergency situation, which supports system fault management.

The isolation barrier inside NSI66x1A is based on a capacitive isolation. The modulation uses OOK modulation technique with key benefits of high noise immunity and low radiation EMI. The digital signal is modulated with RF carrier generated by the internal oscillator at the transmitter side, then it is transferred through the capacitive isolation barrier and demodulated at the receiver side.

The functional block diagram of NSI66x1A is shown in Figure 7.1. Two Input pins with non-inverting and inverting logic support interlock and shoot through protection. Low resistance of high side and low side MOSFET in the output stage ensures high driving capability. Split outputs can control the rise and fall time individually. Active pull-down and short circuit clamping features are implemented to protect power transistor.

In summary, the NSI66x1A is suitable to replace source and sink reinforced gate driver in high reliability, power density and efficiency switching power system.

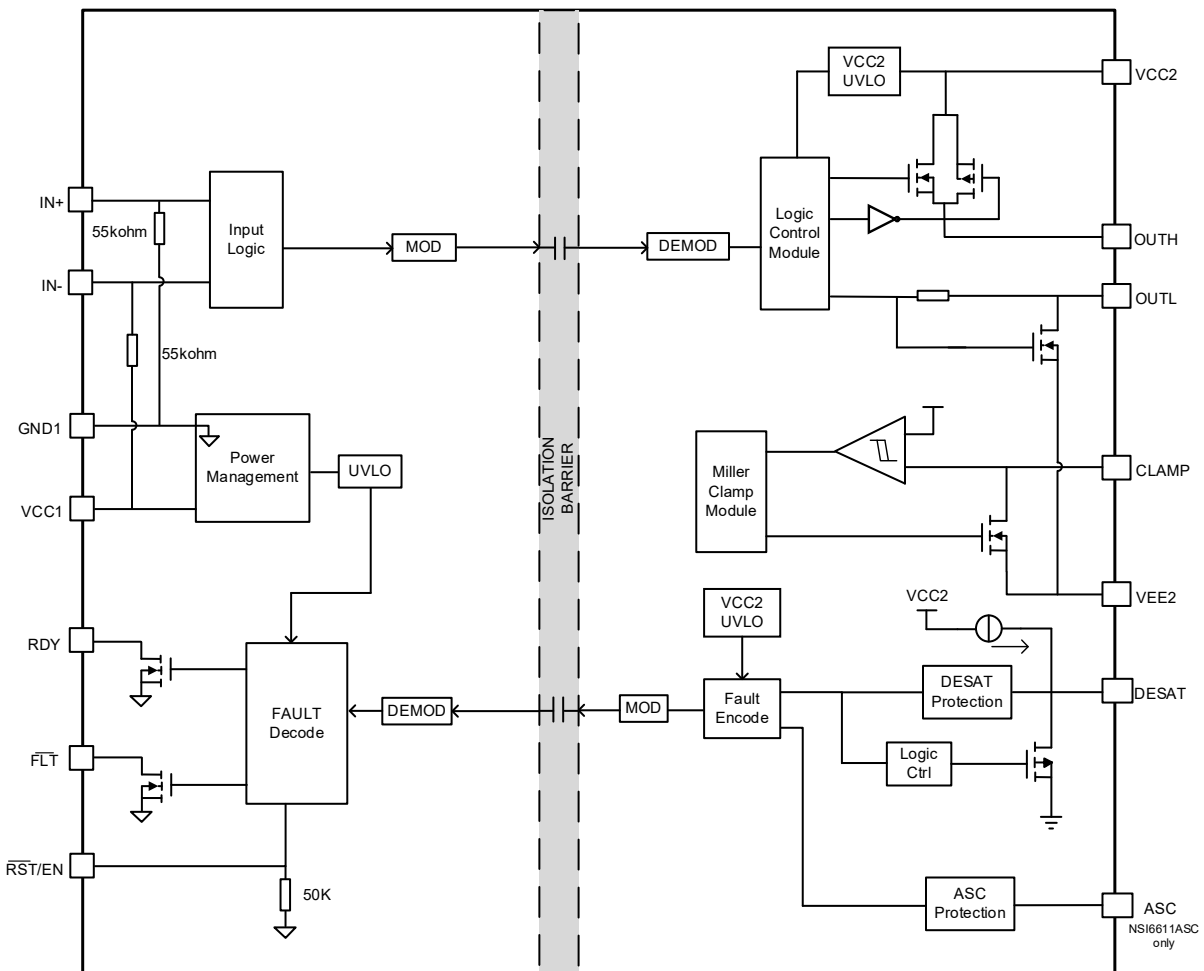


Figure 8.1 NSI66x1A Function Block Diagram

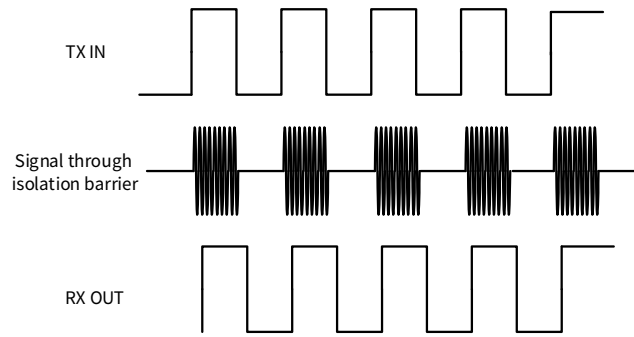


Figure 8.2 OOK Modulation

### 8.2. Power Supply

Power supply  $V_{CC1}$  is able to support from 3.3V to 5.5V. Power supply  $V_{CC2}$  is able to support from 13V to 32V. To be mentioned, NSI66x1A also supports bipolar power supply mode on the driver side. In the case of fast switching speed, the negative power supply is crucial to prevent false turn on from parasitic Miller capacitor.

### 8.3. Output Stage

The NSI66x1A has P-channel and N-channel MOSFET in parallel to pull up the OUTH pin when turning on external power transistor. During DC measurement, only the P-channel MOSFET is conducting. The measurement result  $R_{OH}$  represents the on-resistance of P-channel MOSFET. The voltage and current of external power transistor drain to source or collector to emitter change during turn on. At that time, the NSI66x1A N-channel MOSFET turns on to pull up OUTH more quickly. It results external power transistor faster turn on time, lower turn on power loss, also leads to lower temperature increase of NSI66x1A. The equivalent pull-up resistance of NSI66x1A is the parallel combination  $R_{OH} \parallel R_{NMOS}$ . The result is quite small, indicating the strong driving capability of NSI66x1A. The pull-down structure of NSI66x1A is simply composed of an N-channel MOSFET with on-resistance of  $R_{OL}$ . The result is quite small, indicating the strong driving capability of NSI66x1A.

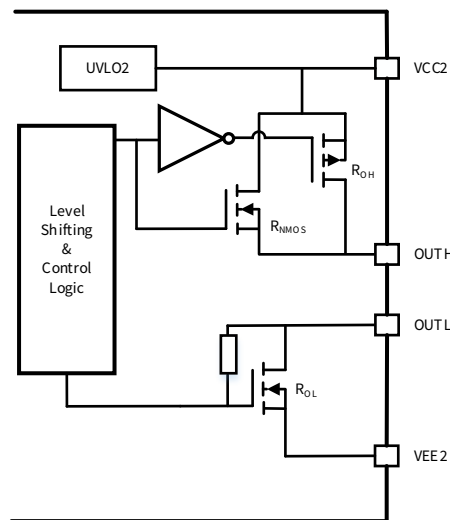


Figure 8.3 NSI66x1A output stage

### 8.4. $V_{CC2}$ and Under Voltage Lock Out(UVLO)

To ensure correct switching NSI66x1A is equipped with an under voltage lockout for input and output power supply independently.  $V_{CC1}$  voltage should not fall below the UVLO threshold for normal operation, or the gate-driver output can become clamped low. Output supply UVLO is referred to GND2 pin. If  $V_{CC2}$ -GND2 falls below the UVLO threshold, OUTL of the gate-driver will be clamped low.

Local bypass capacitors should be placed between the  $V_{CC2}$  and GND2 pins, as well as the  $V_{CC1}$  and GND1 pins. 220nF to 10 $\mu$ F is recommended for device biasing. Additional 100nF capacitor in parallel with the device biasing capacitor is recommended for high

frequency filtering. The capacitors should be positioned as close to the device as possible for better noise filtering. Low-ESR, ceramic surface-mount capacitors are recommended. The RDY pin will report a power good signal if the device is out of UVLO condition.

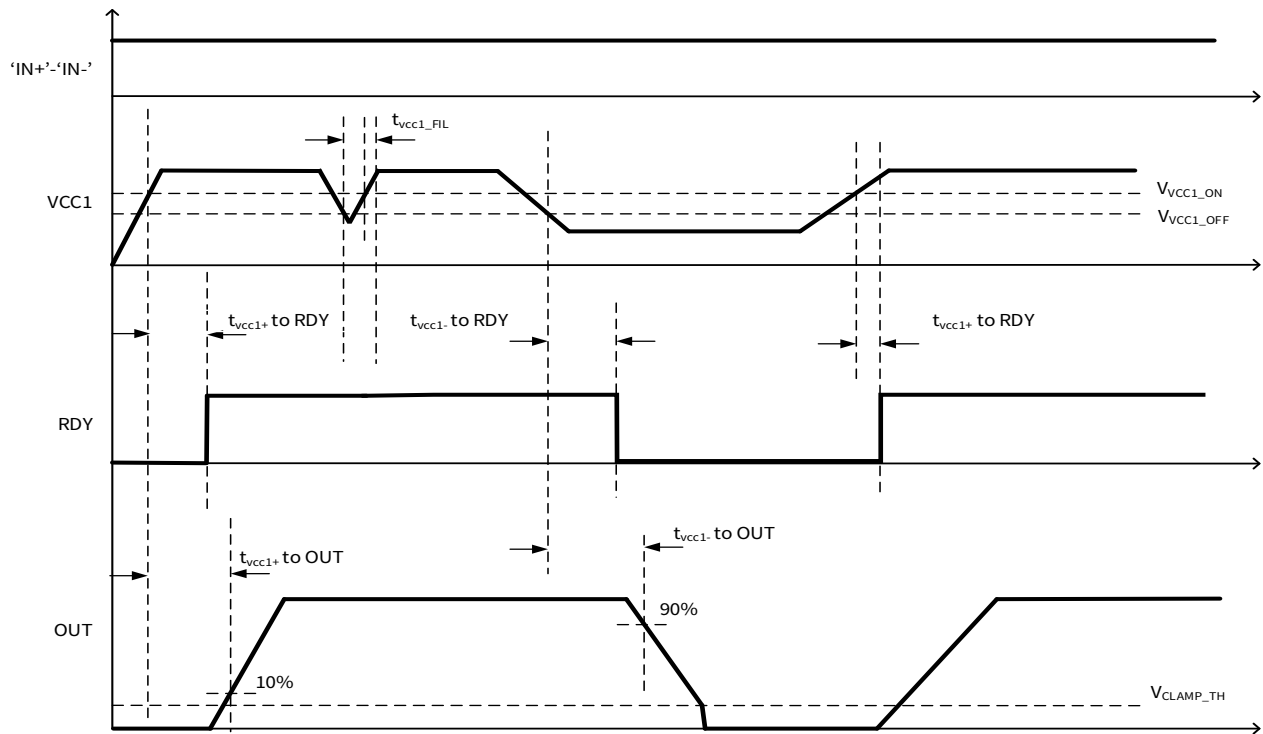


Figure 8.4 RDY vs V<sub>CC1</sub> timing Diagram

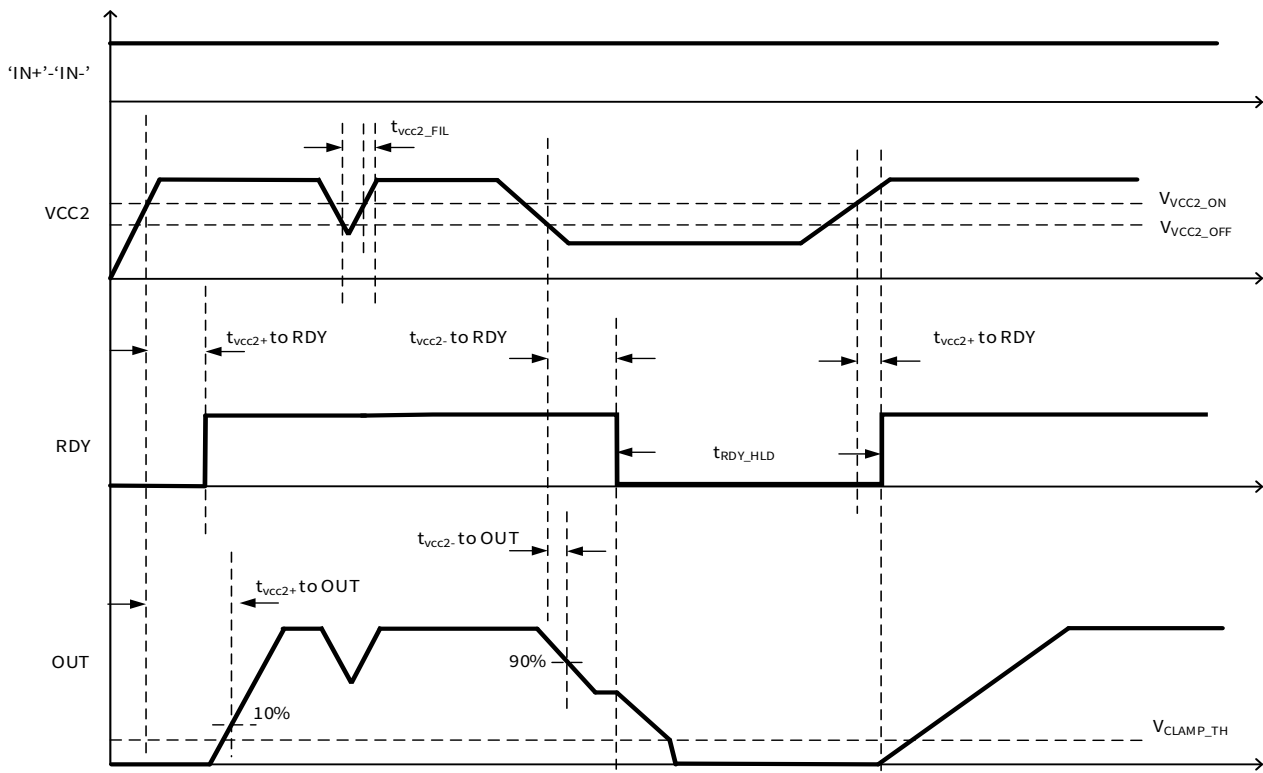


Figure 8.5 RDY vs V<sub>CC2</sub> timing Diagram

### 8.5. Active Pull-Down

The Active Pull-Down feature ensures a safe IGBT or MOSFET off-state if  $V_{CC2}$  is not connected to the power supply. When  $V_{CC2}$  is floating, the driver output is held low and clamping OUT to approximately 1.8V higher than  $V_{EE2}$ .

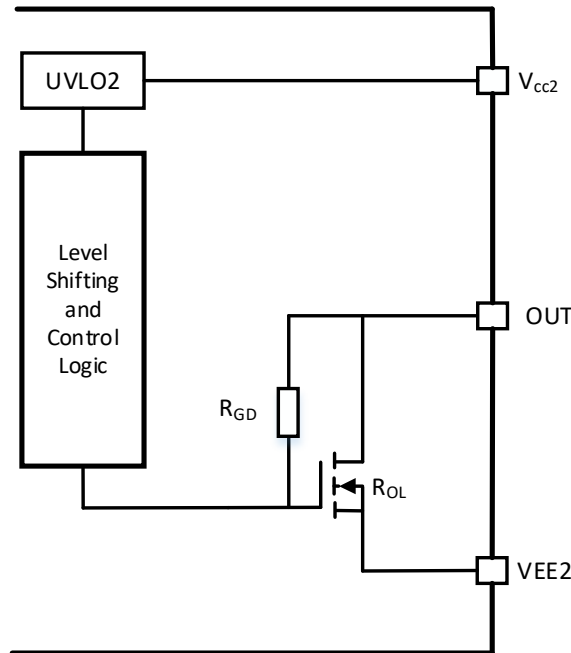


Figure 8.6 Active pulldown

### 8.6. Short circuit Clamping

During short circuit the gate voltage of IGBT or MOSFET tends to rise because of the feedback via the miller capacitance. The diode between OUTH/CLAMP and  $V_{CC2}$  pins inside the driver limits this voltage to approximately 0.7V higher than the supply voltage. A maximum current of 500mA may be fed back to the supply through this path for 10 $\mu$ s. If higher currents are expected or tighter clamping is desired external Schottky diodes may be added.

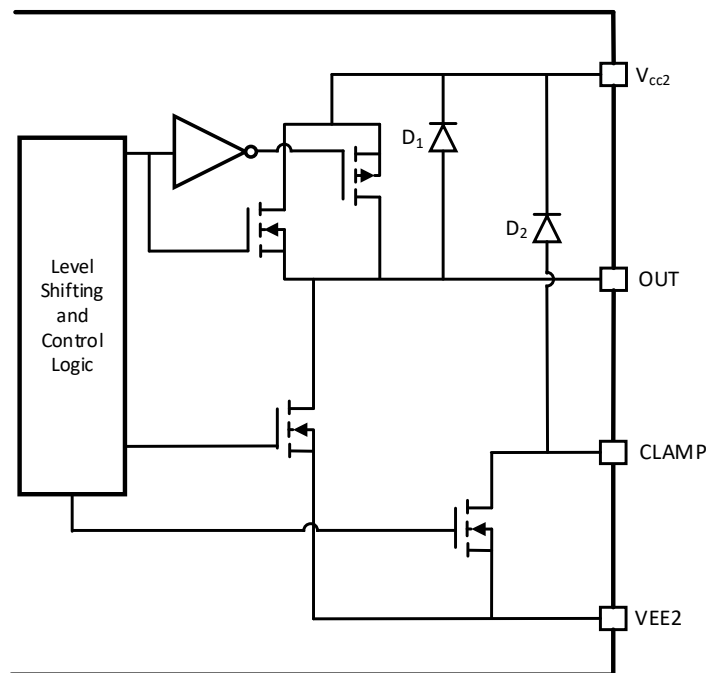


Figure 8.7 Short circuit clamping

### 8.7. Internal Active Miller Clamp

Active miller clamp is used to prevent false turn on. After the external power transistor is turned off, the other one of the phase leg is turned on. The voltage of the drain-source or collector-emitter rises instantly. The  $dv/dt$  will cause a high current on miller parasitic capacitor. The voltage-drop on the gate resistor possibly turn on the external power transistor unintentionally, which will cause a catastrophic damage. To deal with that, NSI66x1A is equipped with a miller clamp pin. The clamp pin detects the gate voltage of IGBT or MOSFET. When the gate voltage is decreasing and reaches the  $V_{CLAMP\_TH}$ , the clamp pin will be pulled down by the internal MOSFET, providing a low impedance path to avoid the false turn on. To be mentioned, the  $V_{CLAMP\_TH}$  is 2V higher than  $V_{EE2}$ . In the situation of fast switching speed, the negative power supply is necessary to avoid false turn on.

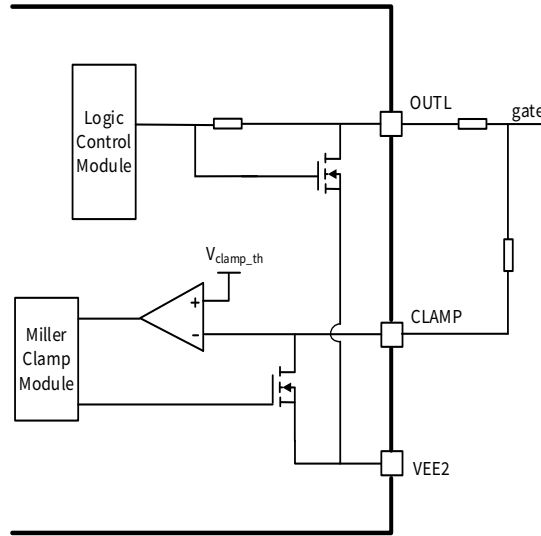


Figure 8.8 Active Miller Clamp

### 8.8. Desaturation (DESAT) Protection

Desaturation protection is used to prevent the power transistor from short circuit. The DESAT pin has a typical 9V threshold, which means the output will be driven low if DESAT pin reaches 9V. By default, the DESAT pin is pulled down by internal MOSFET. The internal 500 $\mu$ A current source is designed to work only when the output is high level. There is a 200ns leading edge blanking time to filter the overshoot when the external power transistor is turned on. The current source begin to charge after the internal leading edge blanking time.

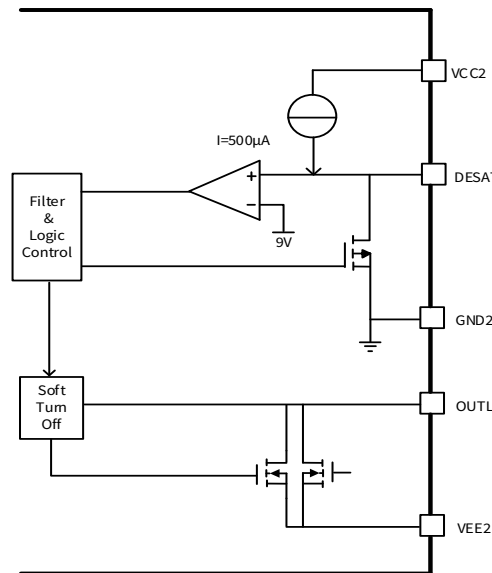


Figure 8.9 DESAT Protection

### 8.9. Soft Turn-off

The soft turn-off is designed to prevent the overshoot breakdown when DESAT protection is triggered. When the short circuit fault occurs, the external power transistor transits from the active zone to ohmic zone very quickly. The high di/dt may result in the overshoot voltage on the parasitic inductance of the emitter. Therefore, the device should be turned off in a soft manner. But the turn off speed should not be too slow. There is a balance between the overshoot and large energy dissipation. 400mA soft turn off current is a compromising choice.

### 8.10. Fault( $\overline{\text{FLT}}$ and $\overline{\text{RST/EN}}$ )

The  $\overline{\text{FLT}}$  pin of NSI66x1A is used to report a warning signal if the fault is detected on DESAT. If the fault occurs, the  $\overline{\text{FLT}}$  pin will be pulled down and held in low state for a mute time. During the mute time, NSI66x1A ignores any reset signal. After that, the  $\overline{\text{FLT}}$  pin will be reset to high impedance status if the reset signal is checked. The  $\overline{\text{RST/EN}}$  pin is pulled down to GND1 by an internal resistor, which means the device is disabled by default. Therefore, the  $\overline{\text{RST/EN}}$  pin must be pulled up externally to enable the device. Timing diagram of fault report is shown below.

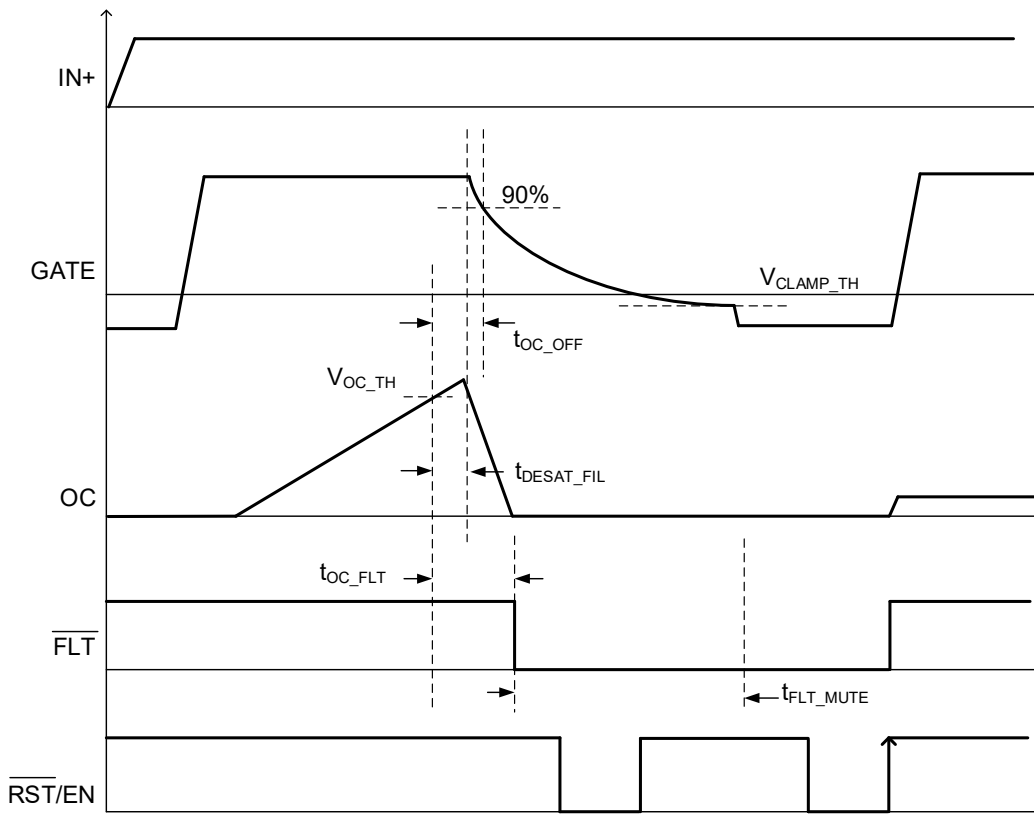


Figure 8.10 DESAT protection Timing Diagram

**8.11. Device Functional Modes**

Table lists the common functional modes of the device.

| Input            |                  |                  |      |      |        |          |      | Output |     |           |       |
|------------------|------------------|------------------|------|------|--------|----------|------|--------|-----|-----------|-------|
| V <sub>CC1</sub> | V <sub>CC2</sub> | V <sub>EE2</sub> | IN+  | IN-  | EN/RST | DESAT    | ASC  | RDY    | FLT | OUTH/OUTL | CLAMP |
| PU               | PD/OPEN          | X                | X    | X    | X      | X        | X    | LOW    | HIZ | LOW       | LOW   |
| PD               | PU               | X                | X    | X    | X      | X        | LOW  | LOW    | HIZ | LOW       | LOW   |
| OPEN             | X                | X                | X    | X    | X      | X        | LOW  | HIZ    | HIZ | LOW       | LOW   |
| PU               | PU               | X                | X    | X    | HIGH   | LOW      | HIGH | HIZ    | HIZ | HIGH      | HIZ   |
| PU               | PU               | X                | X    | X    | LOW    | X        | HIGH | HIZ    | HIZ | HIGH      | HIZ   |
| PD/OPEN          | PU               | X                | X    | X    | X      | X        | HIGH | X      | HIZ | HIGH      | HIZ   |
| PU               | PU               | X                | X    | X    | LOW    | X        | LOW  | HIZ    | HIZ | LOW       | LOW   |
| PU               | PU               | X                | LOW  | X    | HIGH   | X        | LOW  | HIZ    | HIZ | LOW       | LOW   |
| PU               | PU               | X                | HIGH | LOW  | HIGH   | FLOATING | X    | HIZ    | LOW | LOW       | LOW   |
| PU               | PU               | X                | HIGH | LOW  | HIGH   | LOW      | LOW  | HIZ    | HIZ | HIGH      | HIZ   |
| PU               | PU               | X                | HIGH | HIGH | HIGH   | X        | LOW  | HIZ    | HIZ | LOW       | LOW   |

Open: VCC <POR; PU: VCC>VCC UVLO; PD: POR < VCC <VCC UVLO; X: Irrelevant; HIZ: High impedance  
 POR is around 1.8V.



## 9. Application Note

### 9.1. Typical Application Circuit

Bypassing capacitors for  $V_{CC1}$  and  $V_{CC2}$  supplies are needed to achieve reliable performance. To filter noise, 0.1 $\mu$ F/50V ceramic capacitor is recommended to place as close as possible to NSI66x1A, both at  $V_{CC1}$  and  $V_{CC2}$  side. For  $V_{CC2}$  supply, additional 10 $\mu$ F/50V ceramic capacitor is recommended, to support high peak currents when turning on external power transistor. If the  $V_{CC1}$  or  $V_{CC2}$  power supply is located long distance from the IC, bigger capacitance is essential.

The input filter composed by  $R_{in}$  and  $C_{in}$  can be used if input PWM has ring due to long traces or bad PCB layout. However, it will introduce longer propagation delay.

A 5k $\Omega$  resistor can be used as pull-up resistor for  $\overline{FLT}$ , RDY and  $\overline{RST/EN}$  pins.

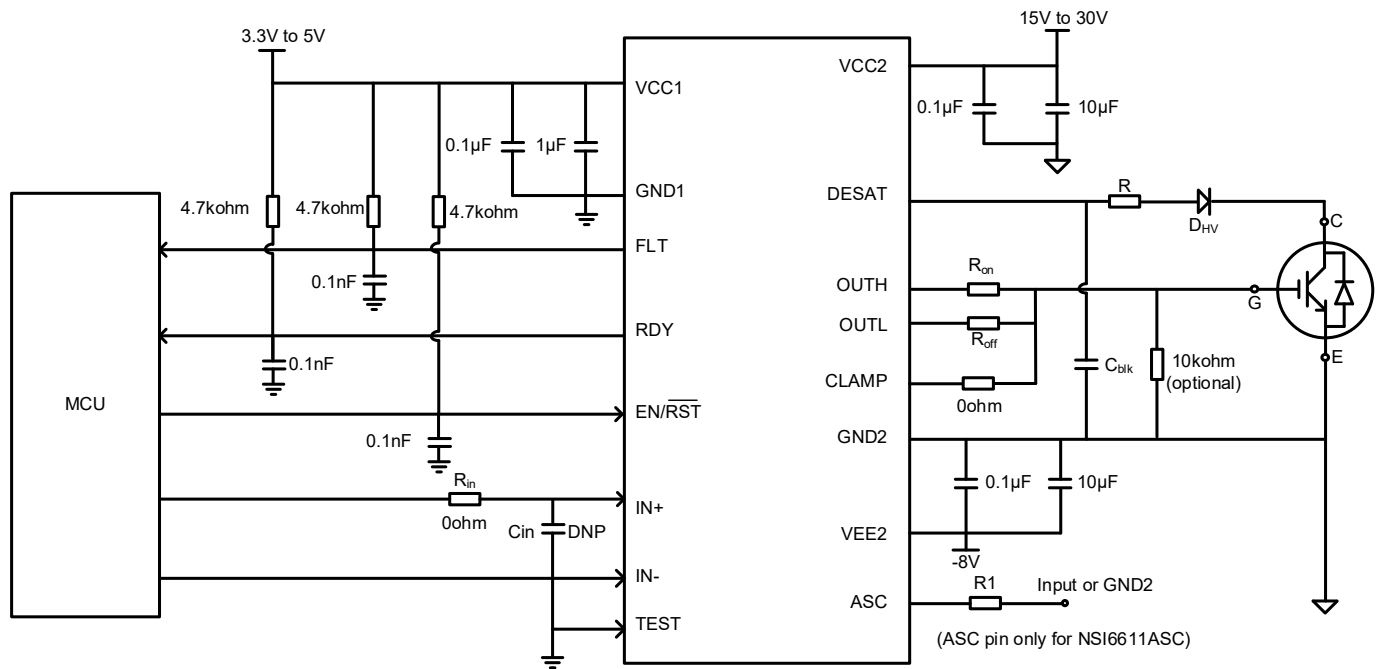


Figure 9.1 Typical Application Schematic

### 9.2. Design for IN+, IN- and $\overline{RST/EN}$

In the application with NSI66x1A, the noise from parasitic inductance and coupled capacitance can not be ignored any more. To filter the noise, NSI66x1A is designed with a 40ns deglitch filter. Besides, the external low pass filter can also be placed near the input pins. Low pass filter will increase the noise immunity and delay time, so it should be based on the requirements.

### 9.3. Design for $\overline{EN/RST}$ , RDY and $\overline{FLT}$

$\overline{EN/RST}$  pin is used to enable the device and reset the fault signal. It is pulled down by default.  $\overline{FLT}$  and RDY pin are open-drain output, which means they can not work without externally pull-up resistor. In this application, a 5k $\Omega$  pull-up resistor is recommended for RDY,  $\overline{FLT}$  and  $\overline{EN/RST}$  pin. A 0.1nF can be placed near the device if it is necessary.

### 9.4. Design for Automatic Reset Control

$\overline{RST/EN}$  pin has two functions. It is used to enable the device and reset the fault signal after DESAT is detected. The  $\overline{RST/EN}$  pin is pulled down to GND by an internal resistor, so the  $\overline{RST/EN}$  pin must be pulled up externally to enable the device.

After DESAT is detected, the FLT pin will be pulled down until the rising edge of the  $\overline{RST/EN}$  pin is coming. To be mentioned, there is a FLT mute time, which means the reset signal must be held for at least  $t_{FLT\_MUTE}$ .

NSI66x1A can be designed for automatic reset mode.  $\overline{RST/EN}$  pin can be connected with IN+ directly when the PWM is applied to

the IN+. Besides,  $\overline{RST}/\overline{EN}$  pin can be connected with IN- through a NOT logic if the PWM is applied to the IN-. Whichever mode is used, the PWM off time should be longer than the  $t_{FLT\_MUTE}$ .

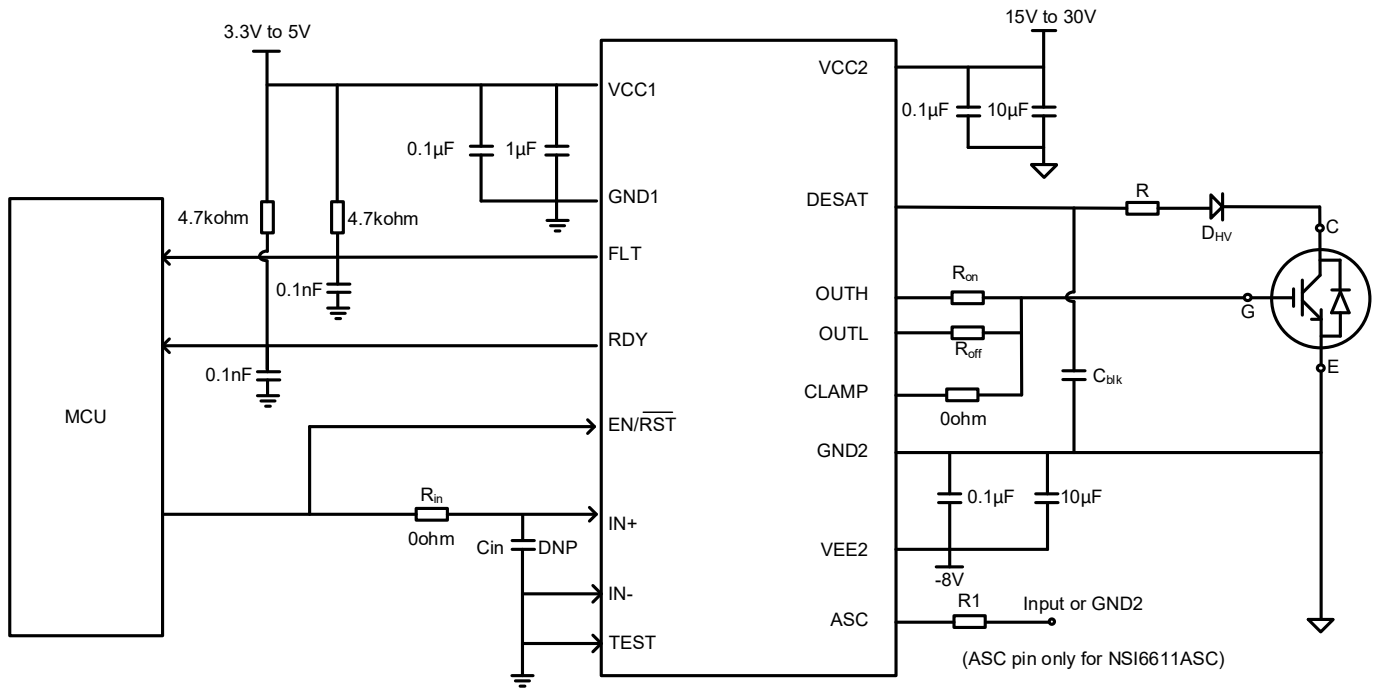


Figure 9.2 Automatic Reset Control (IN+)

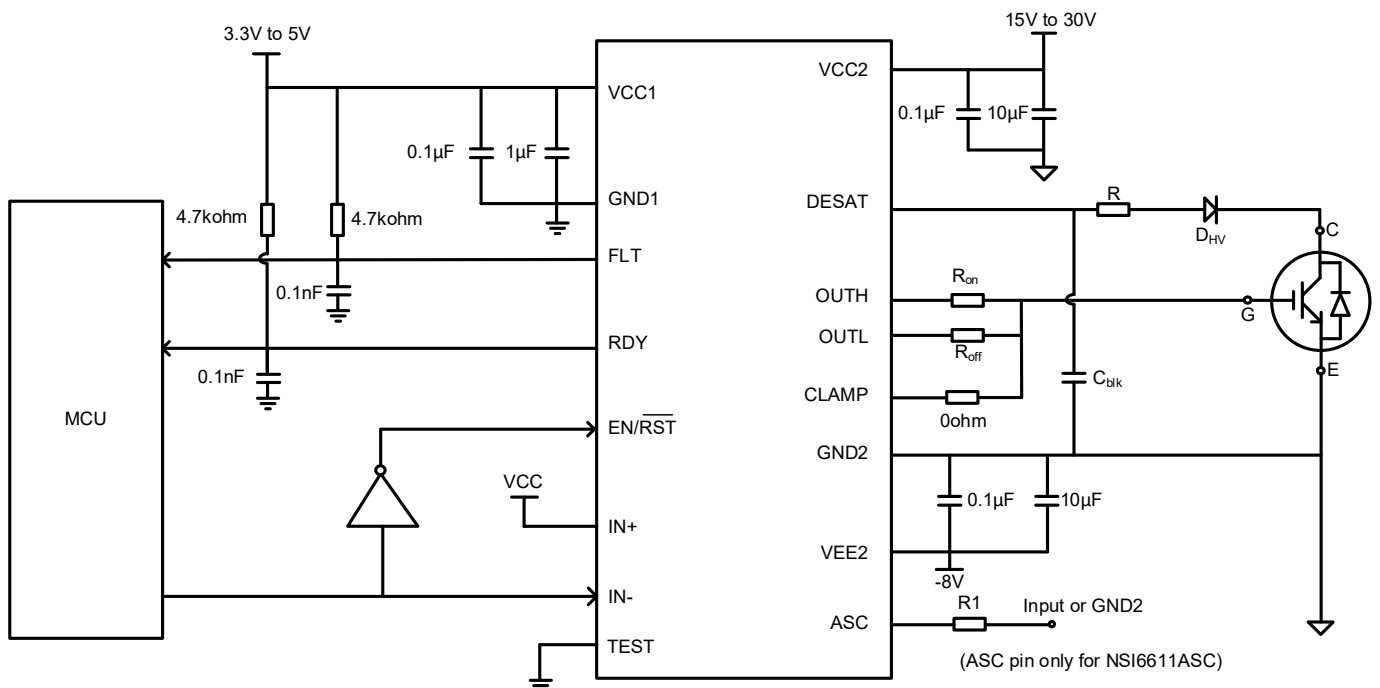


Figure 9.3 Automatic Reset Control (IN-)

### 9.5. PWM Interlock Protection

For applications to drive power transistors in half bridge configuration, two NSI66x1A can be used. NSI66x1A support Interlock protection. If the controller has some mistakes, leading to negative dead time, the output PWM of NSI66x1A is adjusted to avoid power transistor shoot through.

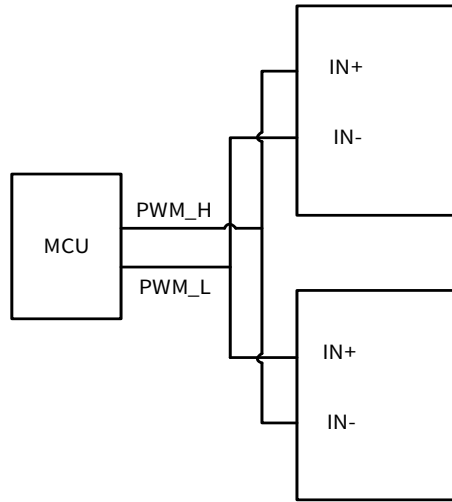


Figure 9.4 Interlock Protection

### 9.6. Design for R<sub>on</sub> and R<sub>off</sub>

NSI66x1A is featured with split output, so the turn on and turn off switching speed can be independently controlled. The turn on and turn off resistance determine the peak source and sink current, which can be estimated by the formula:

$$I_{source} = \min\left(\frac{VCC2 - VEE}{R_{ON} + R_{OH} + R_{Gint}}, 10A\right)$$

$$I_{sink} = \min\left(\frac{VCC2 - VEE}{R_{OFF} + R_{OL} + R_{Gint}}, 10A\right)$$

Where

R<sub>Gint</sub> is the internal resistance of the SiC or IGBT .

### 9.7. Design for DESAT Protection

DESAT is used to protect the power semiconductor from overcurrent. When the voltage of DESAT is over the V<sub>DESAT\_TH</sub>, the block of soft turn off will be activated and the fault pin will be pulled down. For typical application, the crucial components required to build the DESAT circuit are the DESAT diode, DESAT resistor and the blank capacitor.

The DESAT diode function is to conduct forward current. In order to avoid the false detection caused by the reverse recovery spikes, a very fast reverse recovery time diode with small reverse parasitic capacitance is recommended. The DESAT detection threshold voltage of 9V can be reduced by the DESAT diode, which can be calculated as:

$$V_{DESAT}' = 9 - V_F$$

The anti-parallel diode of IGBT have a large transient forward voltage of the diode, which may result in a large negative voltage spike on the DESAT pin, then it may draw a large current from driver. DESAT resistor is used to limit the current. A 100Ω resistor is recommended to be added in series with the DESAT diode.

The DESAT fault detection should remain a short blanking time so that the collector voltage can fall below the V<sub>DESAT\_TH</sub>. This blanking time can make sure that there is no nuisance tripping during the IGBT turn-on. It is based on the blank capacitor, which can be estimated as:

$$t_{BLK} = \frac{C_{BLK} \times V_{DESAT\_TH}}{I_{CHG}}$$

### 9.8. Design for External Current Buffer

Totem structure can be used as an external current buffer to increase the IGBT gate drive current, such as the NPN/PNP buffer shown as below. When the external buffer is used, the external components for soft turn off should be designed in addition. The capacitor is used to adjust the timing and the resistor ensure the sink current lower than the  $I_{OUTL}$ . Both resistor and capacitor can be estimated by the Equation below.

$$C_{STO} = \frac{I_{STO} \times t_{STO}}{V_{CC2} - V_{EE2}}$$

$$R_{STO} = \frac{V_{CC2} - V_{EE2}}{I_{OUTL}}$$

$I_{STO}$  is the internal soft turn off current

$T_{sto}$  is the expected timing

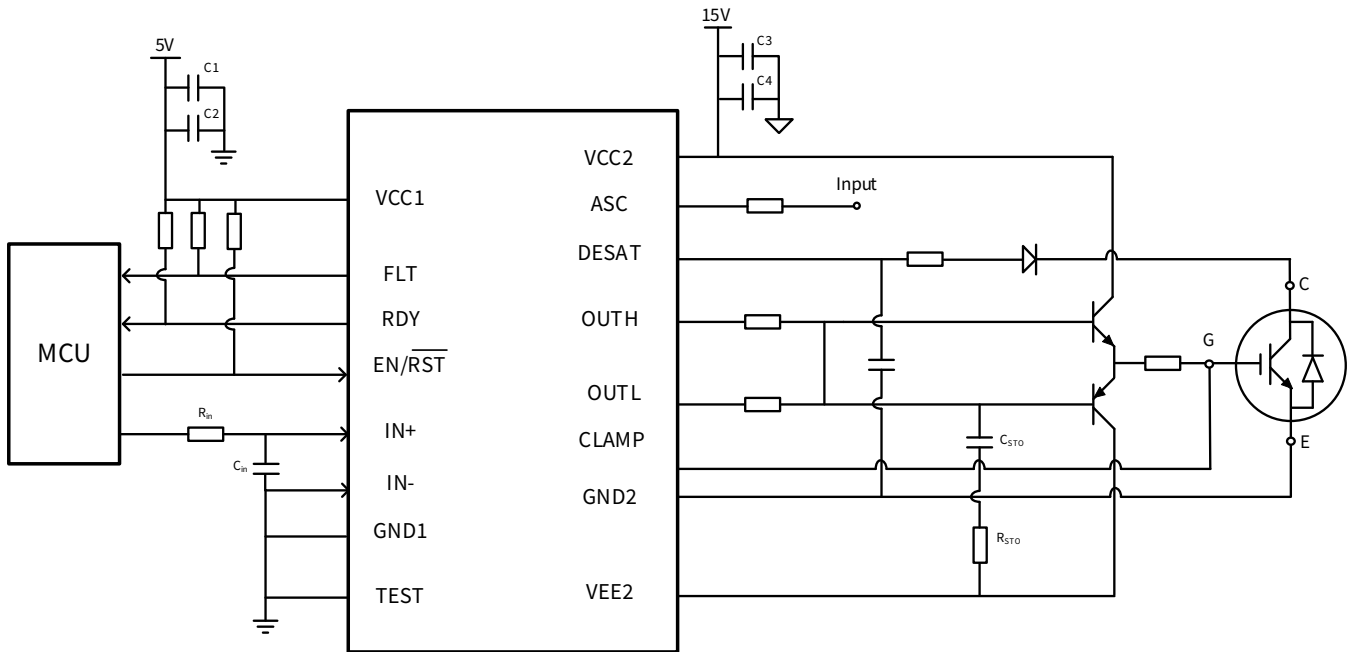


Figure 9.5 External current buffer circuit

## 9.9. PCB Layout

Careful PCB layout is essential for optimal performance. Some key guidelines are:

- The bypass capacitors should be placed close to NSI66x1A, between  $V_{CC1}$  to GND1,  $V_{CC2}$  to GND2 and  $V_{EE2}$  to GND2.
- There is high switching current that charges and discharges the gate of external power transistor, leading to EMI and ring issues. The parasitic inductance of this loop should be minimized, by decreasing loop area and place NSI66x1A close to power transistor.
- Place large amount of copper connecting to  $V_{EE2}$  pin and  $V_{CC2}$  pin for thermal dissipation, with priority on  $V_{EE2}$  pin. If the system has multi-layers of  $V_{EE2}$  or  $V_{CC2}$ , use multiple vias of adequate size for connection.
- To ensure isolation performance between primary and secondary side, the space under the chip should keep free from planes, traces, pads or via.

### 10. Package Information

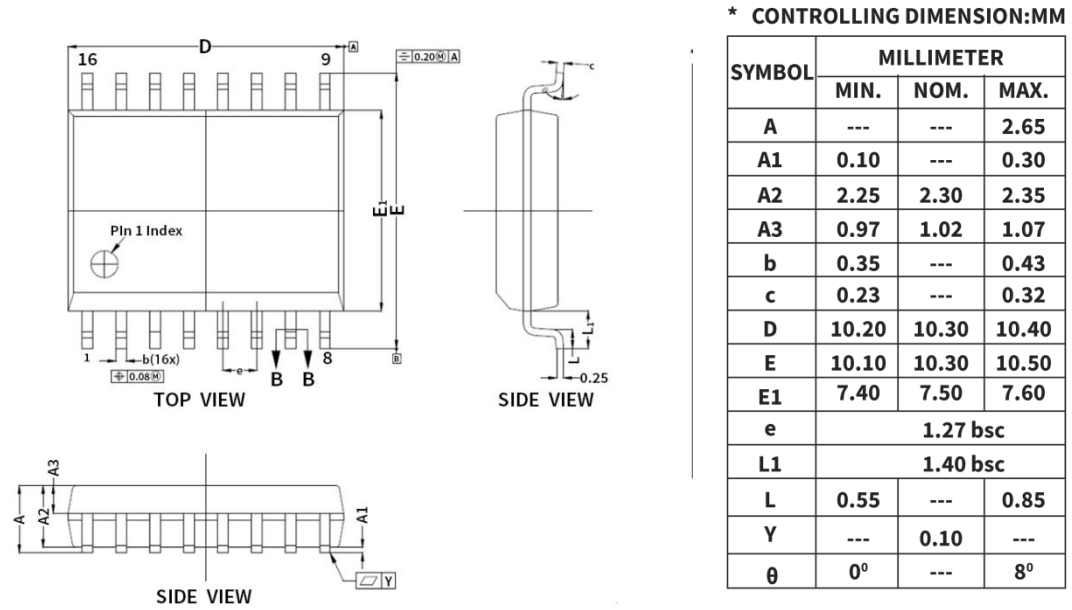


Figure 10.1 SOW16 Package Shape and Dimension  
 Dimensions shown in millimeters

### 11. Ordering Information

| Part Number     | ASC Feature | OUT Pin    | MSL | Category   | SPQ  | Package Type |
|-----------------|-------------|------------|-----|------------|------|--------------|
| NSI6651ASC-DSWR | No          | OUTH, OUTL | 2   | Industrial | 1000 | SOW16        |
| NSI6651ALC-DSWR | No          | OUT        | 2   | Industrial | 1000 | SOW16        |
| NSI6611ASC-DSWR | Yes         | OUTH, OUTL | 2   | Industrial | 1000 | SOW16        |

### 12. Documentation Support

| Part Number | Product Folder             | Datasheet                  | Technical Documents        | Isolated Driver Selection Guide |
|-------------|----------------------------|----------------------------|----------------------------|---------------------------------|
| NSI66x1A    | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a>      |

### 13. Tape and Reel Information

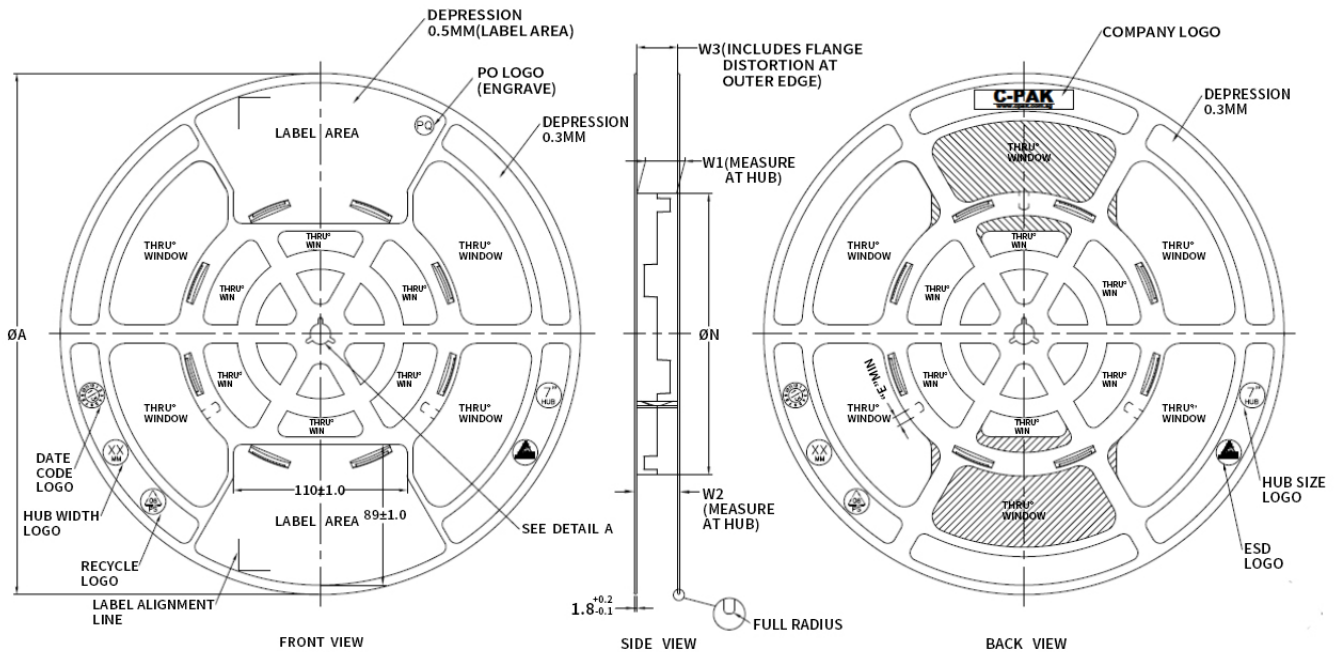
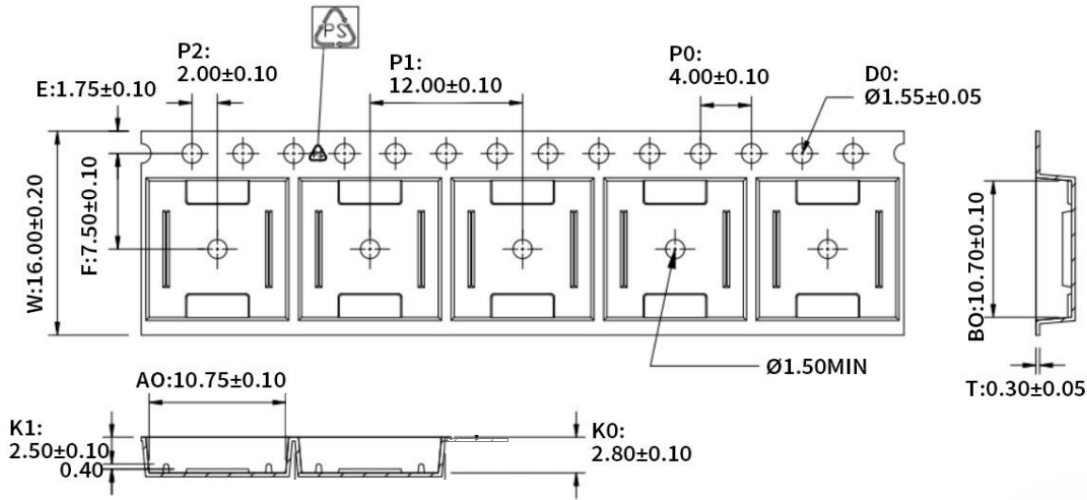


Figure 13.1 Reel Information



1. 10 sprocket hole pitch cumulative tolerance  $\pm 0.20$ .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481 requirements.
5. Thickness:  $0.30 \pm 0.05$ mm.
6. Packing length per 22" reel: 378 Meters.( N=122 )
7. Component load per 13" reel: 1000 pcs.

Figure 13.2 SOW16 Tape Information

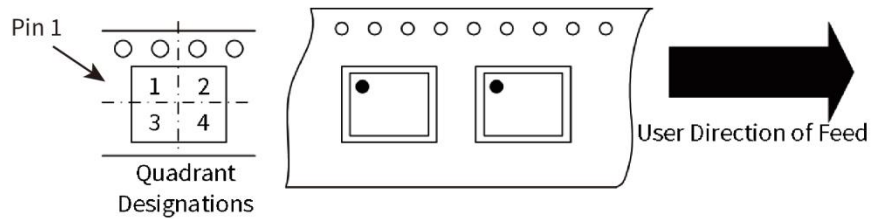


Figure 13.3 Quadrant Designation for Pin1 Orientation in Tape