

Product Overview

The NSI68515 is a single-channel reinforced isolated gate driver which is pin-compatible for popular opto-coupled gate driver. It can source and sink 5A peak current. System robustness is supported by 150kV/us minimum common-mode transient immunity (CMTI).

The NSI68515 includes crucial protection features such as miller clamp, DESAT, UVLO and soft turn off. RDY and short circuit fault are reported through separate pins. With high driving current, wide supply voltage range and excellent protection features, NSI68515 is suitable for high reliability, power density and efficiency switching power system.

Key Features

- 5A peak source and sink output current.
- Pin compatible for opto-coupled gate drivers.
- Driver side supply voltage: up to 32V with UVLO
- Internal active miller clamp
- DESAT protection with 140mA soft turn off
- RDY and FLT report under emergency circumstance
- High CMTI: $\pm 150\text{kV/us}$
- Automatically reset option.
- 100ns typical propagation delay
- 100ns maximum pulse width distortion
- Operation ambient temperature: $-40^{\circ}\text{C} \sim 125^{\circ}\text{C}$
- RoHS& REACH Compliant
- Lead-free component, suitable for lead-free soldering profile: 260°C , MSL2

Safety Regulatory Approvals

- UL recognition: 5700V_{RMS}
- DIN VDE V 0884-11:2017-01
- CSA component notice 5A
- CQC certification per GB4943.1-2011

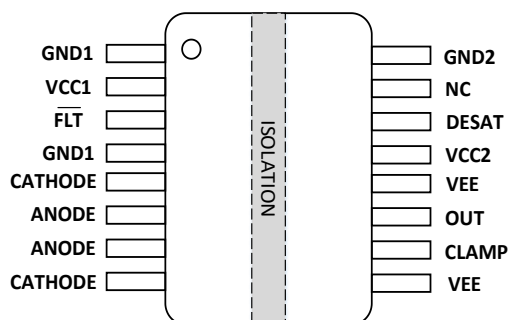
Applications

- Isolated IGBT gate drive
- Industrial Motor Drives and Solar Inverters
- UPS and Power Supplies

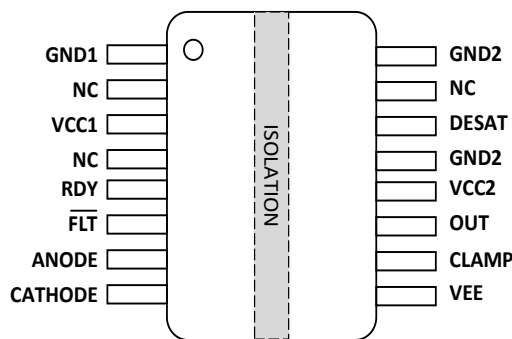
Device Information

Part Number	Auto-Reset	RDY Report	Output Rail to Rail
NSI68515LC	No	No	Yes
NSI68515AC	Yes	No	Yes
NSI68515RC	Yes	No	No
NSI68515UC	Yes	Yes	Yes

Functional Block Diagram



NSI68515LC, NSI68515AC, NSI68515RC



NSI68515UC

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1. Pin Configuration and Functions

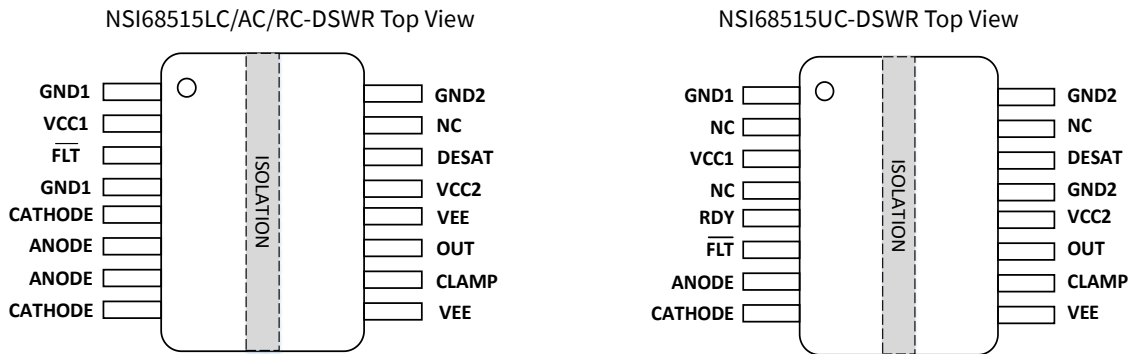


Table 1.1 NSI68515 Pin Configuration and Description

SYMBOL	PIN NUMBER		FUNCTION
	NSI68515xC (x=A,L,R)	NSI68515UC	
GND1	1,4	1	Input-side ground pin
VCC1	2	3	Input power supply
FLT	3	6	Fault output pin. Active low to report overcurrent or short circuit
CATHODE	5,8	8	Cathode of LED emulator
ANODE	6,7	7	Anode of LED emulator
VEE2	9,12	9,16	Driver side negative supply pin
CLAMP	10	10	Internal active miller clamp to prevent false turn-on
OUT	11	11	Driver output pin
VCC2	13	12	Driver side positive supply pin
DESAT	14	14	Desaturation voltage input. When the voltage on DESAT pin exceeds the threshold voltage. Device will response a Fast overcurrent and short circuit protection
NC	15	2,4,15	No Connection
GND2	16	13	Driver side ground pin
RDY	/	5	Power good signal. Active low to report under voltage lock

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Unit
Driver Side Supply Voltage	$V_{CC2}-V_{EE2}$	-0.3	35	V
Driver Side Supply Voltage	$V_{CC2}-GND2$	-0.3	35	V
Driver Side Supply Voltage	$V_{EE2}-GND2$	-17.5	0.3	V
Output Signal Voltage - DC	V_{OUT}, V_{CLAMP}	$V_{EE2}-0.3$	V_{CC2}	V
Average Input Current	I_{F_AVG}		25	mA
Peak Transient Input Current	I_{F_PEAK}		1	A
Reverse Input Voltage	V_{R_MAX}		6.5	V
Operating Junction Temperature	T_J	-40	150	°C
Storage Temperature	T_{stg}	-65	150	°C
Electrostatic Discharge	V_{ESD_HBM}		±2000	V
	V_{ESD_CDM}		±1000	V
Input Side Supply Voltage	V_{CC1}	GND1-0.3	GND1+6	V
Anode-GND1 voltage	V_{Anode}	GND1-0.3	GND1+6	V
Cathode-GND1 voltage	$V_{cathode}$	GND1-0.3	GND1+6	V
$\overline{FLT}/RDY$ Pin Voltage	V_{FLT}/V_{RDY}	GND1-0.3	V_{CC1}	V
$\overline{FLT}/RDY$ Input Current	I_{FLT}/I_{RDY}		20	mA
DESAT Voltage	V_{DESAT}	GND2-0.3	$V_{CC2}+0.3$	V

3. Recommended Operating Conditions

Parameters	Symbol	Min	Max	Unit
Ambient Temperature	T_A	-40	125	°C
Input Current (ON)	$I_{F(ON)}$	7	16	mA
Input Voltage (OFF)	$V_{F(off)}$	-5.5	0.9	V
Input Side Supply Voltage	$V_{CC1}-GND1$	3	5.5	V
Anode-GND1 voltage	V_{Anode}	-0.3	5.5	V
Cathode-GND1 voltage	$V_{cathode}$	-0.3	5.5	V
Driver Side Supply Voltage	$V_{CC2}-GND2$	15	32	V
Driver Side Supply Voltage	$GND2-V_{EE2}$	0	17.5	V
Driver Side Supply Voltage	$V_{CC2}-V_{EE2}$	0	32	V

4. Thermal Information

Parameters	Symbol	SOW16	Unit
Junction-to-ambient thermal resistance	$R_{\theta JA}$	97.0	°C/W
Junction-to-top characterization parameter	Ψ_{JT}	35.8	°C/W
Junction-to-board characterization parameter	Ψ_{JB}	39.0	°C/W
Junction-to-case(top) thermal resistance	$R_{JC(top)}$	23.3	°C/W

- 1) Standard JESD51-3 Low Effective Thermal Conductivity Test Board (1s) in an environment described in JESD51-2a.
- 2) Standard JESD51-3 Low Effective Thermal Conductivity Test Board (1s) by transient dual interface test method described in JESD51-14.
- 3) Obtained by Simulating in an environment described in JESD51-2a.

5. Specifications

5.1. Electrical Characteristics

All min and max specifications are at TA=-40°C to 125°C. Typical values are tested at VCC1=5V, VCC2=15V, VEE2=GND2.

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Input Side Supply						
Input Supply Quiescent Current	I _{CC1}		0.7	1.5	mA	VCC1=5V
VCC1 UVLO Rising Threshold	V _{CC1_ON}		2.7		V	
VCC1 UVLO Falling Threshold	V _{CC1_OFF}		2.5		V	
VCC1 UVLO Hysteresis	V _{CC1_HYS}		0.2		V	
Driver Side Supply						
Driver Supply Quiescent Current	I _{CC2}	2	3.2	5	mA	V _{CC2} =15V, V _{EE2} =GND2, I _F =10mA, OUT=High
VCC2 UVLO Rising Threshold	V _{CC2_ON}		11.5	13	V	
VCC2 UVLO Falling Threshold	V _{CC2_OFF}	9.9	10.7		V	
VCC2 UVLO Hysteresis	V _{CC2_HYS}		0.8		V	
Input Pin Characteristic						
Input Forward Threshold Current Low to High	I _{FLH}	1.5	2.6	4	mA	V _{OUT} >5V, C _g =1nF
Threshold Input Voltage High to Low	V _{FHL}	1	1.5	2	V	V _{OUT} <5V, C _g =1nF
Input Forward Voltage	V _F	1.9	2.17	2.5	V	I _F =10mA
Temp Coefficient of Input Forward Voltage	ΔV _F /ΔT		0.5	1.35	mV/°C	I _F =10mA
Input Reverse Breakdown Voltage	V _R			5	V	I _R =10uA
Input Capacitance	C _{IN}		15		pF	f=0.5MHz
Soft turn off						
Soft turn off current	I _{STO}	30	140	260	mA	
FLT Reporting						
Open drain low output voltage	V _{FLT_L}			0.3	V	I _{SINK_FLT} =5mA
Desaturation						
Blanking Capacitor Discharge Current	I _{DCHG}	10	15		mA	V _{DESAT} =6V
Blanking Capacitor Charge Current	I _{CHG}	200	240	280	uA	V _{DESAT} =2V
Detection Threshold	V _{DESAT_TH}	6	6.5	7	V	
DESAT deglitch filter time	t _{DESAT_FIL}	80	110	140	ns	
DESAT sense to OUT(L) 90% delay	t _{DESAT_OFF}	150	190	230	ns	C _{DESAT} =100pF, VCC2=30V
DESAT sense to FLT low delay	t _{DESAT_FLT}	500	570	650	ns	

Electrical Characteristics(continued)

All min and max specifications are at TA=-40°C to 125°C. Typical values are tested at VCC1=5V, VCC2=15V, VEE2=GND2.

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Output Pin Characteristic						
High Level Peak Output Current	I _{OUTH}		-5		A	V _{CC2} =15V, pulse Width<10us
Low Level Peak Output Current	I _{OUTL}		5		A	
Low Level Output Voltage	V _{OL}		0.04		V	I _{OUT} =200mA, V _F =0V
Low Level Clamp Voltage	V _{CLAMP}		0.4		V	I _{CLAMP} =1A, V _F =0V
Clamp Threshold Voltage	V _{CLAMP-TH}	1.8	2.1	2.3	V	V _{CLAMP} falling, V _F =0V
OUT Short Circuit Clamping Voltage	V _{CLP_OUT}		V _{CC2} +0.9	V _{CC2} +2	V	I _F =10mA, OUT=High, I _{OUTH} =0.5A, pulse width<10us
CLAMP Short Circuit Clamping Voltage	V _{CLP_CLAMP}		V _{CC2} +1.5	V _{CC2} +1.98	V	V _F =0V, I _{CLAMP} =0.5A, pulse width<10us
			V _{CC2} +1		V	V _F =0V, I _{CLAMP} =20mA
OUT Active Pull-Down Voltage	V _{SD_OUT}	2.4	2.7	3	V	V _{CC2} =OPEN, I _{OUTL} =0.1×I _{OUTL} (typ)

Electrical Characteristics(continued)

All min and max specifications are at TA=-40°C to 125°C. Typical values are tested at VCC1=5V, VCC2 =15V, VEE2=GND2.

Parameter	Symbol	Min	Typ	Max	Unit	Condition
NSI68515UC						
RDY reporting						
Open drain low output voltage	V _{RDY_L}			0.3	V	I _{SINK_RDY} =5mA
V _{CC2} UVLO on delay to output high	t _{VCC2H_OUT}		11		us	IF=10mA
V _{CC2} UVLO on delay to output low	t _{VCC2L_OUT}		10		us	
V _{CC2} UVLO on delay to RDY high	t _{VCC2H_RDY}		11		us	IF=10mA DESAT=GND2
V _{CC2} UVLO on delay to RDY low	t _{VCC2L_RDY}		10		us	
FLT Reporting						
FLT mute time	t _{FLT_MUTE_AutoReset}		30		us	
Output Pin Characteristic						
High Level Output Voltage	V _{OH}		V _{CC2} -0.35		V	I _{OUT} =-200mA , I _F =10mA
NSI68515RC						
FLT Reporting						
FLT mute time	t _{FLT_MUTE_AutoReset}		30		us	
Output Pin Characteristic						
High Level Output Voltage	V _{OH}		V _{CC2} -1.8		V	I _{OUT} =-650uA, I _F =10mA
NSI68515AC						
FLT Reporting						
FLT mute time	t _{FLT_MUTE_AutoReset}		30		us	
Output Pin Characteristic						
High Level Output Voltage	V _{OH}		V _{CC2} -0.35		V	I _{OUT} =-200mA , I _F =10mA
NSI68515LC						
FLT Reporting						
FLT mute time	t _{FLT_MUTE}		13		us	
Output Pin Characteristic						
High Level Output Voltage	V _{OH}		V _{CC2} -0.35		V	I _{OUT} =-200mA , I _F =10mA

5.2. Switching Electrical Characteristics

Typical values are at VCC1=5V, VCC2 =15V, VEE2=GND2, TA=25°C. All min and max specifications are at TA=-40°C to 125°C

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Minimum Pulse Width	t_{PWmin}	20	40	60	ns	
Output Rise Time	t_R		35		ns	$C_{LOAD}=10\text{ nF}$, $R_G=0\text{ohm}$
Output Fall Time	t_F		40		ns	
Propagation Delay	t_{PLH}	70	100	150	ns	$I_F=10\text{mA}$, $C_{LOAD}=0.1\text{nF}$, $R_G=0\text{ohm}$
	t_{PHL}	25	100	165	ns	
Pulse Width Distortion $ t_{PHL}-t_{PLH} $	t_{PWD}			100	ns	
Common Mode Transient Immunity	CMTI	150			kV/us	

5.3. Switching Electrical Characteristics

Typical values are at VCC1=5V, VCC2 =15V, VEE2=GND2, TA=25°C. All min and max specifications are at TA=-40°C to 125°C.

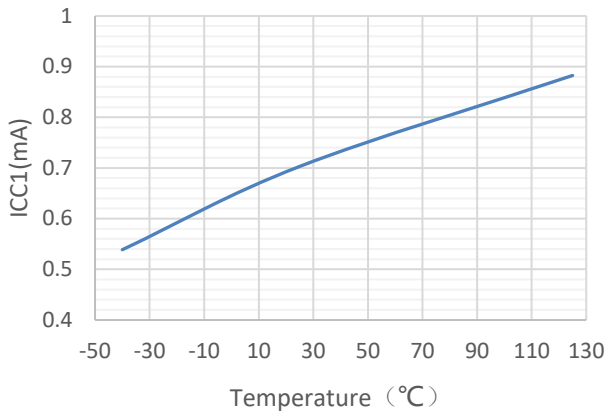


Figure 5.1 ICC1 vs temperature

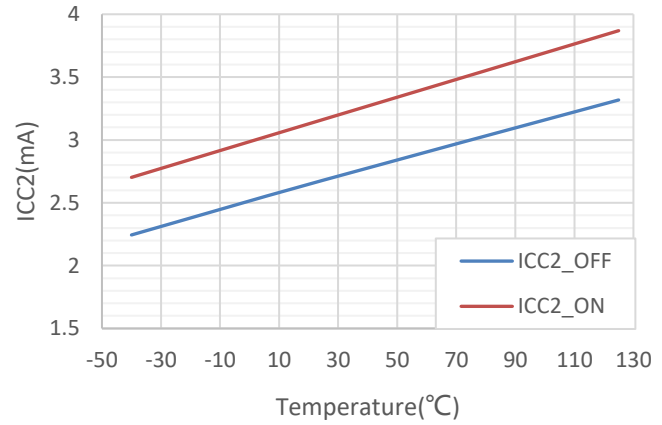


Figure 5.2 ICC2 vs temperature

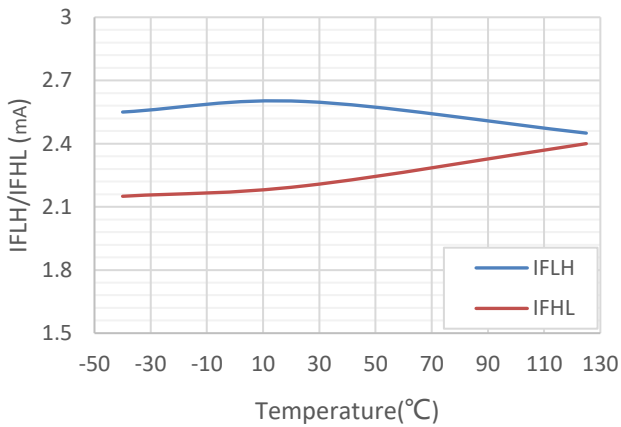


Figure 5.3 IFLH/IFHL vs temperature

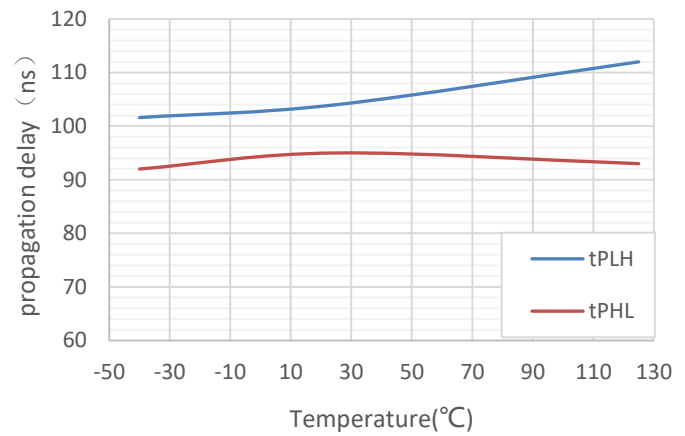


Figure 5.4 Propagation delay vs temperature

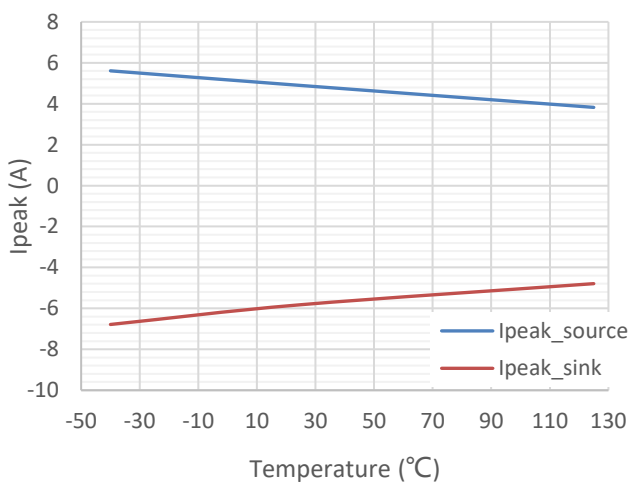


Figure 5.5 Ipeak vs temperature

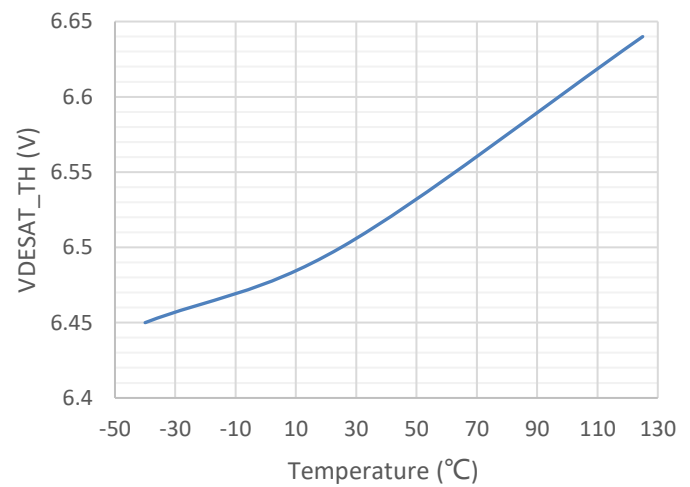


Figure 5.6 VDESAT_TH vs temperature

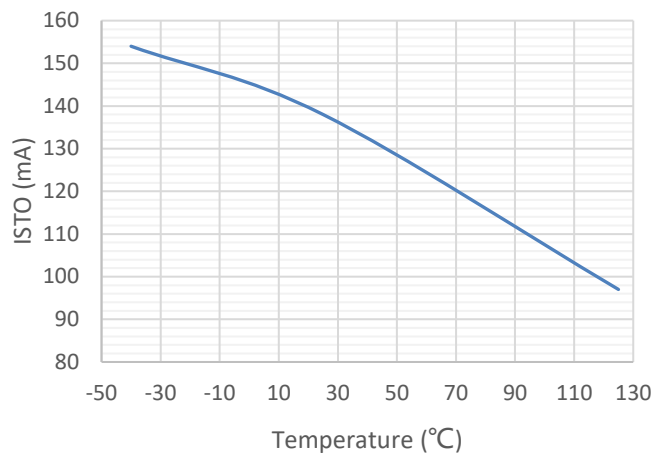


Figure 5.7 I_{STO} vs temperature

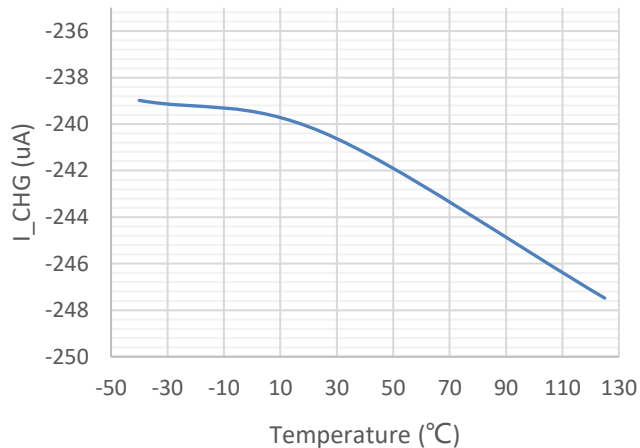


Figure 5.8 I_{CHG} vs temperature

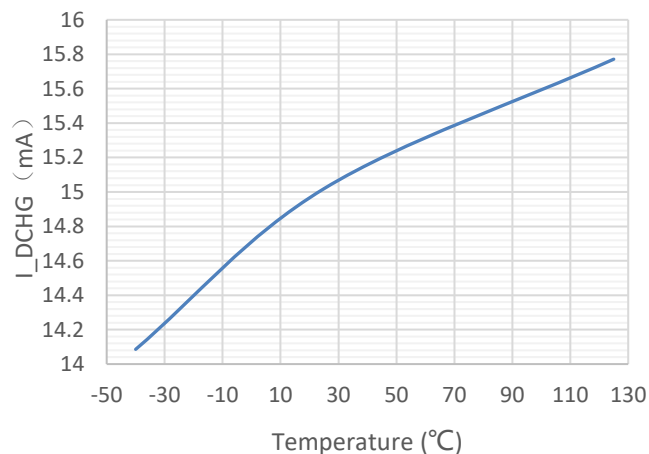


Figure 5.9 I_{DCHG} vs temperature

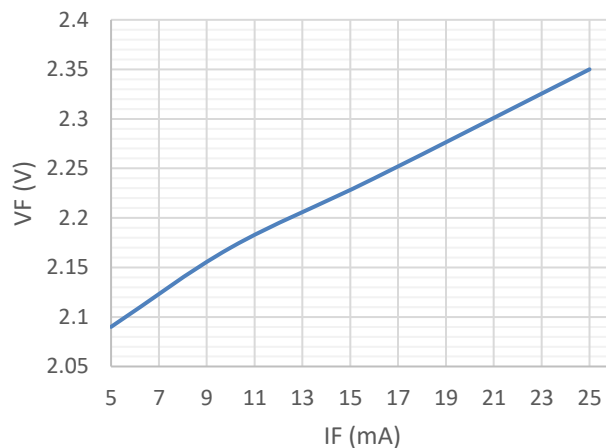


Figure 5.10 V_F vs I_F

6. High Voltage Feature Description

6.1. Insulation and Safety Related Specifications

<i>Parameter</i>	<i>Symbol</i>	<i>SOW16</i>	<i>Unit</i>	<i>Comments</i>
Minimum External Air Gap (Clearance)	CLR	8.0	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	CPG	8.0	mm	Shortest terminal-to-terminal distance across the package surface
Distance Through Insulation	DTI	20	um	Minimum internal gap
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		

6.2. DIN VDE V 0884-11 (VDE V 0884-11): 2017-01 Insulation Characteristics

Description	Test Condition	Symbol	Value	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage $\leq 600V_{RMS}$			I to IV	
For Rated Mains Voltage $\leq 1000V_{RMS}$			I to III	
Climatic Category			40/125/21	
Pollution Degree			2	
Maximum Working Isolation Voltage		V_{IOWM}	1500	V_{RMS}
			2121	V_{DC}
Maximum Repetitive Peak Isolation Voltage		V_{IORM}	2121	V_{PEAK}
Input to Output Test Voltage, Method B1	$V_{pd(m)}=V_{IORM}\times 1.875$, 100% production test, $t_{ini}=t_m=1s$, partial discharge $<5pC$	$V_{pd(m)}$	3977	V_{PEAK}
After Environmental Tests Subgroup 1	$V_{pd(m)}=V_{IORM}\times 1.6$, $t_{ini}=60s$, $t_m=10s$, partial discharge $<5pC$	$V_{pd(m)}$	3394	V_{PEAK}
After Input and Output Safety Test Subgroup 2 and Subgroup 3	$V_{pd(m)}=V_{IORM}\times 1.2$, $t_{ini}=60s$, $t_m=10s$, partial discharge $<5pC$	$V_{pd(m)}$	2545	V_{PEAK}
Maximum Transient Isolation Voltage	$t = 60 s$	V_{IOTM}	8000	V_{PEAK}
Maximum Withstanding Isolation Voltage	$V_{TEST}=V_{ISO}$, $t = 60 s$ (qualification); $V_{TEST}=1.2 \times V_{ISO}$, $t = 1 s$ (100%production)	V_{ISO}	5700	V_{RMS}
Maximum Surge Isolation Voltage	Test method per IEC60065,1.2/50us waveform, $V_{TEST}=V_{IOSM}\times 1.6$	V_{IOSM}	6250	V_{PEAK}
Isolation Resistance	$V_{IO}=500V$ at $T_A=T_S=150^{\circ}C$	R_{IO}	$>10^9$	Ω
	$V_{IO}=500V$ at $100^{\circ}C \leq T_A \leq 125^{\circ}C$		$>10^{11}$	Ω
Isolation Capacitance	$f = 1MHz$	C_{IO}	1	pF

6.3. Safety Limiting Values

Description	Test Condition	Symbol	Value		Unit
Maximum Safety Temperature		T_s	150		°C
Maximum Safety Power Dissipation	$R_{\theta JA}=97^{\circ}\text{C/W}$, $T_J=150^{\circ}\text{C}$, $T_A=25^{\circ}\text{C}$, $V_{CC2}=20\text{V}$, $V_{EE2}=-5\text{V}$	P_s	Total	1288	mW
Maximum Safety Current	$R_{\theta JA}=97^{\circ}\text{C/W}$, $V_{CC2}=15\text{V}$, $V_{EE2}=-5\text{V}$ $T_J=150^{\circ}\text{C}$, $T_A=25^{\circ}\text{C}$	I_s	Driver Side	64.4	mA
	$R_{\theta JA}=97^{\circ}\text{C/W}$, $V_{CC2}=20\text{V}$, $V_{EE2}=-5\text{V}$ $T_J=150^{\circ}\text{C}$, $T_A=25^{\circ}\text{C}$		Driver Side	51.5	

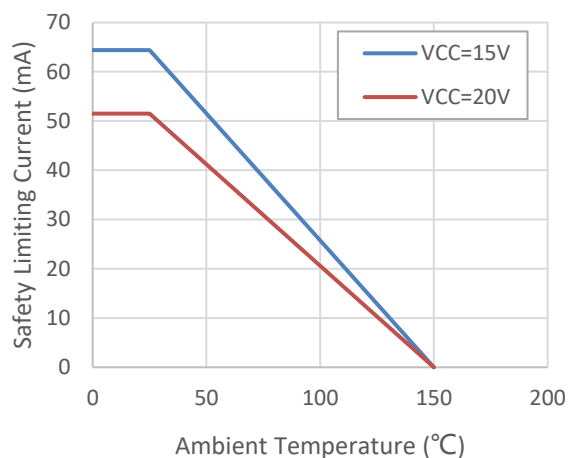


Figure 6.1 Thermal Derating Curve for Limiting Current per DIN VDE V 0884-11 for SOW16 Package

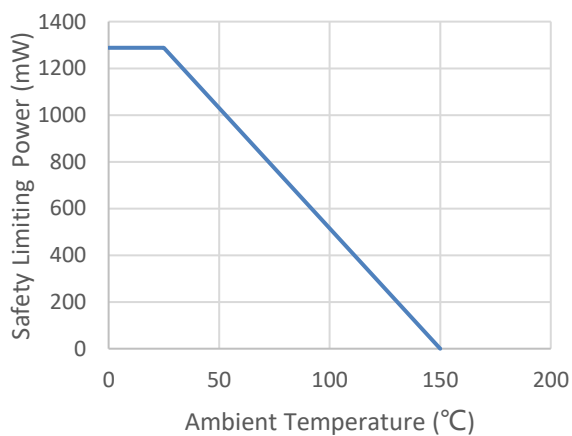


Figure 6.2 Thermal Derating Curve for Limiting Power per DIN VDE V 0884-11 for SOW16 Package

6.4. Regulatory Information

<i>UL</i>		<i>VDE</i>	<i>CQC</i>
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11(VDE V 0884-11):2017-01	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 5700V _{RMS} Isolation Voltage	Single Protection, 5700V _{RMS} Isolation voltage	Reinforced Insulation $V_{IORM}=2121V_{PEAK}$, $V_{IOTM}=8000V_{PEAK}$, $V_{IOSM}=6250V_{PEAK}$	Reinforced Insulation
E500602		Pending	Pending

7. Function Description

7.1. Overview

The NSI68515 is a high reliable power transistor gate driver. It can source and sink 5A peak current, which is suitable to drive MOSFET, IGBT, or SiC MOSFET. The NSI68515 is available in SOW16 package, which can support 5700VRMS isolation per UL1577. System robustness is supported by 150kV/us minimum common-mode transient immunity (CMTI).

Besides, the NSI68515 includes crucial protection features such as miller clamp, DESAT short circuit detection and soft turn off. RDY and short circuit fault are reported through separate pins. The functional block diagram of NSI68515 is shown in Figure 7.1. It requires 7mA to 16mA bias current that flows into the e-diode for normal operation.

The isolation barrier inside NSI68515 is based on a capacitive isolation. The modulation uses OOK modulation technique with key benefits of high noise immunity and low radiation EMI. As shown in Figure 7.2, the digital signal is modulated with RF carrier generated by the internal oscillator at the transmitter side, then it is transferred through the capacitive isolation barrier and demodulated at the driver side.

In summary, the NSI68515 is suitable to replace source and sink reinforced gate driver in high reliability, power density and efficiency switching power system.

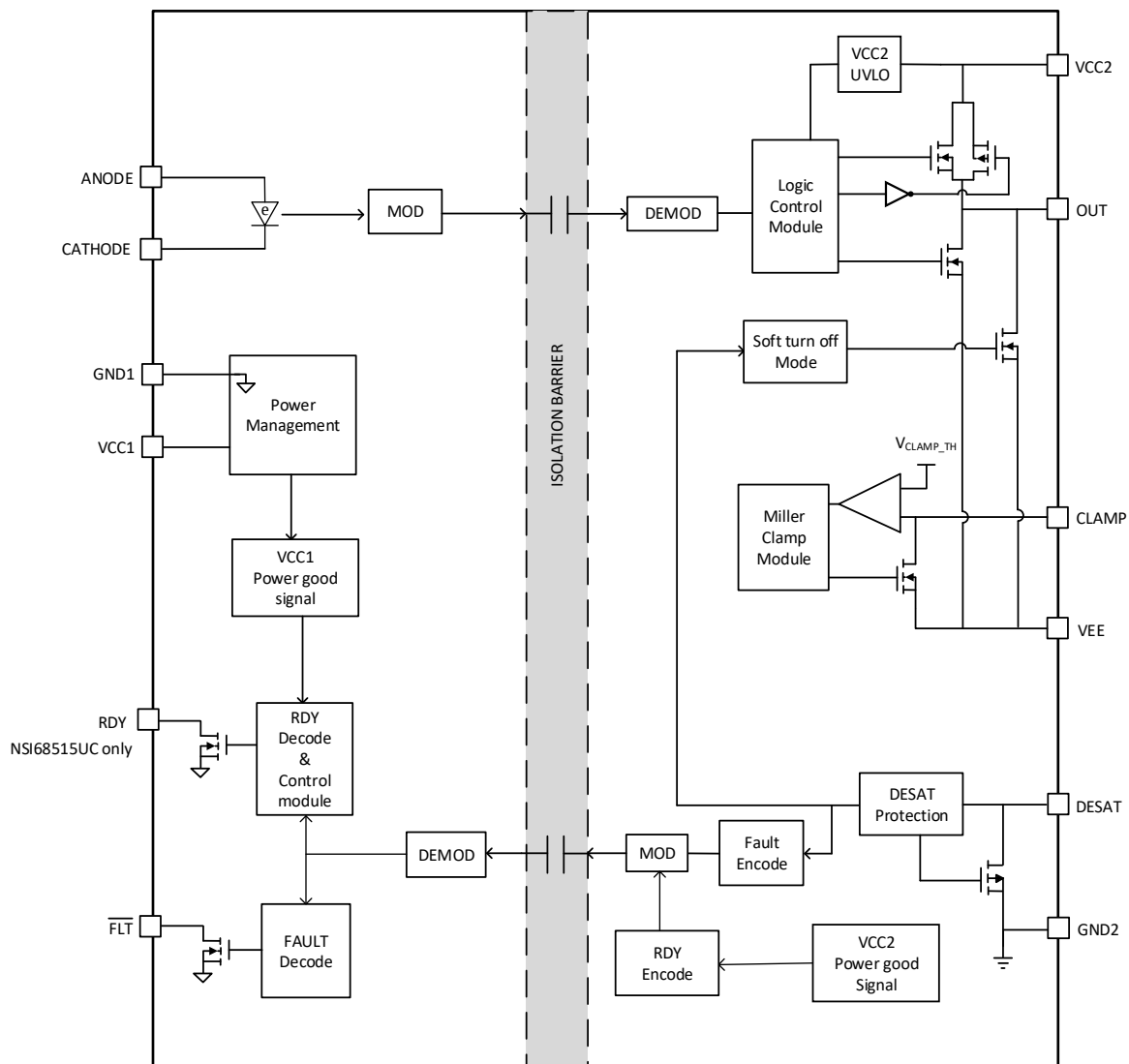


Figure 7.1 NSI68515 Function Block Diagram

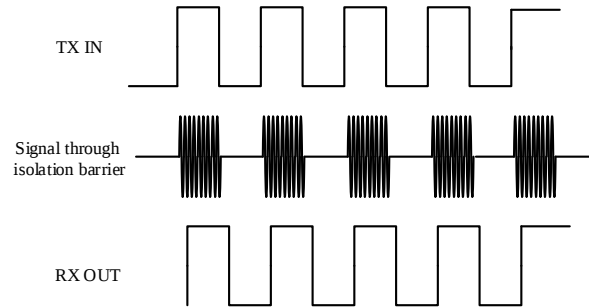


Figure 7.2 OOK Modulation

7.2. Power Supply

Power supply VCC1 can support from 3.3V to 5.5V. Power supply VCC2 is able to support from 13V to 32V. To be mentioned, NSI68515 also supports bipolar power supply mode on the driver side. In the case of fast switching speed, the negative power supply is crucial to prevent false turn on from parasitic Miller capacitor.

7.3. Output Stage

The NSI68515 has P-channel and N-channel MOSFET in parallel to pull up the OUT pin when turning on external power transistor. During DC measurement, only the P-channel MOSFET is conducting. The measurement result R_{OH} represents the on-resistance of P-channel MOSFET. The voltage and current of external power transistor drain to source or collector to emitter change during turn on. At that time, the NSI68515 N-channel MOSFET turns on to pull up OUT more quickly. It results external power transistor faster turn on time, lower turn on power loss, also leads to lower temperature increase of NSI68515. The equivalent pull-up resistance of NSI68515 is the parallel combination $R_{OH} \parallel R_{NMOS}$. The result is quite small, indicating the strong driving capability of NSI68515. The pull-down structure of NSI68515 is simply composed of an N-channel MOSFET with on-resistance of R_{OL} . The result is quite small, indicating the strong driving capability of NSI68515.

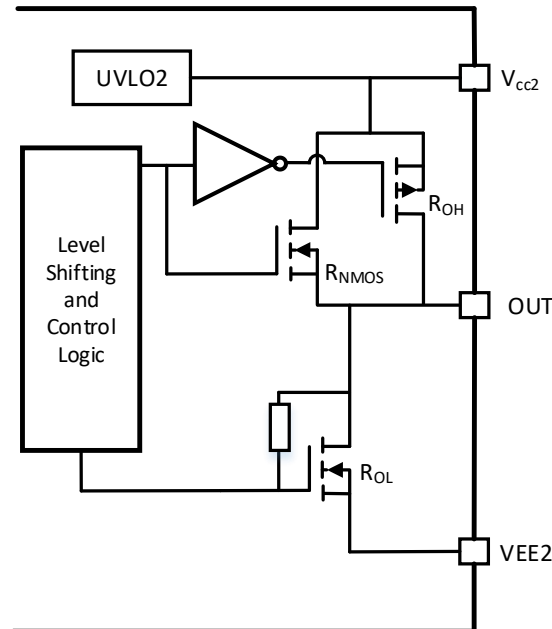


Figure 7.3 NSI68515 Output Stage

Table 7.1 NSI68515 Output Stage On-Resistance

R_{NMOS}	R_{OH}	R_{OL}	Unit
0.25	1.75	0.2	Ω

7.4. VCC1,VCC2and Under Voltage Lock Out(UVLO)

To ensure correct switching NSI68515 is equipped with an under-voltage lockout for input and output power supply independently. V_{CC1} voltage should not fall below the UVLO threshold for normal operation, or the gate-driver output can become clamped low. Output supply UVLO is referred to GND2 pin. If V_{CC2} -GND2 falls below the UVLO threshold, OUT of the gate-driver will be clamped low. Local bypass capacitors should be placed between the V_{CC2} and GND2 pins, as well as the V_{CC1} and GND1 pins. 220 nF to 1 μ F is recommended for device biasing. Additional 100nF capacitor in parallel with the device biasing capacitor is recommended for high frequency filtering. The capacitors should be positioned as close to the device as possible for better noise filtering. Low-ESR, ceramic surface-mount capacitors are recommended.

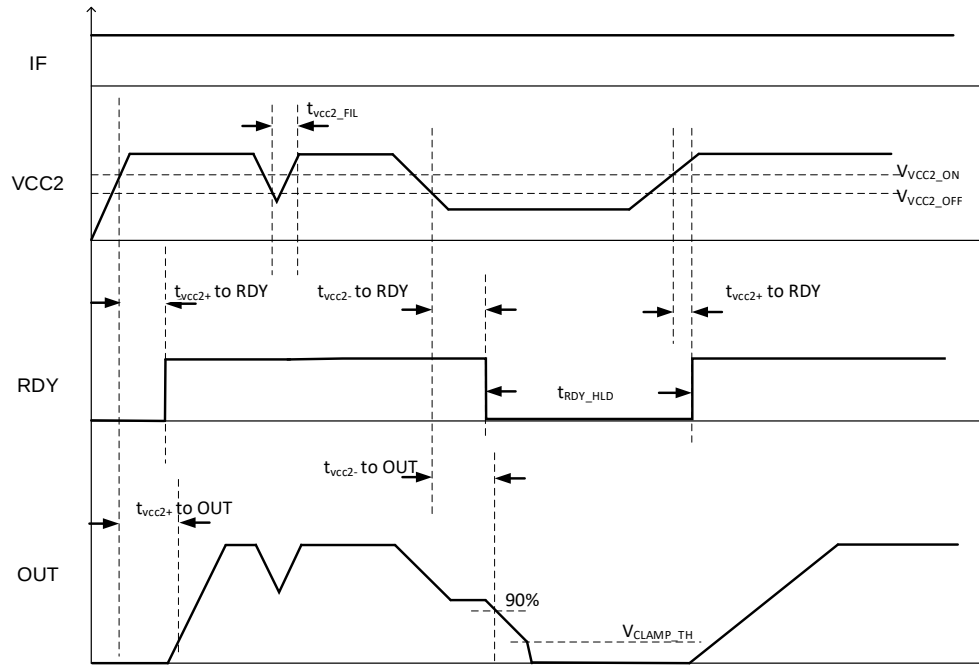


Figure 7.4 RDY vs V_{CC2} timing Diagram

7.5. Active Pull-Down

The Active Pull-Down feature ensures a safe IGBT or MOSFET off-state if V_{CC2} is not connected to the power supply. When V_{CC2} is floating, the driver output is held low and clamping OUT to approximately 1.8V higher than V_{EE2} .

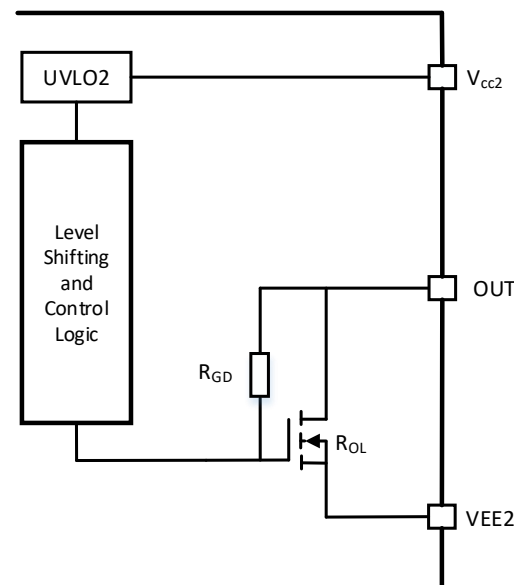


Figure 7.5 Active pulldown

7.6. Short circuit Clamping

During short circuit the gate voltage of IGBT or MOSFET tends to rise because of the feedback via the miller capacitance. The diode between OUT/CLAMP and V_{CC2} pins inside the driver limits this voltage to approximately 0.7V higher than the supply voltage. A maximum current of 500mA may be fed back to the supply through this path for 10 μ s. If higher currents are expected or tighter clamping is desired external Schottky diodes may be added.

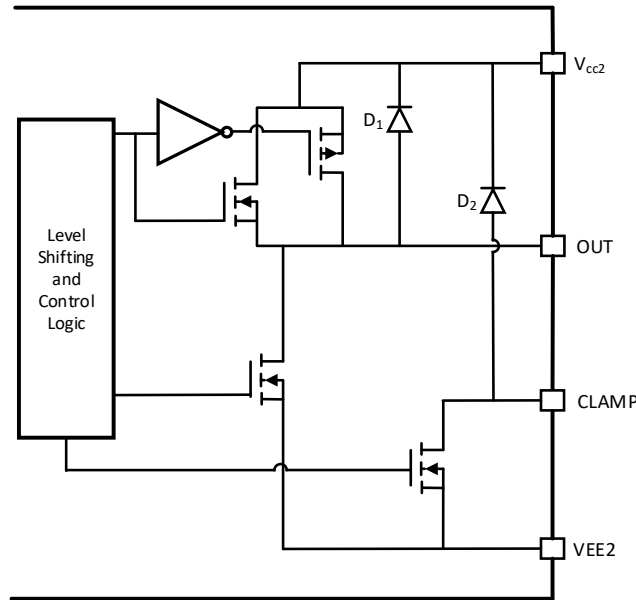


Figure 7.6 Short circuit clamping

7.7. Internal Active Miller Clamp

Active miller clamp is used to prevent false turn on. After the external power transistor is turned off, the other one of the phase leg is turned on. The voltage of the drain-source or collector-emitter rises instantly. The dv/dt will cause a high current on miller parasitic capacitor. The voltage drop on the gate resistor possibly turn on the external power transistor unintentionally, which will cause a catastrophic damage. To deal with that, NSI68515 is equipped with a miller clamp pin. The clamp pin detects the gate voltage of IGBT or MOSFET. When the gate voltage is decreasing and reaches the V_{CLAMP_TH} , the clamp pin will be pulled down by the internal MOSFET, providing a low impedance path to avoid the false turn on. To be mentioned, the V_{CLAMP_TH} is 2V higher than VEE2. In the situation of fast switching speed, The negative power supply is necessary to avoid false turn on.

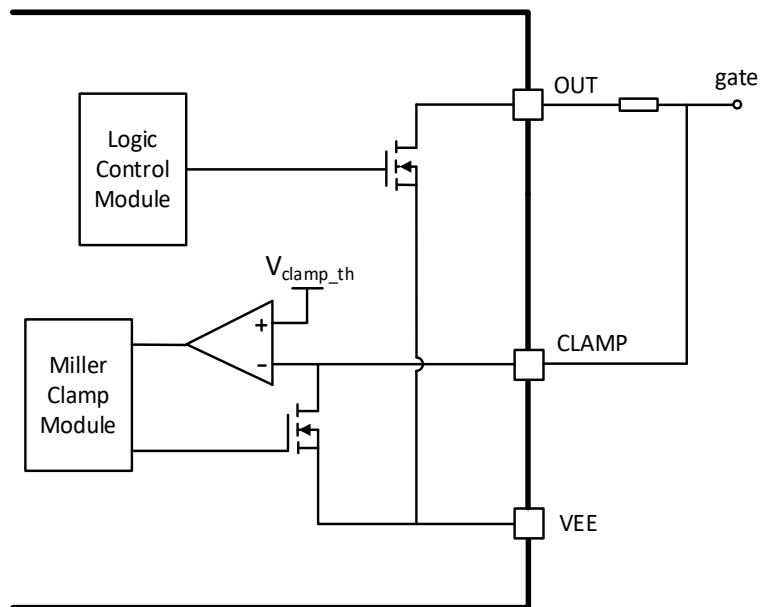


Figure 7.7 Active Miller Clamp

7.8. Desaturation (DESAT) Protection

Desaturation protection is used to prevent the power transistor from short circuit. The DESAT pin has a typical 6.5V threshold, which means the output will be driven low if DESAT pin reaches 6.5V. By default, the DESAT pin is pulled down by internal MOSFET. The internal 240μA current source is designed to work only when the output is high level. There is a 200ns leading edge blanking time to filter the overshoot when the external power transistor is turned on. The current source begins to charge after the internal leading edge blanking time.

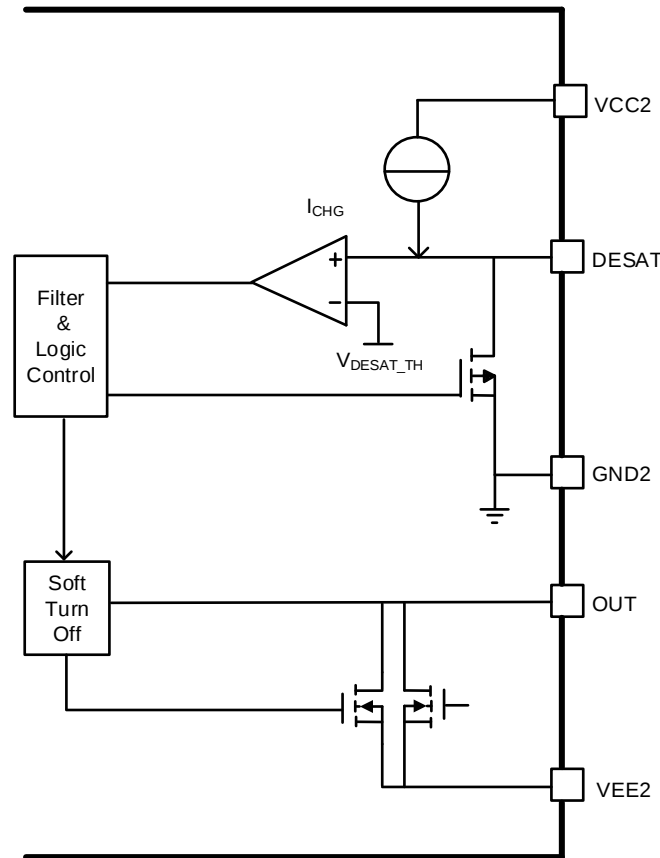


Figure 7.8 DESAT Protection

7.9. Soft Turn-off

The soft turn-off is designed to prevent the overshoot breakdown when DESAT protection is triggered. When the short circuit fault occurs, the external power transistor transits from the active zone to ohmic zone very quickly. The high di/dt may result in the overshoot voltage on the parasitic inductance of the emitter. Therefore, the device should be turned off in a soft manner. But the turn off speed should not be too slow. There is a balance between the overshoot and large energy dissipation. 140mA soft turn off current is a compromising choice. Timing diagram of soft turn off shows below.

7.10. Fault ($\overline{\text{FLT}}$)

The $\overline{\text{FLT}}$ pin of NSI68515 is used to report a warning signal if the fault is detected on DESAT. If the fault occurs, the $\overline{\text{FLT}}$ pin will be pulled down and held in low state for a mute time. During the mute time, NSI68515 ignores any reset signal. For NSI68515LC, it will be reset at the rising edge of IF. The other devices in this family can automatically reset the fault pin after the mute time. The difference of Timing diagram of reset mode shows in Figure 7.9 and Figure 7.10.

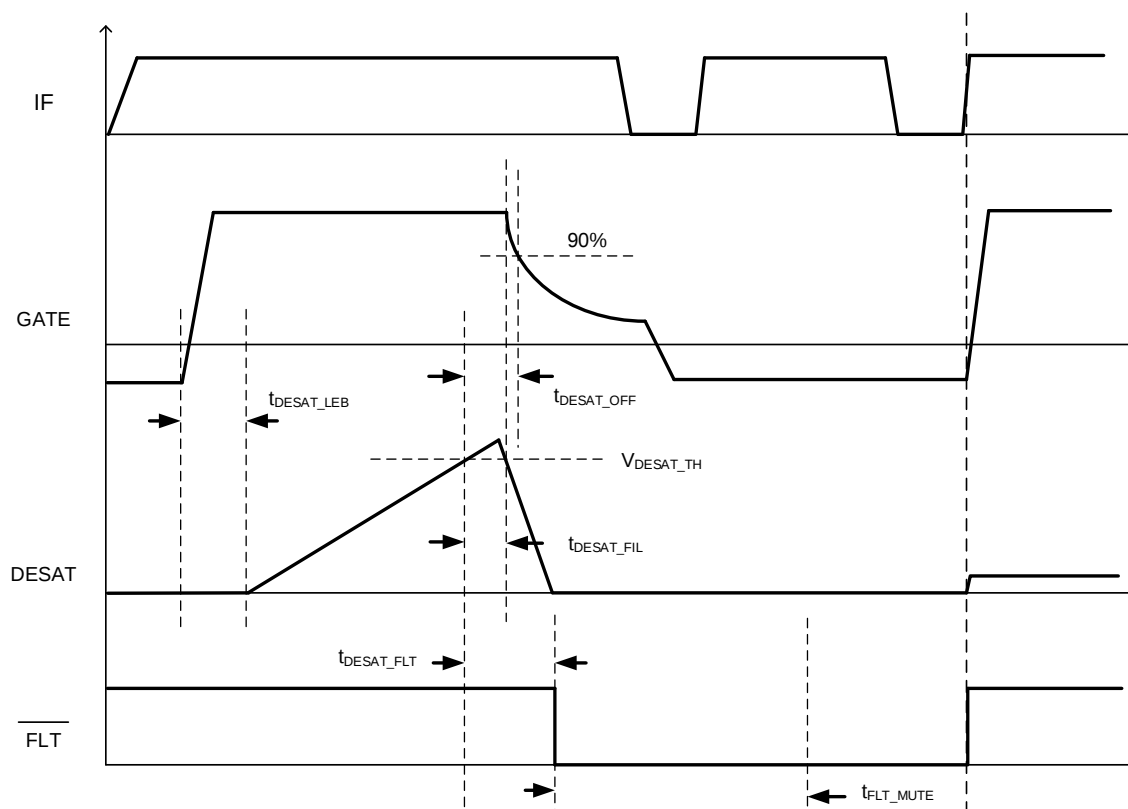


Figure 7.9 Timing Diagram for NSI68515LC

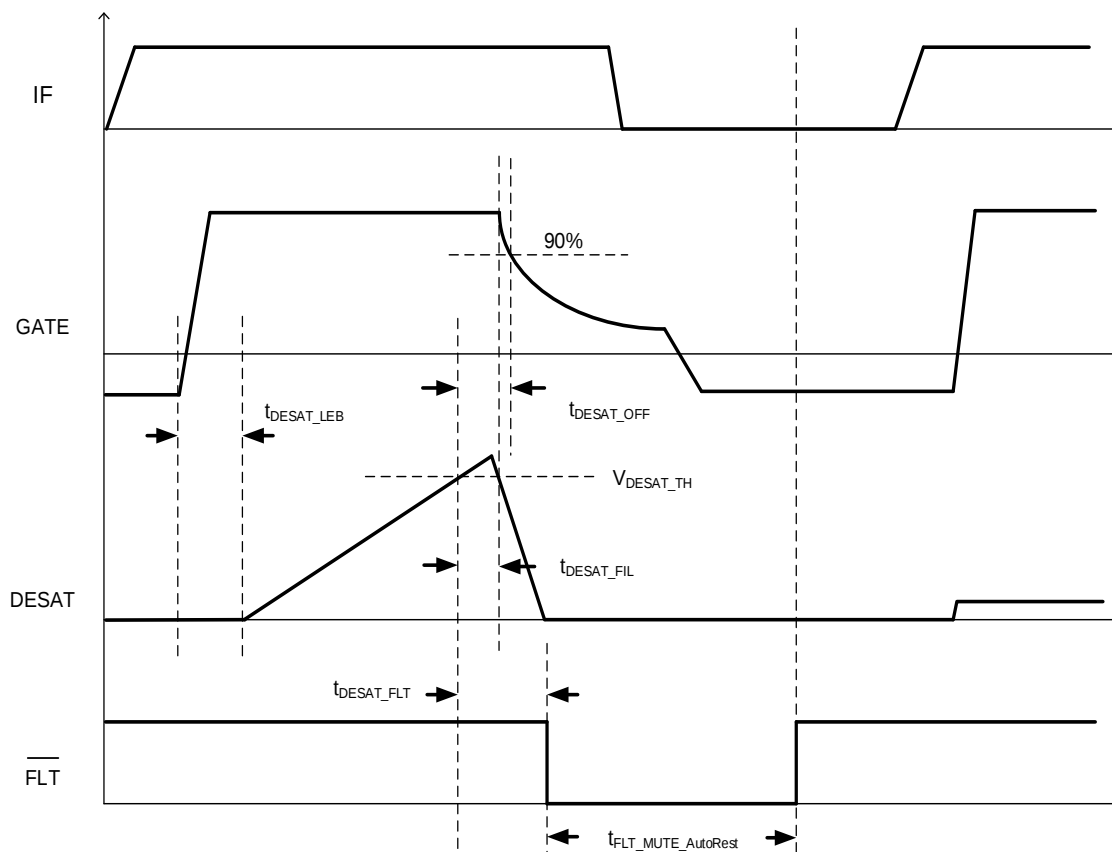


Figure 7.10 Timing Diagram for NSI68515AC, NSI68515RC, NSI68515UC

8. Application Note

8.1. Typical Application Circuit

Bypassing capacitors for VCC1 and VCC2 supplies are needed to achieve reliable performance. To filter noise, 0.1μF/50V ceramic capacitor is recommended to place as close as possible to NSI68515, both at VCC1 and VCC2 side. For VCC2 supply, additional 10μF/50V ceramic capacitor is recommended, to support high peak currents when turning on external power transistor. If the VCC1 or VCC2 power supply is located long distance from the IC, bigger capacitance is essential. VCC1 respects to GND1, providing power for RDY and FAULT.

A 5kΩ resistor can be used as pull-up resistor for $\overline{\text{FLT}}$.

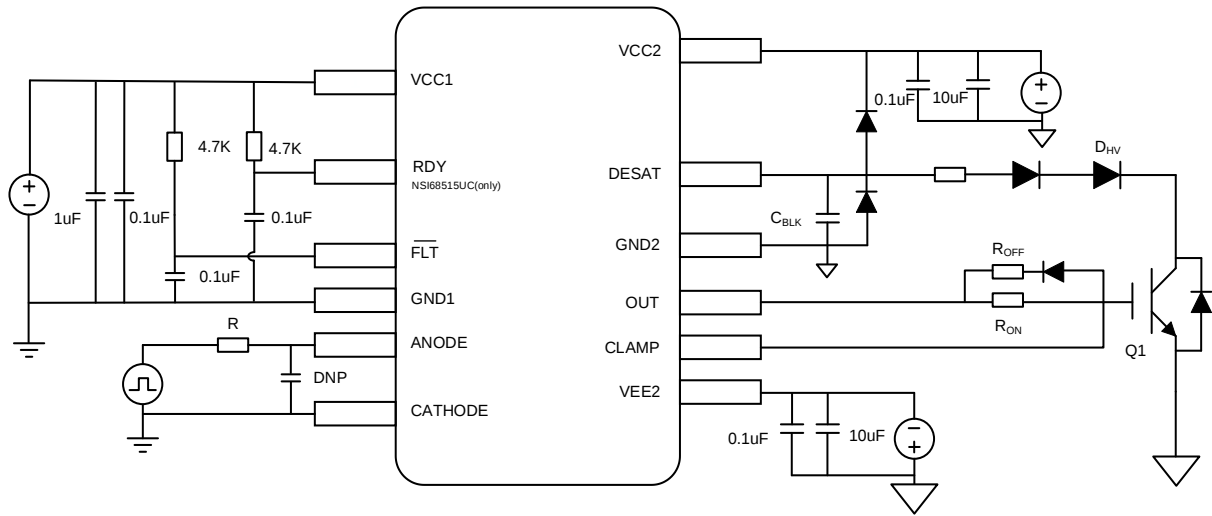


Figure 8.1 Typical Application

8.2. Design for ANODE, CATHODE

NSI68515 requires 7mA to 16mA bias current that flows into the e-diode for normal operation. The PWM from MCU is not suitable to provide such current directly and external circuit is needed. In Figure 8.2, one NMOS is used with split input resistors. Another input drive method is using one buffer, as shown in Figure 8.3.

In the application with NSI68515, the noise from parasitic inductance and coupled capacitance cannot be ignored any more. To filter the noise, NSI68515 is designed with a 40ns deglitch filter. Besides, the external low pass filter can also be placed near the input pins. Low pass filter will increase the noise immunity and delay time, so it should be based on the requirements.

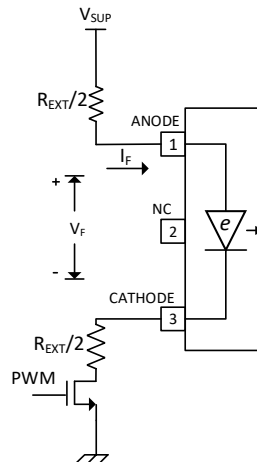


Figure 8.2 NSI68515 typical application circuit with NMOS driving input stage

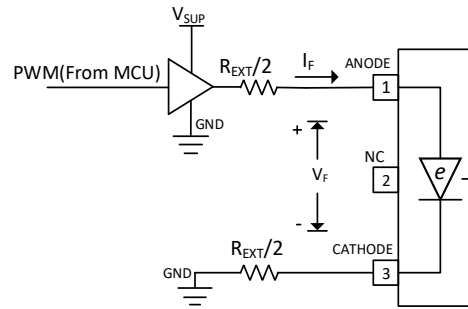


Figure 8.3 NSI68515 typical application circuit with one buffer driving input stage

8.3. Interlock Protection

For applications to drive power transistors in half bridge configuration, two NSI68515 can be used. Interlock protection is possible as shown. If the controller has some mistake, leading to negative dead time, the output PWM of NSI68515 is adjusted to avoid power transistor shoot through. The input side reverse breakdown voltage of NSI68515 is greater than 6.5V, which supports interlock protection of 3.3V or 5V PWM signal source.

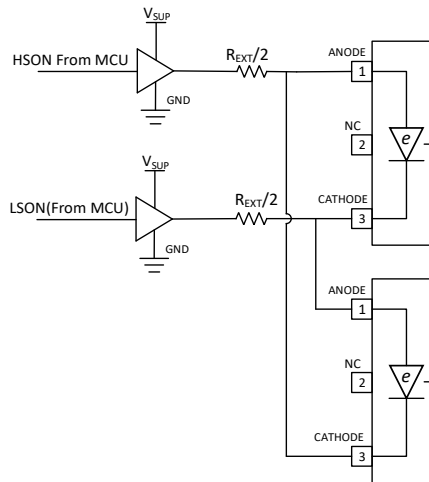


Figure 8.4 Interlock Protection using NSI68515

8.4. Selecting Input Resistor

The recommended forward current range for NSI68515 is 7mA to 16mA. The value of input resistor, buffer supply voltage and buffer internal resistance influence the forward current, as shown in Equation (1). In Figure 8.2, R_{Buffer} is the on-resistance of the external NMOS. In Figure 8.3, R_{Buffer} is the buffer output impedance in output “High” state. In Figure 8.4, R_{Buffer} is the summary of buffer output impedance in “High” and “Low” state.

$$R_{EXT} = \frac{V_{SUP} - V_F}{I_F} - R_{Buffer} \quad (1)$$

The parameter variation needs to be taken into consideration when selecting input resistor. Take Figure 8.2 as an example, Table 8.1 lists assumed parameter variation in this example.

Table 8.1 External parameters range when calculating input resistor

Parameters	Min	Typ	Max
NSI68515 forward current I_F	7mA	10mA	16mA
NSI68515 forward voltage V_F	1.9V	2.17V	2.5V
Buffer supply voltage V_{SUP}	5V*95%	5V	5V*105%
Buffer internal resistance R_{Buffer}	13Ω	18Ω	22Ω
Recommended resistor R_{EXT}	196Ω	265Ω	300Ω

8.5. Design for $\overline{\text{FLT}}/\text{RDY}$

$\overline{\text{FLT}}/\text{RDY}$ pin is open-drain output, which means they cannot work without externally pull-up resistor. In this application, a 4.7kΩ pull-up resistor is recommended for $\overline{\text{FLT}}/\text{RDY}$ pin. A 0.1nF can be placed near the device if it is necessary.

8.6. Design for R_{on} and R_{off}

NSI68515 is featured with split output, so the turn on and turn off switching speed can be independently controlled. The turn on and turn off resistance determine the peak source and sink current, which can be estimated by the formula:

$$I_{\text{source}} = \min\left(\frac{V_{\text{CC2}} - V_{\text{EE}}}{R_{\text{ON}} + R_{\text{OH}} + R_{\text{Gint}}}, 5\text{A}\right)$$

$$I_{\text{sink}} = \min\left(\frac{V_{\text{CC2}} - V_{\text{EE}}}{R_{\text{OFF}} + R_{\text{OL}} + R_{\text{Gint}}}, 5\text{A}\right)$$

Where R_{Gint} is the internal resistance of the SiC or IGBT.

8.7. DESAT Protection

DESAT is used to protect the power semiconductor from overcurrent. When the voltage of DESAT is over the $V_{\text{DESAT_TH}}$, the block of soft turn off will be activated and the fault pin will be pulled down. For typical application, the crucial components required to build the DESAT circuit are the DESAT diode, DESAT resistor and the blank capacitor.

The DESAT diode function is to conduct forward current. To avoid the false detection caused by the reverse recovery spikes, a very fast reverse recovery time diode with small reverse parasitic capacitance is recommended. The DESAT detection threshold voltage of 6.5V can be reduced by the DESAT diode, n is the quantity of diodes. The DESAT detection threshold voltage can be calculated as:

$$V_{\text{DESAT}} = 6.5 - V_F \times n$$

The anti-parallel diode of IGBT have a large transient forward voltage of the diode, which may result in a large negative voltage spike on the DESAT pin, then it may draw a large current from driver. DESAT resistor is used to limit the current. A 1kΩ to 10kΩ resistor is recommended to be added in series with the DESAT diode.

The DESAT fault detection should remain a short blanking time so that the collector voltage can fall below the $V_{\text{DESAT_TH}}$. This blanking time can make sure that there is no nuisance tripping during the IGBT turn-on. It is based on the blank capacitor, which can be estimated as:

$$t = \frac{C_{\text{BLK}} \times V_{\text{DESAT_TH}}}{I_{\text{CHG}}}$$

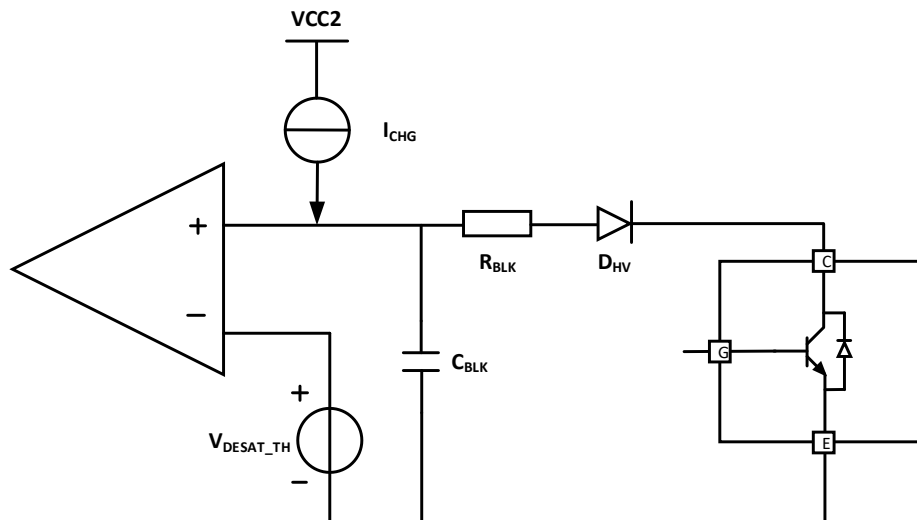


Figure 8.5 DESAT protection

8.8. External current buffer design

Totem structure can be used as an external current buffer to increase the IGBT gate drive current, such as the NPN/PNP buffer shown as below. When the external buffer is used, the external components for soft turn off should be designed in addition. The capacitor is used to adjust the timing and the resistor ensure the sink current lower than the I_{OUTL} . Both resistor and capacitor can be estimated by the Equation below.

$$C_{STO} = \frac{I_{STO} \times t_{STO}}{VCC2 - VEE2}$$

$$R_{STO} = \frac{VCC2 - VEE2}{I_{OUTL}}$$

I_{STO} is the internal soft turn off current

T_{sto} is the expected timing

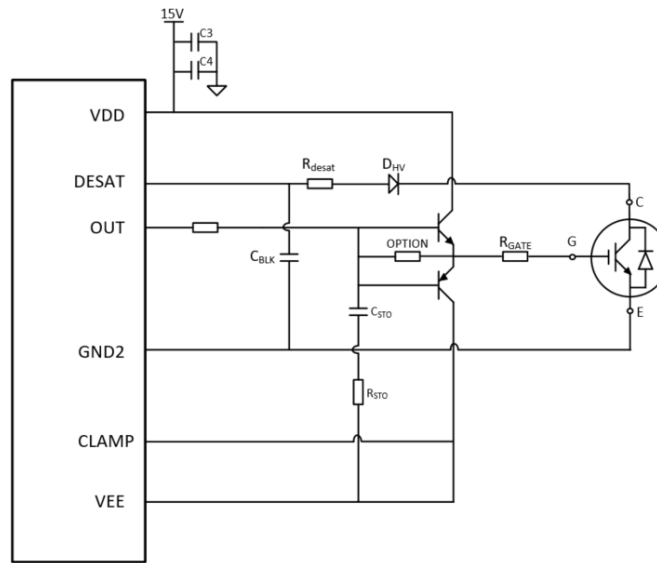


Figure 8.5 External current buffer

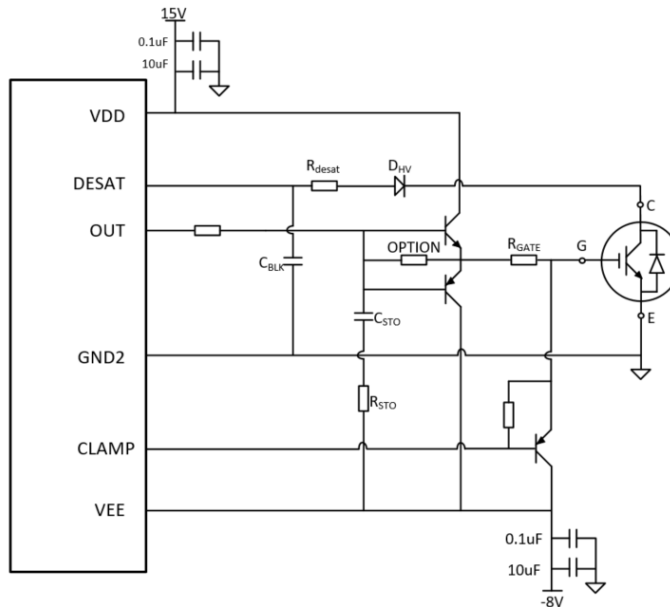


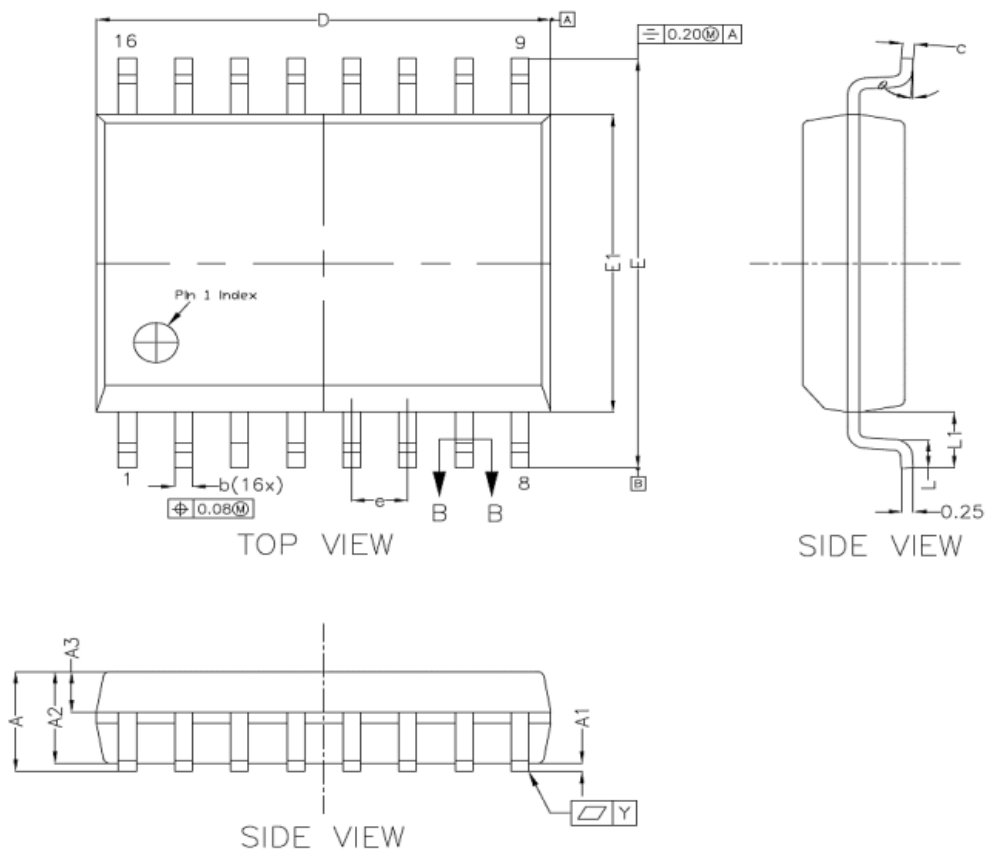
Figure 8.6 Current buffer with external miller clamp

8.9. PCB Layout

Careful PCB layout is essential for optimal performance. Some key guidelines are:

- The bypass capacitors should be placed close to NSI68515, between V_{CC1} to GND1, or V_{CC2} to GND2.
- There is high switching current that charges and discharges the gate of external power transistor, leading to EMI and ring issues. The parasitic inductance of this loop should be minimized, by decreasing loop area and place NSI68515 close to power transistor.
- Place large amount of copper connecting to V_{EE2} pin and V_{CC2} pin for thermal dissipation, with priority on V_{EE2} pin. If the system has multi V_{EE2} or V_{CC2} layers, use multiple vias of adequate size for connection.
- To ensure isolation performance between primary and secondary side, the space under the chip should keep free from planes, traces, pads or via.

9. Package Information



SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	2.65
A1	0.10	---	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	---	0.43
c	0.23	---	0.32
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27 bsc		
L1	1.40 bsc		
L	0.55	---	0.85
Y	---	0.10	---
θ	0°	---	8°

SOW16 Package Shape and Dimension

Dimensions shown in millimeters

10. Ordering Information

<i>Part Number</i>	<i>Auto-Reset Feature</i>	<i>RDY Report</i>	<i>Output Rail to Rail</i>	<i>MSL</i>	<i>SPQ</i>	<i>Category</i>	<i>Package Drawing</i>
NSI68515LC-DSWR	NO	NO	YES	2	1000	Industrial	SOW16
NSI68515UC-DSWR	YES	YES	YES	2	1000	Industrial	SOW16
NSI68515AC-DSWR	YES	NO	YES	2	1000	Industrial	SOW16
NSI68515RC-DSWR	YES	NO	NO	2	1000	Industrial	SOW16

11. Documentation Support

<i>Part Number</i>	<i>Product Folder</i>	<i>Datasheet</i>	<i>Technical Documents</i>	<i>Isolated Driver Selection Guide</i>
NSI68515	Click here	Click here	Click here	Click here

12. Tape and Reel Information

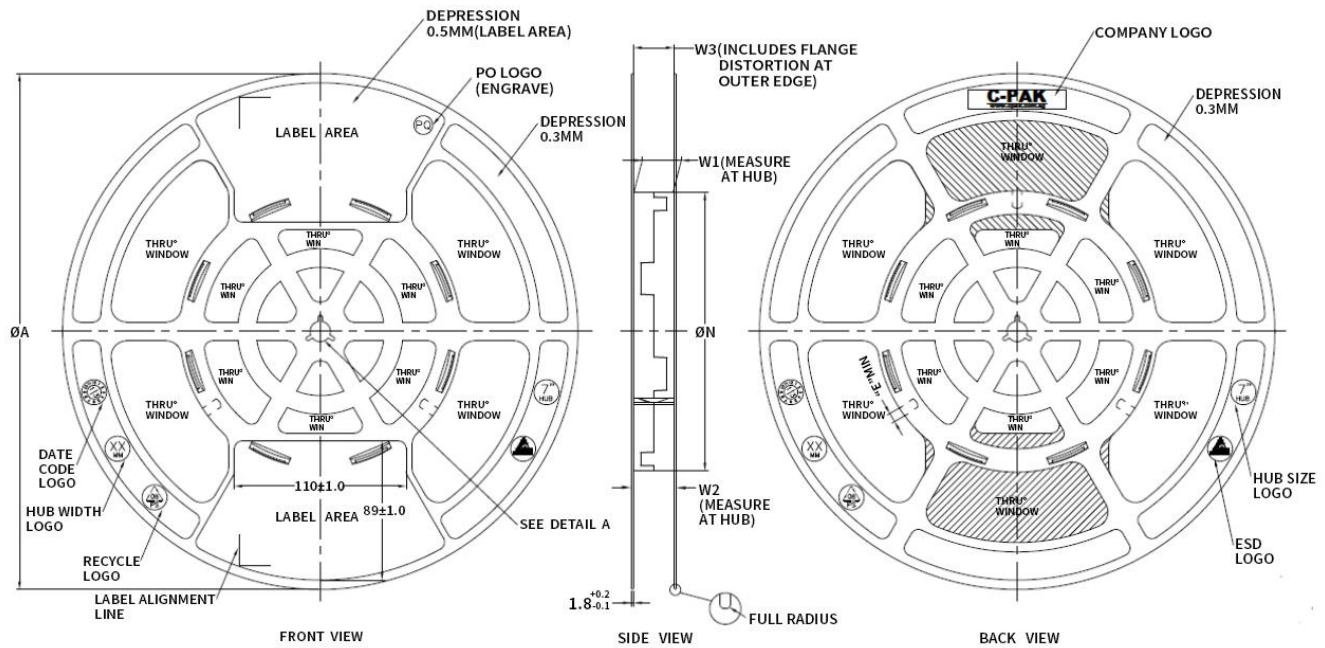
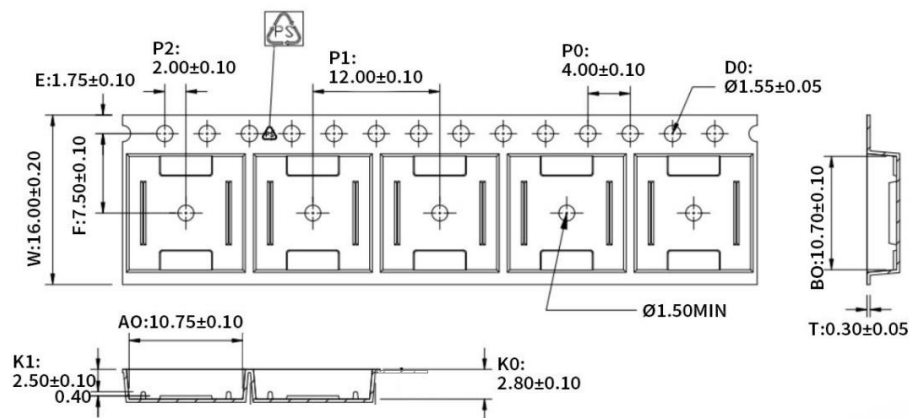


Figure 12.1 Reel Information



1. 1.10 sprocket hole pitch cumulative tolerance ± 0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481 requirements.
5. Thickness: 0.30 ± 0.05 mm.
6. Packing length per 22" reel: 378 Meters. (N=122)
7. Component load per 13" reel: 1000 pcs.

Figure 12.2 SOW16 Tape Information

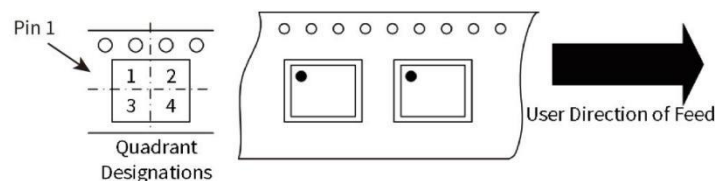


Figure 12.3 Quadrant Designation for Pin1 Orientation in Tape

13. Reversion History

Revision	Description	Date
1.0	Initial version	2023/6/6
1.1	Correct mistakes of V_F - I_F figure	2023/6/12

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