NST118

High-Accuracy, Low-Power Temperature Sensor with SMBus and I²C Interface

Datasheet (EN) 1.2

Product Overview

The NST118 is a low-power, high accuracy digital temperature sensor compatible with SMBus and I²C interfaces, and supports 4 device addresses, and provides SMBus reset and alert functions. The device operates in the power supply voltage range of 1.71V to 3.6V, and offers typical accuracy of ±0.1°C from 25°C to 45°C and maximum accuracy of ±1°C in the full temperature range -40°C to 125°C. The NST118 on-chip 12-bit analog-to-digital converter (ADC) provides resolution down to 0.0625°C. It is highly linear and does not require complex calculations or lookup tables to derive temperature.

NST118 has an operating temperature range of -40°C to 125°C and is available in DFN(6) package, making it suitable for on-board and off-line applications in the automotive, industrial, and consumer markets. Because of low power consumption, it can also be applied to IoT. In addition, it is a good substitute for negative temperature coefficient (NTC) and positive temperature coefficient (PTC) thermistors.

Key Features

- High Accuracy over –40°C to 125°C Wide Temperature Range
  - 25 °C ~ 45 °C: ±0.1°C (Typical)
  - -20 °C ~ 60°C: ±0.5°C (Maximum)
  - -40 °C ~125°C: ±1°C (Maximum)
- Proportional to Temperature with 0.0625°C Resolution
- Power up Defaults Permit Stand-Alone Operation as Thermostat
- Supports up to 4 Device Addresses
- Supply Operation range from 1.71V to 3.6V
- Operating Current:
  - 6.5μA (Typical, 4Hz conversion cycle)
  - 2.9μA (Typical, 1Hz conversion cycle)
- Shutdown current: 0.5μA (Typical)
- Digital Interface: SMBus, I²C
- Package: DFN (6)

Applications

- General System Thermal Management
- Computer Peripheral Thermal Protection
- Notebook Computers
- Industrial Internet of Things (IoT)
- Communications Infrastructure
- Power-system Monitors
- Thermal Protection
- Environmental Monitoring and HVAC

Device Information

Part Number	*Package*	*Body Size*
NST118-CDNR	DFN(6)	2mm×2mm

Typical Application

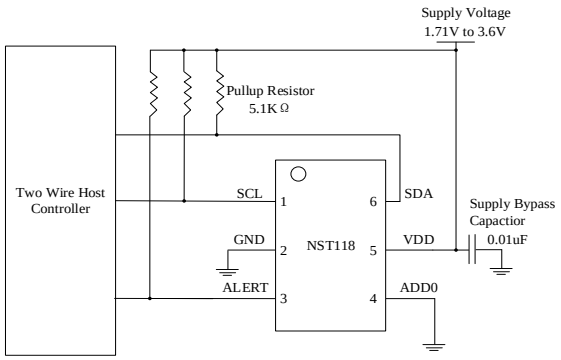


Figure 1 The Typical Application of NST118

INDEX

1 Pin Configuration and Functions

DFN(6) Top View

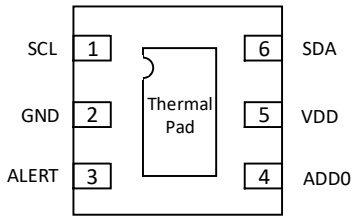


Figure 1.1 NST118 Pin Configuration

Pinout		Type	Description
No.	Name		
1	SCL	I	Serial clock. Open-drain output, requires a pullup resistor.
2	GND	GND	Ground
3	ALERT	O	Over temperature alert. Open-drain output, requires a pullup resistor.
4	ADD0	I	Address Select. Connect to VDD, GND, SDA or SCL
5	VDD	Power	Supply voltage, 1.71 V to 3.6 V
6	SDA	I/O	Serial data. Open-drain output, requires a pullup resistor.

2 Specifications

2.1 Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply Voltage Pin (VDD)	VDD	-0.3		4	V	
Voltage at ADD0 Pins	ADD0	-0.3		4	V	
Voltage at OS, SCL and SDA Pins	ALERT, SCL, SDA	-0.3		4	V	
Storage Temperature		-60		155	°C	
Operation Temperature	$TB_{operation}$	-55		125	°C	
Maximum Junction Temperature				155	°C	
ESD Susceptibility	HBM	±7			KV	
	CDM	±2			KV	

2.2 Electrical Characteristics

at T_A = +25°C and VDD = +1.71V to +3.6V, Rpu = 5.1kohm, unless otherwise noted.

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply						
Supply Voltage Range	VDD	1.71	3.3	3.6	V	
Supply Sensitivity			0.066		°C/V	
Average Quiescent Current	I_Q (1)		6.5		µA	Serial Bus Inactive
			14		µA	Serial Bus Active, SCL Frequency = 400kHz
			62		µA	Serial Bus Active, SCL Frequency = 2.8MHz
Shutdown Current	I_{SD}		0.5		µA	Serial Bus Inactive
			8		µA	Serial Bus Active, SCL Frequency = 400kHz
			56		µA	Serial Bus Active, SCL Frequency = 2.8MHz
Temperature Range and Resolution						
Temperature Range		-40		125	°C	
Resolution			0.0625		°C	
Accuracy(2)			±0.1	±0.2	°C	from 25°C to 45°C
			±0.2	±0.5	°C	from -20°C to 60°C
			±0.5	±1	°C	from -40°C to 125°C
Conversion Time	T_{CONV}		20	24	ms	
ALERT Output Saturation Voltage				0.5	V	I_{OUT} = 4mA
Timeout time	$T_{TIMEOUT}$		30		ms	
Digital DC Characteristic						
High-level Input Voltage	V_H	VDD*0.7		VDD+0.3	V	
Low-level Input Voltage	V_L	-0.3		VDD*0.3	V	
High-level Input Current				1	µA	
Low-level Input Current				-1	µA	
Digital Inputs Capacitance	C_{IN}		5		pF	
Output Leakage Current	I_{OH}			1	µA	V_{OH}=5V
Low-level Output Voltage	V_{OL}			0.4	V	I_{OL}= 3mA
Thermal response						
Thermal Response Time			0.24		s	Stirred Oil Thermal Setting to 63% of Final Value (DFN (6))
Drift						
Drift (3)			TBD		°C	

(1) at 4-Hz conversion cycle.

(2) Accuracy Min and Max value means mean ±3 sigma value.
(3) Drift data is based on a 1000-hour stress test at +125°C with VDD = 3.6V.

2.3 I²C Timing characteristics

Parameters	*Symbol*	*FAST MODE*		*HIGH-SPEED MODE*		*Unit*	*Comments*
		Min	*Max*	*Min*	*Max*		
SCL operating frequency	f_{SCL}	0.001	0.4	0.001	2.8	MHz	
Bus-free time between STOP and START conditions	t_{BUF}	1300		160		ns	
Hold time after repeated START condition; after this period, the first clock is generated	t_{HDSTA}	600		160		ns	
Repeated START condition setup time	t_{SUSTA}	600		160		ns	
STOP condition setup time	t_{SUSTO}	600		160		ns	
Data hold time	T_{HDDAT}	100	900	25	105	ns	
Data setup time	T_{SUDAT}	100		25		ns	
SCL clock low period	T_{LOW}	1300		210		ns	
SCL clock high period	T_{HIGH}	600		60		ns	
Data fall time	t_{FD}		300		80	ns	
Data rise time	t_{RD}		300			ns	
			1000			ns	SCLK ≤ 100 kHz
Clock fall time	t_{FC}		300		40	ns	
Clock rise time	t_{RC}		300		40	ns	

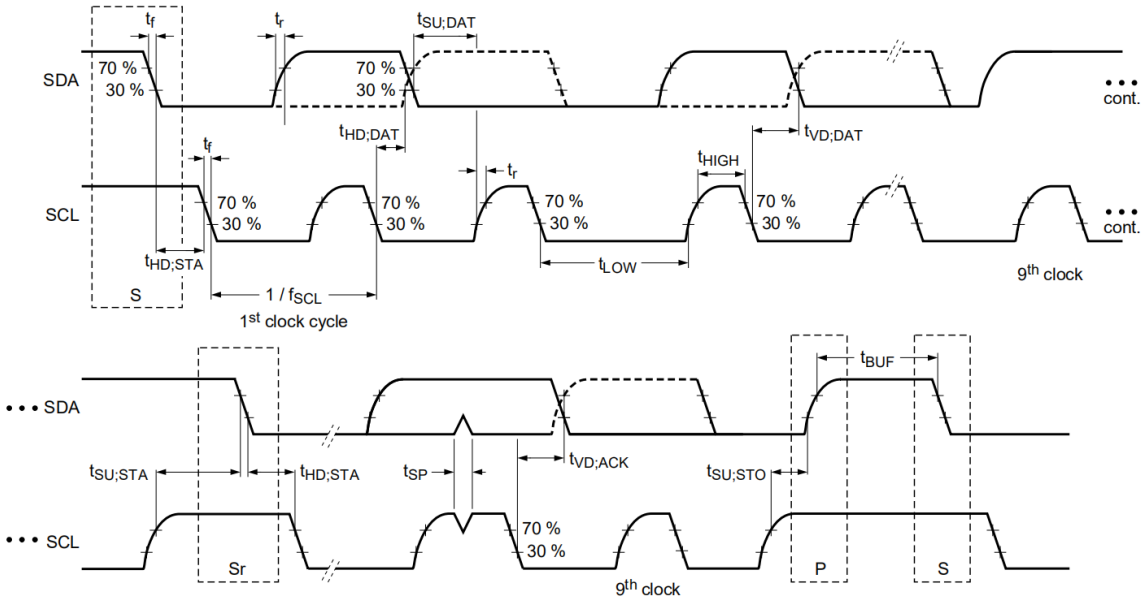


Figure 2.1 I²C Timing Diagram

2.4 Typical Characteristics

at T_A = +25°C and VDD = 3.3 V, Rpu = 5.1kohm, unless otherwise noted.

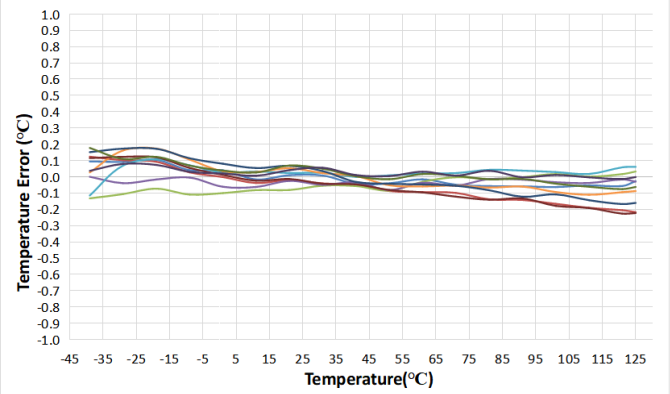


Figure 2.2 Temperature Error vs Temperature

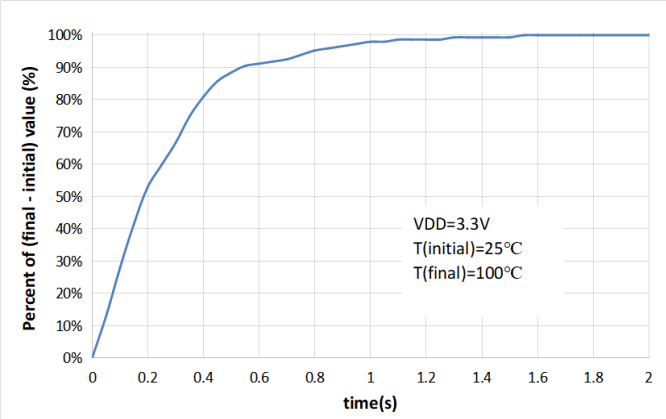


Figure 2.3 Thermal response in stilling Oil

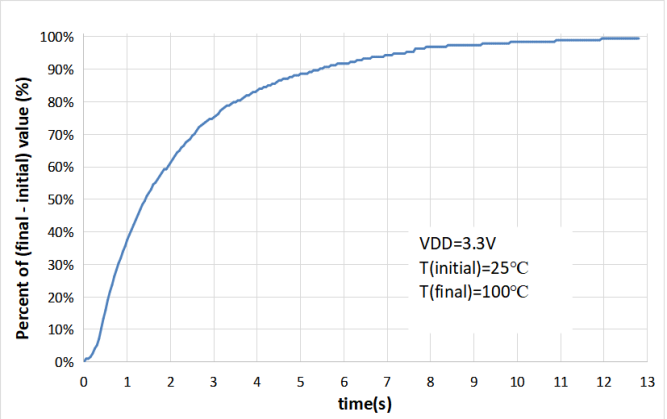


Figure 2.4 Thermal response in stilling Air

3 Function Description

3.1 Overview

The NST118 is an industry-standard digital temperature sensor with an integrated 12-bit, delta-sigma (ΔΣ) analog-to-digital converter (ADC) and two-wire interface. The device operates with a supply voltage from 1.71V to 3.6V, and offers typical accuracy of ±0.1°C from 25°C to 45°C and maximum accuracy of ±1°C in the full temperature range -40°C to 125°C. NST118 also incorporates a digital comparator that compares a series of readings (the number of which can be selected by the user) with user-programmable setpoint. The comparator triggers the ALERT pin state, which is programmable for mode and polarity, and allowing the user to define the number of consecutive error conditions that must occur before ALERT is activated.

The NST118 communicates with the master device through a 2-wire interface (SMBus and I²C), and the fast mode of communication can reach 400kHz, the high speed can reach 2.8MHz. The NST118 has one address pin, allowing up to 4 devices to operate on the same 2-wire bus. In addition, the SDA and SCL lines of NST118 integrate low-pass filter, which improve communication reliability in noise environment. The NST118 also has a bus fault timeout function, if the SDA or SCL line remains low for longer than timeout (see the Electrical Characteristics of Specifications), it will reset to the idle state (SDA and SCL are set to high impedance) and wait for new startup conditions, it should be noted that the timeout function does not work in the shutdown mode.

3.2 Functional Block Diagram

The NST118 Functional Block Diagram as shown in Figure 3.1.

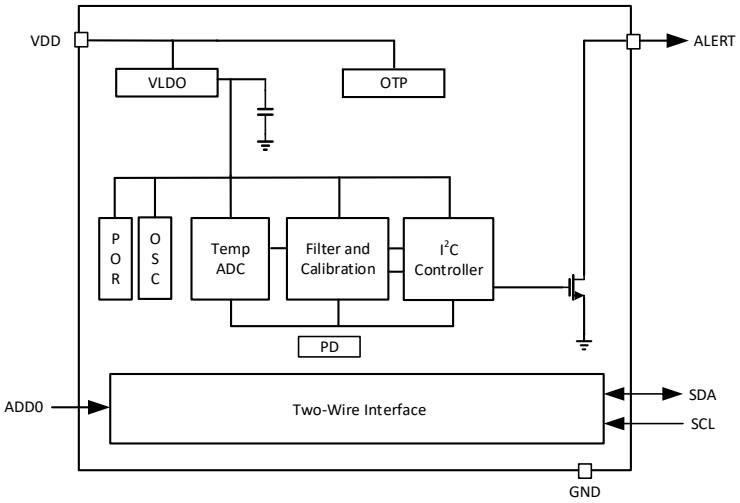


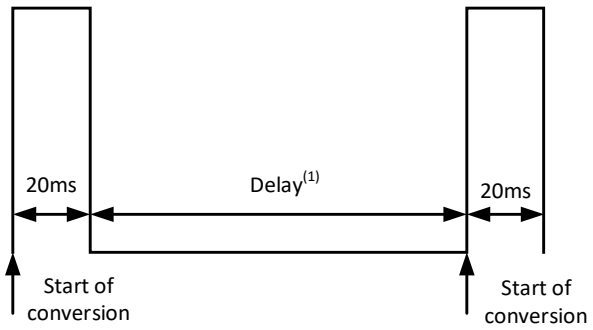
Figure 3.1 NST118 Functional Block Diagram

3.3 Device Functional Modes

3.3.1 Continuous-Conversion Mode

The default mode of the NST118 after power-up is continuous conversion mode. In continuous conversion mode, the ADC performs temperature conversions continuously and saves the result of each conversion to the temperature register, overwriting the result of the previous conversion. The NST118 device provides four conversion rates, which are controlled by CR The NST118 device provides four conversion rates, which are controlled by CR1 and CR0 in the configuration register, the default conversion rate is 4Hz. The conversion rates corresponding to the configuration of CR1 and CR0, please refer to Configuration Register.

As soon as the NST118 is powered up or a general call reset is completed, a temperature transition is immediately performed. As shown in Figure 3.2, the time for each temperature transition is 20ms (typical), the current during temperature conversion is 29uA (+27°C typical), and the current of delay during two conversions is 2.2uA (+27°C typical).



(1) Delay is set by CR1 and CR0.

Figure 3.2 Conversion Start

3.3.2 Extended Mode (EM)

The NST118 has two data format modes, normal mode (EM=0) and extended mode (EM=1), which can be configured through the Configuration Register. In normal mode, temperature data and HIGH and LOW limit data are in 12-bit data format, the extended mode can support temperature data higher than 128°C and is configured to 13-bit data format through configuration registers.

3.3.3 Shutdown Mode (SD)

For power-sensitive applications, The NST118 device offers a low-power shutdown mode, which reducing current consumption to typically less than 0.5μA. Shutdown mode is enabled when write 1 to SD bit of the configuration register. In shutdown mode a One-shot command can be sent to perform a temperature transition, and the device shuts down automatically when the temperature transition is complete. When SD write to 0, the device maintains a continuous conversion state. For the NST118, the time-out feature is turned off in Shutdown Mode.

3.3.4 One-shot (OS)

The NST118 supports a one-shot temperature measurement mode when continuous temperature monitoring is not required. First set the chip into shutdown mode, write 1 to the OS bit to wake up the chip once and perform a temperature conversion. When temperature conversion is in progress, OS bit is 0. After the single conversion is complete, the device returns to the Shutdown state. At the end of the conversion, the OS bit reads 1.

Using one shot mode can achieve faster conversion frequency, temperature conversion takes 20ms typically, however, reading the temperature value needs less than 20μs, Therefore, using the one-shot mode can achieve 30 times faster than the fastest temperature conversion rate in the continuous mode.

3.3.5 Converter Resolution

The converter resolution bits control the resolution of the internal ADC. This control allows the user to maximize efficiency by programming for higher resolution or faster conversion time. The resolution bits and the relationship between resolution and conversion time, please refer to Configuration Register.

3.3.6 Temperature Alert

The AL bit is a read-only function bit that allows user to get the state of ALERT pin in comparator mode by reading the AL. When POL is 0, AL is "1" until the measured temperature is equal to or exceeds the T_{HIGH} temperature of fault queues set, and AL is "0" until the measured temperature is falls below the T_{LOW} temperature of fault queues set, and it again reads as "1". The state of AL is not affected by the TM bit state.

3.3.6.1 Polarity

The polarity bit allows the user to control the output polarity of the NST118 Alert. When POL bit is 0, alert signal is active low, when POL bit is 1, Alert signal is active high, while the state of Alert is inverted. And the operation of ALERT pin in different modes is shown in Figure 3.3.

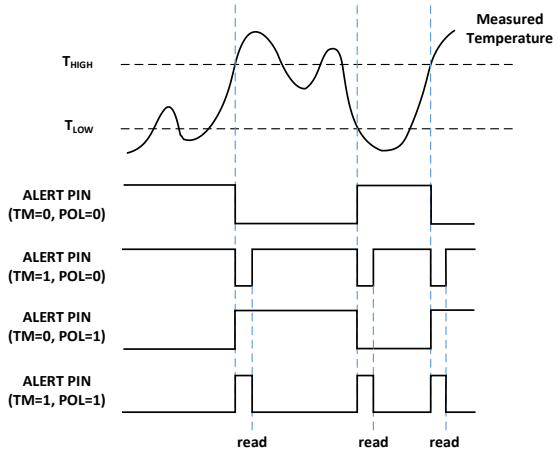


Figure 3.3 Output Transfer Function Diagram

3.3.6.2 Thermostat Mode (TM)

The thermostat mode bit can be configured to make the NST118 work in comparator mode (TM = 0) or interrupt mode (TM = 1). For more information on comparator and interrupt modes, see the *High and Low Limit Registers* section.

Comparator Mode (TM = 0): In comparator mode, when the test temperature is equal to or higher than the T_{HIGH} register value, the Alert pin is activated until the measured temperature is below the T_{LOW} register value.

Interrupt Mode (TM = 1): In interrupt mode, the Alert pin is activated when the test temperature value is above T_{HIGH} or below T_{LOW}, and the Alert state is cleared when the master reads the temperature register.

3.3.6.3 Fault Queue

A fault condition is generated when the temperature measurement value exceeds the T_{HIGH} and T_{LOW} register values, and the number of fault conditions activated by the trigger alert can be programmed by the fault queue. False triggering of alerts due to temperature noise can be avoided by using a fault queue. The number of measured faults that can be programmed to trigger a device alert condition, please refer to Configuration Register.

3.4 Serial Bus

3.4.1 Bus Overview

NST118 is compatible with SMBus and I^2C interfaces and transmits information to the master. NST118 has four slave addresses, which can support the simultaneous use of four NST118 devices on the bus, data on the I^2C-bus can be transferred at rates of up to 100 kbit/s in the Standard-mode, up to 400 kbit/s in the Fast-mode, or up to 2.8 Mbit/s in the High-speed mode. All data bytes are transferred MSB-firstly.

3.4.2 Bus Address

For communication between the master and the slave, a byte address needs to be sent first, including 7bit slave address bits and 1bit read and write direction bits. NST118-DSTR has an ADDR pin, and four different addresses can be obtained through different connections of this pin. Table 3.2 describes the pin logic levels used to properly connect up to four devices.

Table 3.2. Address Pins and Slave Addresses for the NST118

DEVICE TWO-WIRE ADDRESS	*A0 PIN CONNECTION*
1001000	Ground
1001001	VDD
1001010	SDA
1001011	SCL

3.4.3 Bus Function

3.4.3.1 Writing and Reading Operation

Writing operation is triggered by sending the slave address in write mode (R/W=0), then the master sends pointer register, and send the data byte afterwards. The transaction is ended by a STOP condition.

During writing operation, NST118 is used as the slave receiver. The master transfers the slave address byte firstly, including 7 address bits and 1bit write direction bits, NST118 acknowledges after receiving the valid address. the second byte transmitted by master is the pointer register address, then NST118 acknowledges, and the next byte of data is written to the pointer register. The master can terminate communication by generating a STOP condition. The details of this sequence are shown in Figure 3.5 .

To be able to read registers, firstly the register address must be sent in write mode (R/W=0), then either a stop or a repeated start condition must be generated. When the slave is addressed as read mode (R/W=1), then the slave sends out 1 byte data. After reading the data the master needs to generate the NACK and stop condition to end the transaction. The details of this sequence are shown in Figure 3.6.

If repeated reads from the same register are required, it is not necessary to send the pointer register byte repeatedly because the NST118 remembers the pointer register value until it is changed by the next write operation.

3.4.3.2 SMBus Alert Function

When the NST118 is operating in interrupt mode (TM=1), the NST118 supports the SMBus Alert function, the ALERT pin of the NST118 can be connected as a SMBus Alert signal. When the master monitors that the alert is active, the master can send the SMBus alert command (00011001) on the bus, the device responds to the SMBus Alert command by returning its slave address on the SDA line. The eighth bit (LSB) of the slave address byte indicates whether a temperature above T_{HIGH} or below T_{LOW} has caused an ALERT condition: this bit is high if the temperature is greater than or equal to T_{HIGH}. the bit is low if the temperature is less than T_{LOW}. The details of this sequence are shown in Figure 3.7.

If multiple slaves respond to the SMBus alert command issued by the master, the SMBus alert arbiter will arbitrate to determine which slave to clear the alert status. The one with the lowest slave address wins the arbitration. If the NST118 wins arbitration, the alert pin of NST118 activation status is cleared at the end of the SMBus alert command; if the NST118 loses arbitration, the alert activation status is not cleared.

3.4.3.3 General Call

The NST118 provides the general call function. when the general call address (0 000 000) sent by host is received and the R/W bit is 0, the device replies to the command. If the second byte is 00000110, the NST118 latches the state of its address pins and resets its internal registers to the value at power-up.

3.4.3.4 High-Speed Mode

The NST118 supports bus operation above 400 kHz, requiring that the master device must switch the bus to high-speed mode operation by issuing a high-speed mode master code (00001XXX) in the first byte after the START condition. The NST118 does not acknowledge this byte, the NST118 switches the input filter of SCL, SDA and output filter of SDA to high-speed mode, allowing data transfer up to 2.8MHz. After issuing the master code for high-speed mode, the master will transmit a two-wire slave address to initiate the data transfer operation. The bus will continue to operate in high-speed mode until a stop signal appears on the bus. Once the stop signal is received, the SCL, SDA input filter and SDA output filter of the NST118 switch to the fast mode.

3.4.3.5 Time-out Function

The NST118 resets the I^2C interface when the SCL or SDA is continuously pulled low for 30ms (typical) between the START and STOP signals, the NST118 release the SDA and SCL line and waits for the master to initiate a START condition. To avoid activating the timeout function, the SCL operating frequency must be maintained at a rate of at least 1kHz.

3.4.3.6 I^2C Timing

The NST118 of temperature sensor is compatible with SMBus and I^2C. Figure 3.4 to Figure 3.7 describe the various operations of Bus on the NST118. The following list provides bus definitions. Parameters for Figure 3.4 are defined in the *Timing Requirements*. Bus definitions are:

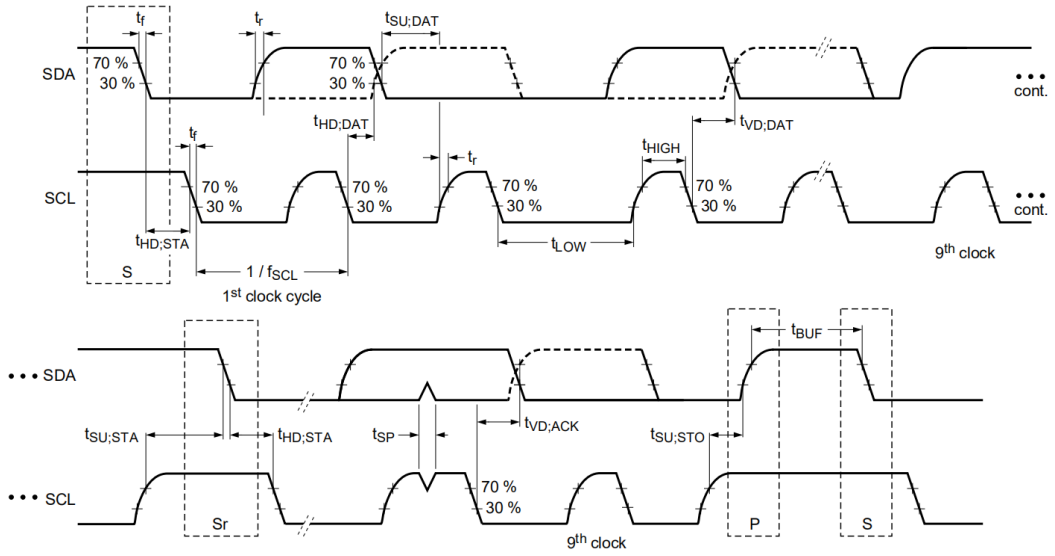


Figure 3.4 Two-Wire Timing Diagram

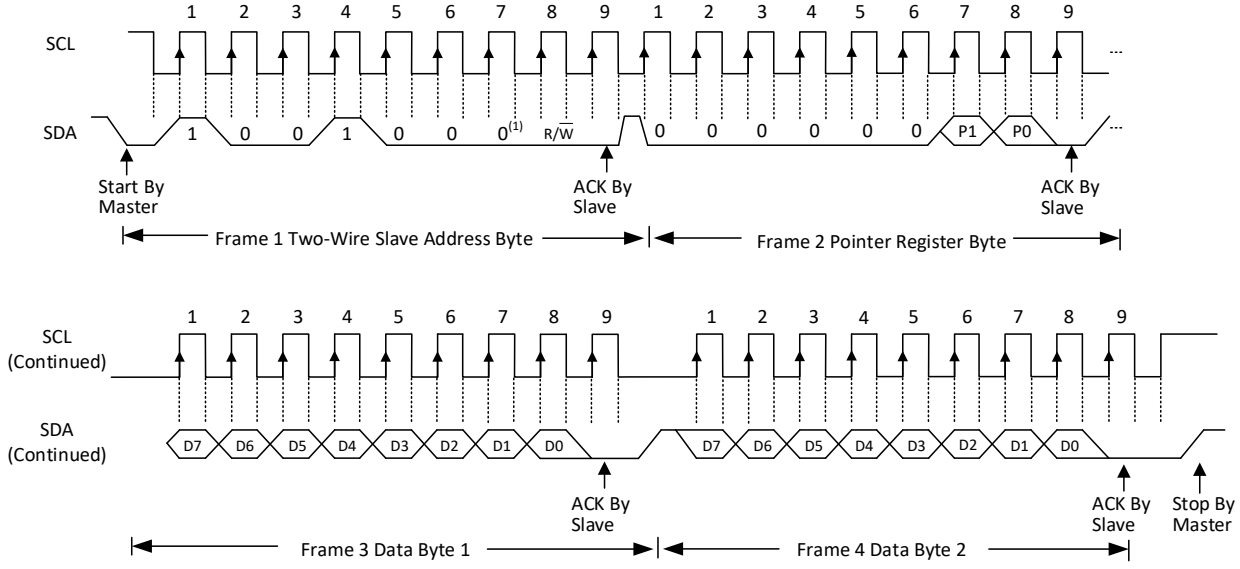
Bus Idle: Both SDA and SCL lines remain high.

Start Data Transfer: A high-to-low transition of SDA with SCL high is a START condition which must precede any other command.

Stop Data Transfer: A low-to-high transition of SDA with SCL high is a STOP condition. The termination of each data transfer can be done with a RESTART or STOP.

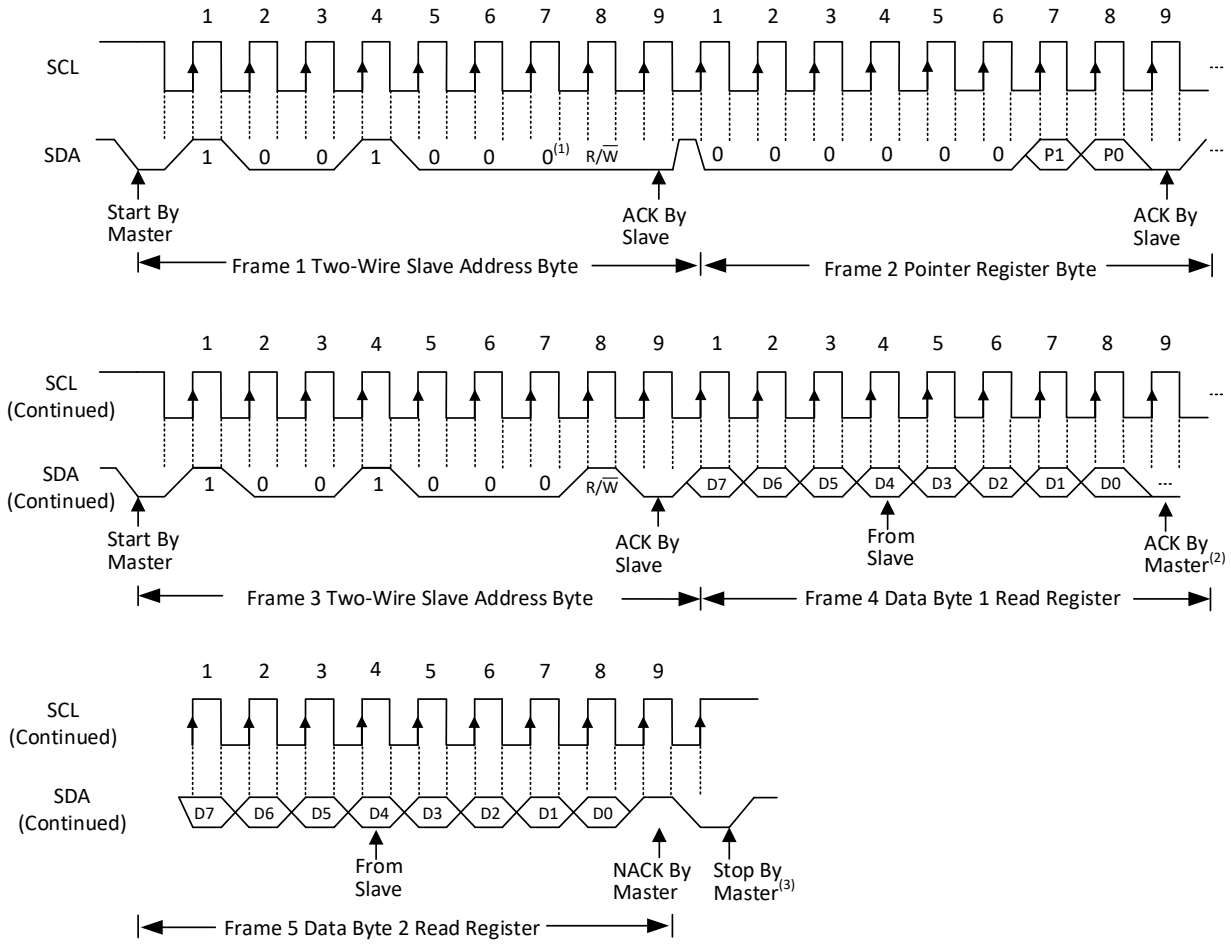
Data Transfer: The amount of data bytes transferred between START and STOP is controlled by the master and is unlimited. The receiver acknowledges the transfer of data.

Acknowledge: All addresses and data words are serially transmitted to and from the device in 8-bit words. The device sends a zero to acknowledge that it has received each word when the address is matched. This happens during the ninth clock cycle. The data transfer can be terminated by the host generating a not-acknowledge during the host receiving data.



(1) Slave address 1001000 is shown.

Figure 3.5 Two-Wire Timing Diagram for the NST118 Write Word Format



(1) Slave address 1001000 is shown.
(2) Master should leave SDA high to terminate a single-byte read operation.
(3) Master should leave SDA high to terminate a two-byte read operation.

Figure 3.6 Two-Wire Timing Diagram for Read Word Format

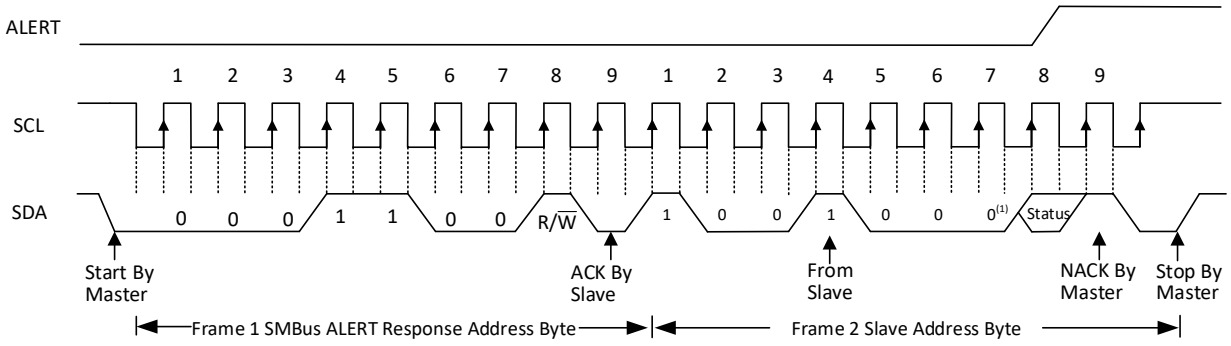


Figure 3.7 Timing Diagram for SMBus ALERT

4 On-Chip Registers

4.1 Pointer Register

The 8-bit Pointer Register is used to address a given data register, and the two LSBs of the Pointer Register determine which data register responds to a read or write operation by the master, Figure 4.1 shows the internal register structure of the NST118. Table 4.1 identifies the bits of the Pointer Register byte. Table 4.2 describes the Pointer Address of the Registers available in the NST118, P2 through P7 must always be 0 during the write command. The default value of Pointer Register P1/P0 after power on is "00", that is, the default state of the NST118 Pointer Register is the Temperature Register.

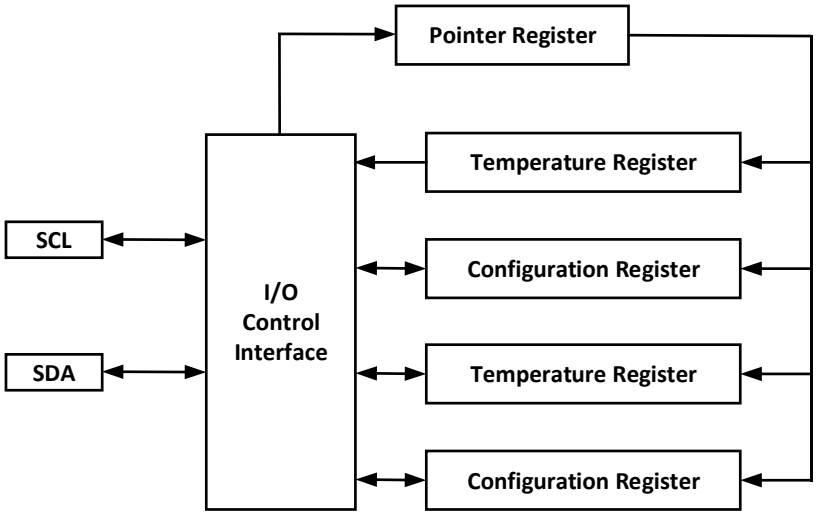


Figure 4.1 Internal Register Structure of the NST118

Table 4.1 Pointer Register Byte

P7	*P6*	*P5*	*P4*	*P3*	*P2*	*P1*	*P0*
0	0	0	0	0	0	Register bits	

Table 4.2 Pointer Register Description

BIT NO.	*Name*	*Description*
Bits 7:2	**NA**	P2 to P7 must always be 0 during the write command.
Bits 1:0	**Pointer[1:0]**	**00:** Temperature register (default) (R only) **01:** Configuration register (R/W) **10:** T_{LOW} register (R/W) **11:** T_{HIGH} register (R/W)

4.2 Temperature Register

The Configuration register of the NST118 can configure the sensor's Temperature Register format as a 12-bit (EM=0) or 13bit (EM=1).The Temperature Register storing the results of each completed temperature conversion, which consists of 2bytes in the format shown in Table 4.3, with MSB output first and followed by the LSB, and 12-bit (13-bit in extended mode) MSBs used to indicate the temperature value. One LSB equals 0.0625°C. Negative numbers are represented in binary twos complement format, data format for temperature is listed in Table 4.4. Following power-up or reset, the Temperature register reads 0°C until the first conversion is complete.

Table 4.3 Temperature Register

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	T11	T10	T9	T8	T7	T6	T5	T4
	(T12)	(T11)	(T10)	(T9)	(T8)	(T7)	(T6)	(T5)
2	T3	T2	T1	T0	0	0	0	0
	(T4)	(T3)	(T2)	(T1)	(T0)	(0)	(0)	(0)

Table 4.4 Temperature Data Format

TEMPERATURE(℃)	DIGITAL OUTPUT			
	12 bits format		13 bits format	
	BINARY	HEX	BINARY	HEX
150	0111 1111 1111 (0000)	7FF0	0100 1011 0000 0	4B00
128	0111 1111 1111 (0000)	7FF0	0100 0000 0000 0	4000
127.9375	0111 1111 1111 (0000)	7FF0	0011 1111 1111 1	3FF8
100	0110 0100 0000 (0000)	6400	0011 0010 0000 0	3200
85	0101 0101 0000 (0000)	5500	0010 1000 0000 0	2A80
50	0011 0010 0000 (0000)	3200	0001 1001 0000 0	1900
20	0001 0100 0000 (0000)	1400	0000 1100 1000 0	0A00
0.125	0000 0000 0010 (0000)	0020	0000 0000 0001 0	0010
0	0000 0000 0000 (0000)	0000	0000 0000 0000 0	0000
-0.125	1111 1111 1110 (0000)	FFE0	1111 1111 1111 0	FFF0
-20	1110 1100 0000 (0000)	EC00	1111 0110 0000 0	F600
-50	1100 1110 0000 (0000)	CE00	1110 0111 0000 0	E700

(1) Extended mode 13-bit configuration shown in parentheses.

4.3 Configuration Register

The configuration register of the NST118 is a 16-bit read/write register used to store the control bits that control the NST118 into different operation modes, and the read/write operation is executed with MSB priority. Table 4.5 lists the configuration register format, power-up and reset values. followed by a breakdown of the register bits, as shown in Table 4.6. All registers are updated byte by byte.

Table 4.5 Configuration and Power-Up/Reset Formats

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Name	OS	R1	R0	F1	F0	POL	TM	SD
Default	0	1	1	0	0	0	0	0
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Name	CR1	CR0	AL	EM	0	0	0	0
Default	1	0	1	0	0	0	0	0

Table 4.6 Configuration register Description

BIT NO.	*Name*	*Description*
Bit 15	**OS**	**0:** Continuous-Conversion Mode (default) **1:** One-shot Mode
Bits 14:13	**Converter Resolution [1:0]**	**00:** 9bit (0.5 °C) **01:** 10bit (0.25 °C) **10:** 11bit (0.125 °C) **11:** 12bit (0.0625 °C, default)
Bits 12:11	**Fault Queue [1:0]**	**00:** Consecutive faults are 1 (default) **01:** Consecutive faults are 2 **10:** Consecutive faults are 4 **11:** Consecutive faults are 6
Bit 10	**Polarity**	**0:** AL bit is active low (default) **1:** AL bit is active High
Bit 9	**Thermostat**	**0:** Comparison mode (default) **1:** Interrupt mode
Bit 8	**Shutdown**	**0:** Shutdown Mode (default) **1:** Continuous-Conversion Mode
Bits 7:6	**Conversion Rate**	**00:** 0.25 Hz **01:** 1 Hz **10:** 4 Hz (default) **11:** 8 Hz
Bit 5	**Alert**	Effective polarity depends on Bit10 **0:** ALERT **1:** NO ALERT (default)
Bit 4	**Extended**	**0:** Normal mode (default) **1:** Extended mode

4.4 High and Low Limit Registers

The temperature limit values in the T_{HIGH} and T_{LOW} registers have the same format as the temperature values in the temperature registers, and the result is used to compare with the limit to determine the status of the ALERT at the completion of each temperature conversion.

In **Comparator Mode** (TM=0), when the measured temperature data equals or exceeds the value of T_{HIGH} and the number of consecutive over-temperature data reaches the programmable queue setting (according to F1, F0), the alert pin is activated until the measured temperature falls below the value of T_{LOW} by the same number. In **Interrupt Mode** (TM=1), when the measured temperature data equals or exceeds the value of T_{HIGH} and the number of consecutive over-temperature data reaches the programmable queue setting (according to F1, F0) the alert pin is activated until the master issues a read operation to any register or the device successfully responds to the SMBus alert address. The alert pin is also cleared when the device is set to SD mode. When the alert pin is cleared, it will be activated again only when the temperature falls below T_{LOW} until the master issues a read operation to any register or the device successfully responds to the SMBus alert address. the above cycle will be repeated after the alert pin is cleared. The alert's active state can also be cleared by general call reset. At the same time, this operation will reset the device registers to the power-up state and the device returns to comparator mode.

Table 4.7, Table 4.8 describe the format for the T_{HIGH} and T_{LOW} registers. The MSB is sent first, followed by the LSB. Power-up reset values for T_{HIGH} and T_{LOW} are: T_{HIGH} = 80 °C and T_{LOW} = 75°C

The data format of T_{HIGH} and T_{LOW} registers is the same as that of the Temperature Register.

Table 4.7 Byte 1 and 2 of T_{HIGH} Register (1)

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	H11	H10	H9	H8	H7	H6	H5	H4
	(H12)	(H11)	(H10)	(H9)	(H8)	(H7)	(H6)	(H5)
2	H3	H2	H1	H0	0	0	0	0
	(H4)	(H3)	(H2)	(H1)	(H0)	(0)	(0)	(0)

Table 4.8 Byte 1 and 2 of T_{LOW} Register (2)

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	L11	L10	L9	L8	L7	L6	L5	L4
	(L12)	(L11)	(L10)	(L9)	(L8)	(L7)	(L6)	(L5)
2	L3	L2	L1	L0	0	0	0	0
	(L4)	(L3)	(L2)	(L1)	(L0)	(0)	(0)	(0)

(1) Extended mode 13-bit configuration shown in parenthesis

(2) Extended mode 13-bit configuration shown in parenthesis

The T_{HIGH} and T_{LOW} register data format are the same as the temperature register. At any resolution, the T_{HIGH}, T_{LOW} register values are used to compare with the temperature test value to determine the function of the ALERT.

5 Application

5.1 Typical Application

No external components are required to operate the NST118 other than pull-up resistors on SCL, SDA and ALERT, a bypass capacitor of 0.01μF is recommended. the sensing device for the NST118 device is the device itself. The thermal path is through the package leads as well as the plastic package. The low thermal resistance of the metal results in the leads providing the primary thermal path. The typical application of NST118 is shown in Figure 5.1.

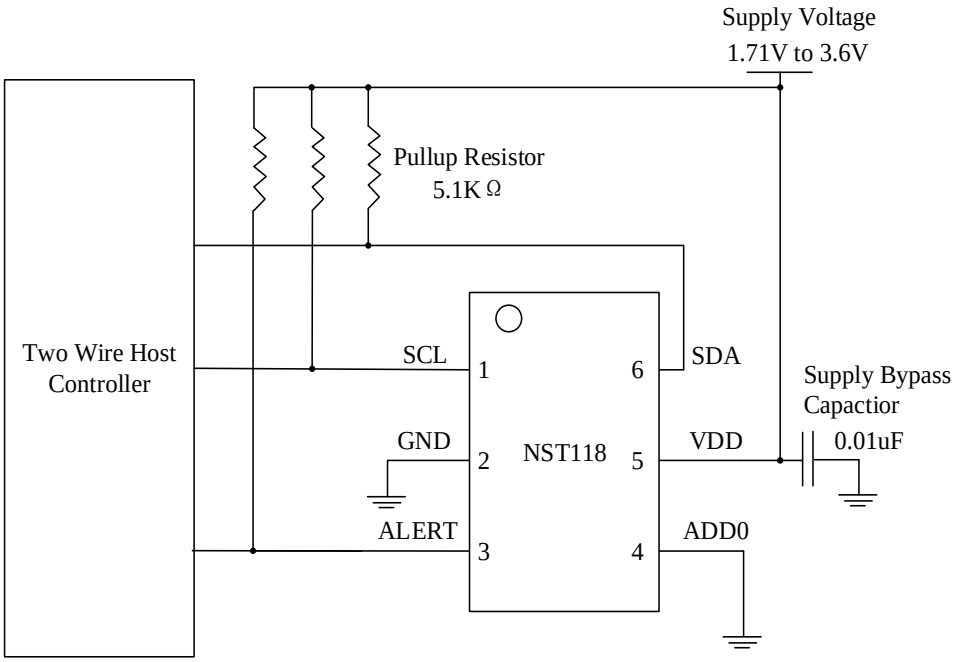
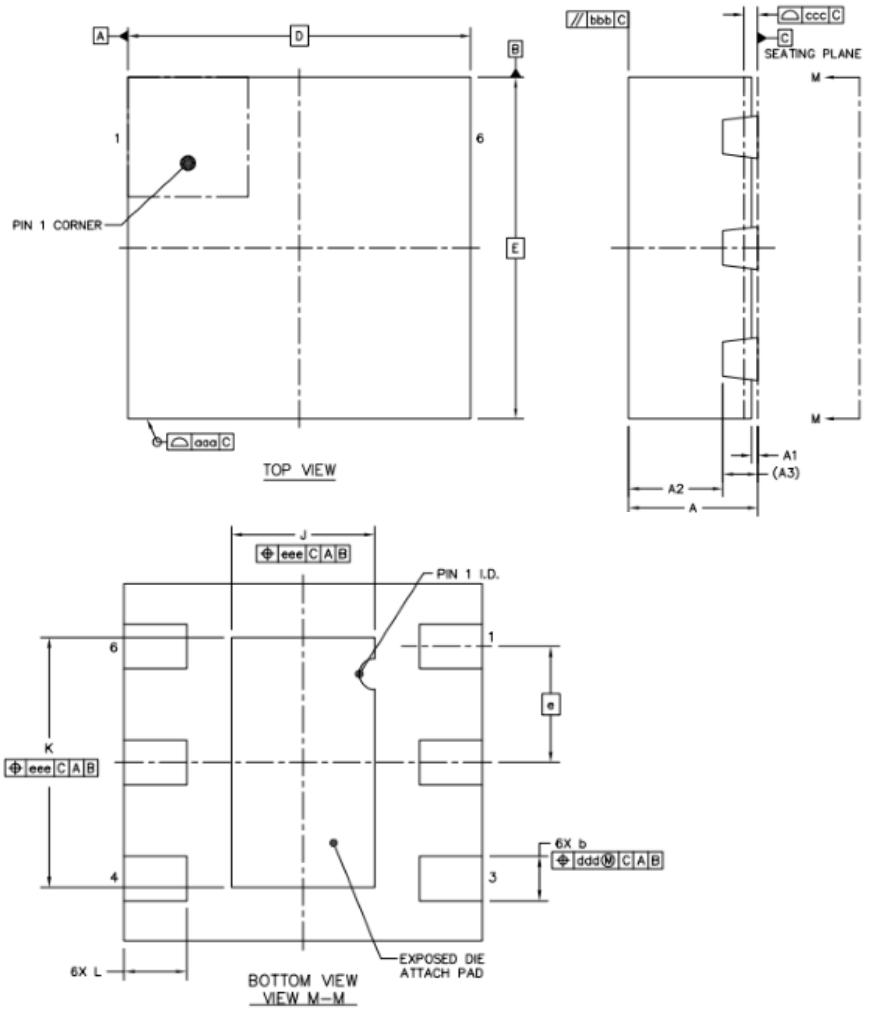


Figure 5.1. Typical Connections of the NST118

6 Package Information

6.1Package

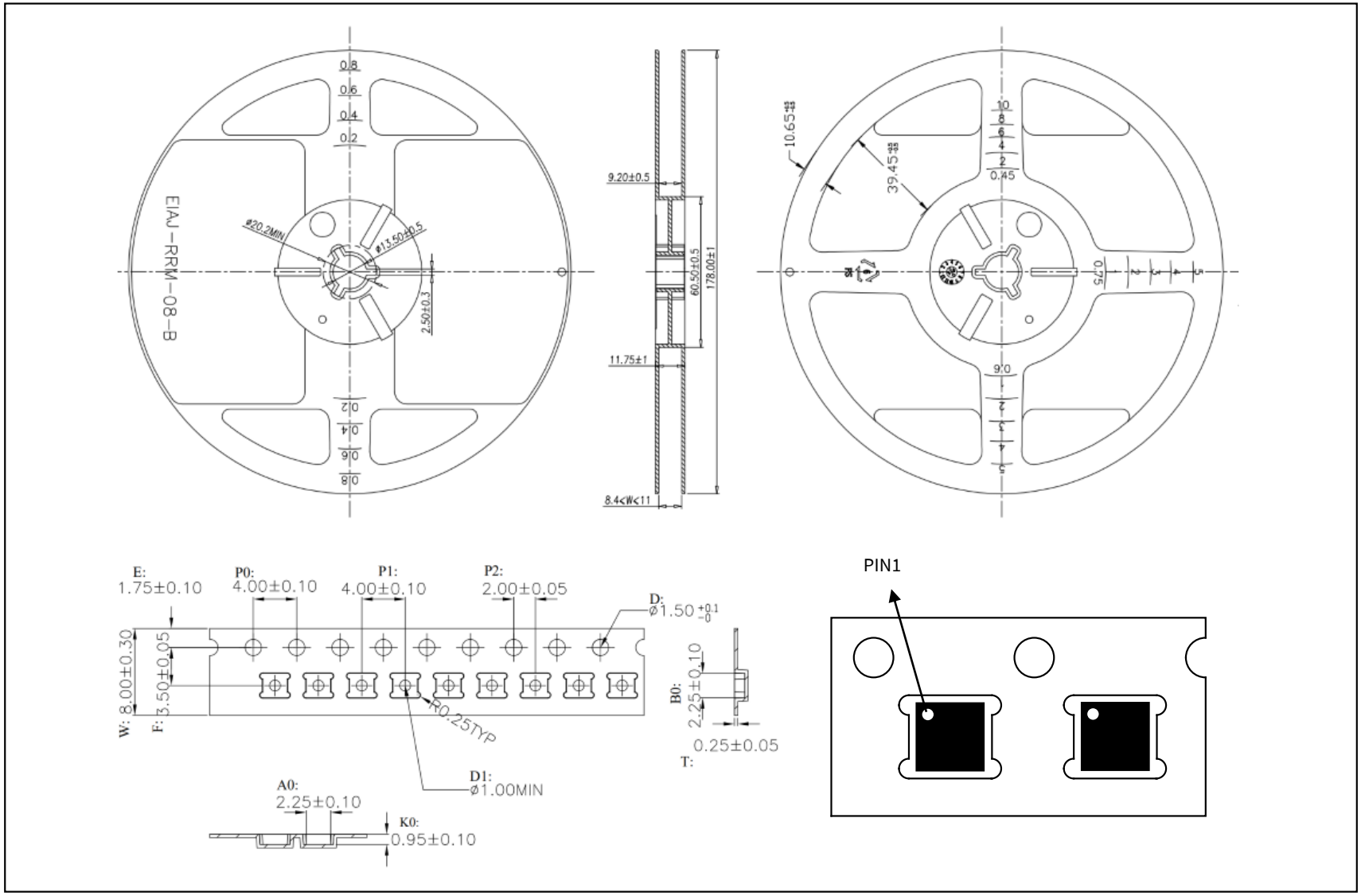


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	-	0.55	-
L/F THICKNESS		A3	0.203 REF		
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D	2 BSC		
	Y	E	2 BSC		
LEAD PITCH		e	0.65 BSC		
EP SIZE	X	J	0.7	0.8	0.9
	Y	K	1.3	1.4	1.5
LEAD LENGTH		L	0.3	0.35	0.4
PACKAGE EDGE TOLERANCE		aaa	0.1		
MOLD FLATNESS		bbb	0.1		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.1		
EXPOSED PAD OFFSET		eee	0.1		

NOTES
1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

DFN (6) Package Shape and Dimension in millimeters and inches

6.2 Tape and Reel Information



Tape and Reel Information of DFN (6)

7 Order Information

Type	*MSL*	*Unit*	Marking (1, 2)	*Description*
NST118-CDNR	3	3000ea/Reel	T118	DFN(6) package, Reel
NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures (Reflow profile: J-STD-020E).				

(1) The marking relates to the logo information.

(2) If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

8 Revision History

Revision	*Description*	*Date*
1.0	Release Version	2021/7/29
1.1	Change Supply voltage Range; Optimize text presentation	2022/02/23
1.2	Revise Electrical Characteristics. Revise Function Description. Modify some descriptions.	2022/08/26

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