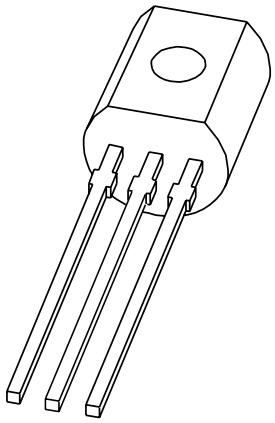
DATA SHEET



BSR52
NPN Darlington transistor

Product data sheet
Supersedes data of 1999 Apr 26

2004 Nov 11

NPN Darlington transistor BSR52

FEATURES

- High current (max. 1 A)
- Low voltage (max. 80 V)
- Integrated diode and resistor.

APPLICATIONS

- Industrial high gain amplification.

DESCRIPTION

NPN Darlington transistor in a TO-92; SOT54 plastic package. PNP complement: BSR62.

PINNING

PIN	DESCRIPTION
1	base
2	collector
3	emitter

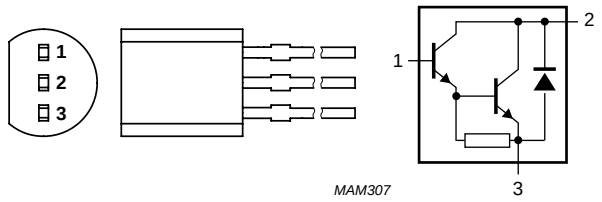


Fig.1 Simplified outline (TO-92; SOT54) and symbol.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
BSR52	SC-43A	plastic single-ended leaded (through hole) package; 3 leads	SOT54

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	90	V
V_{CES}	collector-emitter voltage	V_{BE} = 0 V	–	80	V
V_{EBO}	emitter-base voltage	open collector	–	5	V
I_C	collector current (DC)		–	1	A
I_{CM}	peak collector current		–	2	A
I_B	base current (DC)		–	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	–	830	mW
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	ambient temperature		−65	+150	°C

Note

1. Transistor mounted on an FR4 printed-circuit board.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	note 1	150	K/W

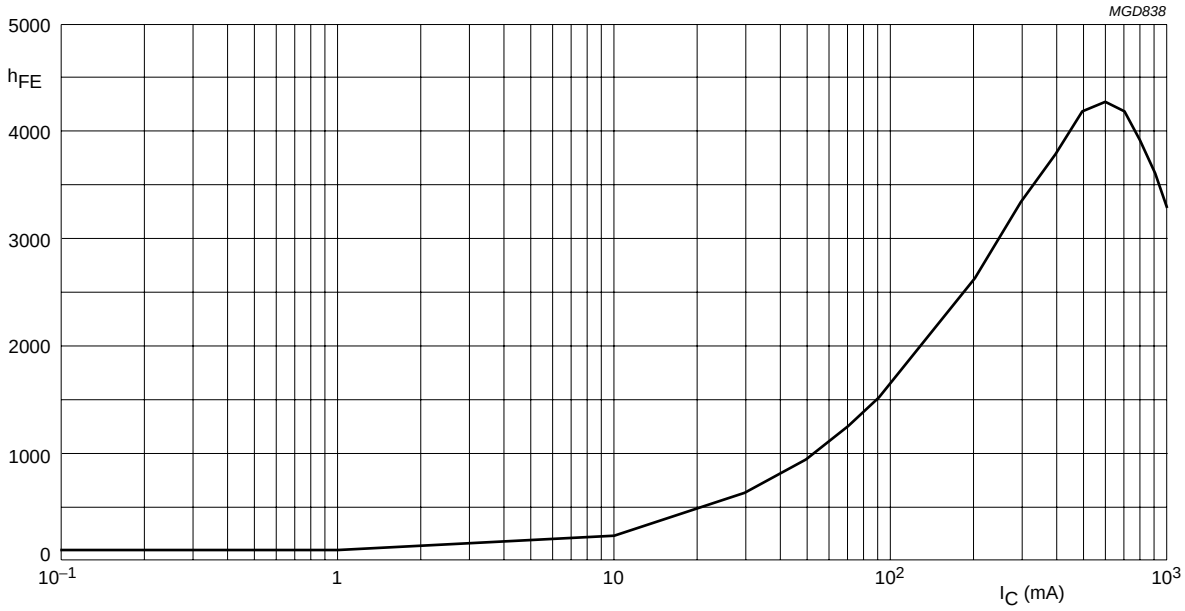
Note

1. Transistor mounted on an FR4 printed-circuit board.

CHARACTERISTICS

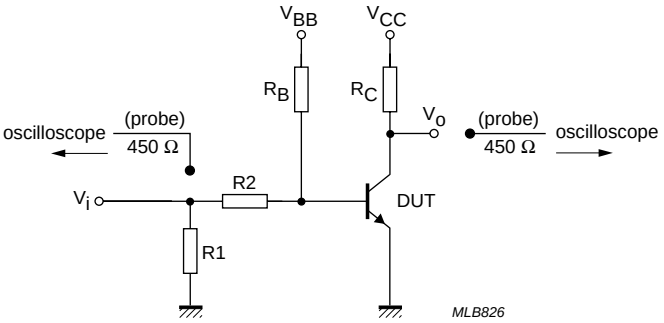
T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CES}	collector-base cut-off current	V_{BE} = 0 V; V_{CE} = 80 V	–	–	50	nA
I_{EBO}	emitter-base cut-off current	V_{EB} = 4 V; I_C = 0 A	–	–	50	nA
h_{FE}	DC current gain	V_{CE} = 10 V; see Fig.2				
		I_C = 150 mA	1000	–	–	
		I_C = 500 mA	2000	–	–	
V_{CEsat}	collector-emitter saturation voltage	I_C = 0.5 A; I_B = 0.5 mA	–	–	1.3	V
		I_C = 1 A; I_B = 4 mA	–	–	1.6	V
V_{BEsat}	base-emitter saturation voltage	I_C = 0.5 A; I_B = 0.5 mA	–	–	1.9	V
		I_C = 1 A; I_B = 4 mA	–	–	2.2	V
f_T	transition frequency	V_{CE} = 5 V; I_C = 500 mA; f = 100 MHz	–	200	–	MHz
Switching times (between 10% and 90% levels); see Fig.3						
t_{on}	turn-on time	I_{Con} = 500 mA; I_{Bon} = 0.5 mA; I_{Boff} = −0.5 mA	–	–	500	ns
t_{off}	turn-off time		–	–	1300	ns



V_{CE} = 10 V.

Fig.2 DC current gain; typical values.

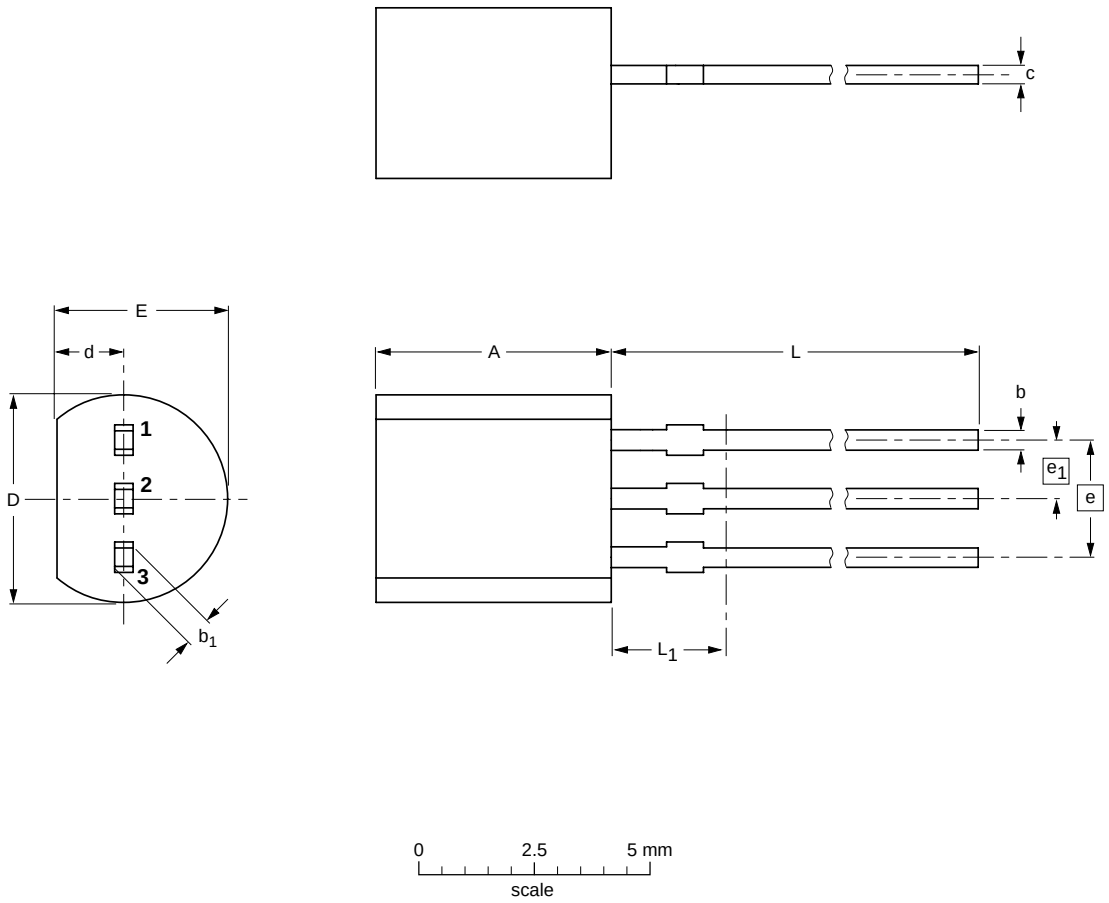


V_i = 10 V; T = 200 μs; t_p = 6 μs; t_r = t_f ≤ 3 ns.
R1 = 56 Ω; R2 = 10 kΩ; R_B = 10 kΩ; R_C = 18 Ω.
V_{BB} = −1.8 V; V_{CC} = 10.7 V.
Oscilloscope: input impedance Z_i = 50 Ω.

Fig.3 Test circuit for switching times.

PACKAGE OUTLINE

Plastic single-ended leaded (through hole) package; 3 leads **SOT54**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b_1	c	D	d	E	e	e_1	L	L_1 (1) max.
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT54		TO-92	SC-43A			~~04-06-28~~ 04-11-16