Digital FET, N-Channel

FDV301N, FDV301N-F169

General Description

This N−Channel logic level enhancement mode field effect transistor is produced using **onsemi's** proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on−state resistance. This device has been designed especially for low voltage applications as a replacement for digital transistors. Since bias resistors are not required, this one N−channel FET can replace several different digital transistors, with different bias resistor values.

Features

- 25 V, 0.22 A Continuous, 0.5 A Peak
  - $R_{DS(on)}$ = 5 Ω @ V_{GS} = 2.7 V
  - $R_{DS(on)}$ = 4 Ω @ V_{GS} = 4.5 V
- Very Low Level Gate Drive Requirements Allowing Direct Operation in 3 V Circuits. $V_{GS(th)}$ < 1.06 V
- Gate−Source Zener for ESD Ruggedness. > 6 kV Human Body Model
- Replace Multiple NPN Digital Transistors with One DMOS FET
- This Device is Pb−Free and Halide Free

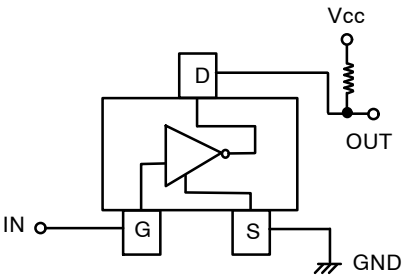
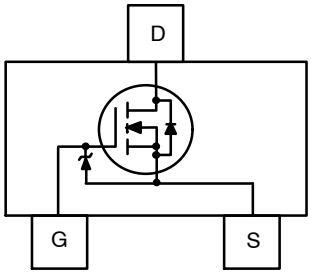
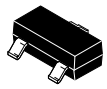


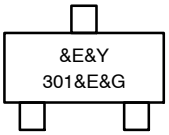
Figure 1. Inverter Application





SOT−23
CASE 318−08

MARKING DIAGRAM



&E	= Designates Space
&Y	= Binary Calendar Year Coding Scheme
301	= Specific Device Code
&G	= Date Code

ORDERING INFORMATION

Device	Package	Shipping†
FDV301N, FDV301N−F169	SOT−23−3 (Pb−Free, Halide−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise noted.

Symbol	Parameter	FDV301N	Unit
V_{DSS}, V_{CC}	Drain−Source Voltage, Power Supply Voltage	25	V
V_{GSS}, V_I	Gate−Source Voltage, V_{IN}	8	V
I_D, I_O	Drain/Output Current − Continuous	0.22	A
		0.5	
P_D	Maximum Power Dissipation	0.35	W
T_J, T_{STG}	Operating and Storage Temperature Range	−55 to 150	°C
ESD	Electrostatic Discharge Rating MIL−STD−883D Human Body Model (100 pF/1500 Ω)	6.0	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS T_A = 25°C unless otherwise noted.

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient	357	°C/W

INVERTER ELECTRICAL CHARACTERISTICS T_A = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$I_{O(off)}$	Zero Input Voltage Output Current	V_{CC} = 20 V, V_I = 0 V	−	−	1	μA
$V_{I(off)}$	Input Voltage	V_{CC} = 5 V, I_O = 10 μA	−	−	0.5	V
$V_{I(on)}$		V_O = 0.3 V, I_O = 0.005 A	1	−	−	
$R_{O(on)}$	Output to Ground Resistance	V_I = 2.7 V, I_O = 0.2 A	−	4	5	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ELECTRICAL CHARACTERISTICS T_A = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain−Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	25	−	−	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	I_D = 250 μA, Referenced to 25°C	−	25	−	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 20 V, V_{GS} = 0 V	−	−	1	μA
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 55°C	−	−	10	
I_{GSS}	Gate − Body Leakage Current	V_{GS} = 8 V, V_{DS} = 0 V	−	−	100	nA
ON CHARACTERISTICS						
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp. Coefficient	I_D = 250 μA, Referenced to 25°C	−	−2.1	−	mV/°C
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	0.70	0.85	1.06	V
$R_{DS(on)}$	Static Drain−Source On−Resistance	V_{GS} = 2.7 V, I_D = 0.2 A	−	3.8	5	Ω
		V_{GS} = 2.7 V, I_D = 0.2 A, T_J = 125°C	−	6.3	9	
		V_{GS} = 4.5 V, I_D = 0.4 A	−	3.1	4	
$I_{D(on)}$	On−State Drain Current	V_{GS} = 2.7 V, V_{DS} = 5 V	0.2	−	−	A
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 0.4 A	−	0.2	−	S

ELECTRICAL CHARACTERISTICS T_A = 25°C unless otherwise noted. (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz	–	9.5	–	pF
C_{oss}	Output Capacitance		–	6	–	
C_{rss}	Reverse Transfer Capacitance		–	1.3	–	
SWITCHING CHARACTERISTICS (Note 1)						
$t_{D(on)}$	Turn − On Delay Time	V_{DD} = 6 V, I_D = 0.5 A, V_{GS} = 4.5 V, R_{GEN} = 50 Ω	–	3.2	8	ns
t_r	Turn − On Rise Time		–	6	15	
$t_{D(off)}$	Turn − Off Delay Time		–	3.5	8	
t_f	Turn − Off Fall Time		–	3.5	8	
Q_g	Total Gate Charge	V_{DS} = 5 V, I_D = 0.2 A, V_{GS} = 4.5 V	–	0.49	0.7	nC
Q_{gs}	Gate−Source Charge		–	0.22	–	
Q_{gd}	Gate−Drain Charge		–	0.07	–	
DRAIN−SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain−Source Diode Forward Current		–	–	0.29	A
V_{SD}	Drain−Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 0.29 A (Note 1)	–	0.8	1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL CHARACTERISTICS

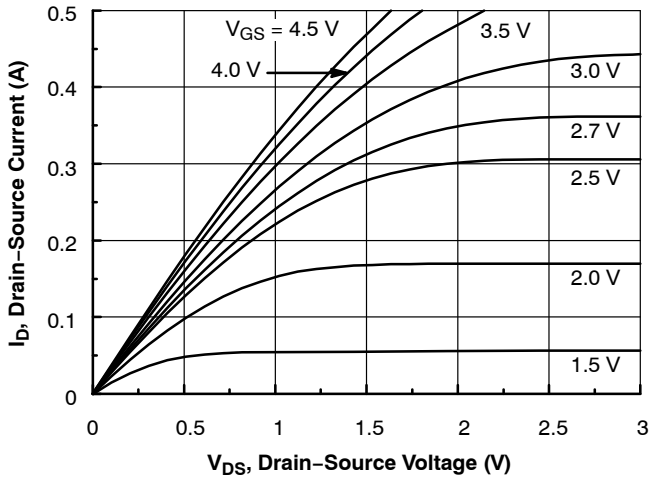


Figure 2. On−Region Characteristics

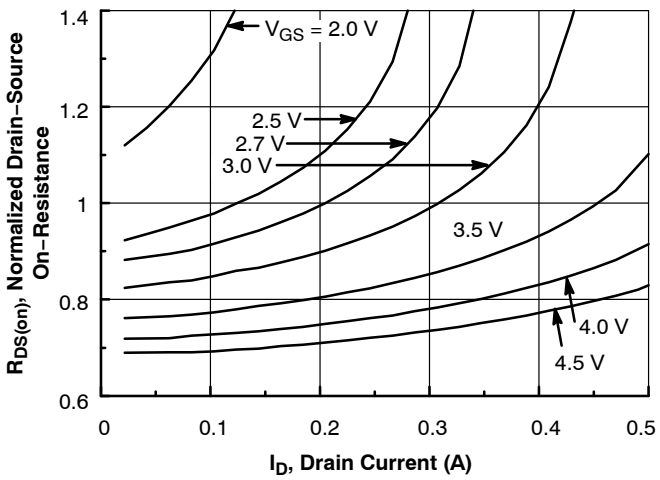


Figure 3. On−Resistance Variation with Drain Current and Gate Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

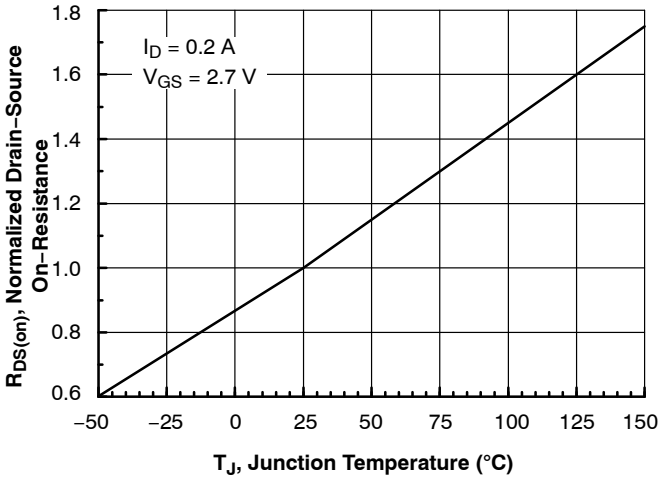


Figure 4. On−Resistance Variation with Temperature

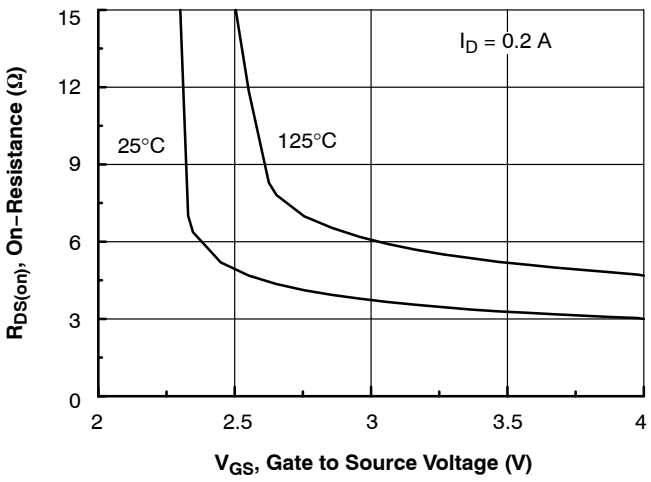


Figure 5. On Resistance Variation with Gate−To−Source Voltage

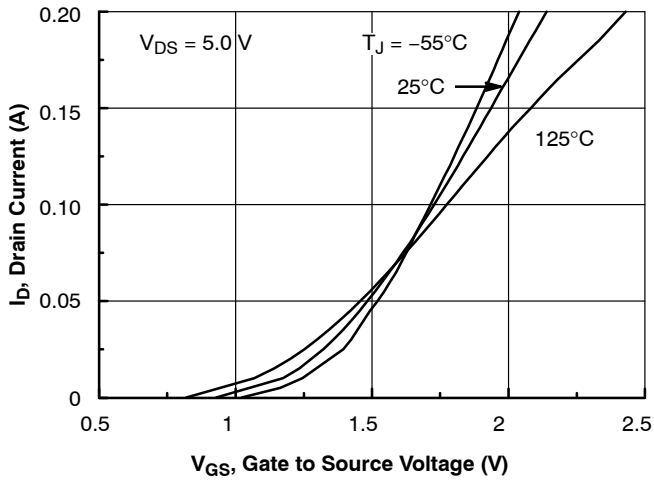


Figure 6. Transfer Characteristics

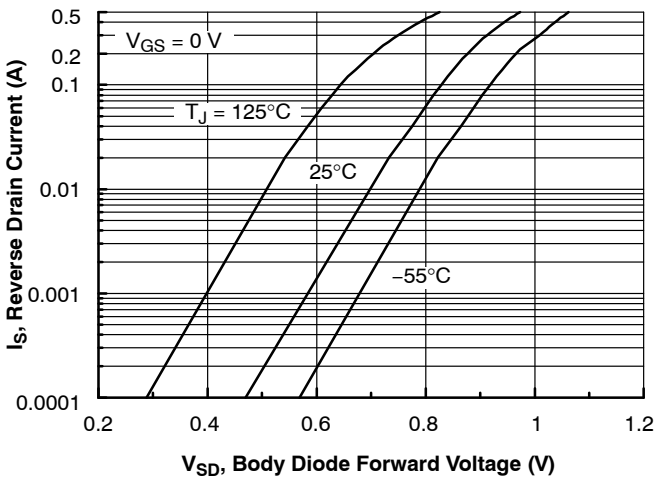


Figure 7. Body Diode Forward Voltage Variation with Source Current and Temperature

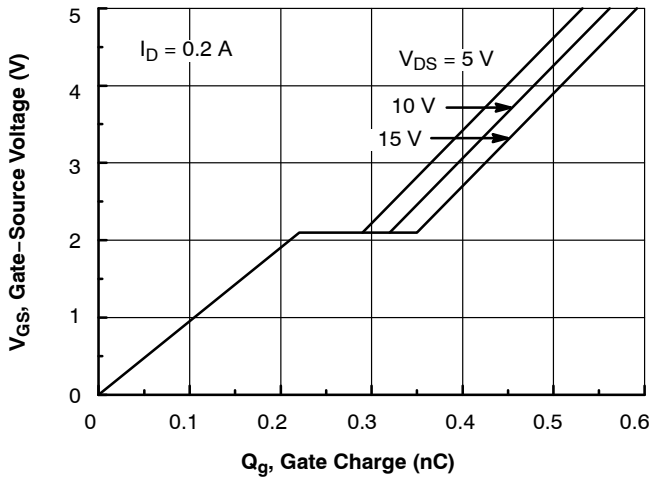


Figure 8. Gate Charge Characteristics

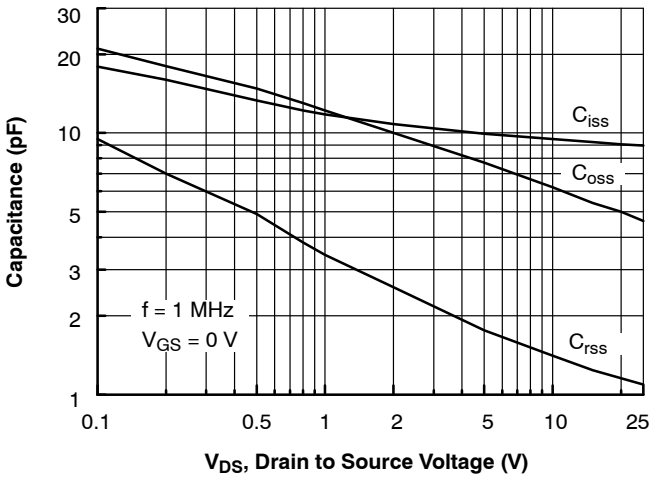


Figure 9. Capacitance Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

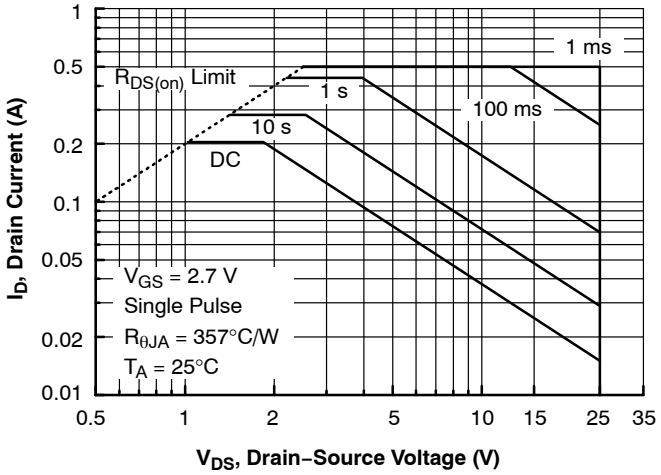


Figure 10. Maximum Safe Operating Area

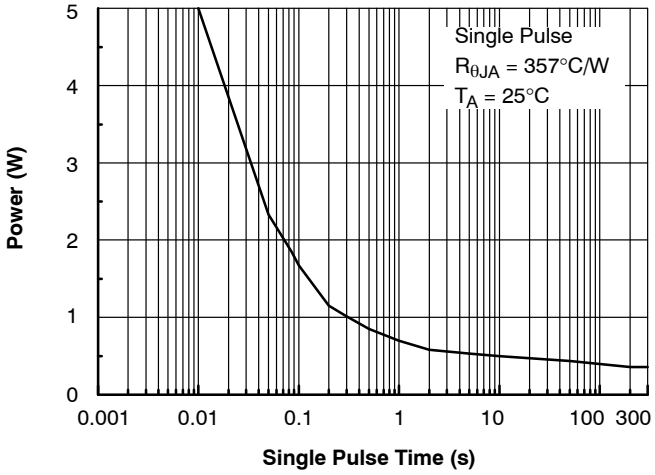


Figure 11. Single Pulse Maximum Power Dissipation

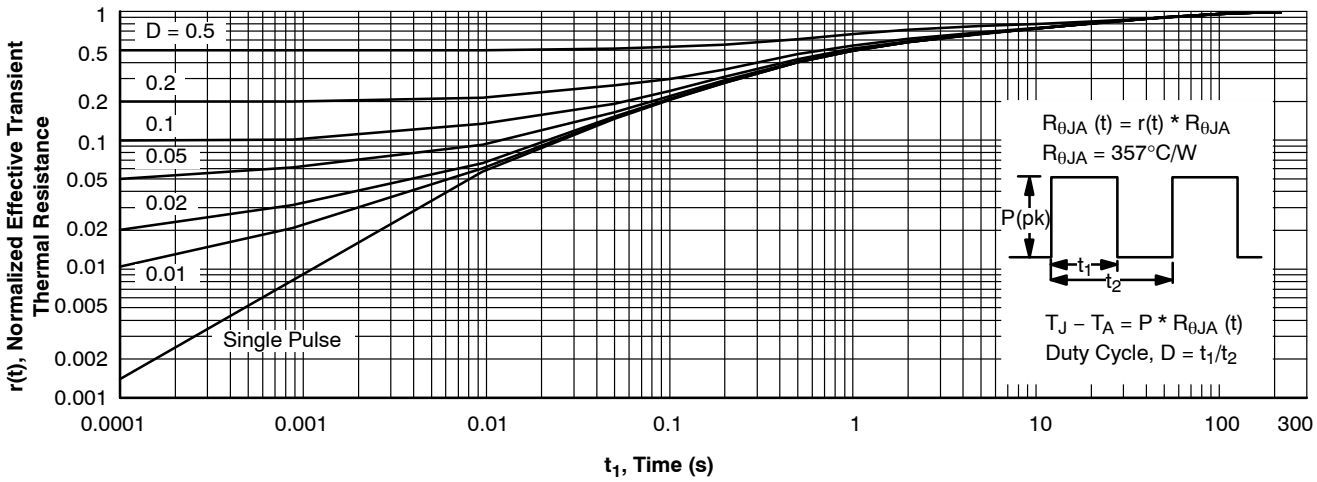
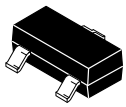


Figure 12. Transient Thermal Response Curve

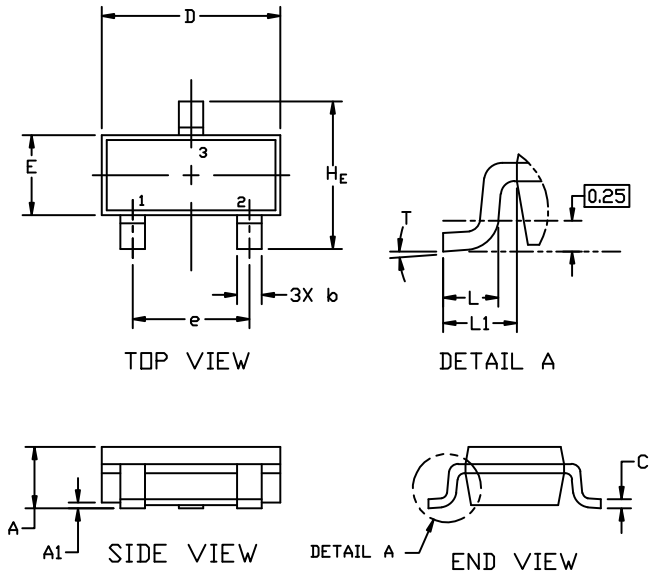
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



SCALE 4:1

SOT−23 (TO−236)
CASE 318
ISSUE AT

DATE 01 MAR 2023

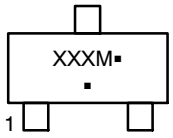


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

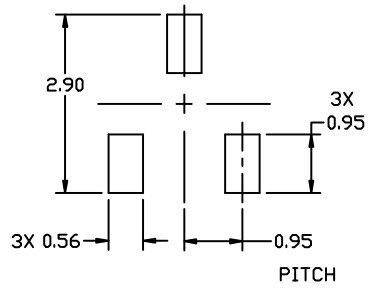
	MILLIMETERS			INCHES		
DIM	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H_E	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	---	10°	0°	---	10°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42226B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SOT−23 (TO−236)**		**PAGE 1 OF 2**

SOT−23 (TO−236)
CASE 318
ISSUE AT

DATE 01 MAR 2023

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE

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For additional information, please contact your local Sales Representative

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