

# MJD44H11 (NPN) MJD45H11 (PNP)

Preferred Device

## Complementary Power Transistors

### DPAK For Surface Mount Applications

Designed for general purpose power and switching such as output or driver stages in applications such as switching regulators, converters, and power amplifiers.

#### Features

- Lead Formed for Surface Mount Application in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves (“-1” Suffix)
- Electrically Similar to Popular D44H/D45H Series
- Low Collector Emitter Saturation Voltage –  
 $V_{CE(sat)} = 1.0$  Volt Max @ 8.0 Amperes
- Fast Switching Speeds
- Complementary Pairs Simplifies Designs
- Epoxy Meets UL 94 V-0 @ 0.125 in
- ESD Ratings: Human Body Model, 3B > 8000 V  
Machine Model, C > 400 V
- Pb-Free Packages are Available

#### MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	$V_{CEO}$	80	Vdc
Emitter-Base Voltage	$V_{EB}$	5	Vdc
Collector Current – Continuous – Peak	$I_C$	8 16	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	20 0.16	W W/ $^\circ\text{C}$
Total Power Dissipation (Note 1) @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	1.75 0.014	W W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

#### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	6.25	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient (Note 1)	$R_{\theta JA}$	71.4	$^\circ\text{C/W}$
Lead Temperature for Soldering	$T_L$	260	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

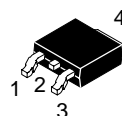


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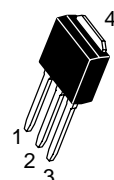
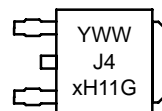
<http://onsemi.com>

### SILICON POWER TRANSISTORS 8 AMPERES 80 VOLTS, 20 WATTS

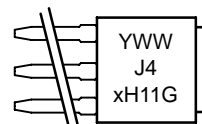
#### MARKING DIAGRAMS



DPAK  
CASE 369C  
STYLE 1



DPAK-3  
CASE 369D  
STYLE 1



Y = Year  
WW = Work Week  
J4xH11 = Device Code  
x = 4 or 5  
G = Pb-Free Package

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

## MJD44H11 (NPN) MJD45H11 (PNP)

### ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector–Emitter Sustaining Voltage (I <sub>C</sub> = 30 mA, I <sub>B</sub> = 0)	V <sub>CEO(sus)</sub>	80	–	–	Vdc
Collector Cutoff Current (V <sub>CE</sub> = Rated V <sub>CEO</sub> , V <sub>BE</sub> = 0)	I <sub>CES</sub>	–	–	10	μA
Emitter Cutoff Current (V <sub>EB</sub> = 5 Vdc)	I <sub>EBO</sub>	–	–	50	μA
<b>ON CHARACTERISTICS</b>					
Collector–Emitter Saturation Voltage (I <sub>C</sub> = 8 Adc, I <sub>B</sub> = 0.4 Adc)	V <sub>CE(sat)</sub>	–	–	1	Vdc
Base–Emitter Saturation Voltage (I <sub>C</sub> = 8 Adc, I <sub>B</sub> = 0.8 Adc)	V <sub>BE(sat)</sub>	–	–	1.5	Vdc
DC Current Gain (V <sub>CE</sub> = 1 Vdc, I <sub>C</sub> = 2 Adc)	h <sub>FE</sub>	60	–	–	–
DC Current Gain (V <sub>CE</sub> = 1 Vdc, I <sub>C</sub> = 4 Adc)		40	–	–	–
<b>DYNAMIC CHARACTERISTICS</b>					
Collector Capacitance (V <sub>CB</sub> = 10 Vdc, f <sub>test</sub> = 1 MHz)	C <sub>cb</sub>	–	130 230	–	pF
Gain Bandwidth Product (I <sub>C</sub> = 0.5 Adc, V <sub>CE</sub> = 10 Vdc, f = 20 MHz)	f <sub>T</sub>	–	50 40	–	MHz
<b>SWITCHING TIMES</b>					
Delay and Rise Times (I <sub>C</sub> = 5 Adc, I <sub>B1</sub> = 0.5 Adc)	t <sub>d</sub> + t <sub>r</sub>	–	300 135	–	ns
Storage Time (I <sub>C</sub> = 5 Adc, I <sub>B1</sub> = I <sub>B2</sub> = 0.5 Adc)	t <sub>s</sub>	–	500 500	–	ns
Fall Time (I <sub>C</sub> = 5 Adc, I <sub>B1</sub> = I <sub>B2</sub> = 0.5 Adc)	t <sub>f</sub>	–	140 100	–	ns

## MJD44H11 (NPN) MJD45H11 (PNP)

### ORDERING INFORMATION

Device	Package Type	Package	Shipping†	
MJD44H11	DPAK	369C	75 Units / Rail	
MJD44H11G	DPAK (Pb-Free)			
MJD44H11-001	DPAK-3	369D		
MJD44H11-001G	DPAK-3 (Pb-Free)			
MJD44H11RL	DPAK	369C	1800 Tape & Reel	
MJD44H11RLG	DPAK (Pb-Free)		2500 Tape & Reel	
MJD44H11T4	DPAK			
MJD44H11T4G	DPAK (Pb-Free)			
MJD44H11T5	DPAK			
MJD44H11T5G	DPAK (Pb-Free)			
MJD45H11	DPAK		75 Units / Rail	
MJD45H11G	DPAK (Pb-Free)			
MJD45H11-001	DPAK-3			369D
MJD45H11-001G	DPAK-3 (Pb-Free)			
MJD45H11RL	DPAK	369C	1800 Tape & Reel	
MJD45H11RLG	DPAK (Pb-Free)		2500 Tape & Reel	
MJD45H11T4	DPAK			
MJD45H11T4G	DPAK (Pb-Free)			

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MJD44H11 (NPN) MJD45H11 (PNP)

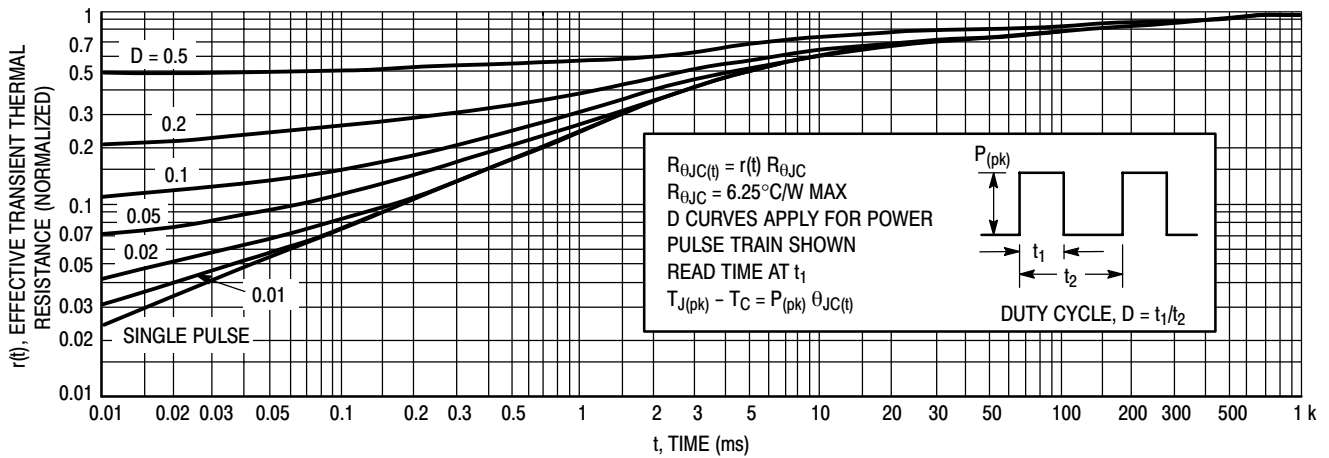


Figure 1. Thermal Response

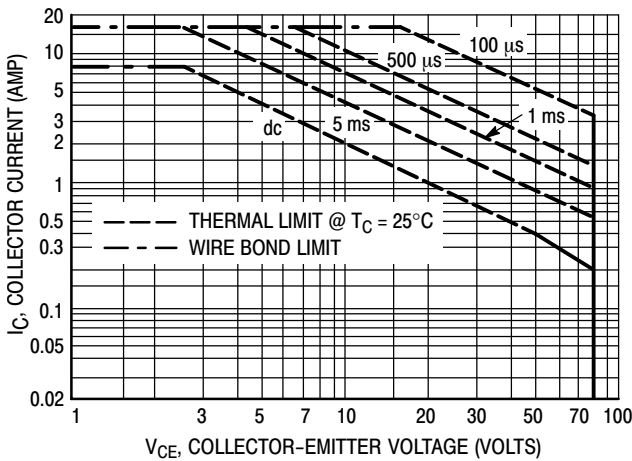


Figure 2. Maximum Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on  $T_{J(pk)} = 150^{\circ}\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^{\circ}\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 1. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

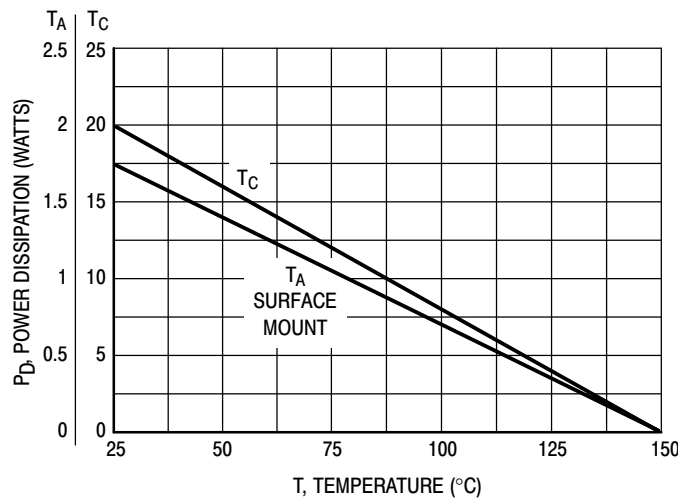


Figure 3. Power Derating

# MJD44H11 (NPN) MJD45H11 (PNP)

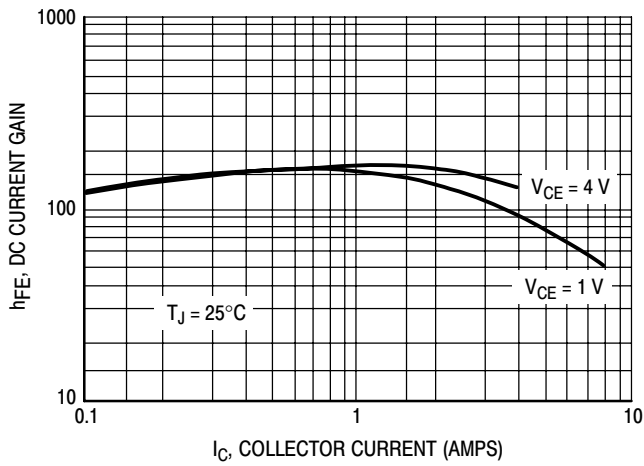


Figure 4. MJD44H11 DC Current Gain

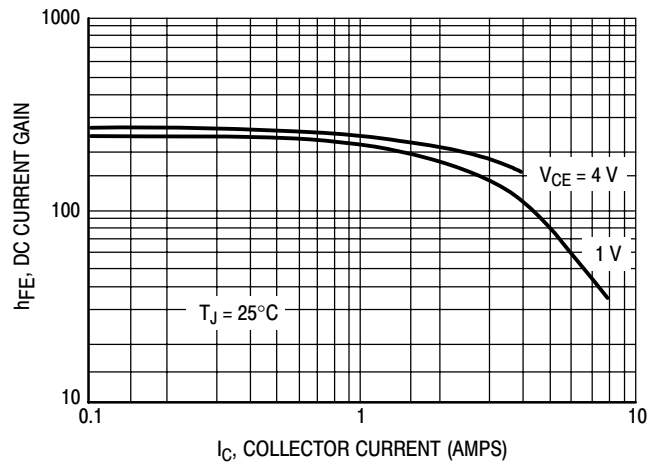


Figure 5. MJD45H11 DC Current Gain

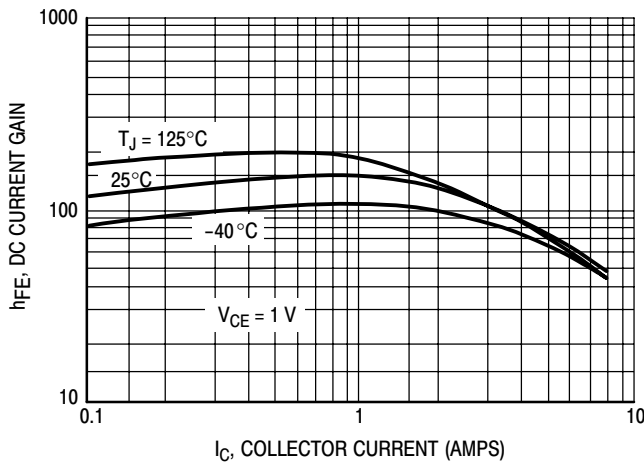


Figure 6. MJD44H11 Current Gain versus Temperature

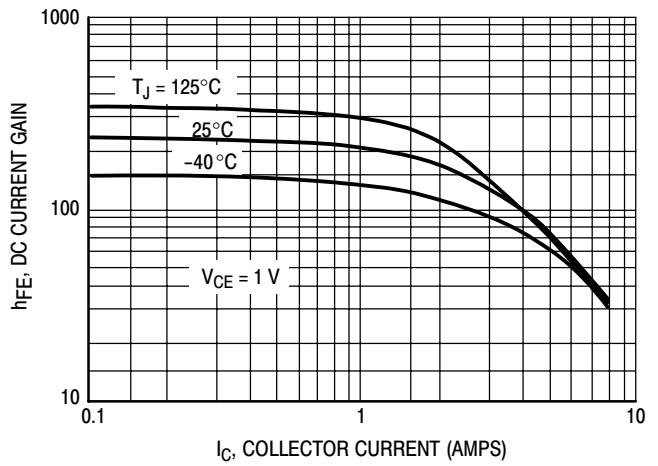


Figure 7. MJD45H11 Current Gain versus Temperature

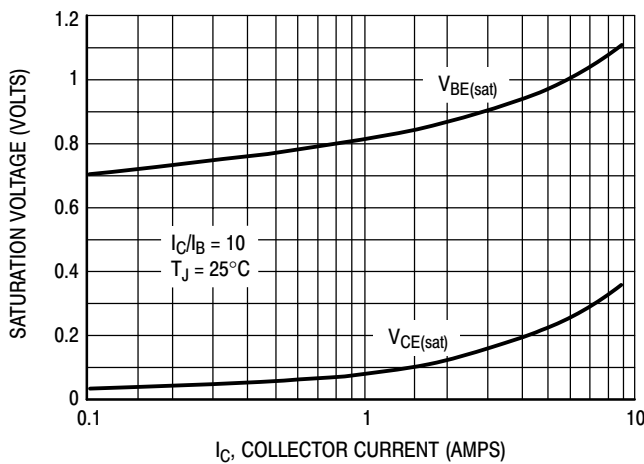


Figure 8. MJD44H11 On-Voltages

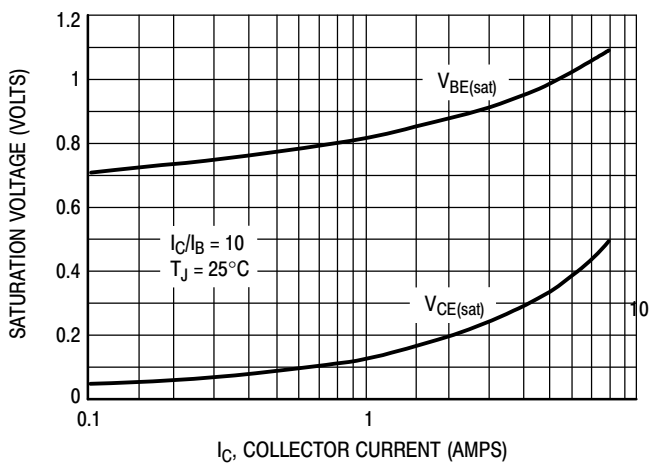
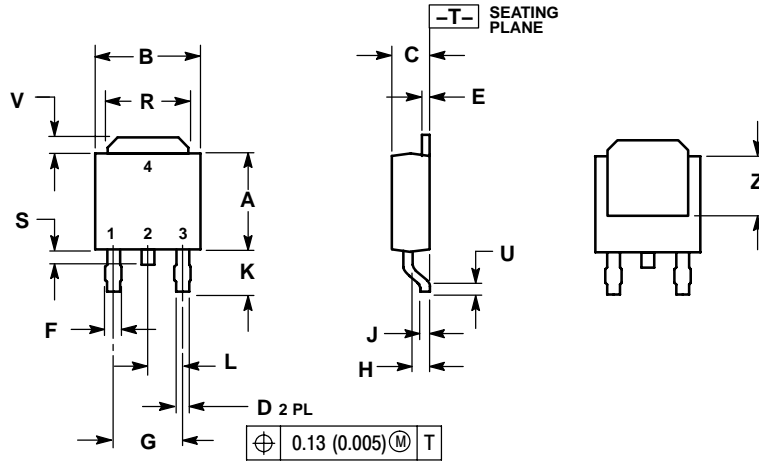


Figure 9. MJD45H11 On-Voltages

# MJD44H11 (NPN) MJD45H11 (PNP)

## PACKAGE DIMENSIONS

**DPAK**  
CASE 369C  
ISSUE O

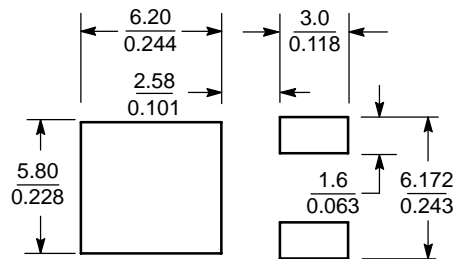


- NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

- STYLE 1:  
PIN 1. BASE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR

### SOLDERING FOOTPRINT\*



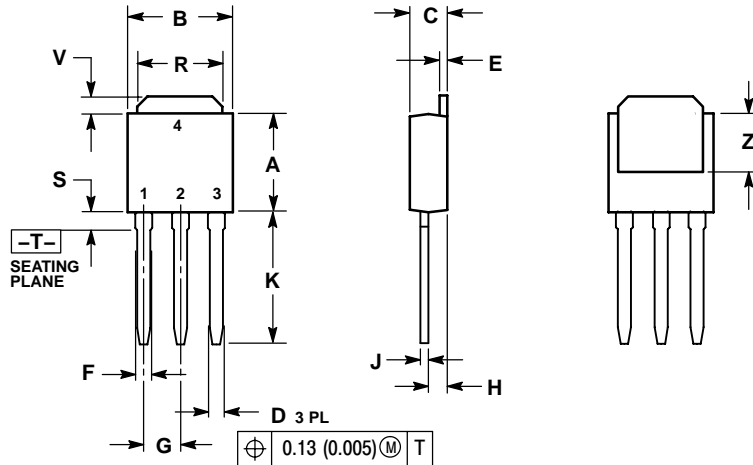
SCALE 3:1  $\left(\frac{\text{mm}}{\text{inches}}\right)$

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MJD44H11 (NPN) MJD45H11 (PNP)

## PACKAGE DIMENSIONS

DKPAK-3  
CASE 369D-01  
ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 1:

- PIN 1. BASE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR

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