

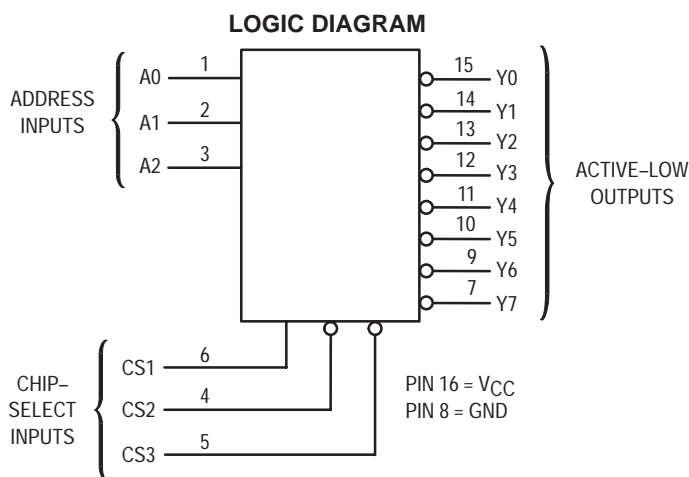
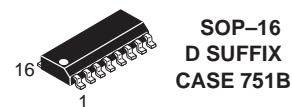
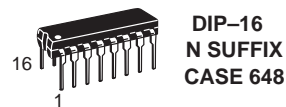
# 1-of-8 Decoder/ Demultiplexer

## High-Performance Silicon-Gate CMOS

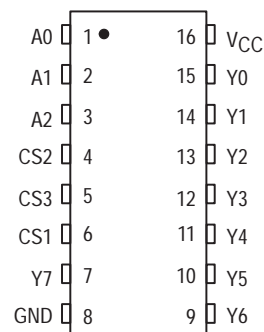
The 74HC138 is identical in pinout to the LS138. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC138A decodes a three-bit Address to one-of-eight active-low outputs. This device features three Chip Select inputs, two active-low and one active-high to facilitate the demultiplexing, cascading, and chip-selecting functions. The demultiplexing function is accomplished by using the Address inputs to select the desired device output; one of the Chip Selects is used as a data input while the other Chip Selects are held in their active states.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 100 FETs or 29 Equivalent Gates



### PIN ASSIGNMENT



### FUNCTION TABLE

Inputs			Outputs										
CS1	CS2	CS3	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	L	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	H	H	H	H	H	L	H	H	H
H	L	L	H	H	L	H	H	H	H	H	L	H	H
H	L	L	H	H	H	H	H	H	H	H	H	L	H

H = high level (steady state); L = low level (steady state); X = don't care

### ORDERING INFORMATION

Device	Package	Shipping
74HC138N	DIP-16	2000 / Box
74HC138M/TR	SOP-16	2500 / Reel

**MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	- 0.5 to V <sub>CC</sub> + 0.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	- 0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	± 20	mA
I <sub>out</sub>	DC Output Current, per Pin	± 25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package)	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C

SOIC Package: - 7 mW/°C from 65° to 125°C

TSSOP Package: - 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 2)	V <sub>CC</sub> = 2.0 V 0 V <sub>CC</sub> = 4.5 V 0 V <sub>CC</sub> = 6.0 V 0	1000 500 400	ns

**DC ELECTRICAL CHARACTERISTICS** (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				-55°C to 25°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			3.0	2.1	2.1	2.1	
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.5	0.5	0.5	V
			3.0	0.9	0.9	0.9	
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 2.4 mA  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	3.0	2.48	2.34	2.20	
			4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	

**DC ELECTRICAL CHARACTERISTICS** (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				-55°C to 25°C	≤ 85°C	≤ 125°C	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 2.4 mA  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	3.0	0.26	0.33	0.40	
			4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	4	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

**AC ELECTRICAL CHARACTERISTICS** (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6.0 ns)

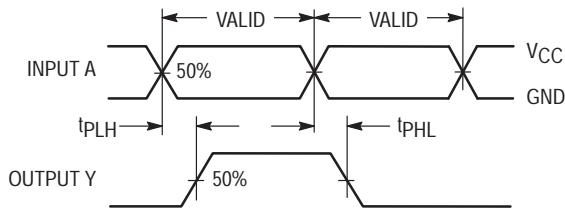
Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			-55°C to 25°C	≤ 85°C	≤ 125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 4)	2.0	135	170	205	ns
		3.0	90	125	165	
		4.5	27	34	41	
		6.0	23	29	35	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, CS1 to Output Y (Figures 2 and 4)	2.0	110	140	165	ns
		3.0	85	100	125	
		4.5	22	28	33	
		6.0	19	24	28	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, CS2 or CS3 to Output Y (Figures 3 and 4)	2.0	120	150	180	ns
		3.0	90	120	150	
		4.5	24	30	36	
		6.0	20	26	31	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 2 and 4)	2.0	75	95	110	ns
		3.0	30	40	55	
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

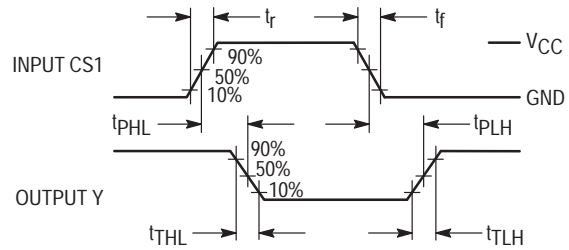
C <sub>PD</sub>	Power Dissipation Capacitance (Per Package)*	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	
		55	

\* Used to determine the no-load dynamic power consumption: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup>f + I<sub>CC</sub> V<sub>CC</sub>. For load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

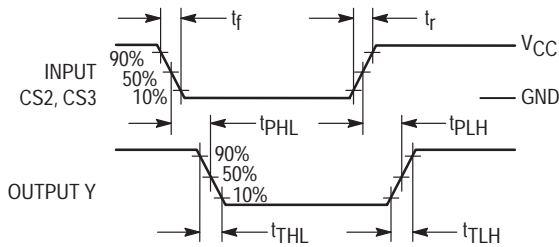
**SWITCHING WAVEFORMS**



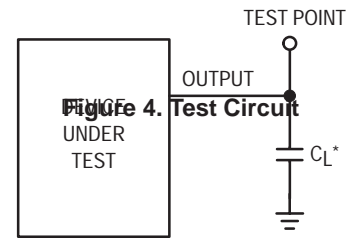
**Figure 1.**



**Figure 2.**



**Figure 3.**



\*Includes all probe and jig capacitance

**PIN DESCRIPTIONS**

**ADDRESS INPUTS  
A0, A1, A2 (Pins 1, 2, 3)**

Address inputs. These inputs, when the chip is selected, determine which of the eight outputs is active-low.

**CONTROL INPUTS  
CS1, CS2, CS3 (Pins 6, 4, 5)**

Chip select inputs. For CS1 at a high level and CS2, CS3 at a low level, the chip is selected and the outputs follow the

Address inputs. For any other combination of CS1, CS2, and CS3, the outputs are at a logic high.

**OUTPUTS  
Y0 – Y7 (Pins 15, 14, 13, 12, 11, 10, 9, 7)**

Active-low Decoded outputs. These outputs assume a low level when addressed and the chip is selected. These outputs remain high when not addressed or the chip is not selected.

**74HC138 EXPANDED LOGIC DIAGRAM**

