NSi8120/NSi8121/NSi8122: High Reliability Dual-Channel Digital Isolators

Datasheet (EN) 1.3

Product Overview

The NSi812x devices are high reliability dual-channel digital isolator. The NSi812x device is safety certified by UL1577 support several insulation withstand voltages (3.75kVrms, 5kVrms), while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSi812x is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 150kV/us. The NSi812x device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSi812x device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use. AEC-Q100 (Grade 1) option is provided for 3.75kV parts.

Key Features

- Up to 5000V_{RMS} Insulation voltage
- Date rate: DC to 150Mbps
- Power supply voltage: 2.5V to 5.5V
- AEC-Q100 Grade 1 available for SOIC-8
- High CMTI: 150kV/us
- Chip level ESD: HBM: ±6kV
- High system level EMC performance:
  Enhanced system level ESD, EFT, Surge immunity
- Default output high level or low level option
- Isolation Barrier Life: >60 years
- Low power consumption: 1.5mA/ch (1 Mbps)
- Low propagation delay: <10ns
- Operation temperature: -40℃~125℃
- RoHS-compliant packages:
  SOIC-8 narrow body
  SOIC-16 wide body

Safety Regulatory Approvals (pending)

- UL recognition: up to 5000V_{RMS} for 1 minute per UL1577
- CQC certification per GB4943.1-2011
- CSA component notice 5A approval
  IEC60950-1 standard
- DIN VDE V 0884-10 (VDE V 0884-10): 2006-12

Applications

- Industrial automation system
- Isolated SPI, RS232, RS485
- General-purpose multichannel isolation
- Motor control

Functional Block Diagrams

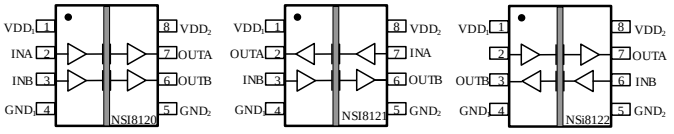

Figure 1. NSi812xN Block Diagram

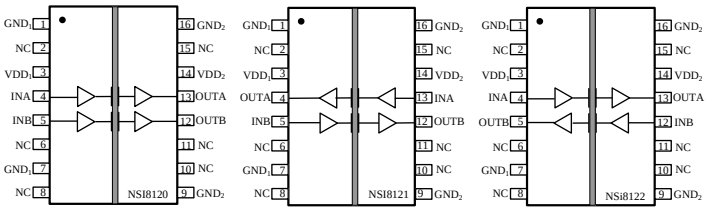

Figure 2. NSi812xW Block Diagram

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1.0 ABSOLUTE MAXIMUM RATINGS

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power Supply Voltage	VDD1, VDD2	-0.5		6.5	V	
Maximum Input Voltage	VINA, VINB	-0.4		VDD+0.4	V	
Common-Mode Transients	CMTI	-150		150	kV/us	
Output current	Io	-15		15	mA	
Maximum Surge Isolation Voltage	V_{IOSM}			10	kV	
Operating Temperature	Topr	-40		125	℃	
Storage Temperature	Tstg	-40		150	℃	
Electrostatic discharge	HBM			±6000	V	
	CDM			±2000	V	

2.0 SPECIFICATIONS

2.1. ELECTRICAL CHARACTERISTICS

(VDD1=2.5V~5.5V, VDD2=2.5V~5.5V, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power on Reset	VDD_{POR}		2.2		V	POR threshold as during power-up
	VDD_{HYS}		0.1		V	POR threshold Hysteresis
Input Threshold	V_{IT}		1.6		V	Input Threshold at rising edge
	V_{IT_HYS}		0.4		V	Input Threshold Hysteresis
High Level Input Voltage	V_{IH}	2			V	
Low Level Input Voltage	V_{IL}			0.8	V	
High Level Output Voltage	V_{OH}	VDD-0.2			V	$I_{OH} \leq 4mA$
Low Level Output Voltage	V_{OL}			0.2	V	$I_{OL} \leq 4mA$
Output Impedance	R_{out}		50		ohm	
Start Up Time after POR	trbs		3		usec	
Common Mode Transient Immunity	CMTI	100	150		kV/us	

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply current	**NSi8120**					
	I_{DD1}(Q0)		0.58		mA	All Input 0V
	I_{DD2}(Q0)		1.18		mA	
	I_{DD1}(Q1)		2.92		mA	All Input at supply
	I_{DD2}(Q1)		1.24		mA	
	I_{DD1}(1M)		1.71		mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		1.38		mA	
	I_{DD1}(10M)		1.78		mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		3.2		mA	
	I_{DD1}(100M)		2.10		mA	All Input with 100Mbps, C_L=15pF
	I_{DD2}(100M)		21.0		mA	
	NSi8121/ NSi8122					
	I_{DD1}(Q0)		1.03		mA	All Input 0V
	I_{DD2}(Q0)		1.00		mA	
	I_{DD1}(Q1)		2.20		mA	All Input at supply
	I_{DD2}(Q1)		2.13		mA	
	I_{DD1}(1M)		1.72		mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		1.68		mA	
	I_{DD1}(10M)		2.62		mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		2.71		mA	
	I_{DD1}(100M)		11.01		mA	All Input with 100Mbps, C_L= 15pF
	I_{DD2}(100M)		12.8		mA	
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t_{PLH}		9.0		ns	
	t_{PHL}		9.0		ns	
Pulse Width Distortion	PWD			5.0	ns	$\lvert t_{PHL} - t_{PLH} \rvert$
Rising Time	t_r			5.0	ns	C_L = 15pF
Falling Time	t_f			5.0	ns	C_L = 15pF
Peak Eye Diagram Jitter	t_{JIT}(PK)		350		ps	

Channel-to-Channel Delay Skew	t_{SK}(c2c)			2.5	ns	
Part-to-Part Delay Skew	t_{SK}(p2p)			5.0	ns	

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 3.3V, VDD2 = 3.3V, Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply current	**NSi8120**					
	I_{DD1}(Q0)		0.55		mA	All Input 0V
	I_{DD2}(Q0)		1.12		mA	
	I_{DD1}(Q1)		2.87		mA	All Input at supply
	I_{DD2}(Q1)		1.18		mA	
	I_{DD1}(1M)		1.7		mA	All Input with 1Mbps, C_L= 15pF
	I_{DD2}(1M)		1.27		mA	
	I_{DD1}(10M)		1.73		mA	All Input with 10Mbps, C_L= 15pF
	I_{DD2}(10M)		2.41		mA	
	I_{DD1}(100M)		2.05		mA	All Input with 100Mbps, C_L= 15pF
	I_{DD2}(100M)		14.05		mA	
	NSi8121/ NSi8122					
	I_{DD1}(Q0)		0.98		mA	All Input 0V
	I_{DD2}(Q0)		0.95		mA	
	I_{DD1}(Q1)		2.14		mA	All Input at supply
	I_{DD2}(Q1)		2.08		mA	
	I_{DD1}(1M)		1.63		mA	All Input with 1Mbps, C_L= 15pF
	I_{DD2}(1M)		1.59		mA	
	I_{DD1}(10M)		2.22		mA	All Input with 10Mbps, C_L= 15pF
	I_{DD2}(10M)		2.25		mA	
	I_{DD1}(100M)		7.57		mA	All Input with 100Mbps, C_L= 15pF
	I_{DD2}(100M)		8.5		mA	
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t_{PLH}		9.0		ns	
	t_{PHL}		9.0		ns	
Pulse Width Distortion	PWD			5.0	ns	$\lvert t_{PHL} - t_{PLH} \rvert$

Rising Time	t_r			5.0	ns	C_L = 15pF
Falling Time	t_f			5.0	ns	C_L = 15pF
Peak Eye Diagram Jitter	t_{JIT}(PK)		350		ps	
Channel-to-Channel Delay Skew	t_{SK}(c2c)			2.5	ns	
Part-to-Part Delay Skew	t_{SK}(p2p)			5.0	ns	

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 2.5V, VDD2 = 2.5V, Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply current	**NSi8120**					
	I_{DD1}(Q0)		0.53		mA	All Input 0V
	I_{DD2}(Q0)		1.1		mA	
	I_{DD1}(Q1)		2.85		mA	All Input at supply
	I_{DD2}(Q1)		1.15		mA	
	I_{DD1}(1M)		1.63		mA	All Input with 1Mbps, C_L= 15pF
	I_{DD2}(1M)		1.21		mA	
	I_{DD1}(10M)		1.68		mA	All Input with 10Mbps, C_L= 15pF
	I_{DD2}(10M)		2.05		mA	
	I_{DD1}(100M)		1.95		mA	All Input with 100Mbps, C_L= 15pF
	I_{DD2}(100M)		10.4		mA	
	NSi8121/ NSi8122					
	I_{DD1}(Q0)		0.96		mA	All Input 0V
	I_{DD2}(Q0)		0.93		mA	
	I_{DD1}(Q1)		2.11		mA	All Input at supply
	I_{DD2}(Q1)		2.05		mA	
	I_{DD1}(1M)		1.58		mA	All Input with 1Mbps, C_L= 15pF
	I_{DD2}(1M)		1.54		mA	
	I_{DD1}(10M)		2.02		mA	All Input with 10Mbps, C_L= 15pF
	I_{DD2}(10M)		2.04		mA	
	I_{DD1}(100M)		6.03		mA	All Input with 100Mbps, C_L= 15pF
	I_{DD2}(100M)		6		mA	
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	

Propagation Delay	t_{PLH}		10		ns	
	t_{PHL}		10		ns	
Pulse Width Distortion	PWD			5.0	ns	$\lvert t_{PHL} - t_{PLH} \rvert$
Rising Time	t_r			5.0	ns	C_L = 15pF
Falling Time	t_f			5.0	ns	C_L = 15pF
Peak Eye Diagram Jitter	t_{JIT}(PK)		350		ps	
Channel-to-Channel Delay Skew	t_{SK}(c2c)			2.5	ns	
Part-to-Part Delay Skew	t_{SK}(p2p)			5.0	ns	

2.2. TYPICAL PERFORMANCE CHARACTERISTICS

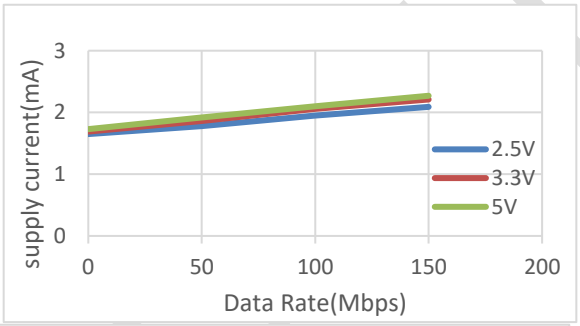


Figure 2.1 NSi8120 VDD1 Supply Current vs Data Rate

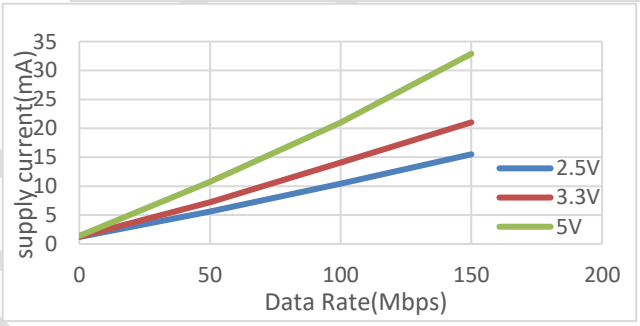
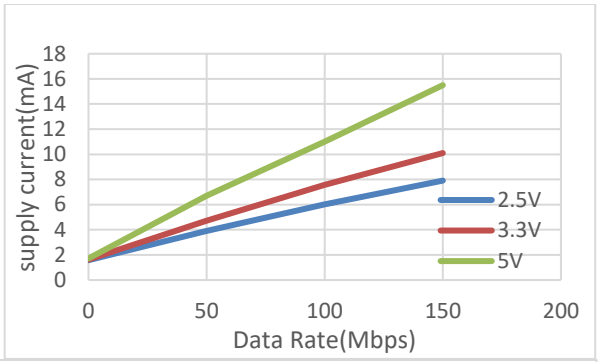


Figure 2.2 NSi8120 VDD2 Supply Current vs Data Rate



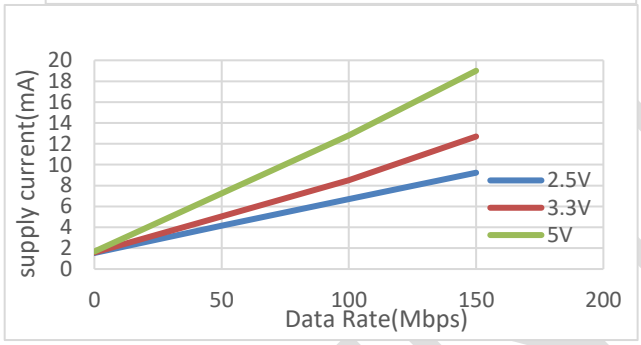


Figure 2.3 NSi8121/ NSi8122 VDD1 Supply Current vs Data Rate Figure 2.4 NSi8121/ NSi8122 VDD2 Supply Current vs Data Rate

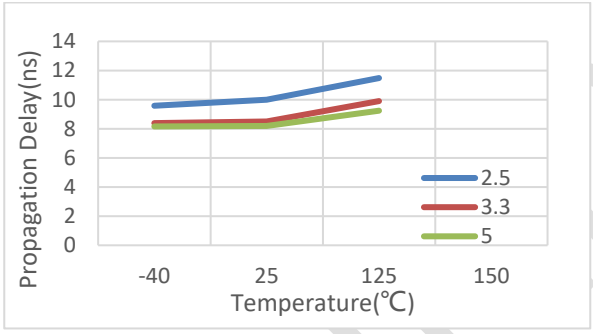


Figure 2.5 Propagation Delay vs Temperature

2.3. PARAMETER MEASUREMENT INFORMATION

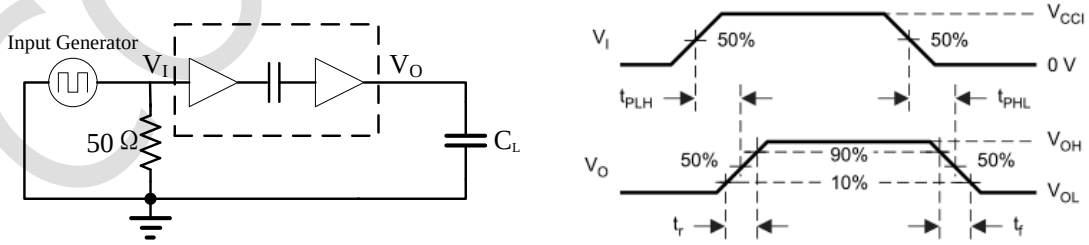


Figure 2.6 Switching Characteristic Test Circuit and Voltage Waveforms

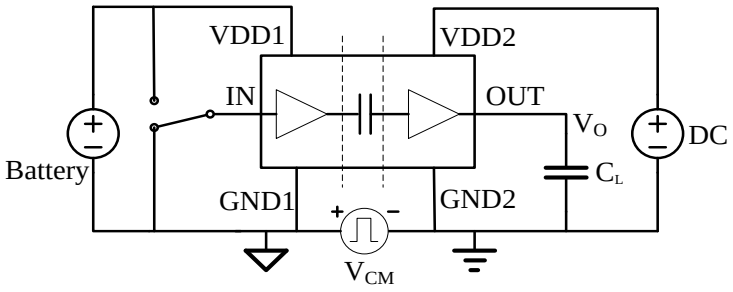


Figure 2.7 Common-Mode Transient Immunity Test Circuit

3.0 HIGH VOLTAGE FEATURE DESCRIPTION

3.1. INSULATION AND SAFETY RELATED SPECIFICATIONS

Parameters	*Symbol*	*Value*		*Unit*	*Comments*
		SOIC-8	*SOIC-16*		
Minimum External Air Gap (Clearance)	L(I01)	4.0	7.8	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	L(I02)	4.0	7.8	mm	Shortest terminal-to-terminal distance across the package surface
Minimum internal gap	DTI	20		um	Distance through insulation
Tracking Resistance(Comparative Tracking Index)	CTI	>600		**V**	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		Ⅰ			

3.2. DIN VDE V 0884-10 (VDE V 0884-10) INSULATION CHARATERISTICS

Description	*Test Condition*	*Symbol*	*Value*		*Unit*
			SOIC-8	SOIC-16	
Installation Classification per DIN VDE 0110					
For Rated Mains Voltage ≤ 150Vrms			Ⅰ to Ⅳ	Ⅰ to Ⅳ	
For Rated Mains Voltage ≤ 300Vrms			Ⅰ to Ⅲ	Ⅰ to Ⅳ	
For Rated Mains Voltage ≤ 400Vrms			Ⅰ to Ⅲ	Ⅰ to Ⅳ	
Climatic Classification			10/105/21	10/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	2	
Maximum repetitive isolation voltage		VIORM	565	849	Vpeak

Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1059	1592	Vpeak
Input to Output Test Voltage, Method A					
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	848	1274	Vpeak
After Input and /or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	678	1019	Vpeak
Maximum transient isolation voltage	t = 60 sec	VIOTM	5300	7000	Vpeak
Maximum Surge Isolation Voltage	Test method per IEC60065,1.2/50us waveform, VTEST=1.6 ×VIOSM	VIOSM	6000	7000	Vpeak
Isolation resistance	VIO =500V	RIO	$>10^9$	$>10^9$	Ω
Isolation capacitance	f = 1MHz	CIO	0.8	0.8	pF
Input capacitance		CI	2	2	pF
Total Power Dissipation at 25℃		Ps		1499	mW
Safety input, output, or supply current	θJA = 140 °C/W, V I = 5.5 V, T J = 150 °C, T A = 25 °C	Is	160		mA
	θJA = 84 °C/W, V I = 5.5 V, T J = 150 °C, T A = 25 °C			237	mA
Case Temperature		Ts	150	150	℃

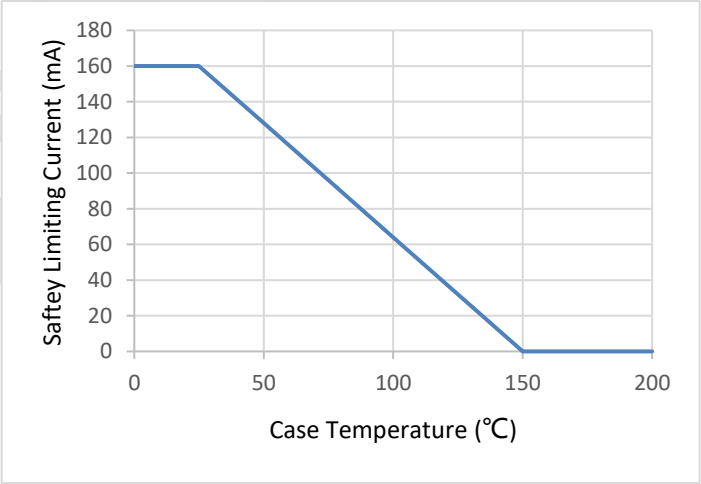


Figure 3.1 NSi8120N/NSi8121N/NSi8122N Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN V VDE V 0884-10

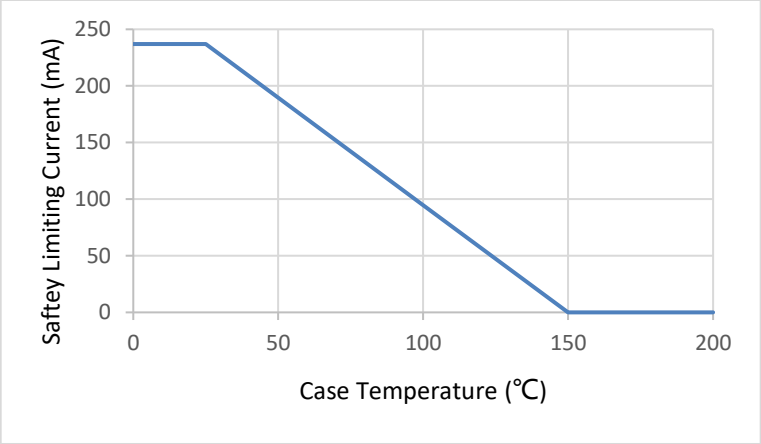


Figure 3.2 NSi8120W/NSi8121W/NSi8122W Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN V VDE V 0884-10

3.3. REGULATORY INFORMATION

The NSi8120N/NSi8121N/NSi8122N are approved or pending approval by the organizations listed in table.

UL	*CSA*	*VDE*	*CQC*
UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A IEC60950-1	DIN V VDE V0884-10 (VDE V 0884-10):2006-12[2]	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 3750Vrms Isolation voltage	$400V_{RMS}$ basic insulation working voltage	Basic Insulation 565Vpeak, V_{IOSM}=6000Vpeak	Basic insulation at $400V_{RMS}$ (565Vpeak)
File (pending)	File (pending)	File (pending)	File (pending)

[1] In accordance with UL 1577, each NSi8120N/NSi8121N/NSi8122N is proof tested by applying an insulation test voltage ≥ 4500 V rms for 1 sec.

[2] In accordance with DIN V VDE V 0884-10, each NSi8120N/NSi8121N/NSi8122N is proof tested by applying an insulation test voltage ≥ 1059 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-10 approval.

The NSi8120W/NSi8121W/NSi8122W are approved or pending approval by the organizations listed in table.

UL	*CSA*	*VDE*	*CQC*
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A IEC60950-1	DIN V VDE V0884-10 (VDE V 0884-10):2006-12	Certified by CQC11-471543-2012 GB4943.1-2011
Double Protection, 5000Vrms Isolation voltage	$780V_{RMS}$ basic insulation working voltage $390V_{RMS}$ Reinforced insulation working voltage	Basic Insulation 849Vpeak, V_{IOSM}=7000Vpeak	Basic insulation at $780V_{RMS}$ (1103Vpeak) Reinforced insulation at $390V_{RMS}$ (552Vpeak)
File (pending)	File (pending)	File (pending)	File (pending)

[1] In accordance with UL 1577, each NSi8120W/NSi8121W/NSi8122W is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 sec.

[2] In accordance with DIN V VDE V 0884-10, each NSi8120W/NSi8121W/NSi8122W is proof tested by applying an insulation test voltage ≥ 1592 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-10 approval.

4.0 FUNCTION DESCRIPTION

The NSi812x is a Dual-channel digital isolator based on a capacitive isolation barrier technique. The digital signal is modulated with RF carrier generated by the internal oscillator at the Transmitter side. Then it is transferred through the capacitive isolation barrier and demodulated at the Receiver side.

The NSi812x devices are high reliability dual-channel digital isolator with AEC-Q100 qualified. The NSi812x device is safety certified by UL1577 support several insulation withstand voltages (3.75kVrms, 5kVrms), while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSi812x is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 150kV/us. The NSi812x device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSi812x device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

The NSi812x has a default output status when VDDIN is unready and VDDOUT is ready as shown in Table 4.1, which helps for diagnosis when power is missing at the transmitter side. The output B follows the same status with the input A within 1us after powering up.

Table 4.1 Output status vs. power status

Input	VDD1 status	VDD2 status	Output	Comment
H	Ready	Ready	H	Normal operation.
L	Ready	Ready	L	
X	Unready	Ready	L H	The output follows the same status with the input within 1us after input side VDD1 is powered on.
X	Ready	Unready	X	The output follows the same status with the input within 1us after output side VDD2 is powered on.

5.0 APPLICATION NOTE

5.1. PCB LAYOUT

The NSi812x requires a 0.1 μF bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be

placed as close as possible to the package. Figure 5.1 to Figure 5.4 show the recommended PCB layout, make sure the space under the chip should keep free from planes, traces, pads and via. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy. The series resistors also improve the system reliability such as latch-up immunity.

The typical output impedance of an isolator driver channel is approximately 50 Ω, ±40%. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

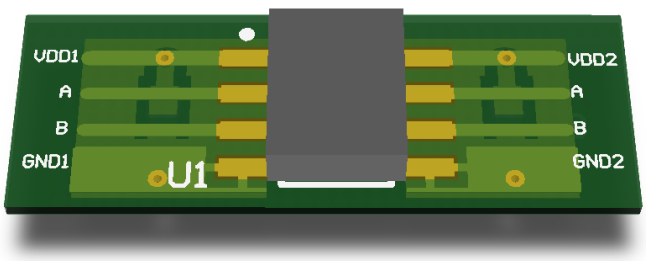


Figure5.1 Recommended PCB Layout — Top Layer

Figure5.2 Recommended PCB Layout — Bottom Layer

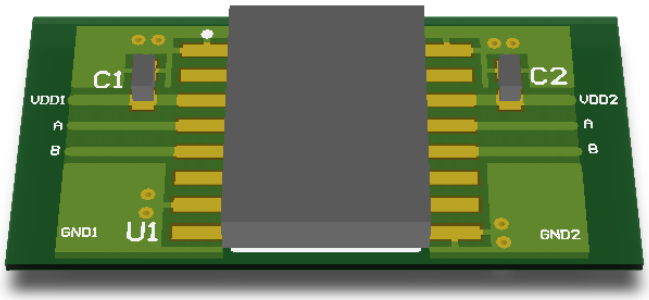


Figure5.3 Recommended PCB Layout — Top Layer

Figure5.4 Recommended PCB Layout — Bottom Layer

5.2. HIGH SPEED PERFORMANCE

Figure 5.5 shows the eye diagram of NSi812x at 200Mbps data rate output. The result shows a typical measurement on the NSi812x with 350ps p-p jitter.

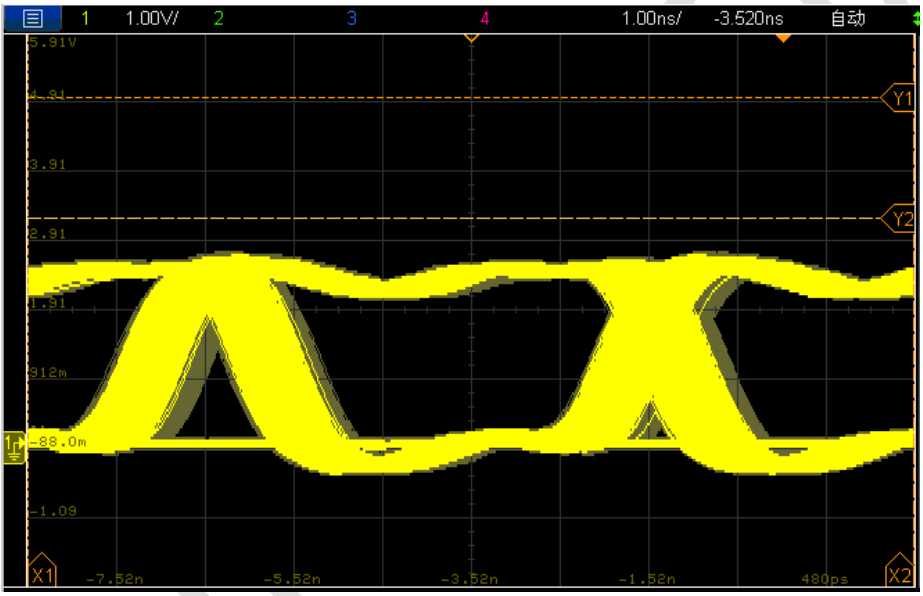


Figure5.5 NSi812x Eye Diagram

5.3. TYPICAL SUPPLY CURRENT EQUATIONS

The typical supply current of NSi812x can be calculated using below equations. I_{DD1} and I_{DD2} are typical supply currents measured in mA, f is data rate measured in Mbps, C_L is the capacitive load measured in pF

NSi8120:

$I_{DD1} = 0.19 *a1+1.45*b1+0.82*c1.$

$I_{DD2} = 1.36+ VDD1*f* C_L *c1*10^{-9}$

When a1 is the channel number of low input at side 1, b1 is the channel number of high input at side 1, c1 is the channel number of switch signal input at side 1.

NSi8121/ NSi8122:

$I_{DD1} = 0.87 +1.26*b1+0.63*c1+ VDD1*f* C_L *c2*10^{-9}$

$I_{DD2} = 0.87 +1.26*b2+0.63*c2+ VDD1*f* C_L *c1*10^{-9}$

When b1 is the channel number of high input at side 1, c1 is the channel number of switch signal input at side 1, b2 is the channel number of high input at side 2, c2 is the channel number of switch signal input at side 2.

6.0 PACKAGE INFORMATION

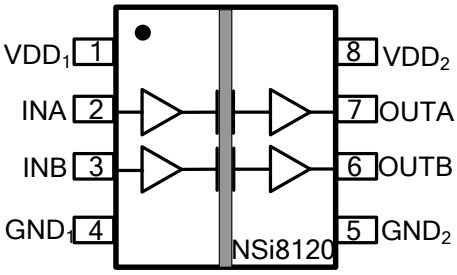


Figure 6.1 NSi8120N Package

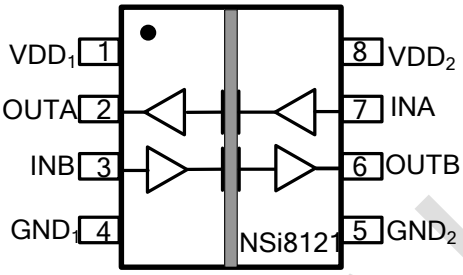


Figure 6.2 NSi8121N Package

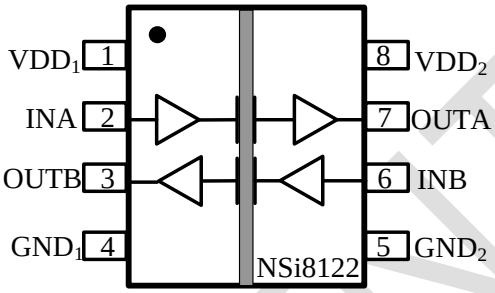


Figure 6.3 NSi8122N Package

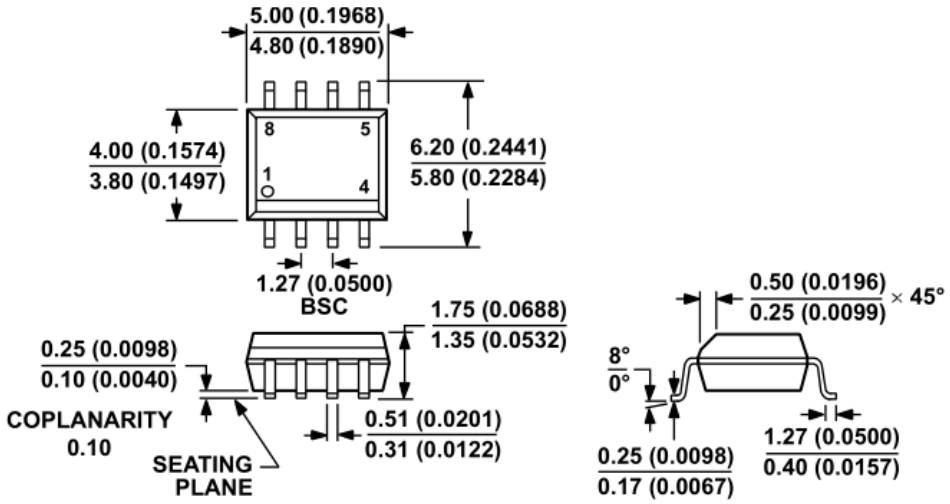


Figure 6.4 SOIC8 Package Shape and Dimension in millimeters (inches)

Table6.1 NSi8120N/ NSi8121N/ NSi8122N Pin Configuration and Description

NSi8120N PIN NO.	*NSi8121N PIN NO.*	*NSi8122N PIN NO.*	*SYMBOL*	*FUNCTION*
1	1	1	VDD1	Power Supply for Isolator Side 1
2	7	2	INA	Logic Input A
3	3	6	INB	Logic Input B
4	4	4	GND1	Ground 1, the ground reference for Isolator Side 1

5	5	5	GND2	Ground 2, the ground reference for Isolator Side 2
6	6	3	OUTB	Logic Output B
7	2	7	OUTA	Logic Output A
8	8	8	VDD2	Power Supply for Isolator Side 2

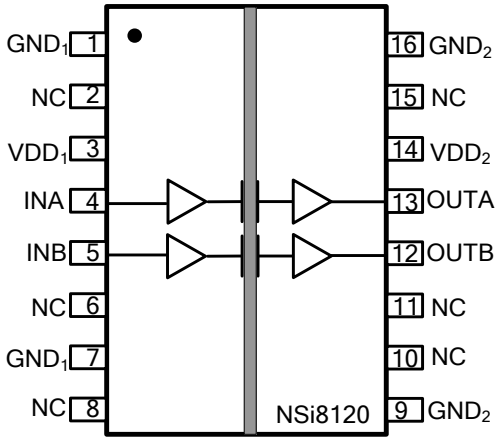


Figure 6.5 NSi8120W Package

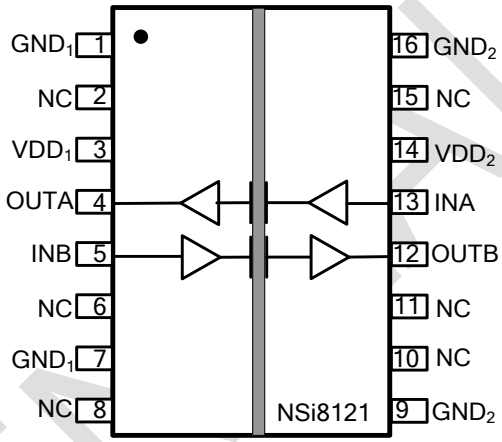


Figure 6.6 NSi8121W Package

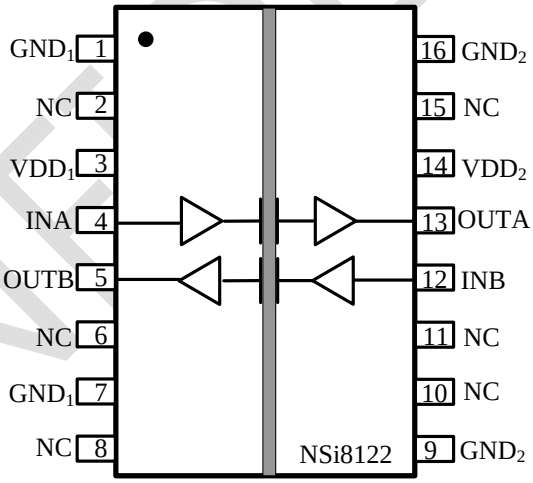


Figure 6.7 NSi8122W Package

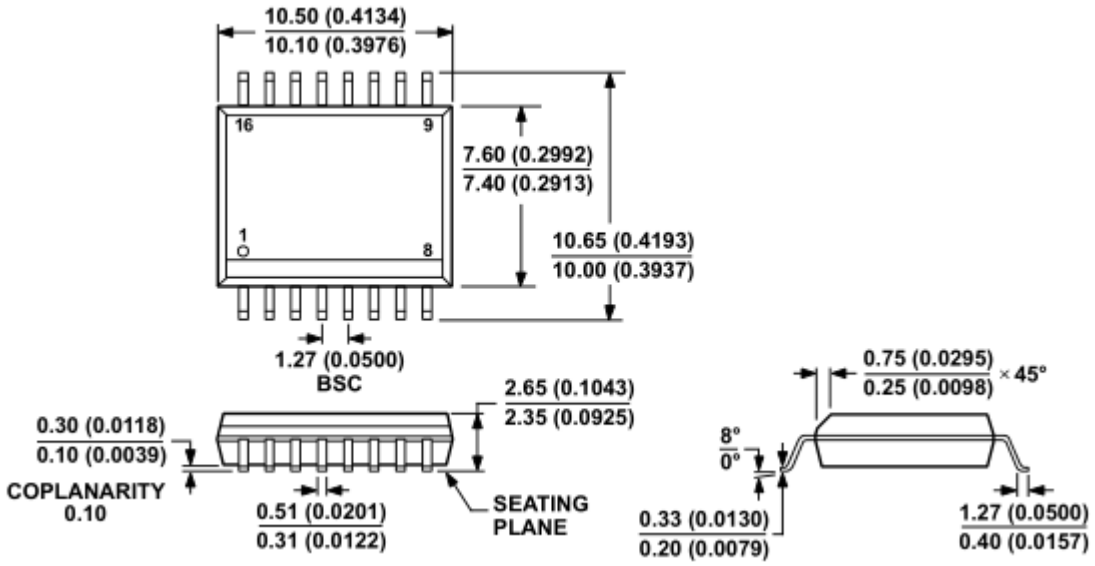


Figure 6.8 WB SOIC16 Package Shape and Dimension in millimeters and (inches)

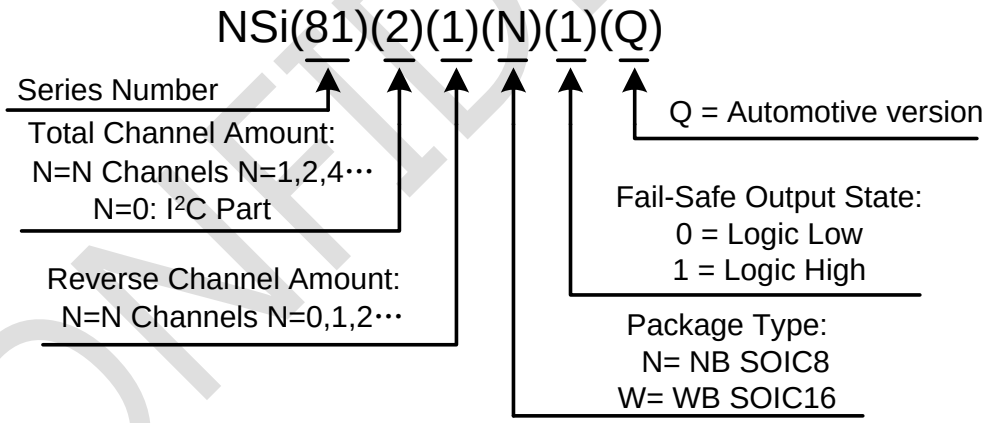
Table 6.2 NSi8120W/ NSi8121W/ NSi8122W Pin Configuration and Description

NSi8120W PIN NO.	*NSi8121W PIN NO.*	*NSi8122W PIN NO.*	*SYMBOL*	*FUNCTION*
1	1	1	GND1	Ground 1, the ground reference for Isolator Side 1
2	2	2	NC	No Connection.
3	3	3	VDD1	Power Supply for Isolator Side 1
4	13	4	INA	Logic Input A
5	5	12	INB	Logic Input B
6	6	6	NC	No Connection.
7	7	7	GND1	Ground 1, the ground reference for Isolator Side 1
8	8	8	NC	No Connection.
9	9	9	GND2	Ground 2, the ground reference for Isolator Side 2
10	10	10	NC	No Connection.
11	11	11	NC	No Connection.
12	12	5	OUTB	Logic Output A
13	4	13	OUTA	Logic Output B
14	14	14	NC	No Connection.
15	15	15	VDD2	Power Supply for Isolator Side 2
16	16	16	GND2	Ground 2, the ground reference for Isolator Side 2

7.0 ORDER INFORMATION

Part No.	Isolation Rating(kV)	Number of side 1 inputs	Number of side 2 inputs	Max Data Rate (Mbps)	Default Output State	Temperature	Automotive	Package
NSi8120N0	3.75	2	0	150	Low	-40 to 125℃	NO	SOIC8
NSi8120N1	3.75	2	0	150	High	-40 to 125℃	NO	SOIC8
NSi8121N0	3.75	1	1	150	Low	-40 to 125℃	NO	SOIC8
NSi8121N1	3.75	1	1	150	High	-40 to 125℃	NO	SOIC8
NSi8122N0	3.75	1	1	150	Low	-40 to 125℃	NO	SOIC8
NSi8122N1	3.75	1	1	150	High	-40 to 125℃	NO	SOIC8
NSi8120W0	5	2	0	150	Low	-40 to 125℃	NO	WB SOIC16
NSi8120W1	5	2	0	150	High	-40 to 125℃	NO	WB SOIC16
NSi8121W0	5	1	1	150	Low	-40 to 125℃	NO	WB SOIC16
NSi8121W1	5	1	1	150	High	-40 to 125℃	NO	WB SOIC16
NSi8122W0	5	1	1	150	Low	-40 to 125℃	NO	WB SOIC16
NSi8122W1	5	1	1	150	High	-40 to 125℃	NO	WB SOIC16
NSi8120N0Q	3.75	2	0	150	Low	-40 to 125℃	YES	SOIC8
NSi8120N1Q	3.75	2	0	150	High	-40 to 125℃	YES	SOIC8
NSi8121N0Q	3.75	1	1	150	Low	-40 to 125℃	YES	SOIC8
NSi8121N1Q	3.75	1	1	150	High	-40 to 125℃	YES	SOIC8
NSi8122N0Q	3.75	1	1	150	Low	-40 to 125℃	YES	SOIC8
NSi8122N1Q	3.75	1	1	150	High	-40 to 125℃	YES	SOIC8

Part Number Rule:



8.0 REVISION HISTORY

Revision	Description	Date
1.0		2017/11/15
1.3		2018/8/21