RS10N80F

N Channel MOSFET

Applications:

- •Adapter & Charger
- •SMPS Standby Power
- •AC-DC Switching Power Supply
- •LED driving power

Features:

- •Low On Resistance
- •Low Gate Charge
- •Peak Current vs Pulse Width Curve
- •RoHS Compliant

Ordering Information

Part Number	Package	Marking
RS10N80F	TO-220F	RS10N80F

Absolute Maximun Ratings Tc=25℃ unless otherwise specified

Symbol	Parameter	RS10N80F	Units
VDSS	Drain-to-Source Voltage (Note*1)	800	V
ID	Continuous Drain Current	10	
ID@ 100 ℃	Continuous Drain Current	6.3	A
ldм	Pulsed Drain Current (Note*2)	40	
DD	Power Dissipation	62	W
PD	Derating Factor above 25℃	0.5	W/℃
VGS	Gate-to-Source Voltage	±30	V
EAS	Single Pulse Avalanche Engergy L=30mH IAS=7.5A VDD=100V RG=25Ω TJ=25℃	938	mJ
	Maximum Temperature for Soldering		
TL TPKG	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	300 260	°C
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

*Drain Current Limited by Maximum Junction Temperature

Caution:Stresses greater than those listed in the "Absolute Maximum Ratings" Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS10N80F	Units	Test Conditions
Rejc	Junction-to-Case	2.02	°C/W	Drain lead soldered to water cooled heatsink,PD adjusted for a peak junction temperature of +150℃.
Reja	Junction-to-Ambient	62.5		1 cubic foot chamber,free air.

Lead Free Package and Finish

	lD	Rds(Vdss	
	10A	(800V	
1	T Not to S	0-220F cale	1.Gate o	2.Drain

(Pb)

OFF Characteristics TJ=25 $^\circ\!\!\mathrm{C}$ unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
BVDSS	Drain-to-source Breakdown Voltage	800			V	Vgs=0V,Id=250µA
ldss	Drain-to-Source Leakage Current			1.0	μA	VDS=800V,VGS=0V
	Gate-to-Source Forward Leakage			100	5	VGS=+30V VDS=0V
IGSS	Gate-to-Source Reverse Leakage			-100	nA	VGS=-30V VDS=0V

ON Characteristics TJ=25°C unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
RDS(on)	Static Drain-to-Source On-Resistance		0.92	1.15	Ω	Vgs=10V,Id=5.0A
Vgs(TH)	Gate Threshold Voltage	2.0		4.0	V	Vgs=Vds,Id=250µA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
td(ON)	Turn-on Delay Time		23		nS	VDS=400V ID=10A RG=25Ω (Note:3,4)
trise	Rise Time		15			
td(OFF)	Turn-OFF Delay Time		90			
t fall	Fall Time		30	-		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
Ciss	Input Capacitance		1979			Vgs=0V
Coss	Output Capacitance		133		pF	VDS=25V
Crss	Reverse Transfer Capacitance		53			f=1.0MHz
Qg	Total Gate Charge		83		nC	VDS=640V ID=10A VGS=10V (Note:3,4)
Qgs	Gate-to-Source Charge		9			
Qgd	Gate-to-Drain("Miller") Charge		49			

Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
ls	Continuous Source Current			10	Α	Integral pn-diode
lsм	Maximum Pulsed Current			40	Α	in MOSFET
Vsd	Diode Forward Voltage			1.4	V	Is=10A,Vgs=0V
trr	Reverse Recovery Time		320		nS	Vgs=0V
Qrr	Reverse Recovery Charge		4.2		μC	Is=10A,di/dt=100A/µs

Notes:

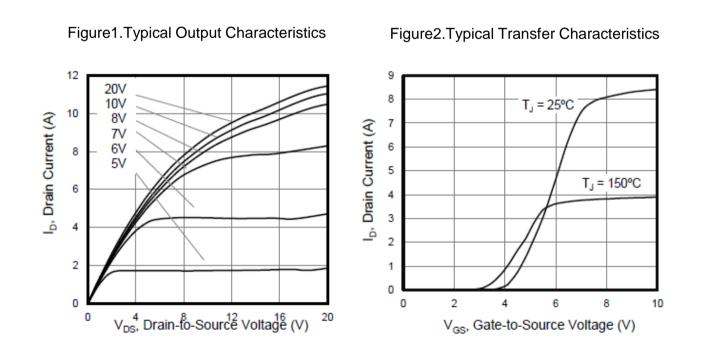
*1.TJ=±25℃ to +150℃.

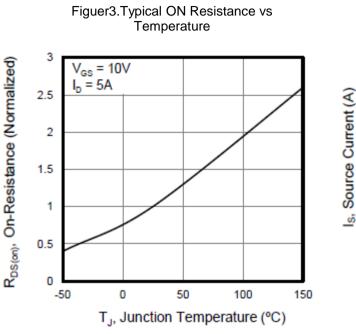
*2.Repetitive rating; pulse width limited by maximum junction temperature.

*3.Pulse width \leq 300 µs; duty cycle \leq 1%.

*4.Basically not affected by temperature.

Typical Feature curve





Figuer4.Typical Body Diode Transfer Characteristics

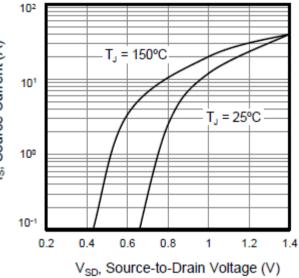
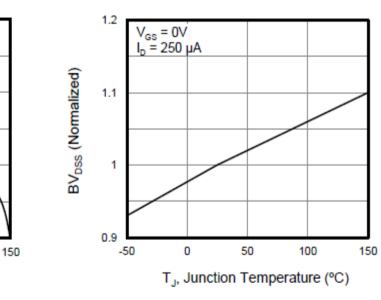


Figure5.Typical Drain Current vs. Temperature

Figure6. BVDSS Variation vs. Temperature



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12

10

8

6

4

2

0

25

50

75

T_J, Case Temperature (°C)

100

I_D, Drain Current (A)

125

Figure7. Capacitance

Figure8. Gate Charge

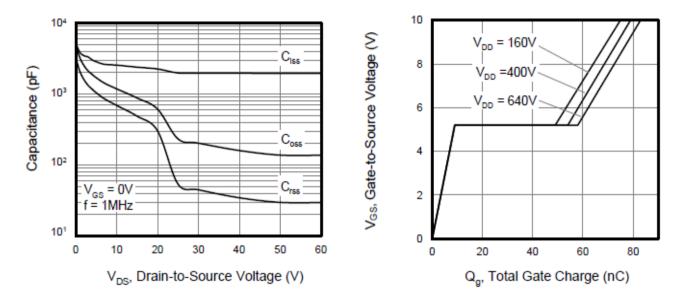
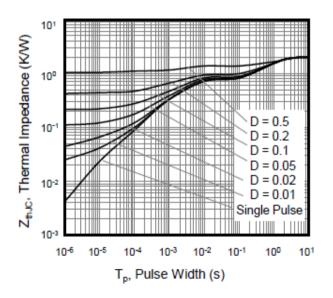
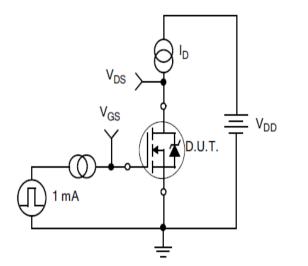


Figure9. Transient Thermal Impedance



Test Circuits and Waveforms



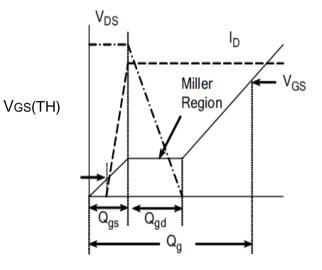
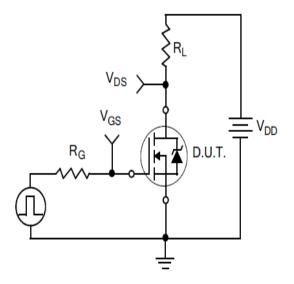


Figure11. Gate Charge Test Circuit

Figure12. Gate Charge Waveform



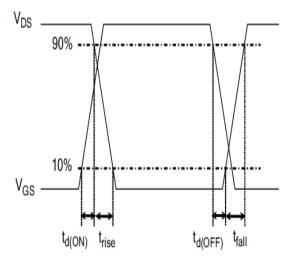
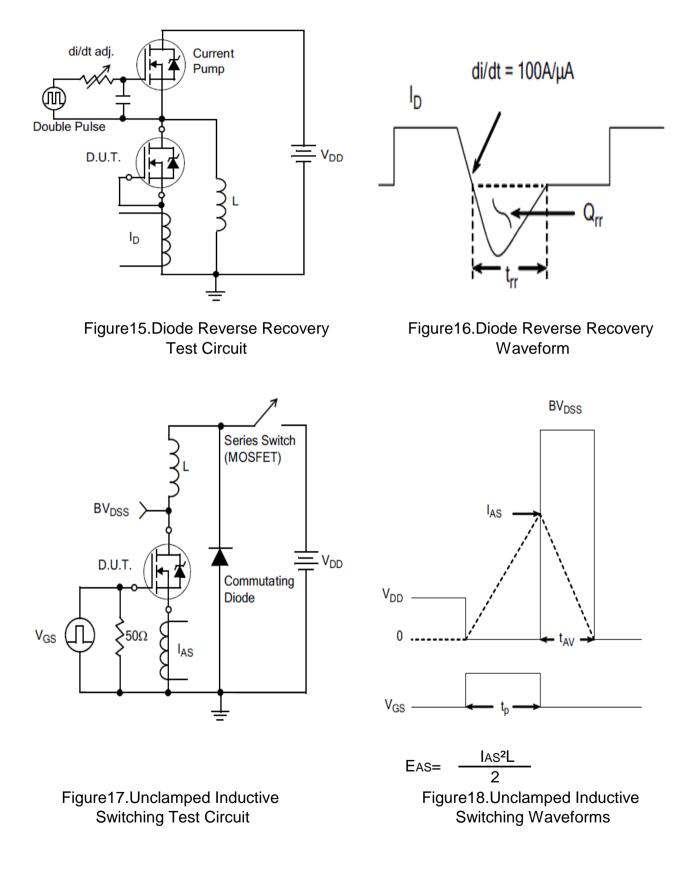


Figure13. Resistive Switching Test Circuit

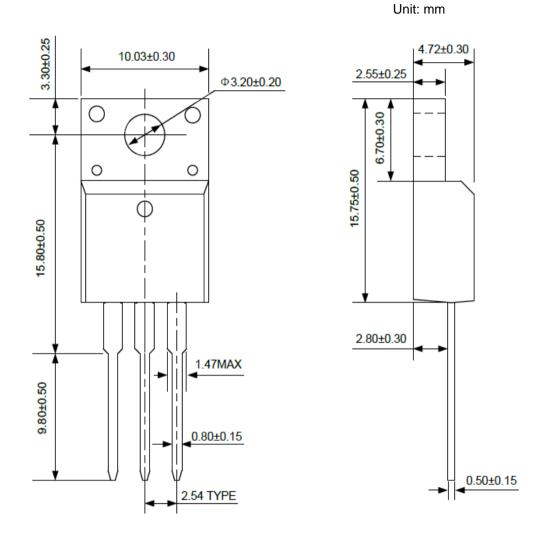
Figure14. Resistive Switching Waveforms

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Test Circuits and Waveforms



Package outline drawing



TO-220F

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