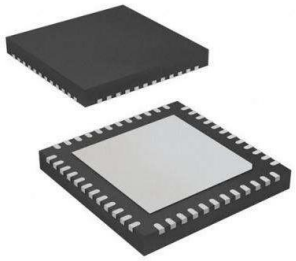
Four-Channel, Ultra-Low Noise, 5V Low Voltage, 256 Microstepping Motor Driver

PRODUCT DESCRIPTION

The MS41949 is four-channel, 5V low voltage stepper motor driver, which can drive four stepper motors. Ultra-low noise microstepping could be realized by voltage driving method with current microstepping and torque ripple correction technology.

The MS41949 has a 5V DC motor driver and the output resistance is low to 1Ω.



QFN48

FEATURES

- Voltage Driving Method, 256 Microstepping
  (Four Channels, Eight H Bridges) Maximum Driving Current ±0.8A of each H Bridge
- 4-Wire SPI Communication
- Load Power Supply : 2.7V~5.5V
- Built-in DC Motor Drive, Maximum Driving Current ±0.5A
- QFN48 Package (Back Thermal Pad)

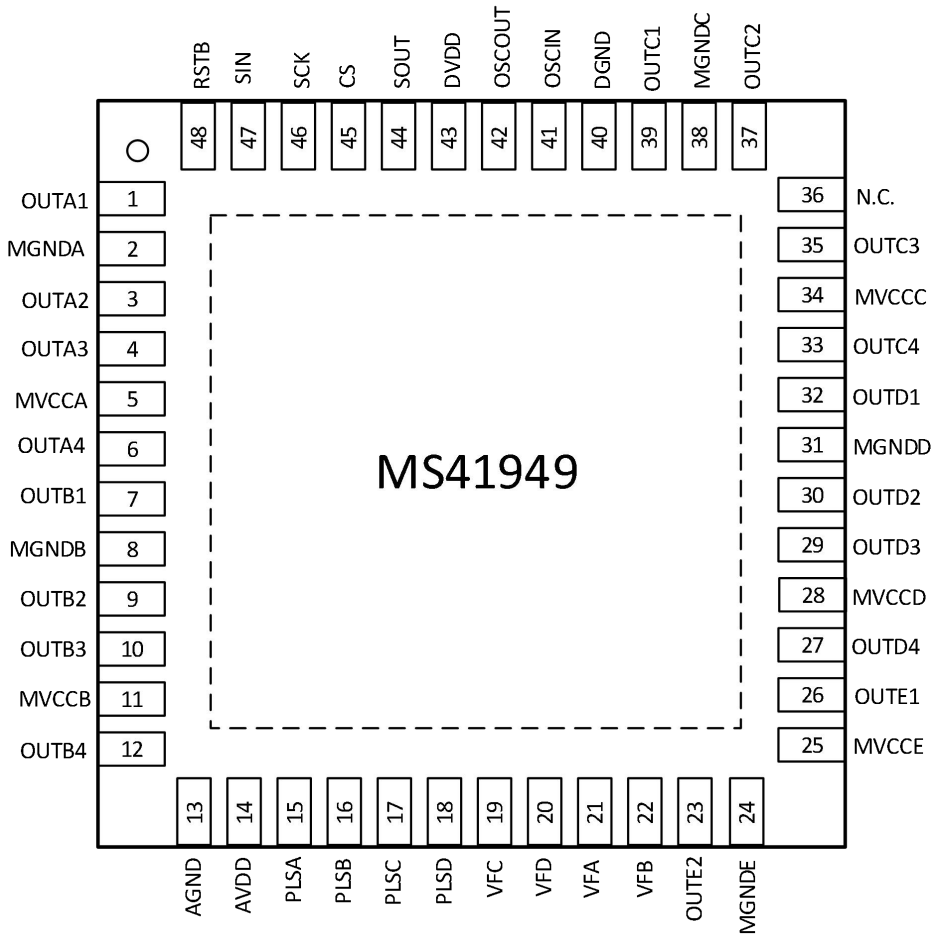
APPLICATIONS

- Robot, Precision Industry Device
- Camera
- Monitoring Camera

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS41949	QFN48	MS41949

PIN CONFIGURATION

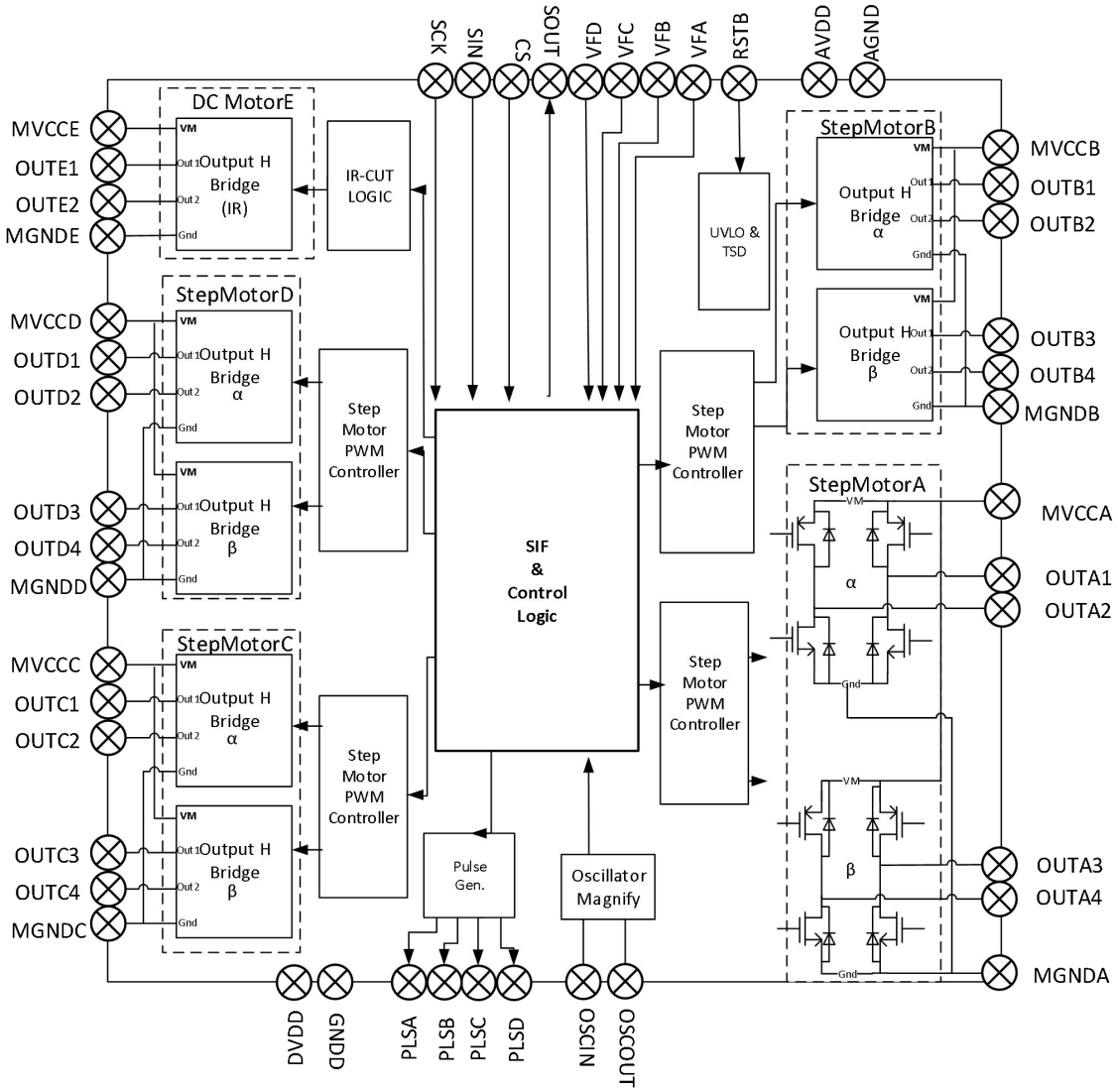


PIN DESCRIPTION

Pin	Name	Type	Description
1	OUTA1	O	Motor A, α Bridge Output 1
2	MGNDA	-	Motor A, GND
3	OUTA2	O	Motor A, α Bridge Output 2
4	OUTA3	O	Motor A, β Bridge Output 3
5	MVCCA	P	Motor A, Power Supply
6	OUTA4	O	Motor A, β Bridge Output 4
7	OUTB1	O	Motor B, α Bridge Output 1
8	MGNDB	-	Motor B, GND
9	OUTB2	O	Motor B, α Bridge Output 2
10	OUTB3	O	Motor B, β Bridge Output 3
11	MVCCB	P	Motor B, Power Supply
12	OUTB4	O	Motor B, β Bridge Output 4
13	AGND	-	Analog GND
14	AVDD	P	Analog Power Supply, Logic Output Power Supply
15	PLSA	O	Motor A, Monitor Output
16	PLSB	O	Motor B, Monitor Output
17	PLSC	O	Motor C, Monitor Output
18	PLSD	O	Motor D, Monitor Output
19	VFC	I	Motor C, Synchronous Signal Input
20	VFD	I	Motor D, Synchronous Signal Input
21	VFA	I	Motor A, Synchronous Signal Input
22	VFB	I	Motor B, Synchronous Signal Input
23	OUTE2	O	Motor E, DC Motor Output 2
24	MGNDE	-	Motor E, DC Motor GND
25	MVCCE	P	Motor E, DC Motor Power Supply
26	OUTE1	O	Motor E, DC Motor Output 1
27	OUTD4	O	Motor D, β Bridge Output 4
28	MVCCD	P	Motor D, Power Supply
29	OUTD3	O	Motor D, β Bridge Output 3
30	OUTD2	O	Motor D, α Bridge Output 2

Pin	Name	Type	Description
31	MGNDD	-	Motor D, GND
32	OUTD1	O	Motor D, α Bridge Output 1
33	OUTC4	O	Motor C, β Bridge Output 4
34	MVCCC	P	Motor C, Power Supply
35	OUTC3	O	Motor C, β Bridge Output 3
36	N.C.	-	Not Connection
37	OUTC2	O	Motor C, α Bridge Output 2
38	MGNDC	-	Motor C, GND
39	OUTC1	O	Motor C, α Bridge Output 1
40	DGND	-	Digital Logic GND
41	OSCIN	I	Oscillator Input
42	OSCOUT	O	Oscillator Output
43	DVDD	P	Digital Power Supply
44	SOUT	O	SPI Output
45	CS	I	SPI Input
46	SCK	I	SPI Input
47	SIN	I	SPI Input
48	RSTB	I	Power-down, Sleep Input

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Absolute Ratings

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Ratings	Unit
Power Supply, Analog and Control Part [1]	AVDD DVDD	-0.3 ~ +6.0	V
Power Supply, Motor Control 1[1]	MVCCx	-0.3 ~ +6.0	V
Power Dissipation [2]	PD	141.1	mW
Operating Temperature [3]	Topr	-40 ~ +85	°C
Storage Temperature [3]	Tstg	-55 ~ +125	°C
Stepper Motor, H Bridge Drive Current	IM1	±1	A/ch
Instantaneous H Bridge Drive Current	IM(pluse)	±1.5	A/ch
Input Voltage, Digital Part[4]	Vin	-0.3 ~ (DVDD + 0.3)	V
Total Current [5]	Itotalmax	2.3	A
ESD	HBM	>±3k	V

Note:

1. Absolute maximum ratings are used in the range of power dissipation.

2. Power dissipation refers to the value of encapsulated monomer at Ta = 85°C.

In practice, it is expected to refer to the technical data and PD-Ta characteristic diagram on the basis of power supply, pressure, load, ambient temperature conditions, and then carry out the heat dissipation design which does not exceed the power dissipation value.

3. Except power dissipation, ambient temperature, and storage temperature parameters,

all parameters are at Ta = 25°C.

4. (DVDD + 0.3) voltage shall not exceed 6.0 V.

5. The constant average total current shouldn't exceed 2A for thermal performance. If the current is more than 2A, the demand for PCB would be higher.

Operating Power Supply

Parameter	Symbol	Range			Unit
		Min	Typ	Max	
Power Supply	DVDD	4.5	5	5.5	V
	AVDD	3	3.3	3.6	
	MVCCx	3	5	5.5	

Note: In general, DVDD is 5V. If it is 3.3V, the maximum frequency of OSC system clock is 20MHz and recommend to use 16MHz.

Terminal Tolerance Current and Voltage Ranges

The parameters cannot exceed the absolute maximum ratings in any conditions.

Rated voltage value refers to each terminal voltage with respect to GND . GND is the voltage of AGND,DGND,MGNDx.

Outside input voltage and current are strictly prohibited except the described terminals below.

For the current, "+" means the current flowing to IC, and "-" means the current flowing out from IC.

Pin	Name	Range	Unit
41	OSCIN	-0.3 ~ (DVDD + 0.3)	V
45	CS	-0.3 ~ (DVDD + 0.3)	V
46	SCK	-0.3 ~ (DVDD + 0.3)	V
47	SIN	-0.3 ~ (DVDD + 0.3)	V
19,20 21,22	VFA,VFB VFC,VFD	-0.3 ~ (DVDD + 0.3)	V
48	RSTB	-0.3 ~ (DVDD + 0.3)	V
1,3,4,6	AOUT	±1	A
7,9,10,12	BOUT	±1	A
27,29 30,32	DOUT	±1	A
33,35 37,39	COUT	±1	A
23	OUTE2	±0.8	A
25	OUTE1	±0.8	A

Note: (DVDD + 0.3) voltage should not exceed 5.5V.

ELECTRICAL CHARACTERISTICS

MVCCx = VDD5 = 5 V, AVDD = 3.3V, DVDD = 5 V

Note: Unless other noted, Ta = 25°C ±2°C.

Current Consumption

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Standby Power Supply Current	Iccstandby	RSTB = low output open-circuit 27MHz input Total currents of all powers		0.9	2	mA
Operating Power Supply Current	ICC1	RSTB = high No load No 27MHz input Total currents of all powers		2.4	4	mA
	ICC2	RSTB = high No load 27MHz input Total currents of all powers		14	20	mA

Digital Input and Output

Parameter	Symbol	Condition	Min	Typ	Max	Unit
High-level Input	Vin(H)	RSTB	0.42× DVDD		DVDD +0.3	V
Low-level Input	Vin(L)	RSTB	-0.3		0.31× DVDD	V
SOUT High-level Output	Vout(H): SDATA	[SOUT] 1mA current source	AVDD -0.5			V
SOUT Low-level Output	Vout(L): SDATA	[SOUT] 1mA current sink			0.5	V
PLSx High-level Output	Vout(H): MUX		0.9× AVDD			V
PLSx Low-level Output	Vout(L): MUX				0.1× AVDD	V
Input Pull-down Impedance	Rpullret	RSTB	50	100	200	kΩ

Stepper Motor Drive (A,B)

Focal length and zoom control in camera

Unless other noted, MVCCA=MVCCB=5V, RL=20Ω, T=25°C.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
H Bridge ON Impedance	RonFZ	IM = 500mA (HS+LS)	0.40	0.62	0.82	Ω
H Bridge Leakage Current	IleakFZ				0.8	μA

DC Motor Drive (DC Motor E)

IR-CUT in camera

Unless other noted, MVCCE=5V，RL=20Ω，T=25°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Output ON Impedance	Roncut	IoutE=300mA Total resistance of high and low side FETs	1.0	1.25	1.5	Ω
Output Leakage Current	IleakE				0.8	μA
Delay from SPI Input to H Bridge Output	T13	SPI input mode, RL=20Ω		25×TSCK		s

Digital Input

DVDD=5 V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
High-level Input Threshold Voltage	Vin(H)	SCK,SIN,CS,VDx		2.3		V
Low-level Input Threshold Voltage	Vin(L)	SCK,SIN,CS,VDx		2.0		V
RSTB Signal Pulse	Trst		100			μs
Input Maximum Lag Error	Vhysin	SCK,SIN,CS,VDx		0.34		V
OSCIN DC High-level Input Voltage	OSCdcH	External CLK or active OSC	4.1		DVDD	V
OSCIN DC Low-level Input Voltage	OSCdcL	External CLK or active OSC	0		1	V
OSCIN AC Input	OSCdc	DC operation point		DVDD/2		V
OSCIN AC Input Vpp	OSCacvpp	External CLK or active OSC,AC-coupled 0.1μF	2		DVDD	V
Active OSC Power Supply	OSCvp	Active OSC		DVDD		V
Synchronization Signal Width	VFxw		80			μs
CS Signal Wait Signal 1	T(VD-CS)		400			ns
CS Signal Wait Signal 2	T(CS-DT1)		5			μs

Thermal Shutdown

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Operating Temperature of Thermal Shutdown	Ttsd			155		°C
Maximum Hysteresis Error of Thermal Shutdown	ΔTtsd			24		°C

Power Supply Monitor Circuit

Parameter	Symbol	Condition	Min	Typ	Max	Unit
VDD Reset	Vrston			2.40		V
VDD Reset Maximum Hysteresis Error	Vrsthys			0.24		V
MVCCx Reset	VrstFZon			2.34		V
MVCCx Reset Maximum Hysteresis Error	VrstFZhys			0.21		V

FUNCTION DESCRIPTION

1. Serial Interface

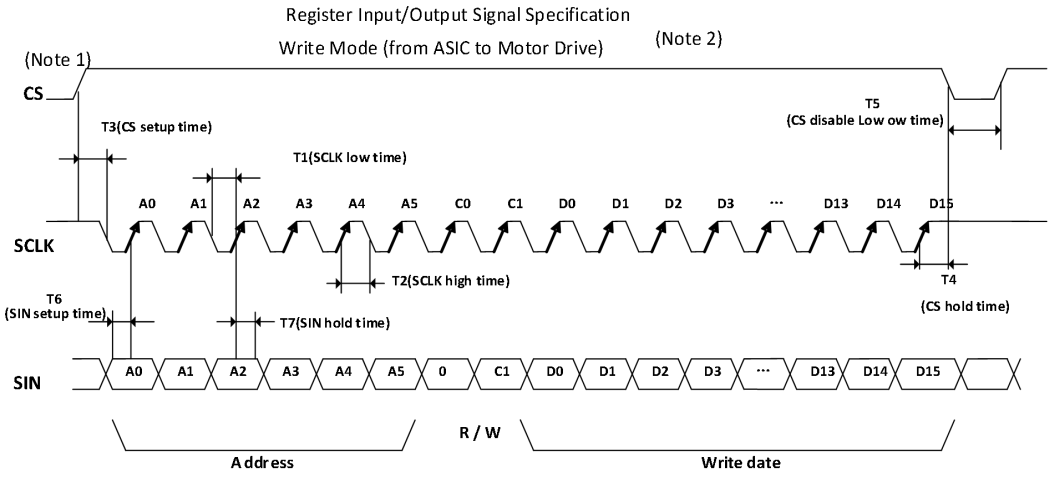


Figure 1. Data Write

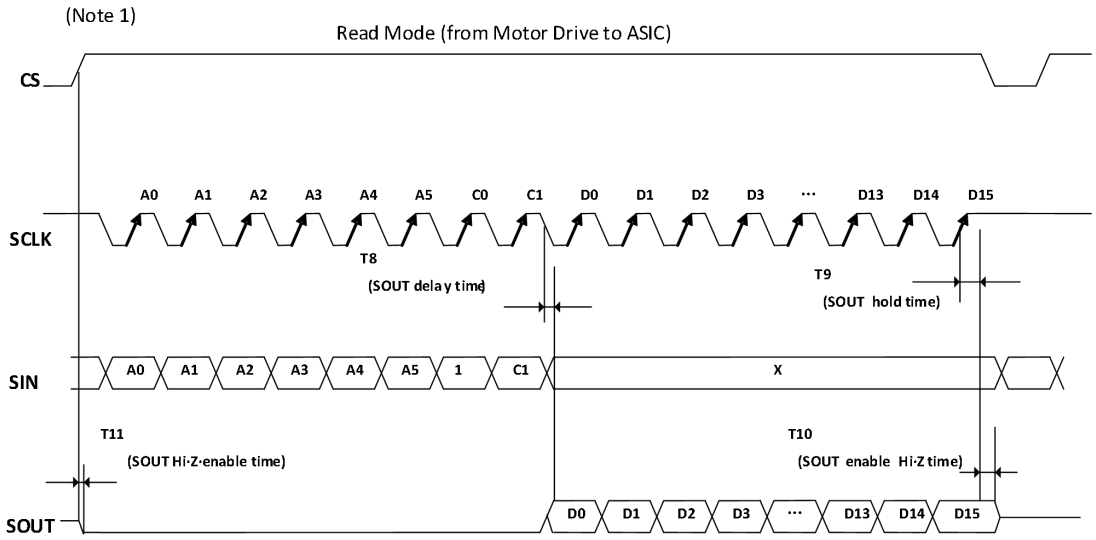


Figure 2. Data Read

Note: 1. In read/write mode, CS starts from 0 by default every cycle.

2. When in write mode, the system clock must be input from OSCIN terminal.

Electrical Parameters (Design Reference)

MVCCx = 5V, DVDD = 5V, AVDD = 3.3V

Unless other noted, Ta = 25°C ±2°C。The characteristics are only design values and only for references.

1.1 Serial Port Input

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Serial clock	Sclock				5	MHz
SCK low time	T1		100			ns
SCK high time	T2		100			ns
CS setup time	T3		60			ns
CS hold time	T4		60			ns
CS disable high time	T5		100			ns
SIN setup time	T6		50			ns
SIN hold time	T7		50			ns
SOUT delay time	T8				60	ns
SOUT hold time	T9		60			ns
SOUT Enable-Hi-Z time	T10				60	ns
SOUT Hi-Z-Enable time	T11				60	ns
Sout C load	Tsc				40	pF

1. The data conversion starts on the rising edge of CS and stops on the falling edge of CS.

2. The data stream unit of a conversion is 24 bits.

3. When the address and data are input from the SIN pin, the clock signal SCK remains consistent under the condition of CS=1.

4. The data is driven into IC on the rising edge of SCK signal. At the same time, when the data is output, it is read out from SOUT pin (the data is output on the rising edge of SCK).

5. SOUT outputs a high impedance state when CS=0, and when CS = 1, outputs "0" unless there is a data read.

6. The control of entire serial interface is reset when CS=0.

1.2 Data Format

0	1	2	3	4	5	6	7
A0	A1	A2	A3	A4	A5	C0	C1

8	9	10	11	12	13	14	15
D0	D1	D2	D3	D4	D5	D6	D7

16	17	18	19	20	21	22	23
D8	D9	D10	D11	D12	D13	D14	D15

C0：Register Read and Write Options: 0: Write Mode, 1: Read Mode

C1：No Use

A5~A0：Register Address

D15~D0 Data Written to Register

1.3 Register Map

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
20H		PWMRESAB [1:0]		PWMMODEAB[4:0]					DT1AB[7:0]							
21H									TEST EN2AB			FZTESTAB[4:0]				
22H			PHMODA[5:0]						DT2A[7:0]							
23H	PPWAβ[7:0]								PPWAα[7:0]							
24H			MICROA [1:0]		Reserved	ENDISA	BRAKEA	CCWCWA	PSUMA[7:0]							
25H	INTCTA[15:0]															
27H			PHMODB[5:0]						DT2B[7:0]							
28H	PPWBβ[7:0]								PPWBα[7:0]							
29H			MICROB [1:0]		Reserved	ENDISB	BRAKEB	CCWCWB	PSUMB[7:0]							
2AH	INTCTB[15:0]															
2CH														IN SWICH	IN1	IN2
0BH	Reserved						MODE SEL_FZ	Reserved	Reserved							
00H		PWMRESCD [1:0]		PWMMODECD[4:0]					DT1CD[7:0]							
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
01H									TEST EN2CD			FZTESTCD[4:0]				
02H			PHMODC[5:0]						DT2C[7:0]							
03H	PPWCβ[7:0]								PPWCα[7:0]							
04H			MICROC [1:0]		Reserved	ENDISC	BRAKEC	CCWCWC	PSUMC[7:0]							
05H	INTCTC[15:0]															
07H			PHMODD[5:0]						DT2D[7:0]							
08H	PPWDβ[7:0]								PPWDα[7:0]							
09H			MICROD [1:0]		Reserved	ENDISD	BRAKED	CCWCWD	PSUMD[7:0]							
0AH	INTCTD[15:0]															

1.4 Register List

Address	Register Name/Bit Width	Description	Page
20h	DT1AB[7:0]	Start Point Wait Time (A,B Stepper Motor)	22
	PWMMODEAB[4:0]	Microstep Output PWM Frequency (A,B Stepper Motor)	23
	PWMRESAB[1:0]	Microstep Output PWM Resolution (A,B Stepper Motor)	23
21h	FZTESTAB[4:0]	PLSA/B Monitor Output Select (A,B Stepper Motor)	32
	TESTEN2AB	TEST Mode Enable 2 (A,B Stepper Motor)	32
22h	DT2A[7:0]	Start Point Excitation Wait Time (A Stepper Motor)	22
	PHMODA[5:0]	Motor Phase Correction (A Stepper Motor)	24
23h	PPWAα[7:0]	Peak Pulse Width of α Phase (A Stepper Motor)	25
	PPWAβ[7:0]	Peak Pulse Width of β Phase (A Stepper Motor)	25
24h	PSUMA[7:0]	Step Number of Stepper Motor (A Stepper Motor)	26
	CCWCWA	Motor Rotation Direction (A Stepper Motor)	27
	BRAKEA	Motor Brake State (A Stepper Motor)	28
	ENDISA	Motor Enable/Disable (A Stepper Motor)	29
	MICROA[1:0]	Sine Wave Microstep (A Stepper Motor)	29
25h	INTCTA[15:0]	Microstep Cycle (A Stepper Motor)	30
27h	DT2B[7:0]	Start Point Excitation Wait Time (B Stepper Motor)	22
	PHMODB[5:0]	Motor Phase Correction (B Stepper Motor)	24
28h	PPWBα[7:0]	Peak Pulse Width of α Phase (B Stepper Motor)	25
	PPWBβ[7:0]	Peak Pulse Width of β Phase (B Stepper Motor)	25
29h	PSUMB[7:0]	Step Number of Stepper Motor (B Stepper Motor)	27
	CCWCWB	Motor Rotation Direction (B Stepper Motor)	27
	BRAKEB	Motor Brake State (B Stepper Motor)	28
	ENDISB	Motor Enable/Disable(B Stepper Motor)	29
	MICROB[1:0]	Sine Wave Microstep (B Stepper Motor)	30
2Ah	INTCTB[15:0]	Microstep Cycle (B Stepper Motor)	30
0Bh	MODESEL_FZ	Synchronous Signal VFX Polarity Select	18
00h	DT1CD[7:0]	Start Point Wait Time (C, D Stepper Motor)	22
	PWMMODECD[4:0]	Microstep Output PWM Frequency (C, D Stepper Motor)	23
	PWMRESCD[1:0]	Microstep Output PWM Resolution (C, D Stepper Motor)	23

Address	Register Name/Bit Width	Description	Page
01h	FZTESTCD[4:0]	PLSC/DMonitor Output Select(C, D Stepper Motor)	32
	TESTEN2CD	TEST Mode Enable 2(C, D Stepper Motor)	32
02h	DT2C[7:0]	Start Point Excitation Wait Time (C Stepper Motor)	22
	PHMODC[5:0]	Motor Phase Correction (C Stepper Motor)	25
03h	PPWCα[7:0]	Peak Pulse Width of α Phase (C Stepper Motor)	26
	PPWCβ[7:0]	Peak Pulse Width of β Phase (C Stepper Motor)	26
04h	PSUMC[7:0]	Step Number of Stepper Motor(C Stepper Motor)	27
	CCWCWC	Motor Rotation Direction (C Stepper Motor)	28
	BRAKEC	Motor Brake State (C Stepper Motor)	28
	ENDISC	Motor Enable/Disable(C Stepper Motor)	29
	MICROC[1:0]	Sine Wave Microstep (C Stepper Motor)	30
05h	INTCTC[15:0]	Microstep Cycle (C Stepper Motor)	30
07h	DT2D[7:0]	Start Point Excitation Wait Time (D Stepper Motor)	23
	PHMODD[5:0]	Motor Phase Correction (D Stepper Motor)	25
08h	PPWDα[7:0]	Peak Pulse Width of α Phase (D Stepper Motor)	26
	PPWDβ[7:0]	Peak Pulse Width of β Phase (D Stepper Motor)	26
09h	PSUMD[7:0]	Step Number of Stepper Motor (D Stepper Motor)	27
	CCWCWD	Motor Rotation Direction (D Stepper Motor)	28
	BRAKED	Motor Brake State (D Stepper Motor)	28
	ENDISD	Motor Enable/Disable(D Stepper Motor)	29
	MICROD[1:0]	Sine Wave Microstep (D Stepper Motor)	30
0Ah	INTCTD[15:0]	Microstep Cycle (D Stepper Motor)	31
2Ch	INSWICH	DC Motor Enable	
	IN1	DC Motor Input Control 1	
	IN2	DC Motor Input Control 2	

All register bit data is initialized at RSTB = 0.

1.5 Register Setup Time

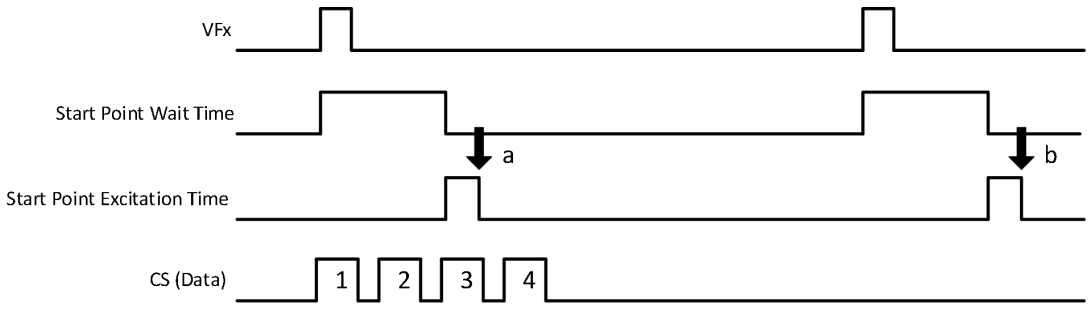
Address	Name	Setup Time
20h	DT1AB[7:0]	VFA or VFB
	PWMMODAB[4:0]	DT1AB
	PWMRESAB[1:0]	DT1AB
21h	FZTESTAB[4:0]	CS
	TESTEN2AB	CS
22h	DT2A[7:0]	DT1AB
	PHMODA[5:0]	DT2A
23h	PPWAα[7:0]	DT1AB
	PPWAβ[7:0]	DT1AB
24h	PSUMA[7:0]	DT2A
	CCWCWA	DT2A
	BRAKEA	DT2A
	ENDISA	DT1AB or DT2A*
	MICROA[1:0]	CS
	PSUMA[7:0]	DT2A
25h	INTCTA[15:0]	DT2A
27h	DT2B[7:0]	DT1AB
	PHMODB[5:0]	DT2B
28h	PPWBα[7:0]	DT1AB
	PPWBβ[7:0]	DT1AB
29h	PSUMB[7:0]	DT2B
	CCWCWB	DT2B
	BRAKEB	DT2B
	ENDISB	DT1AB or DT2B*
	MICROB[1:0]	CS
2Ah	INTCTB[15:0]	DT2B
0Bh	MODESEL_FZ	CS
2Ch	INSWICH	CS
	IN1	CS
	IN2	CS

Address	Name	Setup Time
00h	DT1CD[7:0]	VFC or VFD
	PWMMODECD[4:0]	DT1CD
	PWMRESCD[1:0]	DT1CD
01h	FZTESTCD[4:0]	CS
	TESTEN2CD	CS
02h	DT2C[7:0]	DT1CD
	PHMODC[5:0]	DT2C
03h	PPWCα[7:0]	DT1CD
	PPWCβ[7:0]	DT1CD
04h	PSUMC[7:0]	DT2C
	CCWCWC	DT2C
	BRAKEC	DT2C
	ENDISC	DT1CD or DT2C*
	MICROC[1:0]	DT2C
05h	INTCTC[15:0]	DT2C
07h	DT2D[7:0]	DT1CD
	PHMODD[5:0]	DT2D
08h	PPWDα[7:0]	DT1CD
	PPWDβ[7:0]	DT1CD
09h	PSUMD[7:0]	DT2D
	CCWCWD	DT2D
	BRAKED	DT2D
	ENDISD	DT1CD or DT2D*
	MICROD[1:0]	CS
0Ah	INTCTD[15:0]	DT2D

* 0→1: it works on DT1x ; 1→0: it works on DT2x

In principle, the setup of registers for microsteps should be completed during the time period when the start point is delayed (see figure on page 18). Data written outside the start delay can also be stored in registers. However, if the write operation is executed after the refresh time, the written register will not be valid at the scheduled time. For example, if the updated data 1~4 is written as shown in the following figure after the start point excitation delay, data 1 and 2 are immediately updated at time a, and data 3 and 4 are updated at time b. Even if the data is written continuously, the update time interval is 1 VFx cycle.

For the above reasons, in order to update data timely, the establishment of the register data needs to be completed during the start point delay.



2. VFx Internal Process

In this system, the reflection time and rotation time of stepper motor are respectively based on the rising edge of VFx. The polarity of VFx is set by the following registers.

Register Detail

MODESEL_FZ (VFx Polarity Select)

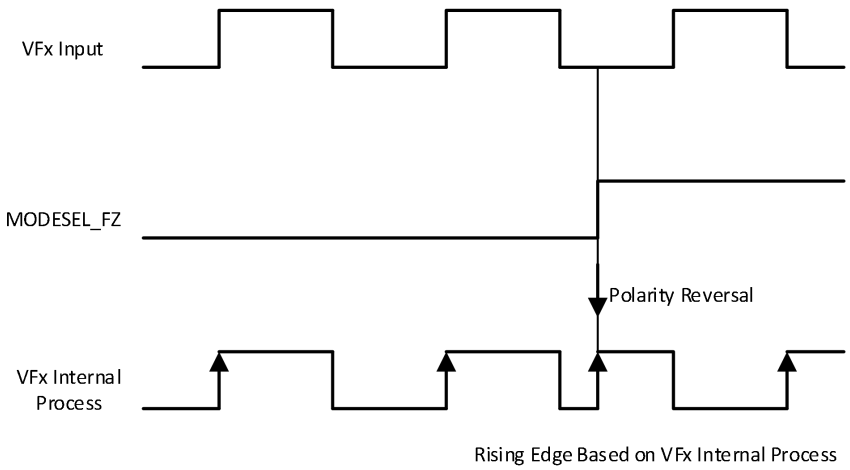
Address			0Bh			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						MODESEL_FZ									

MODESEL_FZ sets the VFx polarity.

When set to "0", the polarity is based on the rising edge of VFx . When set to "1", the polarity is based on the falling edge of VFx .

MODESEL_FZ selects the polarity of input VFx. When MODESEL_FZ is reversed as follows, a VFx signal would be generated and the moment is independent of VFx edge.

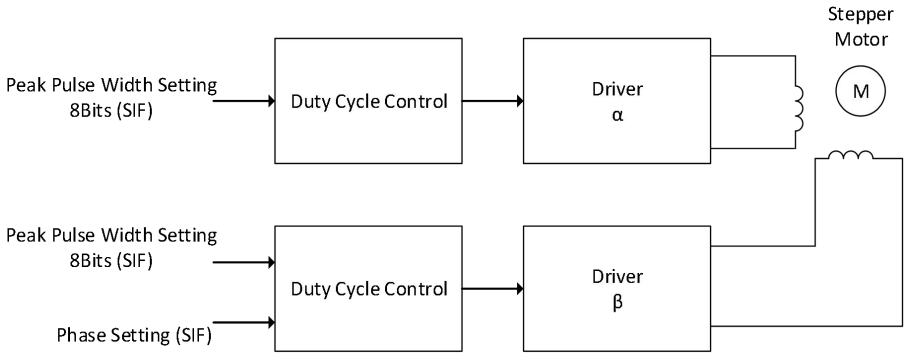
Set Value	VFx Polarity
0	Non-inverting
1	Inverting



Rising Edge Based on VFx Internal Process

3. Stepper Motor Microstep Drive

3.1 Block Diagram



The following settings can be used to perform a series of controls. The following is the description of the motor A: driver α/β. B,C, D perform the same algorithm as the motor A.

Main Setting Parameters:

Phase correction: The phase difference between driver α and driver β is targeted on 90°, and can be adjusted from -22.5° to +21.8°.	—>PHMODx[5:0]
Amplitude Setting: Set the load current of driver α/β independently	—>PPWAα[7:0],PPWAβ[7:0]
PWM Frequency: PWM frequency setting of driver output	—>PWMMODEAB[4:0],PWMRESAB[1:0]
Microstep Number: Can be set to 64,128, 256	—>MICROAB[1:0]
Step cycle: Motor Rotation Speed Setting. It is independent of microstep mode of sine wave.	—>INTCTA[15:0]

3.2 Setup Time of Related Settings

The setup time and related time are shown below.

The setting of addresses 07h to 0Ah is the same as 02h to 05h, so the description of 07h to 0Ah is omitted.If the related registers are updated, a setting load refresh is implemented for each VF cycle. When the same setting is executed with more than 2 VF pulses, it is not necessary to write register data on each VF pulse.

DT1AB[7:0] (Start Point Delay, Address 20h)

Update data time Setting. It must be set after the system hardware reset (48 Pin RSTB: Low → High), before starting the excitation and driving motor (DT1AB ends).

Since this setting is updated every time a VF pulse comes, it is not necessary to write during the start point delay.

PWMMODEAB[4:0], PWMRESAB[1:0] (Microstep Output PWM Frequency, Address 20h)

Set PWM frequency of the microstep output. Need to be set to execute before starting excitation and driving motor (DT1AB ends).

DT2A[7:0] (Start Point Excitation Delay, Address 22h)

Update data time setting. After reset (48 Pin RSTB: Low→High), need to be set to execute before starting excitation and driving motor (DT1AB ends).

PHMODA[5:0] (Phase Correction, Address 22h)

By correcting the phase difference between coils α and β, the driver produces less noise.The appropriate phase correction must be based on the rotation direction and speed. This setting must be changed with the rotation direction (CCWCWA) or the rotation speed (INTCTA).

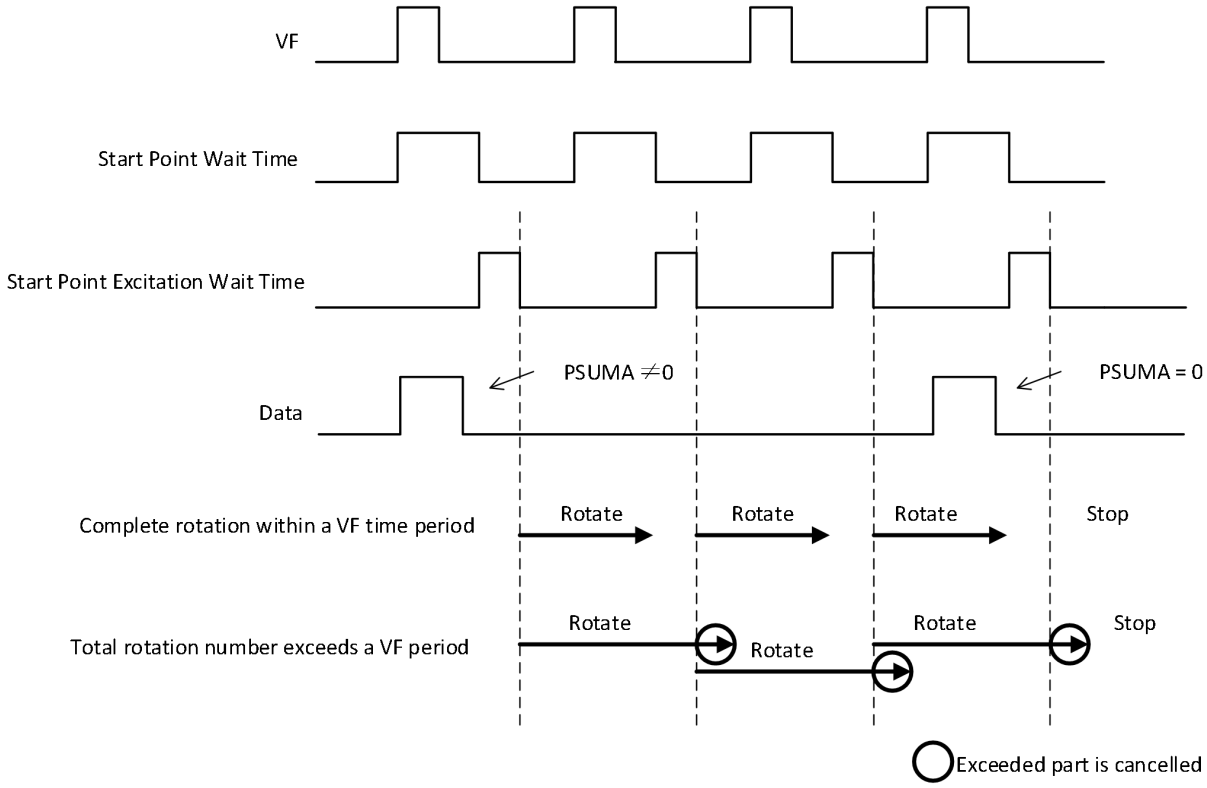
PPWAα[7:0],PPWAβ[7:0] (Peak Pulse Width, Address 23h)

Set the PWM maximum duty cycle. Setting needs to be set before starting the excitation and driving motor (DT1AB ends).

PSUMA[7:0] (Step Number of Stepper Motor, Address 24h)

The rotation number of the motor is set within 1 VFx time interval.

The number of the motor rotation is set when each VFx pulse is input. Therefore, setting the frequency to "0" can stop the motor rotation. When the total number of rotations exceeds the time of 1 VFx pulse, the exceeded part will be canceled.



CCWCWA (Rotation Direction, Address 24h)

Motor rotation direction setting. Just set it before selecting the rotation direction.

BRAKEA (Motor Brake Setting, Address 24h)

Set the current to 0 when braking. This setting is generally used to stop the motor immediately because it is difficult to obtain final position when this setting is performed.

ENDISA (Motor Operation Enable/Disable, Address 24h)

Set the motor work enable. When set to disable, the motor pin outputs high impedance state, and should not be set to disable while the motor is rotating.

MICROA[1:0] (Sine Wave Frequency Division, Address 24h)

Set the frequency division number of sine wave. This setting does not change the number and speed of rotation. It is set only when the rotation speed doesn't reach the demand. After reset (48 Pin RSTB: Low→High), setting is effective.

INTCTA[15:0] (Pulse Period, Address 25h)

Pulse period setting. The rotation speed depends on this setting.

3.3 How to adjust the register value when the stepper motor is driven by microstep

In order to control the stepper motor, it is required to set the number and speed of motor rotation for each VF.The related registers are:

INTCTx[15:0]: Set the time of each step (corresponding to the rotation speed)

PSUMx[7:0]: Total number of rotation steps in each VF period

When the motor is continuously driven in a continuous VF period, the continuous rotation time needs to be set to adapt to the VF period.

The followings are how to calculate INTCTx[15:0] and PSUMx[7:0] when the motor is rotating

(1) Calculate INTCTx[15:0] (determine the motor rotation speed)

$$INTCTx[15:0] \times 768 = OSCIN\ Frequency/Rotation\ Frequency$$

(2) PSUMx[7:0] is calculated by INCTx[15:0]. Don't just only look at the value of PSUMx[7:0].

When the following equation holds, the continuous rotation time and VD time are the same, and the motor achieves uniform rotation.

$$INTCTx[15:0] \times PSUMx[7:0] \times 24 = OSCIN\ Frequency/\ VF\ Frequency$$

(3) After the setting of PSUMx[7:0] is completed, INTCTx[15:0] is recalculated from above formula.

For example, OSCIN Frequency= 27 MHz, VF Frequency = 60Hz

Calculate PSUMx[7:0] and INTCTx[15:0] to make the motor rotate at 800pps (1-2 phase)

800pps is equal to 100Hz, so

$$INTCTx[15:0] = 27MHz / (100Hz \times 768) = 352$$

The corresponding

$$PSUMx[7:0] = 1/(60Hz) \times 27MHz/ (352 \times 24) = 53$$

Recalculate INTCTxx[15:0]

$$INTCTx[15:0] = 1/(60Hz) \times 27MHz/ (53 \times 24) = 354$$

If the left side of the equation in (2) is smaller than the right side, the rotation time is smaller than the VF period, which will cause discontinuous rotation. On the contrary, rotation beyond VF time period will be canceled.

3.4 Register Detail

Motor A,B setting is same as motor C,D and just the register addressed are differential , 0xh and 2xh. Therefore, motor C,D are not described repeatedly. For example, DT1AB is described and DT1CD is not described .

Motor A and motor B are mirroring. The registers of same name are PPWAα and PPWBα. The setting methods of DT2A and DT2B are same and makes no repeated descriptions.

DT1AB[7:0] (Motor A, B Start Point Wait Time)

Address			20h			Initial Value			2Ah						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								DT1AB[7:0]							

DT1CD[7:0] (Motor C, D Start Point Wait Time)

Address			00h			Initial Value			0Ah						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								DT1CD[7:0]							

DT1AB[7:0] sets the delay time of data writing to the system (start point wait time)

The motor can be activated precisely after the start point wait time is flipped from "1" to "0". The start point wait time is calculated from the rising edge of the synchronization video signal (VFx).

Because the start point delay time is mainly used to wait for the serial data to be written. The register value should be set to greater than "0". If it is "0", the corresponding data cannot be updated.

Refer to page 18 for the relationship between VF and the start point wait time.

DT1AB/DT1CD	Start Point Wait
0	Prohibit
1	303.4μs
255	77.4ms
n	n×8192/27MHz

DT2A[7:0] (Start Point Excitation Wait Time Motor A)

Address			22h			Initial Value			03h						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								DT2A[7:0]							

DT2B[7:0] (Start Point Excitation Wait Time Motor B)

Address			27h			Initial Value			03h						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								DT2B[7:0]							

DT2C[7:0] (Start Point Excitation Wait Time Motor C)

Address			02h			Initial Value			03h						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								DT2C[7:0]							

DT2D[7:0] (Start Point Excitation Wait Time Motor D)

Address			07h			Initial Value			03h						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								DT2D[7:0]							

DT2A[7:0] and DT2B[7:0] set the wait delay time before the motor A and the motor B start to rotate.

The motor starts to rotate after the start point excitation wait time is flipped from "1" to "0". The wait delay is calculated from the rising edge of the synchronization signal (VF).

This signal is a separate delay for motor AB.The register value should be set to greater than "0". If it is "0", the corresponding data can't be updated.

Refer to page 18 for the relationship between VF and the start point excitation wait time.

DT2A/B/C/D	Start Point Excitation Wait
0	Prohibit
1	303.4μs
255	77.4ms
n	n×8192/27MHz

PWMMODEAB[4:0] (Microstep Output PWM Frequency)

Address			20h			Initial Value			1Ch						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
			PWMMODEAB[4:0]												

PWMMODECD[4:0] (Microstep Output PWM Frequency)

Address			00h			Initial Value			1Ch						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
			PWMMODECD[4:0]												

PWMRESAB[1:0] (Microstep Output PWM Resolution)

Address			20h			Initial Value			1						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	PWMRESAB														

PWMRESCD[1:0] (Microstep Output PWM Resolution)

Address			00h			Initial Value			1						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	PWMRESCD														

PWMMODEAB[4:0] sets the microstep output PWM frequency by setting the frequency division of system clock OSCIN.

PWMMODEAB[4:0] can be set in the range of 1 to 31. The frequency of PWM wave is same when PWMMODE = 0 and PWMMODE = 1.

PWM frequency is decided by PWMRESAB[1:0] and PWMMODEAB[4:0].

The PWM frequency is calculated by the following formula

PWM Frequency = OSCIN Frequency / ((PWMMODE × 23) × 2PWMRES)

When OSCIN=27MHz, PWM frequency is shown in the following table (kHz) :

PWMMODE	PWMRESAB/CD			PWMMODE	PWMRESAB/CD		
AB/CD	0	1	2	AB/CD	0	1	2
1	3375.0	1687.5	843.8	17	198.5	99.3	49.6
2	1687.5	843.8	421.9	18	187.5	93.8	46.9
3	1125.0	526.5	281.3	19	177.6	88.8	44.4
4	843.8	421.9	210.9	20	168.8	84.4	42.2
5	675.0	337.5	168.8	21	160.7	80.4	40.2
6	526.5	281.3	140.6	22	153.4	76.7	38.4
7	482.1	241.1	120.5	23	146.7	73.4	36.7
8	421.9	210.9	105.5	24	140.6	70.3	35.2
9	375.0	187.5	93.8	25	135.0	67.5	33.8
10	337.5	168.8	84.4	26	129.8	64.9	32.5
11	306.8	153.4	76.7	27	125.0	62.5	31.3
12	281.3	140.6	70.3	28	120.5	60.3	30.1
13	259.6	129.8	64.9	29	116.4	58.2	29.1
14	241.1	120.5	60.3	30	112.5	56.3	28.1
15	225.0	112.5	56.3	31	108.9	54.4	27.2
16	210.9	105.5	52.7				

PHMODA[5:0] (Motor A Phase Correction)

Address			22h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		PHMODA[5:0]													

PHMODB[5:0] (Motor B Phase Correction)

Address			27h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		PHMODB[5:0]													

PHMODC[5:0] (Motor C Phase Correction)

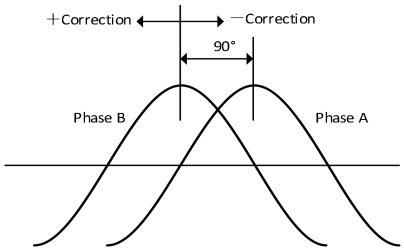
Address			02h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		PHMODC[5:0]													

PHMODD[5:0] (Motor D Phase Correction)

Address			07h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		PHMODD[5:0]													

The current phase difference of α and β phase H-bridge current in motor A is set by PHMODA[5:0].The default value is 90° and set 1 unit to 0.7°. Meanwhile, the data can be subject to positive and negative deviation.

PHMODA/B/C/D	Phase Correction Number
000000	±0°
000001	+0.7°
011111	+21.80°
100000	-22.50°
111111	-0.7°
Damping Unit	360°/512 = 0.70°



The phase difference between the stepper motor coils is generally 90°. However, due to different motors or process deviations, the phase difference will also be shifted by 90°. Therefore, even if the phase difference of the drive waveform current is 90°, but the motor itself is not 90° difference, it will produce torque ripple, and the noise still exists.

The main purpose of this setting is to reduce the torque ripple caused by motor changes.

PPWAα[7:0] (Peak Pulse Width of α Phase for Driver A)

PPWAβ[7:0] (Peak Pulse Width of β Phase for Driver A)

Address			23h			Initial Value			0,0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PPWAβ[7:0]								PPWAα[7:0]							

PPWBα[7:0] (Peak Pulse Width of α Phase for Driver B)

PPWBβ[7:0] (Peak Pulse Width of β Phase for Driver B)

Address			28h			Initial Value			0,0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PPWBβ[7:0]								PPWBα[7:0]							

PPWCα[7:0] (Peak Pulse Width of α Phase for Driver C)

PPWCβ[7:0] (Peak Pulse Width of β Phase for Driver C)

Address			03h			Initial Value			0,0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PPWCβ[7:0]									PPWCα[7:0]						

PPWDα[7:0] (Peak Pulse Width of α Phase for Driver D)

PPWDβ[7:0] (Peak Pulse Width of β Phase for Driver D)

Address			08h			Initial Value			0,0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PPWDβ[7:0]									PPWDα[7:0]						

The maximum duty cycle of the PWM wave is set by PPWAx[7:0] to PPWDx[7:0], which determines the position of the peak output current from driver A to D.

The maximum duty cycle is calculated by the following equation:

Driver X Maximum Duty Cycle = PPWxx/ (PWMMODExx × 8)

When PPWxx = 0, coil current is 0.

For example, when PPWAx[7:0]=200, PWMMODEAB[4:0]=28, maximum duty cycle is:

200 / (28 × 8) = 0.89

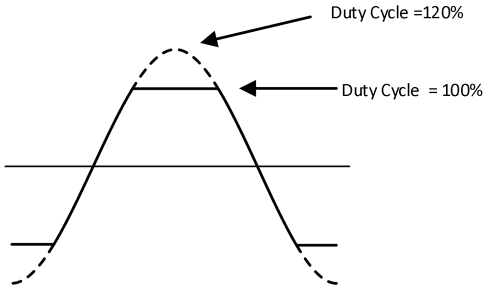
Depending on the values of PWMMODExx and PPWxx, the maximum duty cycle may exceed 100%.

Of course, the duty cycle cannot exceed 100% in fact and the peak point of sine wave will be truncated as shown in the following figure.

For example, when PWMMODExx = 10, PPWxx = 96,

Maximum Duty Cycle = 90/(10 × 8) = 120%

The waveform of the target current is shown as follows:



PSUMA[7:0] (Step Number of Motor A)

Address			24h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								PSUMA[7:0]							

PSUMB[7:0] (Step Number of Motor B)

Address			29h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								PSUMB[7:0]							

PSUMC[7:0] (Step Number of Motor C)

Address			04h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								PSUMC[7:0]							

PSUMD[7:0] (Step Number of Motor D)

Address			09h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								PSUMD[7:0]							

PSUMA[7:0] and PSUMB[7:0] respectively set the total step number of the motor A and motor B.

If want to stop the motor, set PSUMx[7:0]=0.

Register Value PSUM	Total Step Number		
	64 Microstep	128 Microstep	256 Microstep
0	0	0	0
1	2	4	8
255	510	1020	2040
n	2n	4n	8n

As long as the maximum duty cycle of PWM wave is not set as "0", when PSUMx[7:0]=0, the motor can keep in the release state.

An example to know the meaning of setting :

When PSUMA[7:0]=8 is set, run 2x8=16 steps in 64 microstep mode, i.e. 16/64=1/4 sine cycle. Similarly, in 128 and 256 microstep modes, it is also a quarter of the period of sine wave.

CCWCWA (Rotation Direction of Motor A)

Address			24h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
							CCWCWA								

CCWCWB (Rotation Direction of Motor B)

Address			29h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
							CCWCWB								

CCWCWC (Rotation Direction of Motor C)

Address			04h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
							CCWCWC								

CCWCWD (Rotation Direction of Motor D)

Address			09h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
							CCWCWD								

CCWCWA and CCWCWB respectively set the rotation direction of the motor A and motor B.

Direction Definition:

Set Value	Motor Rotation Direction
0	Forward
1	Reverse

BRAKEA (Brake State of Motor A)

Address			24h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						BRAKEA									

BRAKEB (Brake State of Motor B)

Address			29h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						BRAKEB									

BRAKEC (Brake State of Motor C)

Address			04h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						BRAKEC									

BRAKED (Brake State of Motor D)

Address			09h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						BRAKED									

BRAKEA and BRAKEB set the brake mode of the motor A and B respectively.

Set Value	Motor Brake
0	Normal State
1	Brake State

In brake state, the two upper-side PMOS FETs of H bridge are all turned on. The brake mode cannot be used in normal operation and can only be used during emergency shutdown. It is recommended to be used in abnormal state.

ENDISA (Motor A Enable/Disable)

Address			24h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
					ENDISA										

ENDISB (Motor B Enable/Disable)

Address			29h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
					ENDISB										

ENDISC (Motor C Enable/Disable)

Address			04h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
					ENDISC										

ENDISD (Motor D Enable/Disable)

Address			09h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
					ENDISD										

ENDISA and ENDISB respectively set the output control of the motor A and motor B.

When ENDISx = 0, motor outputs high impedance state. However, internal excitation position counter still keeps counting at ENDISxx=0. Therefore, when you want to stop the motor in normal state, set PSUMx[7:0] = 0 instead of ENDISx = 0.

Set Value	Motor Output State
0	Output Off (High-impedance State)
1	Output On

MICROA (Sine Wave Frequency Division of Motor A)

Address			24h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		MICROA													

MICROB (Sine Wave Frequency Division of Motor B)

Address			29h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		MICROB													

MICROC (Sine Wave Frequency Division of Motor C)

Address			04h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		MICROC													

MICROD (Sine Wave Frequency Division of Motor D)

Address			09h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		MICROD													

MICROA and MICROB set the frequency division of sine wave for motor A and motor B respectively.

The 64 division waveform is shown on page 31.

MICROx	Frequency Division
00	256
01	256
10	128
11	64

INTCTA[15:0] (Step Cycle of Motor A)

Address			25h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
INTCTA[15:0]															

INTCTB[15:0] (Step Cycle of Motor B)

Address			2Ah			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
INTCTB[15:0]															

INTCTC[15:0] (Step Cycle of Motor C)

Address			05h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
INTCTC[15:0]															

INTCTD[15:0] (Step Cycle of Motor D)

Address			0Ah			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
INTCTD[15:0]															

INTCTA[15:0] and INTCTB[15:0] respectively set a microstep cycle of the motor A and motor B .

Register Value	Microstep Cycle		
	64 Microstep	128 Microstep	256 Microstep
0	0	0	0
1	444ns	222ns	111ns
Max	29.1ms	14.6ms	7.3ms
n	12n/27MHz	6n/27MHz	3n/27MHz

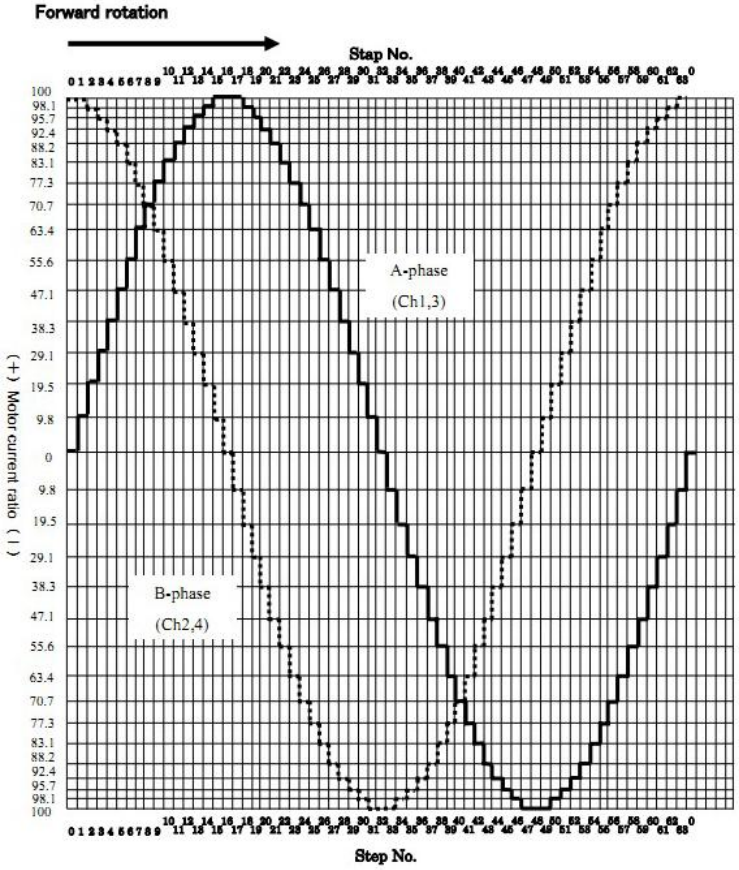
When INTCTA[15:0]=0, as long as PWM maximum duty cycle is not 0, the motor will remain in release state .

Examples: When INTCTA[15:0]=400, step cycle in 64 microstep:

12×400/27MHz=0.178ms

Therefore, the period of each sine wave is 0.178x64=11.4ms (87.9Hz). Similarly, in 128 microstep and 256 microstep it is also 11.4ms.

Stepper Motor Drive (64 Microstep Current Curve)



4. Test Signal

FZTESTAB[4:0] (Test Signal Output Setting of Motor A,B)

Address			21h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
											FZTESTAB[4:0]				

TESTEN2AB (ABTest Set 2)

Address			21h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								TESTEN2AB							

FZTESTCD[4:0] (Test Signal Output Setting of Motor C,D)

Address			01h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
											FZTESTCD[4:0]				

TESTEN2CD (CDTest Setting 2)

Address			01h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								TESTEN2CD							

FZTESTAB[4:0] selects the test signals output by PLSA and PLSB.

FZTESTCD[4:0] selects the test signals output by PLSC and PLSD.

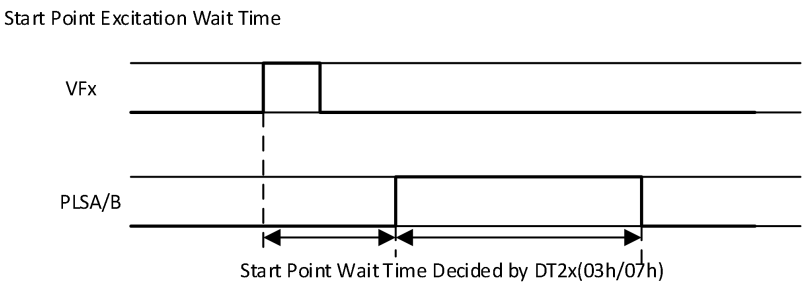
TESTEN2 need to be set to "1" to allow the test signal output.

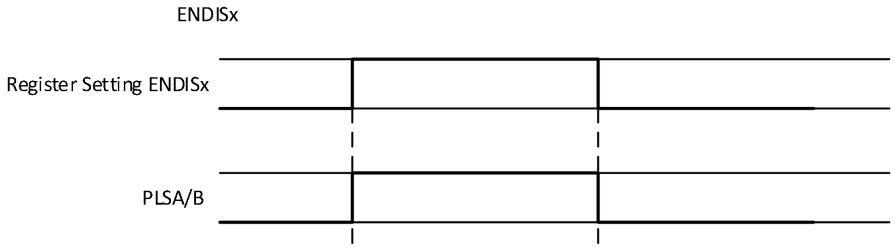
The following table is the output setting signal.

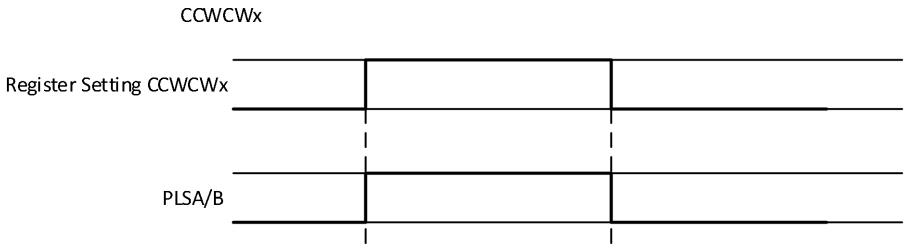
Register Value	Setting	A Cycle		Description
21h/01h	FZTEST AB/CD[4:0]	PLSA/C	PLSB/D	
81H	1	Start Point Wait Time	0	H Bridge Output for Start Point Wait Time
82H	2	Start Point Excitation Wait Time A	Start Point Excitation Wait Time B	H Bridge Output for Start Point Excitation Wait Time
83H	3	ENDISA	ENDISB	ENDISx Setting

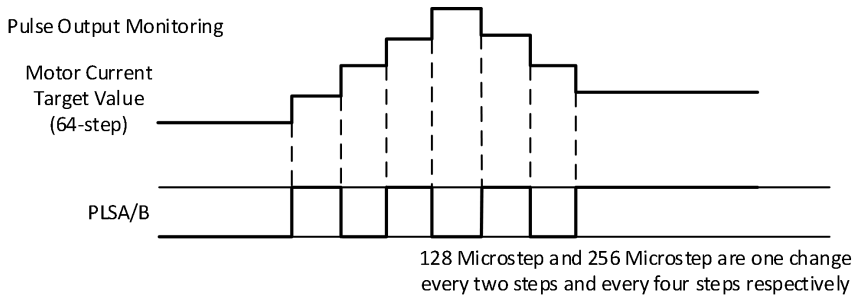
Register Value	Setting	A Cycle		Description
21h/01h	FZTEST AB/CD[4:0]	PLSA/C	PLSB/D	
84H	4	CCWCWA	CCWCWB	CCWCWx Setting
85H	5	Monitor Output Pulse A	Monitor Output Pulse B	“H”/“L” change in 64 microstep when motor is rotating
86H	6	PWM Cycle Monitoring	0	PWM Period Signal of Motor Output
87H	7	Complete Pulse Output of Motor A	Complete Pulse Output of Motor B	Total Rotation Time
8BH	11	“H” Bridge PMOS1 A	“H”Bridge NMOS1 A	Monitor α Bridge of Motor A
8CH	12	“H”Bridge PMOS2 A	“H”Bridge NMOS2 A	
8DH	13	“H”Bridge PMOS3 A	“H”Bridge NMOS3 A	Monitor β Bridge of Motor A
8EH	14	“H”Bridge PMOS4 A	“H”Bridge NMOS4 A	
8FH	15	“H”Bridge PMOS1 B	“H”Bridge NMOS1 B	Monitor α Bridge of Motor B
90H	16	“H”Bridge PMOS2 B	“H”Bridge NMOS2 B	
91H	17	“H”Bridge PMOS3 B	“H”Bridge NMOS3 B	Monitor β Bridge of Motor B
92H	18	“H”Bridge PMOS4 B	“H”Bridge NMOS4 B	
96H	22	Step for Motor A, Tsin/4	Step for Motor A,Tsin/8	Motor A operate one and half step clock waveform
98H	24	Step for Motor B, Tsin/4	Step for Motor B,Tsin/8	Motor B operate one and half step clock waveform

The relevant waveforms are described as follows:

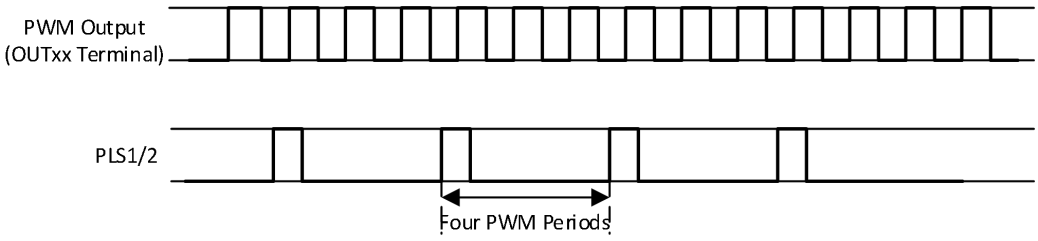




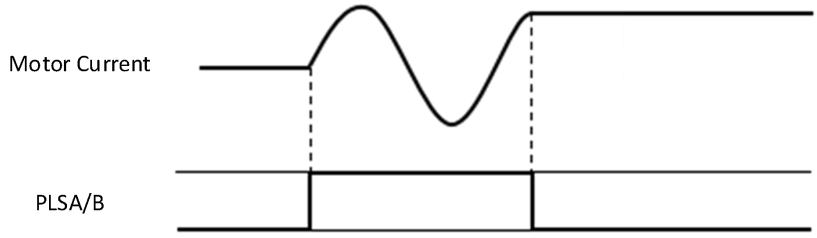




PWM Circle Monitoring

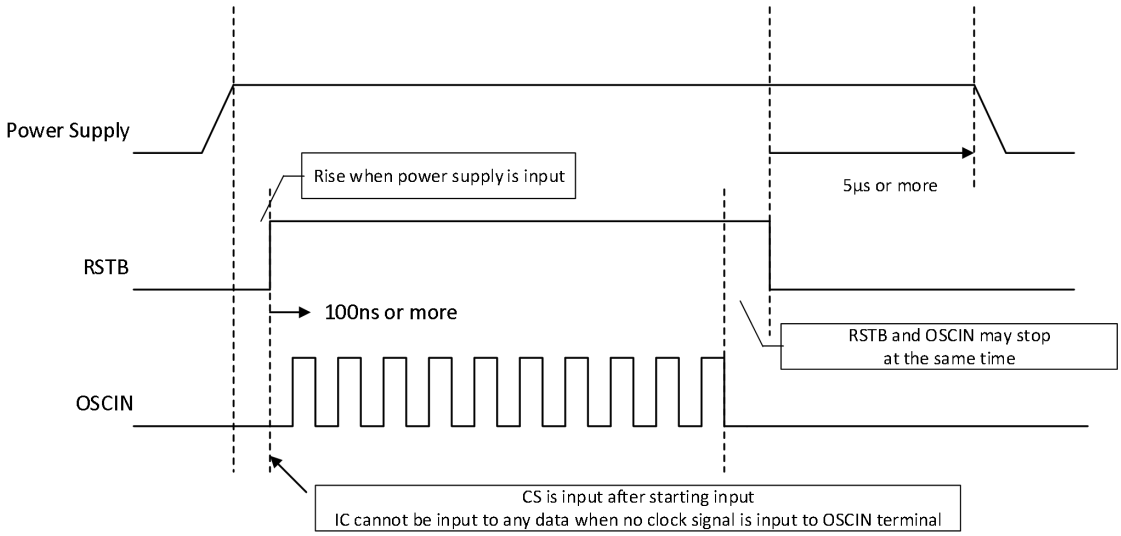


Complete Pulse Output



(1) Start and Finish Timing

The start and finish timing of power signal, RSTB and OSCIN are shown in the following figure.



(2) Input Capacitance of Input Pin

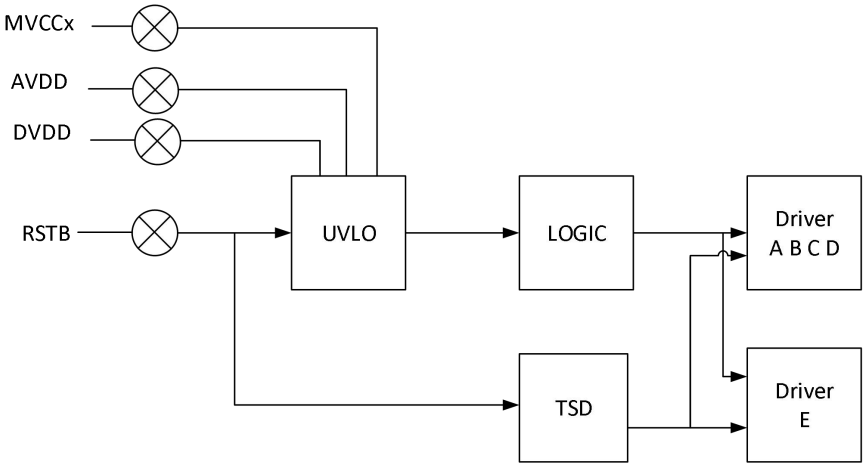
The capacitance of input pin is 10pF or less.

(3) OSCIN, VFx Moment

Once VFx signal is synchronized with OSCIN, the VFx and OSCIN signals have no constraint on input time.

5. Reset/Protection Circuit

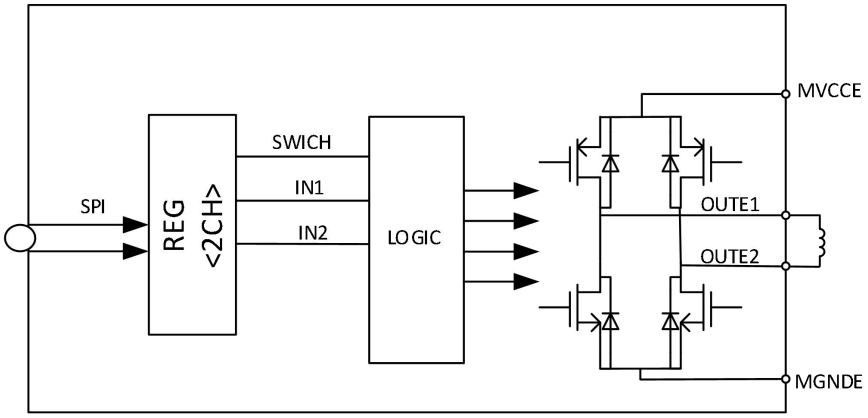
The following figure shows the relationship between RSTB, UVLO, TSD and other circuits.



The corresponding specifications are shown in the following table

	Setting	Motor Output
RSTB	Disable	Logic Reset -> Output Shutdown
Thermal Shutdown (TSD)	×	Output Shutdown
Undervoltage Lockout (UVLO)	×	Logic Reset -> Output Shutdown

6. DC Driver E Circuit



DC motor (used in IR-CUT in camera) driver adopts SPI input control method. H bridge output id controlled by writing register 2CH.

SWICH Register: Register REG_2CH<2> bit2, Power-up Default '0''

IN1 Register: Register REG_2CH<1> bit1, Power-up Default '0'

IN2 Register: RegisterREG_2CH<0> bit0 Power-up Default '0'

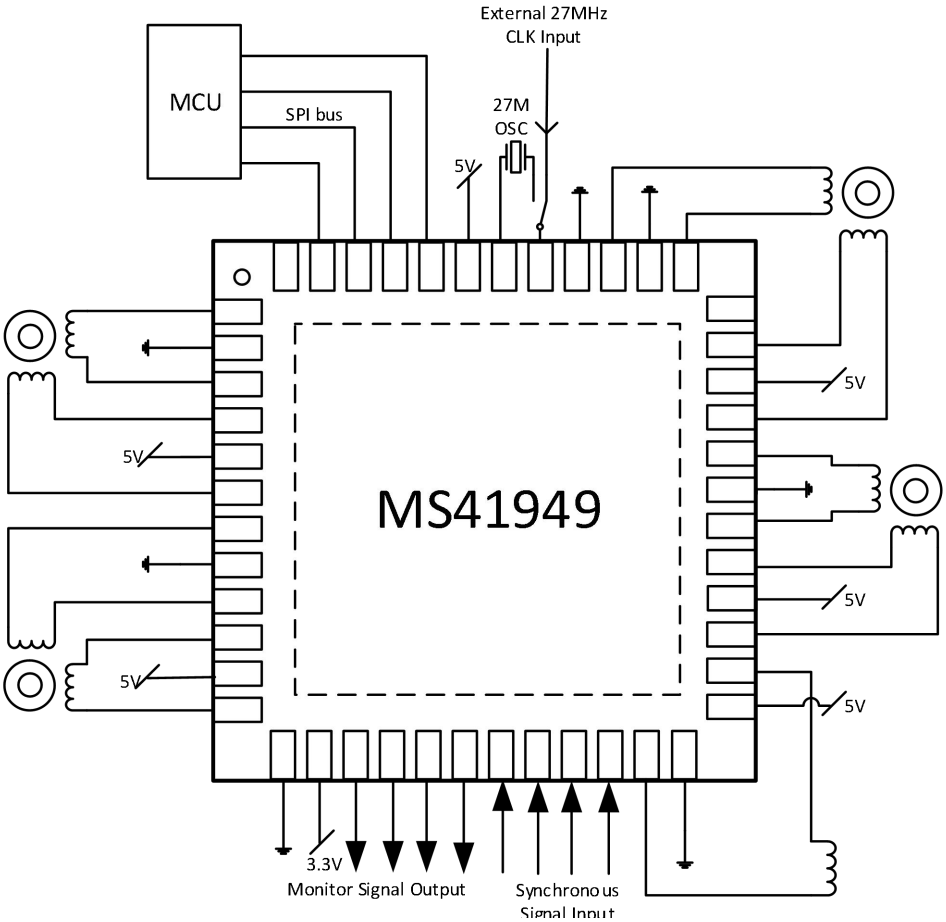
Truth table of input and output is as follows:

Equivalent Control Signal for Internal Signal		Register Control Mode	Output		
IN1	IN2	Lower 8bits of 2CH Register	OUTE1	OUTE2	Motor State
0	0	0004h	L	L	Brake
0	1	0005h	L	H	Reverse
1	0	0006h	H	L	Forward
1	1	0007h	Z	Z	High -impedance

Delay Time of DC Motor in SPI Mode

22 data and 3 control bits are written every writing in SPI mode. The transmission delay is about Tsclk×25 from writing register2CH to actual work of control time. If the serial clock of writing data is 0.5MHz, the delay time is 25×1/0.5M=50μs. And the maximum output frequency of H bridge is 10kHz.

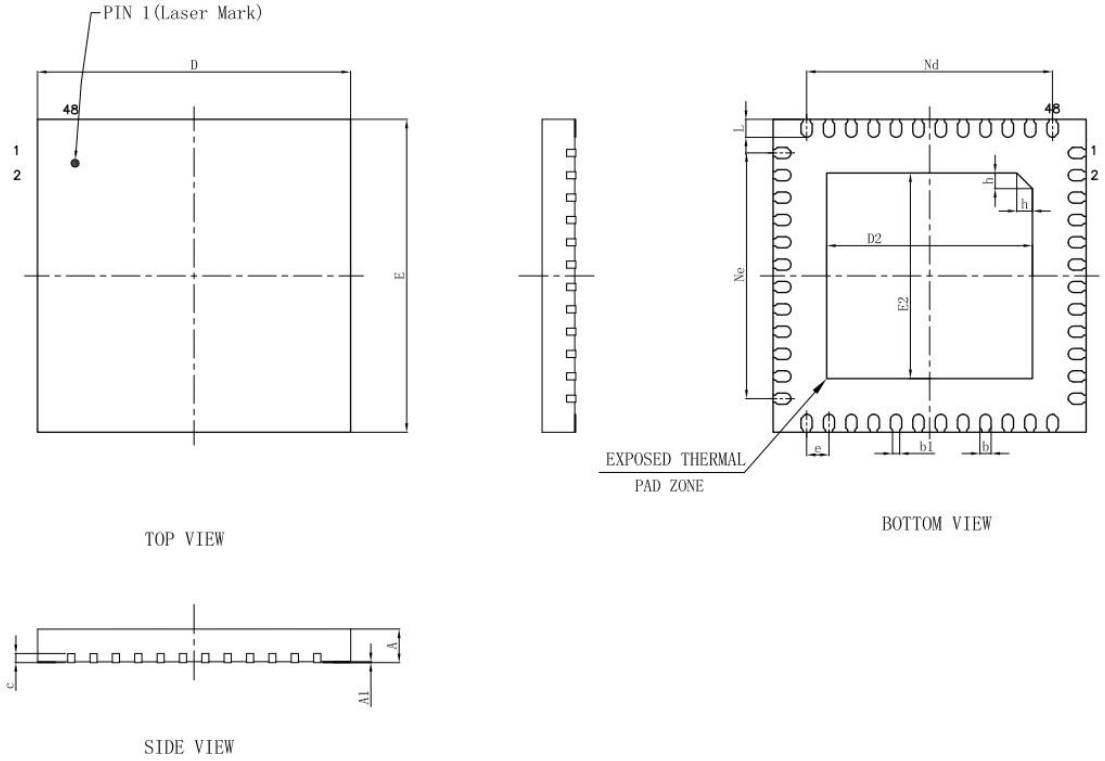
TYPICAL APPLICATION DIAGRAM



1. The MS41949 has back thermal pad and it must be grounded in large power applications.
2. Amplification and SMIT circuits are built between OSCIN pin (PIN41) and OSCOUT(PIN42). Therefore, low-cost passive crystal oscillator can be used between OSCIN and OSCOUT. OSCIN pin is connected with active crystal oscillator output or other CLK output of MCU (OSCOUT floating) . The demands for DC and AC inputs are differential. The detailed parameters refer to page 9.

PACKAGE OUTLINE DIMENSIONS

QFN48 (07X07) (Back Thermal Pad)



Symbol	Dimensions In Millimeters		
	Min	Typ	Max
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.18	0.25	0.30
b1		0.16REF	
c	0.18	0.20	0.23
D	6.90	7.00	7.10
E	6.90	7.00	7.10
Nd		5.50BSC	
Ne		5.50BSC	
D2	4.50	4.60	4.70
e		0.5BSC	
E2	4.50	4.60	4.70
L	0.35	0.40	0.45
h	0.30	0.35	0.40

MARKING and PACKAGING SPECIFICATIONS

1. Marking Drawing Description

Product Name: MS41949

Product Code： XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specifications

Device	Package	Piece/Reel	Reel/Box	Piece /Box	Box/Carton	Piece/Carton
MS41949	QFN48	2000	1	2000	8	16000

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MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

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