Application Note: SA59401

Bidirectional, Zero-Drift, High-accuracy Analog-to-Digital Converter With Internal Reference and Temperature Sensor

Advance Design Specification

General Description

The SA59401 is a precision, low power, analog-to-digital converter (ADC) that provides all features necessary to measure the most common sensor signals in a MSOP-10 package.

The SA59401 integrates a 16-bit high precision ADC, oscillator and high-accuracy temperature sensor. SA59401 can perform conversions at data rates up to 890 samples per second (SPS). The input ranges from -128 mV to +127.996mV.

The SA59401 integrates an input multiplexer (MUX) allows to measure two differential or four single-ended inputs. An integrated high-accuracy temperature sensor can be used for system-level temperature monitoring or cold-junction compensation for thermocouples. These features, along with a wide power supply range from 2.7 V to 5.5 V, make the SA59401 ideally suited for power- and space-constrained, sensor-measurement applications.

The SA59401 operates either in continuous-conversion mode, or in a single-shot mode that automatically powers down after a conversion. Single-shot mode significantly reduces current consumption during idle periods. Data are transferred through a serial peripheral interface (SPI™). The SA59401 is specified from –40°C to +125°C.

Ordering Information

SA59401□(□□□)

Package Code

Optional Spec Code

Ordering Number	Package type	Note
SA59401FBP	MSOP10	--

Features

- Wide Supply Range: 2.7V to 5.5V
- Low Current Consumption:
  - Continuous Mode: 350μA
  - Single-Shot Mode: Automatic Power Down
- Programmable Data Rate: 8 SPS to 890 SPS
- Single-Cycle Settling
- Internal Low-Drift Voltage Reference
- Internal Temperature Sensor:
  - 1.5°C (Maximum) Error: 0°C to 70°C
- Internal Oscillator
- Four Single-Ended or Two Differential Inputs
- MSOP-10 Package

Applications

- Temperature Measurement:
  - Thermocouple Measurement
  - Cold-Junction Compensation
  - Thermistor Measurement
- Portable Instrumentation
- Factory Automation and Process Controls

Typical Application

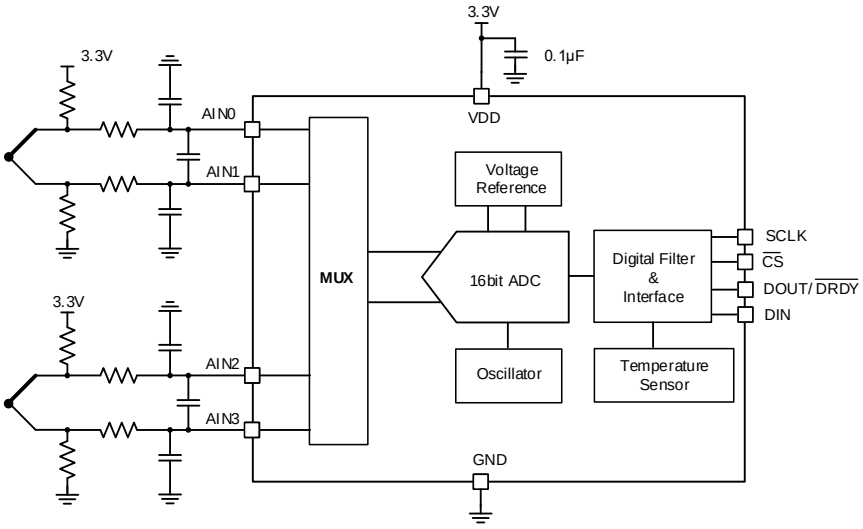
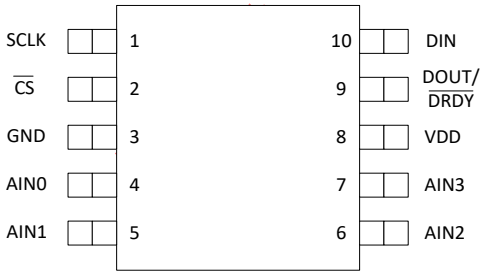


Figure1. Typical Application Circuit

Pinout (Top View)



(MSOP-10)

Top Mark: **FQN*xyz*, (**Device code: FQN, ***x=year code, y=week code, z= lot number code*****)**

Pin No.	Pin Name	Pin Description
1	SCLK	Serial clock input.
2	$\overline{CS}$	Chip select; active low. Connect to GND if not used.
3	GND	Ground.
4	AIN0	Analog input 0. Leave unconnected or tie to VDD if not used.
5	AIN1	Analog input 1. Leave unconnected or tie to VDD if not used.
6	AIN2	Analog input 2. Leave unconnected or tie to VDD if not used.
7	AIN3	Analog input 3. Leave unconnected or tie to VDD if not used.
8	VDD	Power supply. Connect a 100nF power supply decoupling capacitor to GND.
9	DOUT/$\overline{DRDY}$	Serial data output combined with data ready; active low.
10	DIN	Serial data input.

Absolute Maximum Ratings (Note 1)

VDD ---------- -0.3V to 6V
AIN0/ AIN1/ AIN2/ AIN3 ---------- -0.3V to VDD + 0.3V
DIN/ DOUT/$\overline{\text{DRDY}}$/ SCLK/ $\overline{\text{CS}}$ ---------- -0.3V to VDD + 0.3V
Input current into any pin ---------- -10mA to +10mA
Power Dissipation, PD @ T_A = 25°C---------- TBD W
Package Thermal Resistance (Note 2)

θ_{JA} ---------- TBD °C/W

θ_{JC} ---------- TBD °C/W

Junction Temperature Range---------- -40°C to 150°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions

VDD_S ---------- 2.7V to 5.5V
AIN0/ AIN1/ AIN2/ AIN3 ---------- 0V to VDD
DIN/ DOUT/$\overline{\text{DRDY}}$/ SCLK/ $\overline{\text{CS}}$ ---------- 0V to VDD
Operating ambient temperature ---------- -40°C to 125°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

T_A = 25°C, VDD = 3.3V, data rate (DR) = 8 SPS, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Analog Inputs						
Input Range			-128		+127.996	mV
Common-mode Range			0		VCC	
Common-mode Input Impedance				100		MΩ
Differential Input Impedance				710		kΩ
System Performance						
Resolution		no missing codes	16			Bits
Data Rate	DR		8		890	SPS
Data Rate Variation		All data rates	-10		+10	%
Output Noise				TBD		
Integral Nonlinearity	INL	DR = 8 SPS (Note 1)			1	LSB
Offset Error	V_{OS}	differential inputs		±10	±50	µV
		single-ended inputs		±20		
Offset Drift		T_A = – 40°C to +125°C		0.02		µV/°C
Offset Power-Supply Rejection	PSRR	2.7V≤VS≤5.5V		5		µV/V
Offset Channel Match		Match between any two inputs		0.25		LSB
Gain Error (Note 2)		T_A = 25°C		0.01	0.15	%
Gain Drift (Note 2, 3)					40	ppm/°C
Gain Power-supply Rejection				10		ppm/V
Gain Channel Match		Match between any two inputs		0.01	0.1	%
Common-mode Rejection Ratio	CMRR			120		dB
Temperature Sensor						
Temperature Range			-40		+125	°C
Temperature Resolution				0.125		°C/LSB
Accuracy		T_A = 0°C to 70°C		0.25	±1.5	°C
		T_A = – 40°C to +125°C		0.5	±2	°C
		vs supply		0.125	±1	°C/V
Digital Input/output						
High-level Input Voltage	V_{IH}		1		VDD	V
Low-level Input Voltage	V_{IL}		GND		0.5	
Low-level Output Voltage	V_{OL}	I_{OL} = 1 mA	GND		0.4	
Hysteresis				250		mV
Input Leakage, High	I_H	V_{IH} = 5.5 V	-10		10	µA
Input Leakage, Low	I_L	V_{IL} = GND	-10		10	
Power Supply						
Operating Supply Range			2.7		5.5	V
Quiescent Current	I_Q	Operating, T_A = 25°C		350	420	µA
		Operating			500	
		Power down mode, T_A = 25°C		5	10	
		Power down mode			35	

Note 1: Best-fit INL; covers 99% of full-scale.

Note 2: Includes all errors from onboard PGA and voltage reference.

Note 3: Maximum value specified by characterization.

Detailed Description

Overview

The SA59401 is a precision, low power delta-sigma (ΔΣ) analog-to-digital converter (ADC). The SA59401 consists of a ΔΣ ADC core, an internal voltage reference, a clock oscillator, and an SPI. This device is also a highly linear and accurate temperature sensor. All of these features are intended to reduce required external circuitry and improve performance. The Functional Block Diagram section shows the SA59401 functional block diagram.

The SA59401 ADC core measures a differential signal, VIN, that is the difference of V(INP) and V(INN). The converter core consists of a differential, switched-capacitor ΔΣ modulator followed by a digital filter. This architecture results in a very strong attenuation in any common-mode signals. Input signals are compared to the internal voltage reference. The digital filter receives a high-speed bit stream from the modulator and outputs a code proportional to the input voltage.

The SA59401 has two available conversion modes: single-shot and continuous-conversion. In single-shot mode, the ADC performs one conversion of the input signal upon request and stores the value to an internal conversion register. The device then enters a power-down state. This mode is intended to provide significant power savings in systems that require only periodic conversions or when there are long idle periods between conversions. In continuous-conversion mode, the ADC automatically will begin a conversion of the input signal as soon as the previous conversion is completed. The rate of continuous conversion is equal to the programmed data rate. Data can be read at any time and always reflect the most recently completed conversion.

Functional Block Diagram

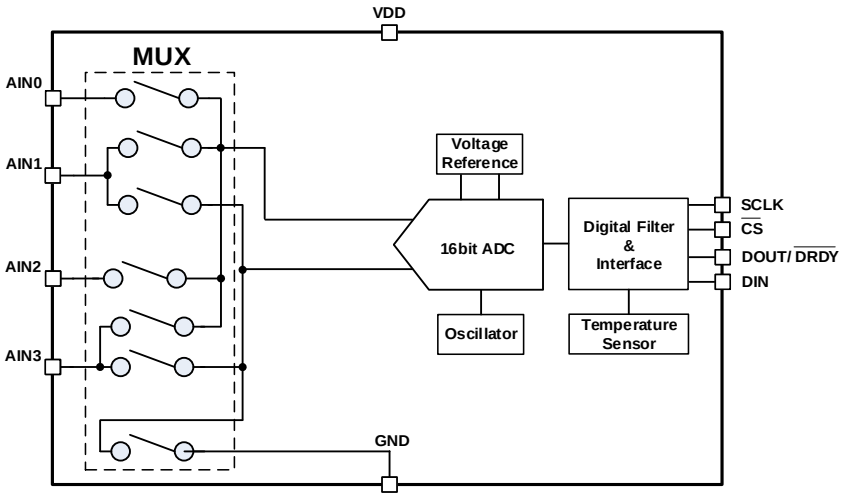


Figure 2. Block Diagram

Multiplexer

The SA59401 contains an input multiplexer (MUX), either four single-ended or two differential signals can be measured. Additionally, AIN0, AIN1, and AIN2 can be measured differentially to AIN3. The multiplexer is configured by bits MUX[2:0] in the Config register. When single-ended signals are measured, the negative input of the ADC will be internally connected to GND by a switch within the multiplexer.

When measuring single-ended inputs, the device will not output negative codes. These negative codes indicate negative differential signals; that is, (V(INP) – V(INN)) < 0. Electrostatic discharge (ESD) diodes to VDD and GND protect the SA59401 inputs. To prevent the ESD diodes from turning on, it is necessary to keep the absolute voltage on any input within the range between GND – 0.3 V to VDD + 0.3 V

If the voltages on the input pins can possibly violate these conditions, use external Schottky diodes and series resistors can limit the input current to safe values (see the Absolute Maximum Ratings table).

Also, overdriving one unused input on the SA59401 may affect conversions currently taking place on other input pins. If overdriving unused inputs is possible, clamp the signal with external Schottky diodes.

Full-Scale Range (FSR) and LSB Size

The SA59401 is suitable for High-accuracy occasions.

The full-scale range is ±128 mV. Table 1 show the FSR together with the corresponding LSB size. From the full-scale voltage by the formula shown below.

$$LSB = FSR / 2^{16}$$

Table 1. SA59401 Full-Scale Range and Corresponding LSB Size

FSR	LSB Size
±128mV	3.90625μV

Temperature Sensor

The SA59401 offers an integrated precision temperature sensor. To enable the temperature sensor mode, set bit TS_MODE = 1 in the Config register. Temperature data are represented as a 12-bit result that is left-justified within the 16-bit conversion result. Data are output starting with the most significant byte (MSB). When reading the two data bytes, the first 12 bits will be used for indicating the temperature measurement result. One 12-bit LSB equals 0.125°C. Negative numbers are represented in binary twos complement format, as shown in Table 2.

Table 2. 12-Bit Temperature Data Format

Temperature (°C)	Digital Output (Binary)	Hex
128	0 100 0000 0000	400
127.875	0 011 1111 1111	3FF
100	0 011 0010 0000	320
80	0 010 1000 0000	280
75	0 010 0101 1000	258
50	0 001 1001 0000	190
25	0 000 1100 1000	0C8
0.25	0 000 0000 0010	002
0	0 000 0000 0000	000
–0.25	1 111 1111 1110	FFE
–25	1 111 0011 1000	F38
–40	1 110 1100 0000	EC0

Converting from Temperature to Digital Codes

For positive temperatures:

Twos complement is not performed on positive numbers. Therefore, simply convert the number to binary code in a 12-bit, left justified format with the MSB = 0 to denote the positive sign.

Example: 50°C / (0.125°C/count) = 400 = 190h = 0001 1001 0000

For negative temperatures:

Generate the twos complement of a negative number by complementing the absolute binary number and adding 1. Then, denote the negative sign with the MSB = 1.

Example: |–25°C| / (0.125/count) = 200 = 0C8h = 0000 1100 1000

Twos complement format: 1111 0011 01111 + 1 = 1111 0011 100

Converting from Digital Codes to Temperature

To convert from digital codes to temperature, first check whether the MSB is a 0 or a 1. If the MSB is a 0, simply multiply the decimal code by 0.125°C to obtain the result. If the MSB = 1, subtract 1 from the result and complement all of the bits. Then, multiply the result by –0.125°C.

Example: The device reads back 258h: 258h has an MSB = 0. 258h × 0.125°C = 600 × 0.125°C = +75°C

Example: The device reads back F38h: F38h has an MSB = 1. Subtract 1 and complement the result: F38h → C8h

C8h × (–0.125°C) = 200 × (–0.125°C) = –25°C

Device Functional Modes

Reset and Power-Up

When the SA59401 powers up, the device will be reset. As part of the reset process, the SA59401 sets all bits in the Config register to the respective default settings. By default, the SA59401 enters a power-down state at start-up. The device interface and digital blocks are active, but no data conversions are performed. The initial power-down state of the SA59401 relieves systems with tight power-supply requirements from encountering a surge during power-up.

Operating Modes

The SA59401 operates in one of two modes: continuous-conversion or single-shot. The MODE bit in the Config register selects the respective operating mode.

Single-Shot Mode and Power-Down

When the MODE bit in the Config register is set to 1, the SA59401 will enter a power-down state, and operate in single-shot mode. This power-down state is the default state for the SA59401 when power is first applied. Although powered down, the device still responds to commands. The SA59401 remains in this power-down state until a 1 is written to the single-shot (SS) bit in the Config register. When the SS bit is asserted, the device will power up, reset the SS bit to 0, and starts a single conversion. When conversion data are ready for retrieval, the device will power down again. Writing a 1 to the SS bit while a conversion is ongoing has no effect. To switch to continuous-conversion mode, write a 0 to the MODE bit in the Config register.

Continuous-Conversion Mode

In continuous-conversion mode (MODE bit set to 0), the SA59401 continuously performs conversions. When a conversion completes, the SA59401 will place the result in the Conversion register and immediately begins another conversion. To switch to single-shot mode, write a 1 to the MODE bit in the Config register, or reset the device.

Duty Cycling for Low Power

The noise performance of a ΔΣ ADC generally improves when lowering the output data rate because more samples of the internal modulator are averaged to yield one conversion result. In applications where power consumption is critical, the improved noise performance at low data rates may not be required. For these applications, the SA59401 supports duty cycling that can yield significant power savings by periodically requesting high data-rate readings at an effectively lower data rate.

For example, an SA59401 in power-down state with a data rate set to 890 SPS can be operated by a microcontroller that instructs a single-shot conversion every 125ms (8 SPS). A conversion at 890 SPS only requires approximately 1.1ms; therefore, the SA59401 enters power-down state for the remaining 123.9ms. The duty cycling rate is completely arbitrary and is defined by the master controller. The SA59401 offers lower data rates that do not implement duty cycling and also offers improved noise performance, if required.

Programming

Serial Interface

The SPI-compatible serial interface consists of either four signals ($\overline{CS}$, SCLK, DIN, and DOUT/$\overline{DRDY}$), or three signals (SCLK, DIN, and DOUT/$\overline{DRDY}$, with $\overline{CS}$ tied low). The interface is used for reading conversion data, read from and write to registers, and control device operation.

Chip Select ($\overline{CS}$)

The chip select pin ($\overline{CS}$) selects the SA59401 for SPI communication. This feature is useful when multiple devices share the same serial bus. Keep $\overline{CS}$ low for the duration of the serial communication. When $\overline{CS}$ is taken high, the serial interface will reset, SCLK will be ignored, and DOUT/$\overline{DRDY}$ will enter a high-impedance state. In this state, DOUT/$\overline{DRDY}$ cannot provide data-ready indication. In situations where multiple devices are present and DOUT/$\overline{DRDY}$ must be monitored, lower $\overline{CS}$ periodically. At this point, the DOUT/$\overline{DRDY}$ pin either immediately goes high to indicate that no new data are available, or immediately goes low to indicate that new data are present in the Conversion register and are available for transfer. New data can be transferred at any time without concern of data corruption. When a transmission starts, the current result will be locked into the output shift register and does not change until the communication completes. This system avoids any possibility of data corruption.

Serial Clock (SCLK)

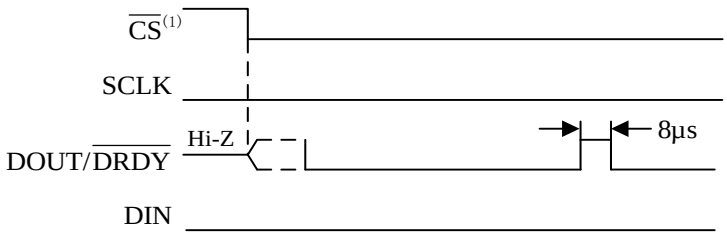
The serial clock pin (SCLK) features a Schmitt-triggered input and is used for clock data on the DIN and DOUT/$\overline{DRDY}$ pins into and out of the SA59401. Even though the input has hysteresis, keep SCLK as clean as possible to prevent glitches from accidentally shifting the data. To reset the serial interface, hold SCLK low for 28ms, and the next SCLK pulse starts a new communication cycle. Use this time-out feature to recover communication when a serial interface transmission is interrupted. When the serial interface is idle, hold SCLK low.

Data Input (DIN)

The data input pin (DIN) is used along with SCLK to send data to the SA59401. The device latches data on DIN at the SCLK falling edge. The SA59401 never drives the DIN pin.

Data Output and Data Ready (DOUT/DRDY)

The data output and data ready pin (DOUT/$\overline{DRDY}$) is used with SCLK to read conversion and register data from the SA59401. Data on DOUT/$\overline{DRDY}$ are shifted out on the SCLK rising edge. DOUT/DRDY is also used for indicating that a conversion is complete and new data are available. This pin transitions low when new data are ready for retrieval. DOUT/$\overline{DRDY}$ is also able to trigger a microcontroller to start reading data from the SA59401. In continuous-conversion mode, DOUT/$\overline{DRDY}$ transitions high again 8μs before the next data ready signal (DOUT/DRDY low) if no data are retrieved from the device. This transition is shown in Figure 3. Complete the data transfer before DOUT/$\overline{DRDY}$ returns high.



(1) $\overline{CS}$ can be held low if the SA59401 does not share the serial bus with another device. If $\overline{CS}$ is low, DOUT/$\overline{DRDY}$asserts low indicating new data are available.

Figure 3. DOUT/DRDY Behavior without Data Retrieval in Continuous-Conversion Mode

When $\overline{CS}$ is high, DOUT/$\overline{DRDY}$ is configured by default with a weak internal pullup resistor. This feature reduces the risk of DOUT/$\overline{DRDY}$ floating near midsupply and causing leakage current in the master device. To disable this pullup resistor and place the device into a high-impedance state, set the PULL_UP_EN bit to 0 in the Config register.

Data Format

The SA59401 provides 16 bits of data in binary twos complement format that is left justified within the 16-bit data word. A positive full-scale (+FS) input produces an output code of 7FFFh and a negative full-scale (–FS) input produces an output code of 8000h. The output clips at these codes for signals that exceed full-scale. Table 3 summarizes the ideal output codes for different input signals. Table 3 summarizes the ideal output codes for different input signals respectively.

Table 3. Input Signal versus Ideal Output Code

Input Signal, VIN (INP – INN)	Ideal Output Code
≥ +FS (2^{15} – 1) / 2^{15}	7FFFh
+FS / 2^{15}	0001h
0	0
–FS / 2^{15}	FFFFh
≤ –FS	8000h

Data Retrieval

Data are written to and read from the SA59401 in the same manner for both single-shot and continuous conversion modes, without having to issue any commands. The operating mode for the SA59401 is selected by the MODE bit in the Config register.

Set the MODE bit to 0 to put the device in continuous-conversion mode. In continuous-conversion mode, the device is constantly starting new conversions even when $\overline{CS}$ is high.

Set the MODE bit to 1 for single-shot mode. In single-shot mode, a new conversion only starts by writing a 1 to the SS bit.

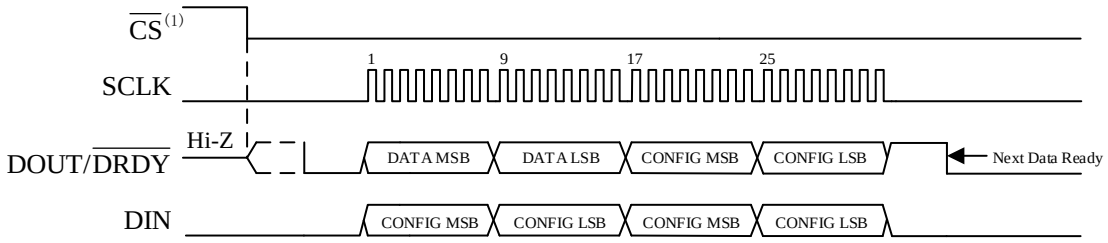
The conversion data are always buffered, and retain the current data until replaced by new conversion data. Therefore, data can be read at any time without concern of data corruption. When DOUT/$\overline{DRDY}$ asserts low, indicating that new conversion data are ready, the conversion data are read by shifting the data out on DOUT/DRDY. The MSB of the data (bit 15) on DOUT/$\overline{DRDY}$ is clocked out on the first SCLK rising edge. At the same time that the conversion result is clocked out of DOUT/$\overline{DRDY}$, new Config register data are latched on DIN on the SCLK falling edge.

The SA59401 also offers the possibility of direct readback of the Config register settings in the same data transmission cycle. One complete data transmission cycle consists of either 32 bits (when the Config register data readback is used) or 16 bits (only used when the $\overline{CS}$ line can be controlled and is not permanently tied low).

32-Bit Data Transmission Cycle

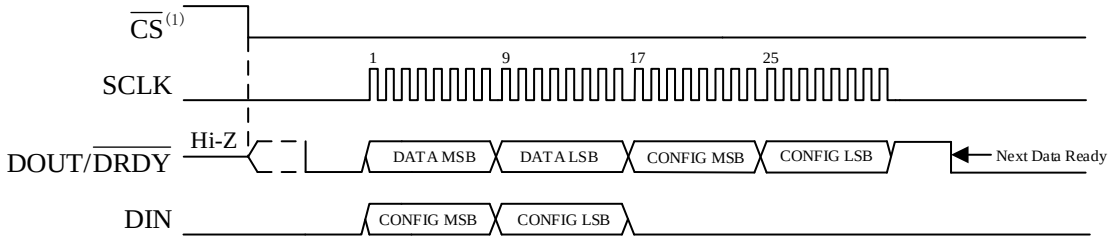
The data in a 32-bit data transmission cycle consist of four bytes: two bytes for the conversion result, and an additional two bytes for the Config register readback. The device always reads the MSB first.

Write the same Config register setting twice during one transmission cycle as shown in Figure 4. If convenient, write the Config register setting once during the first half of the transmission cycle, and then hold the DIN pin either low (as shown in Figure 5) or high during the second half of the cycle. If no update to the Config register is required, hold the DIN pin either low or high during the entire transmission cycle. The Config register setting written in the first two bytes of a 32-bit transmission cycle is read back in the last two bytes of the same cycle.



(1) $\overline{CS}$ can be held low if the SA59401 does not share the serial bus with another device. If $\overline{CS}$ is low, DOUT/$\overline{DRDY}$ asserts low indicating new data are available.

Figure 4. 32-Bit Data Transmission Cycle with Config Register Readback



(1) $\overline{CS}$ can be held low if the SA59401 does not share the serial bus with another device. If $\overline{CS}$ is low, DOUT/$\overline{DRDY}$ asserts low indicating new data are available.

Figure 5. 32-Bit Data Transmission Cycle: DIN Held Low

16-Bit Data Transmission Cycle

If Config register data are not required to be read back, the SA59401 conversion data can be clocked out in a short 16-bit data transmission cycle, as shown in Figure 6. Take $\overline{CS}$ high after the 16th SCLK cycle to reset the SPI interface. The next time $\overline{CS}$ is taken low, data transmission starts with the currently buffered conversion result on the first SCLK rising edge. If DOUT/$\overline{DRDY}$ is low when data retrieval starts, the conversion buffer will already be updated with a new result. Otherwise, if DOUT/$\overline{DRDY}$ is high, the same result from the previous data transmission cycle is read.

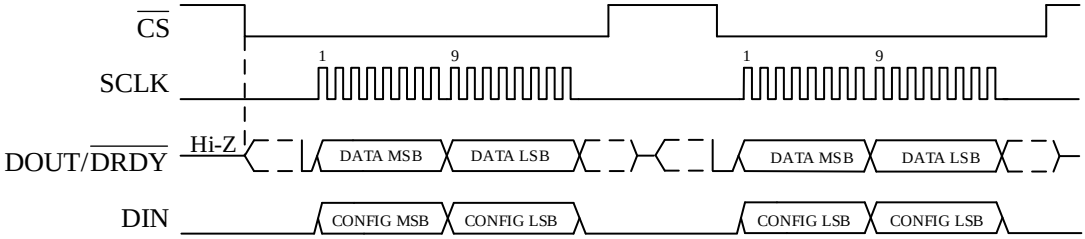


Figure 6. 16-Bit Data Transmission Cycle

Register Maps

The SA59401 has two registers that are accessible through the SPI. The Conversion register contains the result of the last conversion. The Config register allows the user to change the SA59401 operating modes and query the status of the devices.

Conversion Register [reset = 0000h]

The 16-bit Conversion register contains the result of the last conversion in binary twos complement format. Following power up, the Conversion register is cleared to 0, and remains 0 until the first conversion is complete. The register format of SA59401 is shown in Figure 7.

Figure 7. Conversion Register

15	14	13	12	11	10	9	8
D15	D14	D13	D12	D11	D10	D9	D8
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 4. Conversion Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	D[15:0]	R	0000h	16-bit conversion result

Config Register [reset = 0F8Bh]

The 16-bit Config register can be used to control the SA59401 operating mode, input selection, data rate, full- scale range, and temperature sensor mode. The register format is shown in Figure 8.

Figure 8. Config Register

15	14	13	12	11	10	9	8
SS	MUX[2:0]			PGA[2:0]			MODE
R/W-0h	R/W-0h			R/W-2h			R/W-1h
7	6	5	4	3	2	1	0
DR[2:0]			TS_MODE	PULL_UP_EN		NOP[1:0]	Reserved
R/W-4h			R/W-0h	R/W-1h		R/W-1h	R-1h

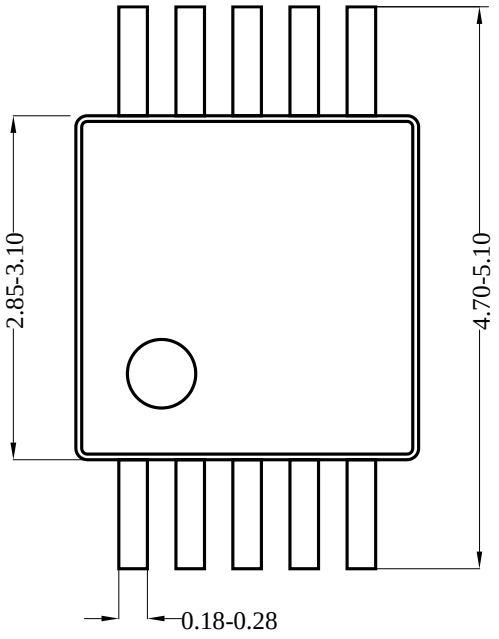
LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5. Config Register Field Descriptions

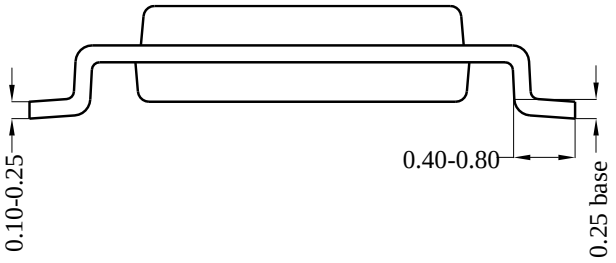
Bit	Field	Type	Reset	Description
15	SS	R/W	0h	**Single-shot conversion start** This bit is used to start a single conversion. SS can only be written when in power-down state and has no effect when a conversion is ongoing. When writing: 0 = No effect 1 = Start a single conversion (when in power-down state) Always reads back 0 (default).
14:12	MUX[2:0]	R/W	0h	**Input multiplexer configuration** These bits configure the input multiplexer. 000 = INP is AIN0 and INN is AIN1 (default) 001 = INP is AIN0 and INN is AIN3 010 = INP is AIN1 and INN is AIN3 011 = INP is AIN2 and INN is AIN3 100 = INP is AIN0 and INN is GND 101 = INP is AIN1 and INN is GND 110 = INP is AIN2 and INN is GND 111 = INP is AIN3 and INN is GND
11:9	PGA[2:0]	R	7h	111

8	MODE	R/W	1h	**Device operating mode** This bit controls the SA59401 operating mode. 0 = Continuous-conversion mode 1 = Power-down and single-shot mode (default)
7:5	DR[2:0]	R/W	4h	**Data rate** These bits control the data-rate setting. 000 = 8 SPS 001 = 15 SPS 010 = 30 SPS 011 = 61 SPS 100 = 121 SPS (default) 101 = 239 SPS 110 = 468 SPS 111 = 890 SPS
4	TS_MODE	R/W	0h	**Temperature sensor mode** This bit configures the ADC to convert temperature or input signals. 0 = ADC mode (default) 1 = Temperature sensor mode
3	PULL_UP_EN	R/W	1h	**Pullup enable** This bit enables a weak internal pullup resistor on the DOUT/$\overline{\text{DRDY}}$ pin only when $\overline{\text{CS}}$ is high. When enabled, an internal 400-kΩ resistor connects the bus line to supply. When disabled, the DOUT/ DRDY pin floats. 0 = Pullup resistor disabled on DOUT/ DRDY pin 1 = Pullup resistor enabled on DOUT/ $\overline{\text{DRDY}}$ pin (default)
2:1	NOP[1:0]	R/W	1h	**No operation** The NOP[1:0] bits control whether data are written to the Config register or not. For data to be written to the Config register, the NOP[1:0] bits must be 01. Any other value results in a NOP command. DIN can be held high or low during SCLK pulses without data being written to the Config register. 00 = Invalid data; do not update the contents of the Config register 01 = Valid data; update the Config register (default) 10 = Invalid data; do not update the contents of the Config register 11 = Invalid data; do not update the contents of the Config register
0	Reserved	R	1h	**Reserved** Writing either 0 or 1 to this bit has no effect. Always reads back 1.

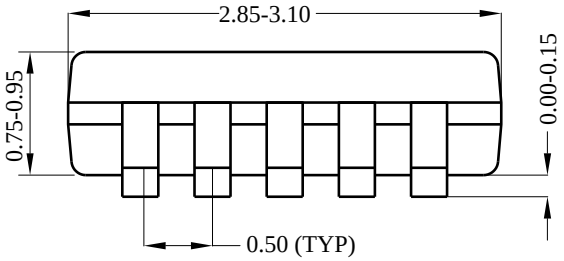
MSOP10 Package outline & PCB layout



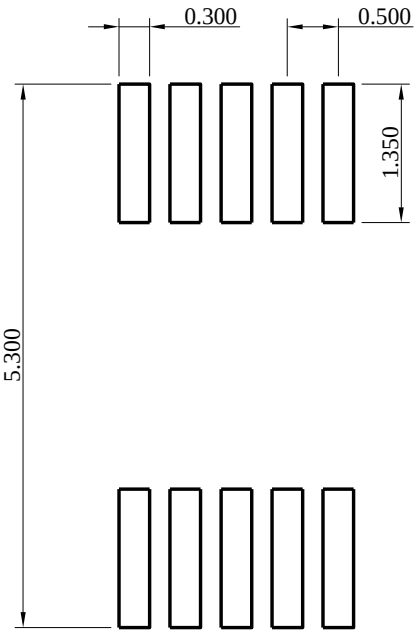
Top view



Side view



Front view



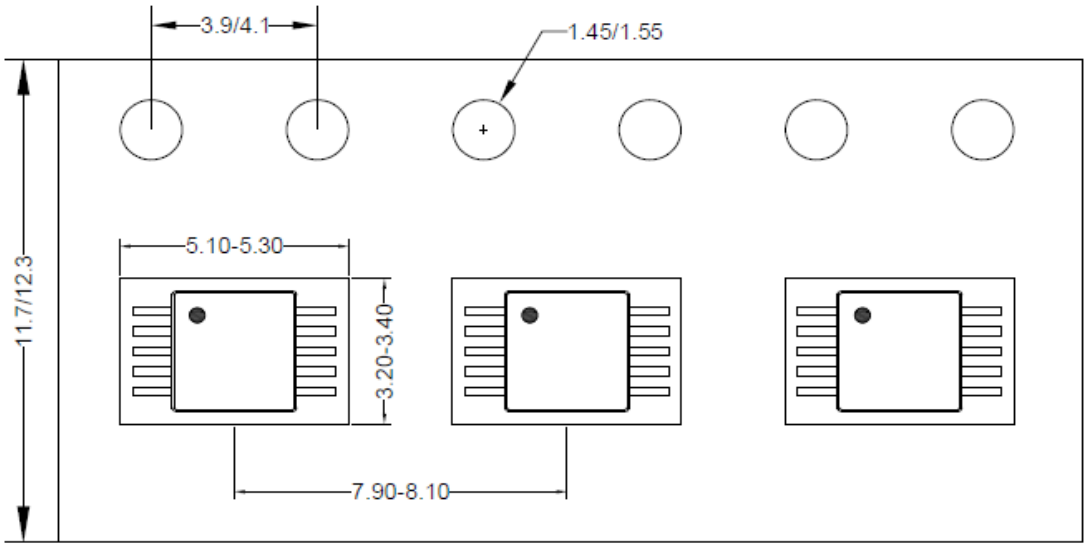
Recommended Pad Layout

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Taping & Reel Specification

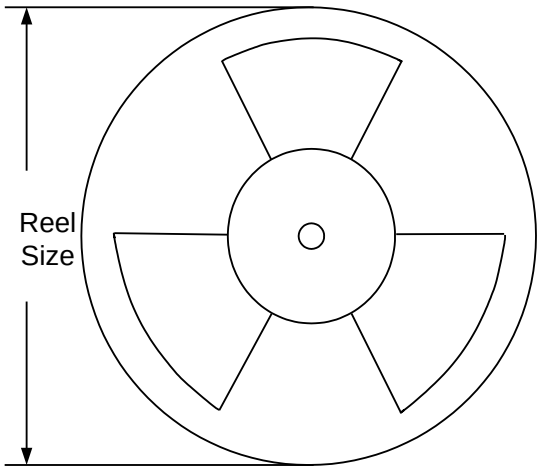
1. Taping Orientation

MSOP10



Feeding direction ⟶

2. Carrier Tape & Reel Specification for Packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
MSOP10	12	8	13"	400	400	3000

3. Others: NA