SQ35702C

Boost/Flyback Current Mode Controller

General Description

SQ35702C is a fixed frequency and current mode controller for Boost/ Flyback/Sepic topology. UVLO and OTP protection are available to protect IC. Cycle by cycle current limit (1V) and over current limit (1.1V) for ISEN.Typical 170uA starting up current and 1.5mA operating supply current exclude MOS driving current. Flexible frequency and minimum off time set by FS pin and up to 250 kHz switching frequency. Up to 1A GATE sourcing and sinking capability for driving large external MOSFET.SQ35702C is available in a SO8 package.

Features

- 10-22V input voltage range
- ±2% accuracy for REF and FB reference
- Flexible frequency and minimum off time set by FS pin and up to 500kHz switching frequency
- Cycle by cycle current limit(1V) and over current limit (1.1V) for ISEN
- Package:SO8

Application

- Switch mode power supplies (SMPS)
- DC-to-DC converters
- Power modules
- Battery-operated Power Supply Unit

Typical Applications

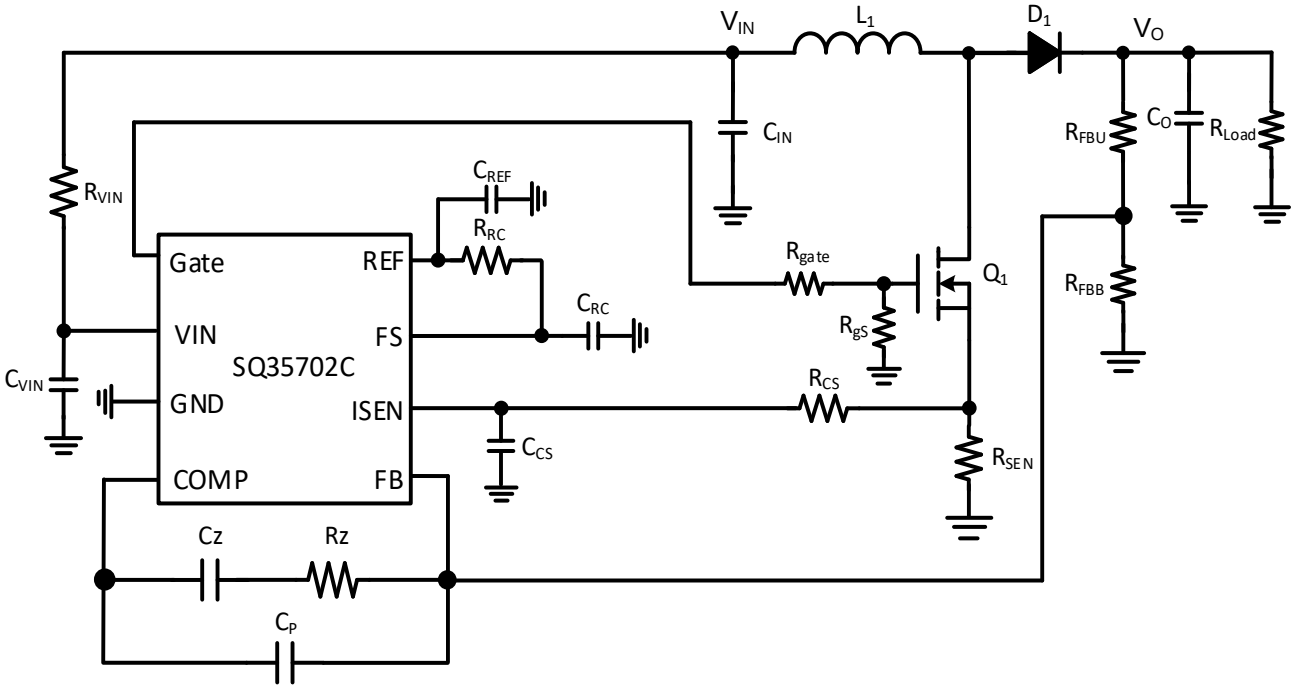


Fig.1 Schematic Diagram (Boost Topology)

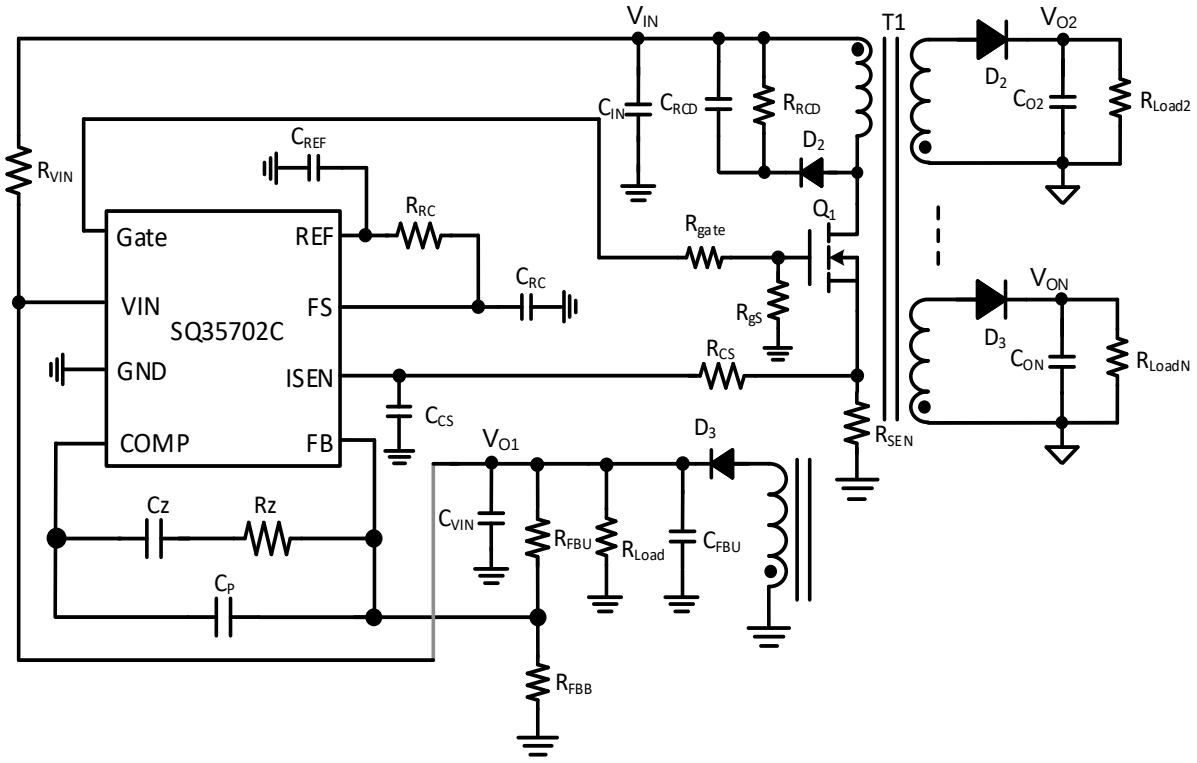


Fig.2 Schematic Diagram (Flyback Topology)

Ordering Information

Ordering Number	Package type	Top Mark
SQ35702CFAP	SO8	GKK***xyz***

x=year code, y=week code, z= lot number code

Pinout (Top view)

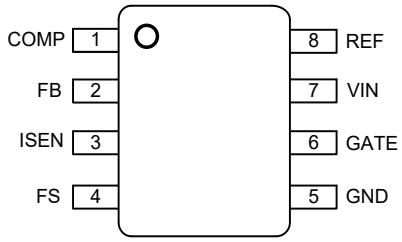


Fig.3 Pin-out

Pin Name	Pin Description	
COMP	1	External compensation pin. Connect RC network from this pin to GND to compensate the control loop.
FB	2	Output voltage feedback pin. The output voltage reference is 2.5V.
ISEN	3	Current sense pin. Connect an external current sensing resistor R_{SEN} from this pin to GND. The voltage on this pin is used to provide mosfet current feedback in the control loop and peak current limit. The cycle by cycle peak current limit threshold and the hiccup peak current limit threshold are 1.0V and 1.1V repectively.
FS	4	FS is used to set the oscillator frequency and minimum off time pin. Connecting a resistor from REF to FS and a capacitor from FS to GND to set the frequency and minimum off time. The frequency can be calculated as follow: $f_{OSC} = \frac{K_{RC}}{R_{RC} \times C_{RC}}$ Where • K_{RC} is the frequency coefficient K_{RC}=1.65 • frequency is in Hz • resistance is in Ω • capacitance is in farads • Fsw=Fosc/2
GND	5	Ground Pin.
GATE	6	GATE is the MOSFET driving pin. Connect to the gate of power MOSFET.
VIN	7	Input supply pin. Decouple this pin to GND pin with at least 1uF ceramic capacitor.
REF	8	5V Internal LDO output from VIN. A 1uF capacitor is recommended to be connected from this pin to GND.

Block Diagram

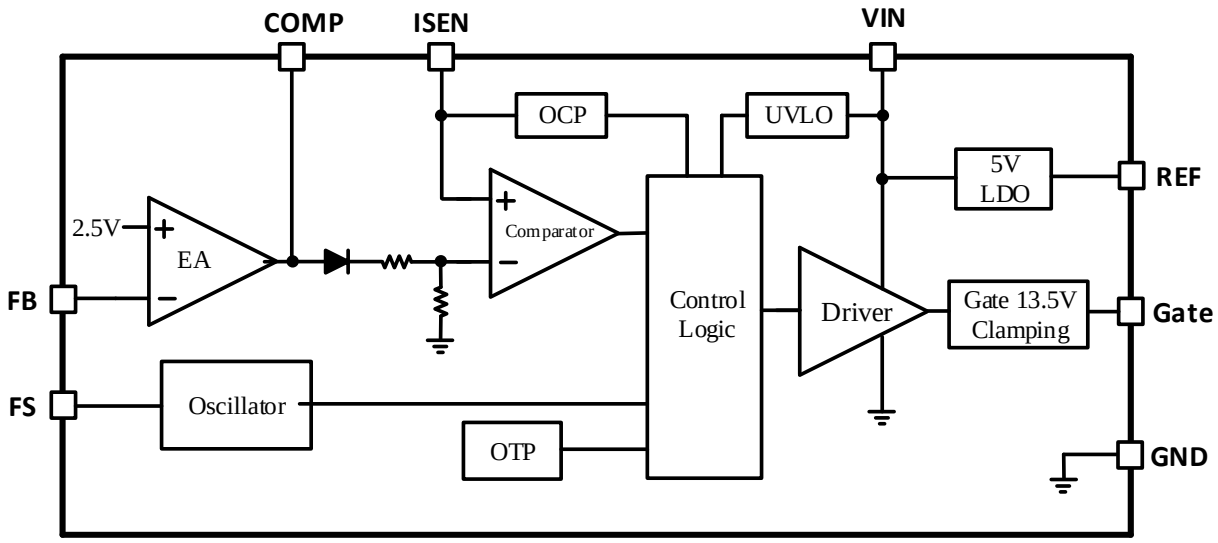


Fig.4 Detailed Block Diagram

Absolute Maximum Ratings (Note 1)

VIN---------- -0.3V to 24V
GATE---------- -0.3V to 16V
COMP,REF ---------- -0.3V to 7V
FB,ISEN,FS ---------- -0.3V to 4V
Power dissipation@TA = 25℃ ---------- 0.65W
Package Thermal Resistance (Note 2)
ΘJA ---------- 107°C/W
ΘJC(Top)---------- 49°C/W
Junction Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
ESD Susceptibility(Note3)
HBM(Human Body Mode) ---------- 2000V
CDM (Charge Device Mode) All pins----------500V
Corner pins----------750V

Recommended Operating Conditions (Note 3)

Supply Voltage VIN ---------- 10V to 22V
COMP,REF ---------- -0.3 to 6V
FB,ISEN,FS---------- -0.3V to 3.6V
Junction Temperature Range ---------- -40°C to 105°C

Electrical Characteristics

(-40℃≤T_j≤105℃,VIN = 15V,C_{VIN}=1uF,C_{REF}=100nF,R_{RC}=10k,C_{RC}=3.3nF unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VIN Pin						
VIN UVLO ON Threshold	V_{VIN_START}		8.3	9	9.7	V
UVLO ON OFF Hysteresis	V_{UVLO_HYS}		0.8	1	1.2	V
Start Up Current	I_{START}	V_{VIN}=3V,V_{FB}=0V	0.07	0.17	0.27	mA
Operating Current	I_{OP}	V_{ISEN}=0V,V_{FB}=0V	1	1.5	2	mA
VIN Pin Clamping Voltage	V_{IN_CL}	I_{VIN}=10mA	23	25.5	28	V
REF Pin						
Output Volatge Of REF	V_{REF}	I_{REF} = 1mA	4.9	5	5.1	V
Load regulation	$\triangle V_{REF\_LOR}$	1mA ≤ I_{REF} ≤20 mA		15	30	mV
Line regulation	$\triangle V_{REF\_LIR}$	T_J= 25℃, V_{VIN} = 12V to 24V (I_{REF} =5mA)			1.9	mV/V
		T_J= –40℃ to 105℃, V_{VIN} =12V to 24V (I_{REF} =5 mA) guarantee by design			2.5	mV/V
REF Short Circuit Current	I_{REF_LIMH}		60	100	140	mA
FS Pin						
Oscillator Frequency	f_{OSC}	R_{RC}=10k,C_{RC}=3.3nF	47	50	53	kHz
Oscillator Upper Threshold	V_{OSC_H}		2.5	2.7	2.9	V
Maximum duty cycle	D_{MAX}	R_{RC}=10k,C_{RC}=3.3nF	46	48	50	%
FB&COMP Pins (ERROR AMPLIFIER)						
Output Feedback Reference	V_{FB}		2.45	2.5	2.55	V
COMP Sinking Current	I_{COMP_SINK}	FB=2.7V,COMP=1.1V	2	4.6	8	mA
COMP Sourcing Current	I_{COMP_SOURCE}	FB=2.3V,COMP=5.0V	-0.2	-0.7	-1.5	mA
ISEN Pins						
COMP To ISEN Coefficient	K_{COMP_ISEN}		2.55	3	3.45	V/V
COMP to ISEN Offset	V_{OFFSET}	ISEN=0V,I_{F_DIODE}=200uA	0.7	1.4	2	V
ISEN Input Bias Current	I_{ISEN_BIAS}		1.1	2.3	3.8	uA
Cycle By Cycle Current Limit Threshold	V_{ISEN_OCP}	COMP=6V	0.92	1.0	1.08	V
Hiccup Operation Current Limit Threshold	V_{ISEN_HICCUP}	COMP=6V	1.02	1.1	1.18	V
Thermal						
Thermal Shutdown Threshold	T_{SD}		150	165	180	ºC
Thermal Shutdown Hysteresis	T_{SDHYS}			15		ºC

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

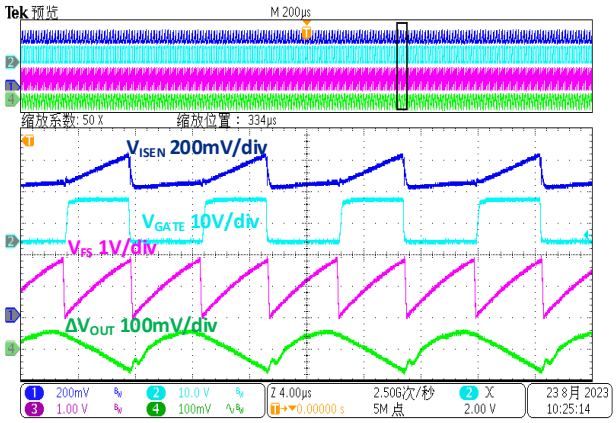
Note 2: θJA is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2” x 2” FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Operation Characteristics

Steady State

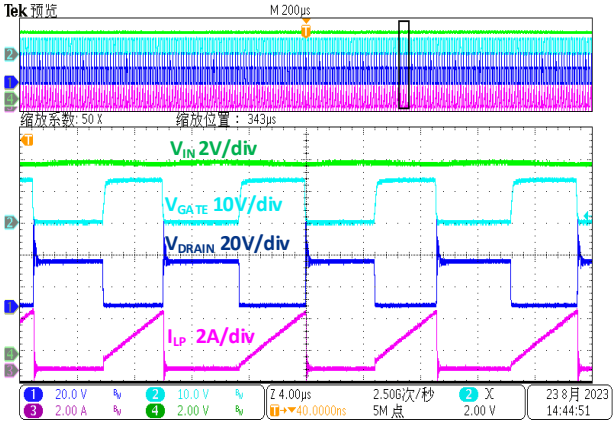
(VIN=PVIN=15V,VOUT=12V,IOUT=1A,Steady State)



Time(4us/div)

Steady State

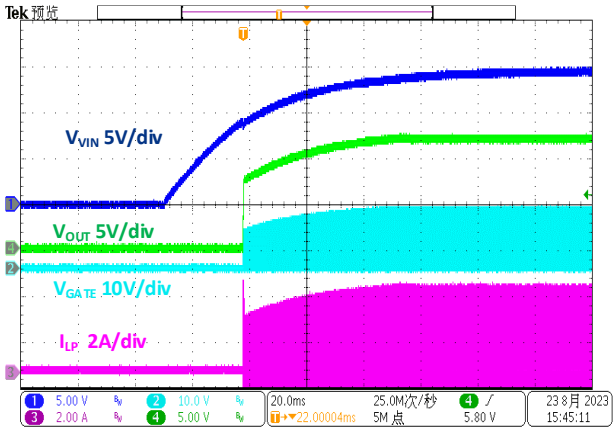
(VIN=PVIN=15V,VOUT=12V,IOUT=1A)



Time(4us/div)

Start Up

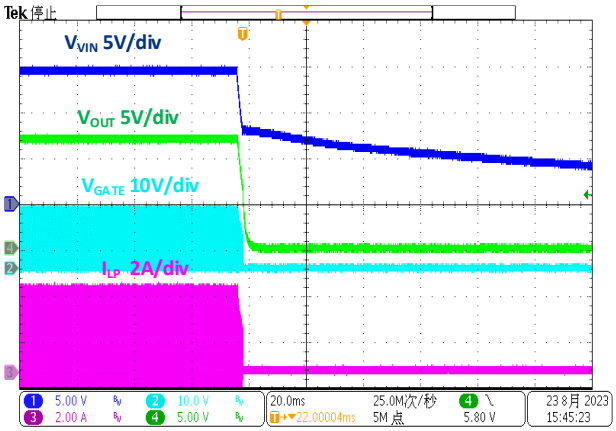
(VIN=PVIN=15V,VOUT=12V,IOUT=1A,VCC Power On)



Time(20ms/div)

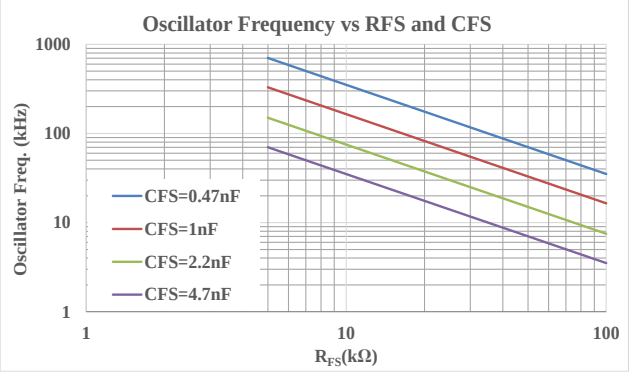
Shut Down

(VIN=PVIN=15V,VOUT=12V,IOUT=1A,VCC Power Off)



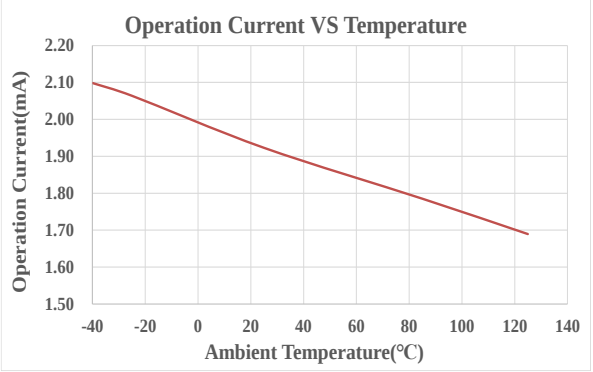
Time(20ms/div)

Oscillator Frequency vs RFS and CFS



Iop vs Temperature

(VIN=15V,VFB=0V,VISEN=0V)



Operation Principle

SQ35702C is a fixed frequency and current mode controller for Boost/ Flyback/Sepic topology. UVLO、 OCP and OTP protection are available to protect IC. Flexible frequency and minimum off time set by FS pin and up to 250 kHz switching frequency.

1. Applications Information

1.1 Switching Frequency Formula

FS is the frequency set pin. Connect a resistor R_{RC} to REF pin and a C_{RC} to GND pin to set f_{SW} .

F_{SW} can be calculated to be:

$$f_{SW} \approx \frac{1}{2} \times \frac{1.65}{R_{RC} \times C_{RC}} \quad (1)$$

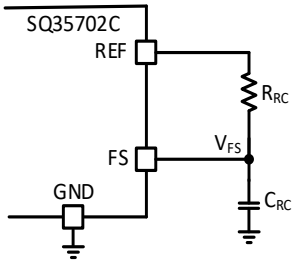


Fig.5 FS RC Network

1.2 Feedback Resistor Dividers R1 and R2

Choose R1 and R2 to program the output voltage under CV mode. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R1 and R2. A value of between 1k and 100k is highly recommended for R2. VOUT can be calculated to be:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

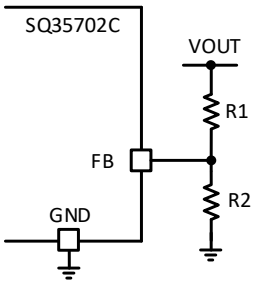


Fig.6 Feedback Resistance Network

1.3 Peak Current Sense Resistor

An external sensing resistor Rcs is used to sense the current flow through the MOSFET. The sensed voltage is for peak current mode control and cycle by cycle peak current limit. The cycle-by-cycle current limit threshold is 1V and hiccup current limit threshold is 1.1V.

1.4 MOSFET and Diode

When power MOS is turned off, the drain to source voltage is equal to Vin plus Vo*Nps, so the break down voltage of power MOS should be larger than the maximum value of Vin plus Vo*Nps. When power MOS is turned off, a voltage spike is always generated due to the parasitic inductance, so voltage rating safe margin should be taken into consideration.

$$V_{MOS\_MAX} = V_{IN} + (V_{OUT} + V_f) \times N_{ps} \quad (3)$$

Where N_{ps} is the turns ratio of the Flyback transformer

Average current flowing through the diode is equal to the output current, so the diode current rating should be larger than the maximum output current. Reverse voltage of the diode is equal to VIN plus VO, so the reverse voltage of the diode should be selected

to be larger than the maximum value of VIN plus Vo. It is better to select a Schottky diode to reduce the reverse recovery loss.

$$V_{D1\_MAX} = V_{OUT} + V_{IN} \times \frac{1}{N_{ps}} \qquad (4)$$

1.5 Main Inductor L for Flayback Design

Choose proper inductance to achieve desired current ripple.It is suggested to choose the ripple current rate Krp to be about 50% of the maximum input current. The inductance is calculated as:

$$L_m = \frac{V_{IN}^2 \times N_{ps}^2 \times \frac{V_{OUT}}{(V_{IN} + N_{ps} \times V_{OUT})^2} \times (1 - \frac{Krp}{2})}{Krp \times I_{OUT} \times f_{SW}} \qquad (5)$$

Where Krp is equal to $\triangle I_L/I_{LPK}$

2. Layout Design

(a)The circuit loop of all switching circuit should be kept small: primary power loop, secondary loop and auxiliary power loop.

(b)A decoupling capacitor is required for both the VIN pin and REF pin and both must be returned to GND as close to the IC as possible.

(c)The ISEN pin filter capacitor must be as close to the IC possible and grounded right at the IC ground pin.

(d)Gate driver loop area must be minimized to reduce the EMI noise because of the high di/dt current in the loop

Fig.7 Layout Example (Boost Topology)

3. Design Example

A design example of Flyback application is shown below .

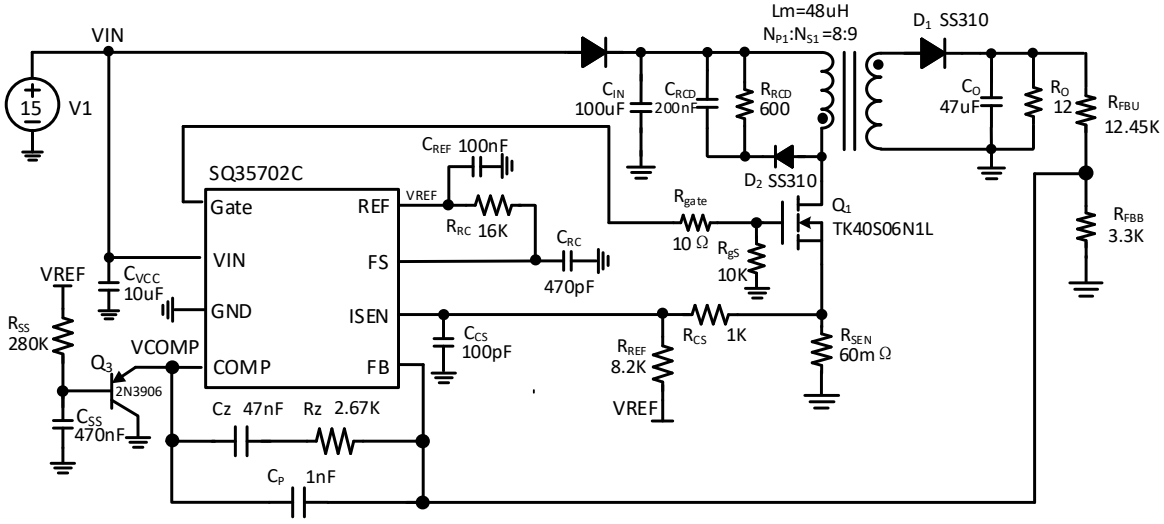


Fig.8 Flyback Application Circuit

3.1 Identify design specification

Design Specification			
V_{IN}	15V	V_{OUT}	12V
Fsw	110 kHz	I_{OUT}	1A
		η	85%

3.2 Switching Frequency

For this example,R_{RC}=16k and C_{RC}=0.47nf were selected to operate at 110 kHz.

$$fsw \approx \frac{1.65}{R_{RC} \times C_{RC}} \times \frac{1}{2} = 110\,kHz$$

3.3 Inductor Selection

The transformer turns ratio can be selected as :

$$N_{ps} = \frac{8}{9}$$

The average input current I_{IN_MAX} and duty cycle D_{MAX} can be calculated as :

$$I_{IN\_AVG} = \frac{V_{OUT} \times I_{OUT}}{V_{IN\_MIN} \times \eta} = 0.969A$$

$$D_{MAX} = \frac{Nps \times V_{OUT}}{V_{IN\_MIN} + N_{ps} \times V_{OUT}} = 0.416$$

The primary inductor peak current I_{PK_P} and valley current I_{VAL_P} can be calculated as:

$$I_{PK\_P} = \frac{P_{IN}}{V_{IN\_MIN} \times (1 - \frac{Krp}{2}) \times \frac{t_{ON\_MAX}}{t_{SW}}} = 2.913A$$

$$I_{VAL\_P} = I_{PK\_P} \times (1 - Krp) = 1.748A$$

The primary inductor L_m can be calculated as:

$$L_m = \frac{V_{IN\_MIN} \times t_{ON\_MAX}}{Krp \times I_{PK\_P}} = 48uH$$

The primary inductor RMS Current I_{RMS_P} can be calculated as:

$$I_{RMS\_P} = \sqrt{\frac{1}{t_{SW}} \times \int_0^{t_{ON\_MAX}} (I_{PK\_P}(t))^2 \, dt} = 1.518A$$

It is important that the RMS current and saturation current ratings of the inductor are not exceeded.

3.4 Transformer Design Specifications

Item	Partnumber
Bobbin	PQ2016(Core PC40)
Lm(uH)	48uH
Primary Turns	8
Secondary Turns	9
Primary Winding(mm)	Φ0.23×7
Secondary Winding(mm)	Φ0.23×7

3.5 MOSFET and Diode Selection

The peak current and RMS current of MOSFET are same as primary inductor.

$$V_{MOS\_MAX} \geq 1.2 \times (V_{IN} + (V_{OUT} + Vf) \times N_{ps}) = 31.2\,V$$

$$I_{MOS\_RMS} > 2 \times I_{RMS\_P} = 3.04\,A$$

TK40S06N1L is used in this design.The TK40S06NIL have $R_{DS(ON)}$ = 8.7 mΩ,V_{DSS}=60V and I_D=40A.
Output diode RMS current I_{RMS} and maximum voltage can be calculated as:

$$I_{D\_RMS} > 2 \times I_{OUT} = 2\,A$$

$$V_{D1\_MAX} \geq 1.2 \times (V_{OUT} + \frac{V_{IN\_MAX}}{N_{ps}}) = 34.65V$$

SS310 diode is used in this design.

3.6 Output capacitor Selection

Output capacitor is selected according to the output voltage ripple requirement.Suppose the output voltage ripple is 0.5% of V_{OUT},the capacitor valye can be calculated as:

$$C_{OUT} \geq \frac{I_{OUT} \times D_{MAX}}{0.5\% \times V_{OUT} \times f_{SW}} = 32uF$$

4 PCS low ESR 10uF ceramic capacitor is recommended.

3.7 Current Sense Resistor Selection

The current sensing network consists of R_{SEN},R_{REF}, R_{CS},C_{CS}.For this converter,to achieve 2.913A primary side peak current,a 60mΩ resistor is chosen for R_{SEN}.

C_{CS} is chosen to be 100pf to provide enough filtering to suppress the leading edge spike.

R_{REF} and R_{CS} form a resistor divider network from the current sense signal to the reference voltage to offset the current sense

voltage.Offset voltage can be calculated when chose R_{REF}=8.2kΩ and R_{CS}=1kΩ:

$$V_{offset} = \frac{R_{CS}}{R_{CS} + R_{REF}} \times V_{REF} = 0.534V$$

R_{SLOP}=47kΩ and Q2=MMBT3904 were chosen as slope compensation network.

3.8 Control Loop Compensation Design

SQ35702C is a fixed frequency and current mode controller.It integrates a volage mode error amplifier.For this example,a type II compensator is applied to stable the system.Rz=2.67k,Cz=47nF,Cp=1nF in this example is recommended.

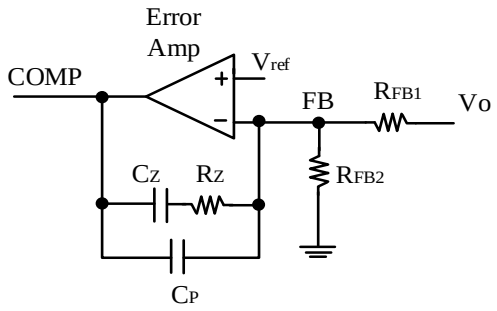
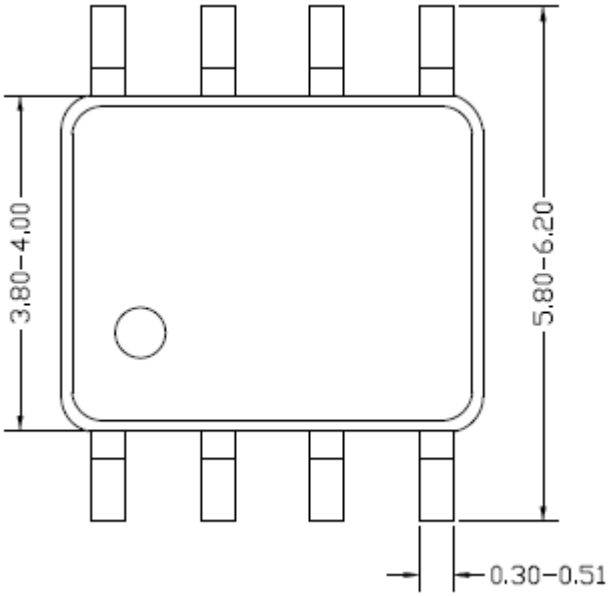
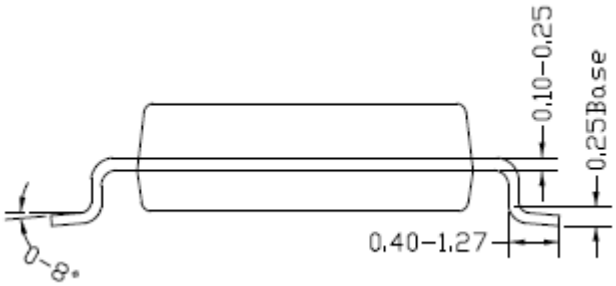


Fig.9 Loop Compensation Circuit

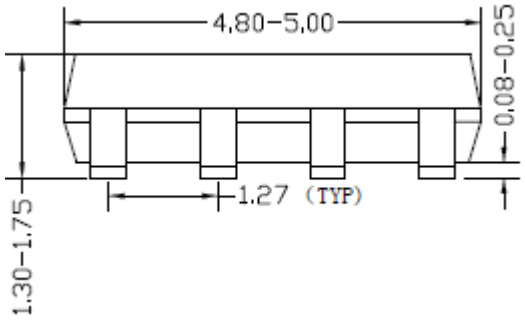
SO8 Package outline & PCB layout design



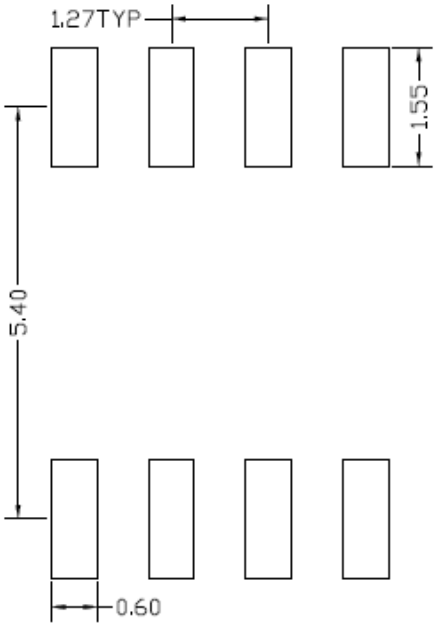
Top view



Side view



Front view

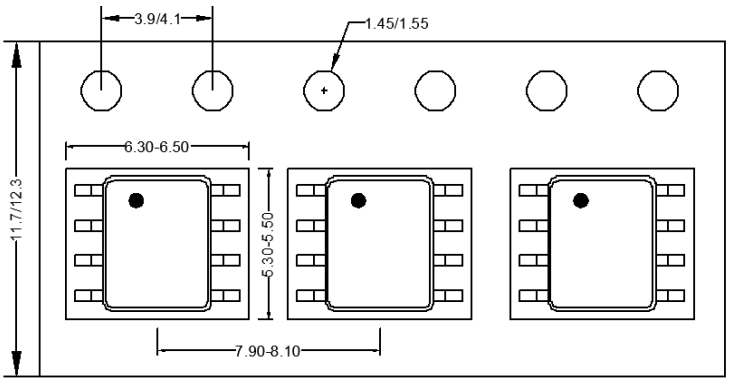


Recommended Pad Layout
(Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

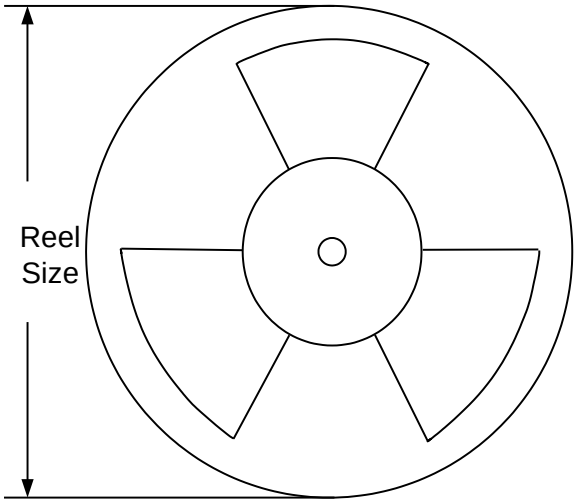
Taping & Reel Specification

1. Taping orientation for packages（SO8）



Feeding direction

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SO8	12	8	13"	400	400	2500

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Jan.16, 2023	Revision 0.9	Initial Release
Jan.17, 2023	Revision 1.0	Production Release

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