Application Note: SY50223

Flyback controller
For adapters or chargers

General Description

SY50223 is a PWM/PFM controller with several features to enhance performance of Flyback converters that targeting at adapter or charger applications. It integrates a 700V MOSFET to decrease physical volume and drives Flyback controller in the Quasi-Resonant mode for higher efficiency and better EMI performance. SY50223 adopt burst mode control for improved efficiency and the output current is detected by internal primary detection technology to achieve more reliable Over Current Protection and Short Circuit Protection. The output voltage is achieved by secondary side control technology for good load and line regulation. SY50223 provides a fast internal HV start up circuit without consuming any standby power to achieve lowest no-load power consumption.

Ordering Information

SY50223□(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY50223FAC	SO8	----

Features

- Quasi-Resonant (QR) mode operation: Valley turn-on of the primary MOSFET to achieve low switching losses
- Output current is monitored by primary detection for reliable Over Current Protection and Short Circuit Protection
- PWM/PFM conrol for higher average efficiency
- Burst mode control for low no-load power and efficiency
- HV start up circuit is used to reduce no-load power
- Maximum frequency limitation 125kHz
- Auto-Recovery OVP/OCP/SCP/OTP
- Integrated 700V MOSFET
- Compact package: SO8

Applications

- AC/DC Adapters
- Battery Chargers
- Consumer Electronics
- Auxiliary power supplies

Recommended operating output power	
Products	90Vac~264Vac
SY50223	12W

Typical Applications

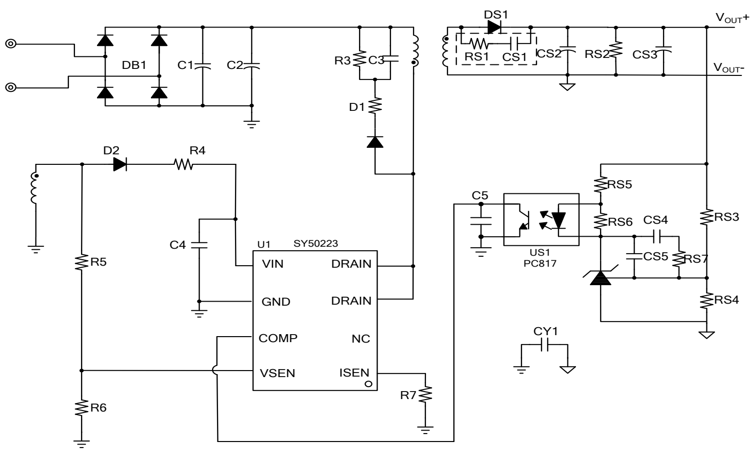

Fig.1 Schematic Diagram

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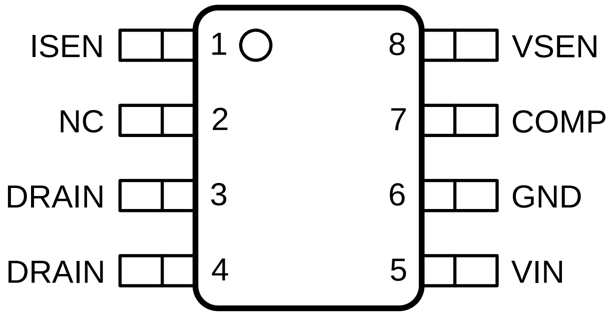
Pinout (Top view)



(SO8)

Top Mark: AJN*xyz* (device code: AJN, ***x=year code, y=week code, z= lot number code***)

1	ISEN	Current sense pin. Connect this pin to the source of the primary switch.
2	NC	NC pin.
3	DRAIN	Drain of the internal power MOSFET.
4	DRAIN	Drain of the internal power MOSFET.
5	VIN	Power supply pin.
6	GND	Ground pin.
7	COMP	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin. It's connected to a optocoupler.
8	VSEN	Inductor current zero-crossing detection pin. This pin receives the auxiliary winding voltage by a resistor divider and detects the inductor current zero crossing point.

Block Diagram

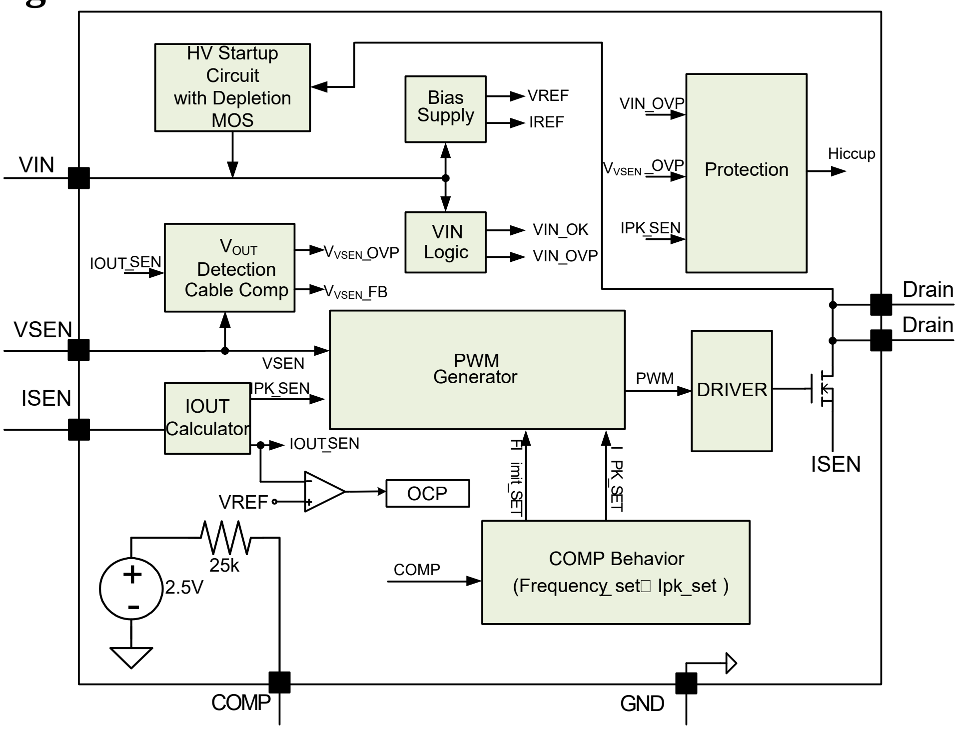


Fig.2 Block Diagram

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Absolute Maximum Ratings (Note 1)

VIN--- -0.3V~21V
Supply Current I_{VIN} --- 20mA
ISEN, COMP --- -0.3V~3.6V
VSEN--- -0.3V~V_{VIN}+0.3V
DRAIN-- 700V
Power Dissipation, @ T_A = 25°C SO8 ---1.1W
Package Thermal Resistance (Note 2)
SO8, θ_{JA} ---125°C/W
SO8, θ_{JC} ---60°C/W
Junction Temperature Range --- -45°C to 150°C
Lead Temperature (Soldering, 10 sec.) --- 260°C
Storage Temperature Range -- -65°C to 150°C

Recommended Operating Conditions

VIN -- 9V~17.5V
Junction Temperature Range --- -40°C to 125°C
Ambient Temperature Range --- -40°C to 105°C

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Electrical Characteristics

(V_{VIN} = 12V(Note 3) , T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Section						
VIN operating range	V_{VIN_RANGE}		9		17.5	V
VIN turn-on threshold	V_{VIN_ON}		13.7	14.7	15.7	V
VIN turn-off threshold	V_{VIN_OFF}		6.3	7	8.3	V
VIN OVP voltage	V_{VIN_OVP}		17.5	18.5	19.5	V
HV start up current	I_{HV_ON}			0.35		mA
HV leakage current	I_{HV_OFF}			5		μA
Start up Current	I_{ST}	$V_{VIN}<V_{VIN\_OFF}$		1.2		μA
Operating Current	I_{VIN}	C_L=100pF,f=100kHz		1		mA
Quiescent Current	IQ	V_{COMP}=0	250	350	500	μA
Shunt current in OVP mode	I_{VIN_OVP}	$V_{VIN}>V_{VIN\_OVP}$		9		mA
Current Feedback Modulator Section						
Internal reference voltage	V_{REF}		0.414	0.42	0.426	V
ISEN Pin Section						
Current limit reference voltage	V_{ISEN_MAX}	V_{FBV}<0.4V		0.7		V
		V_{FBV}>0.4V	0.9	1	1.1	V
Latch Voltage for ISEN	V_{ISEN_EX}			2		V
VSEN Pin Section						
OVP voltage threshold	V_{VSEN_OVP}		1.38	1.45	1.55	V
Integrated MOSFET Section						
Breakdown Voltage	V_{BV}	V_{GS}=0V,I_{DS}=250μA	700			V
Switching Section						
Max ON Time	T_{ON_MAX}	V_{COMP}=2.5V，I_{ISEN}=0		24		μs
Min ON Time	T_{ON_MIN}			300	0	ns
Min OFF Time	T_{OFF_MIN}		1.1	1.2	1.7	μs
Minimum switching period	T_{PERIOD_MIN}		7	8	9	μs
COMP section						
Internal voltage bias	V_{CVB}			2.5		V
Sleep mode voltage ON threshold	V_{COMP_ON}		0.3	0.4	0.5	V
Sleep mode voltage OFF threshold	V_{COMP_OFF}		0.35	0.45	0.55	V
Internal pull-up resistor	R_{COMP}			25		kΩ
Thermal Section						
Thermal Shutdown Temperature	T_{SD}			150		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on “2 x 2” FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal via to bottom layer ground plane.

Note 3: Increase VIN pin voltage gradually higher than V_{VIN_ON} voltage then turn down to 12V.

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Operation

SY50223 is a high performance Flyback controller with secondary side control and constant current and constant voltage regulation.

It integrates a 700V MOSFET to decrease physical volume.

In order to reduce the switching losses and improve EMI performance, Quasi-Resonant switching mode is applied, which means to turn on the integrated MOSFET at voltage valley; the start up current of the device is rather small(1.2μA typical) to reduce the standby power loss further and the maximum switching frequency is limited below 125kHz.

In order to improve the stability, the self-adaption compensation is applied.

SY50223 provides a fast internal HV start up circuit without consuming any standby power to achieve lowest no-load power consumption.

The output current is monitored by primary side detection technology, and the maximum output current can be programmed in Over Current Protection and Short Circuit Protection. In addition to SY50223 provides VIN Over Voltage Protection, Over Temperature Protection (OTP), Output voltage OVP protection(OVP) , VSEN pin short protection ,etc..

SY50223 can be applied in AC/DC adapters, Battery Chargers and other consumer electronics.

SY50223 is available with SO8 package.

Applications Information

Start up

To achieve better light load performance, HV start up design is added. After AC supply or DC BUS is powered on, the capacitor C_{VIN} across VIN and GND pin is charged up by internal HV start up circuit. Once V_{VIN} rises up to V_{VIN_ON}, the internal blocks start to work. V_{VIN} will be pulled down by internal consumption of IC until the auxiliary winding of Flyback transformer could supply enough energy to maintain V_{VIN} above V_{VIN_OFF}.

The whole start up procedure is divided into two sections shown in Fig.3. t_{STC} is the C_{VIN} charged up section, and t_{STO} is the output voltage built-up section. The start up time t_{ST} composes of t_{STC} and t_{STO}, and usually t_{STO} is much smaller than t_{STC}.

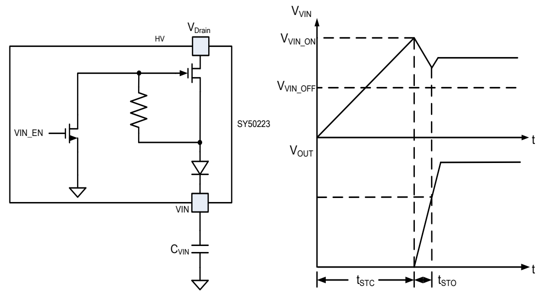

Fig.3 Start up

The start up capacitor C_{VIN} is designed by rules below:

(a) Select C_{VIN} to obtain an ideal start up time t_{ST}, and ensure the output voltage is built up at one time.

$$C_{VIN} = \frac{(I_{HV\_ON} - I_{HV\_OFF} - I_{ST}) \times t_{ST}}{V_{VIN\_ON}} \quad (1)$$

(b) If the C_{VIN} is not big enough to build up the output voltage at one time. Increase C_{VIN} until the ideal start up procedure is obtained.

Shut down

After AC supply or DC BUS is powered off, the energy stored in the BUS capacitor will be discharged. When the auxiliary winding of Flyback transformer can not supply enough energy to VIN pin, V_{VIN} will drop down. Once V_{VIN} is below V_{VIN_OFF}, the IC will stop working.

Quasi-Resonant Operation(valley detection)

QR mode operation provides low turn-on switching losses for Flyback converter.

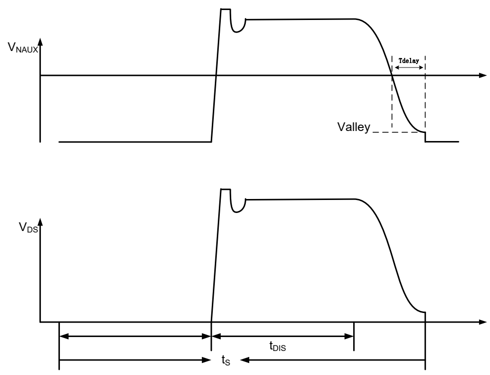

Fig.4 QR mode operation

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The voltage across drain and source of the primary integrated MOSFET is reflected by the auxiliary winding of the Flyback transformer. VSEN pin detects the voltage across the auxiliary winding by a resistor divider.When the voltage on VSEN pin across zero, the MOSFET would be turned on after 400ns delay.

Output Voltage Control(CV control)

SY50223 is compatible with opto-coupler to achieve output voltage control, which is shown by Fig.5.

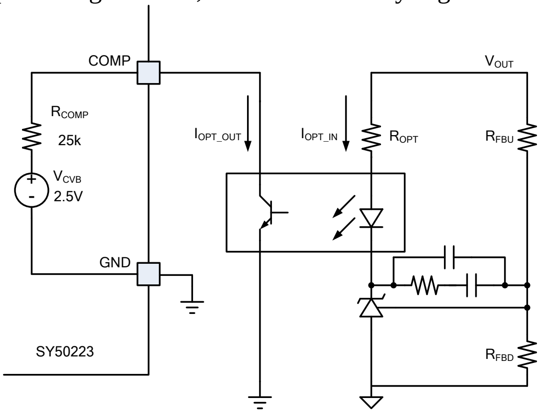

Fig.5 Output voltage feedback circuit

The OFF time of MOSFET is up to the valley detection of VSEN pin, and the ON time of MOSFET is a function of V_{COMP}, so the output power can be controlled by V_{COMP}.

SY50223 integrates an internal 2.5V voltage bias and 25kΩ resistor to interface the output of opto-coupler. V_{COMP} is in relation with the output current of the opto-coupler I_{OPT_OUT} by

$$V_{COMP} = V_{CVB} - I_{OPT\_OUT} \times R_{COMP} \quad (2)$$

R_{OPT} is the resistor across the output node and the anode of the opto-coupler. The selection of R_{OPT} is related with system loop stability, and higher loop gain of the system is achieved by smaller R_{OPT}.

At the same time, R_{OPT} is designed by

$$V_{CVB} - I_{OPT\_IN\_MAX} \times \beta \times R_{COMP} < V_{COMP\_ON} \quad (3)$$

Where β is the transfer ratio of the opto-coupler; $I_{OPT\_IN\_MAX}$ is the maximum input current through the opto-coupler, which is limited by R_{OPT}.

Output current detection by Primary side(CC control)

The output current is monitored by SY50223 with primary side detection technology. The maximum output current I_{OUT_LIM} can be regulated by：

$$I_{OUT\_LIM} = \frac{k_1 \times k_2 \times V_{REF} \times N_{PS}}{R_S} \quad (4)$$

Where k_1 is the output current weight coefficient, the value is 0.5; k_2 is the output modification coefficient, the value is 1; V_{REF} is the internal reference voltage, the value is 0.42; N_{PS} is the turns ratio of the Flyback transformer; R_S is the current sense resistor.

k_1, k_2 and V_{REF} are all internal constant parameters, I_{OUT_LIM} can be programmed by N_{PS} and R_S.

$$R_S = \frac{k_1 \times k_2 \times V_{REF} \times N_{PS}}{I_{OUT\_LIM}} \quad (5)$$

When over current operation or short circuit operation happens. V_{COMP} will be pulled down, and the output current will be limited at I_{OUT_LIM}. The V-I curve is shown as Fig.6.

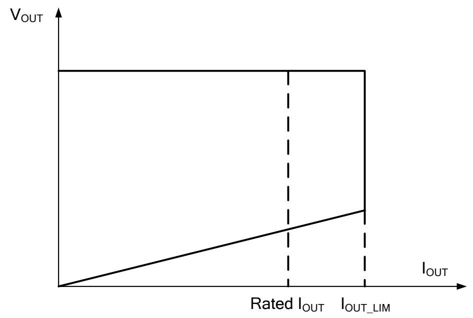

Fig.6 V-I curve

Line regulation modification

The IC provides line regulation modification function to improve line regulation performance of the output current.

Due to the sample delay of ISEN pin and other internal delay, the output current increases with increasing input BUS line voltage. A small compensation voltage ΔV_{ISEN_C} is added to ISEN pin during ON time to improve such performance. This ΔV_{ISEN_C} is adjusted by the upper resistor of the divider connected to VSEN pin.

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$$\Delta V_{ISEN\_C} = V_{BUS} \times \frac{N_{AUX}}{N_P} \times \frac{1}{R_{VSENU}} \times k_3 \quad (6)$$

Where R_{VSENU} is the upper resistor of the divider; k3 is an internal constant as the modification coefficient.

The compensation is mainly related with R_{VSENU}, larger compensation is achieved with smaller R_{VSENU}. Normally, R_{VSENU} ranges from 50kΩ~150kΩ.

Short Circuit Protection (SCP)

When the output is shorted to ground, the output voltage is clamped to zero. The voltage of the auxiliary winding is proportional to the output winding, so valley signal cannot be detected by VSEN. There are two cases，the one is without valley detection, MOSFET cannot be turned on until maximum off time is reached. Once VSEN>1V, if MOSFET is turned on with maximum off-time for 16 times continuously which can not detected valley, IC will be shut down and discharge the VIN voltage, then enter into hiccup mode. Otherwise, if VSEN cannot larger than 1V, this "valley detection protection method " will not be effective, IC will shut down until VIN is below V_{VIN_OF} and enter into hiccup mode.

When the output voltage is not low enough to disable valley detection in short condition, SY50223 will operate in CC mode until VIN is below V_{VIN_OFF}.

In order to guarantee SCP function not effected by voltage spike of auxiliary winding, a filter resistor R_{AUX} is needed.

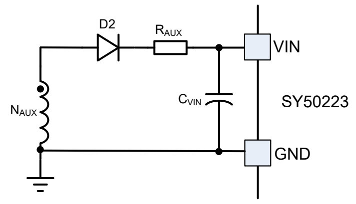

Fig. 7 Filter resistor R_{AUX}

Output voltage OVP protection

The secondary maximum voltage is limited by the SY50223.When the VSEN pin signal exceeds 1.45V, SY50223 will stop switching and discharge the VIN voltage. Once V_{VIN} is below V_{VIN_OFF}, the IC will shut down and then enter into hiccup mode.

VSEN pin short protection

The SY50223 has a protection against faults caused by a shorted VSEN pin or a shorted pull-down resistor. During start-up, the voltage on the VSEN pin is monitored. In normal situations, the voltage on the VSEN pin reaches the sense protection trigger level. When the VSEN voltage does not reach this level, the VSEN pin is shorted and the protection is activated. The IC stops switching and discharge the VIN voltage. Once V_{VIN} is below V_{VIN_OFF}, the IC will shut down and then enter into hiccup mode. In order to ensure reliable detection, the pull-down resistor should larger than 2kΩ.

ISEN Pin Latch Protection

The ISEN pin voltage is limited by the SY50223.When the ISEN pin signal exceeds 2V, SY50223 will stop switching and discharge the VIN voltage. Once VVIN is below V_{VIN_OFF}, the IC will shut down and then enter into hiccup mode.

Power Design

A few applications are shown as below.

Products	Input range	Output		Temperature rise
SY50223	90Vac~264Vac	10W	5V/2.0A	40℃
	90Vac~264Vac	12W	5V/2.4A	60℃
	90Vac~264Vac	12W	12V/1A	50℃

The test is operated in natural cooling condition at 25 ℃ ambient temperature.

Power Device Design

Diode

When the operation condition is with maximum input voltage and full load, the voltage stress of secondary power diode is maximized.

$$V_{D\_R\_MAX} = \frac{\sqrt{2}V_{AC\_MAX}}{N_{PS}} + V_{OUT} \quad (7)$$

Where V_{AC_MAX} is maximum input AC RMS voltage; N_{PS} is the turns ratio of the Flyback transformer; V_{OUT} is the rated output voltage.

When the operation condition is with minimum input voltage and full load, the current stress of and power diode is maximized.

$$I_{D\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} \quad (8)$$

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$$I_{D\_AVG}=I_{OUT} \quad (9)$$

Where $I_{P\_PK\_MAX}$ is maximum primary peak current , which will be introduced later.

Transformer (N_{PS} and L_M)

N_{PS} is limited by the electrical stress of the integrated power MOSFET:

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 80\%\text{-}\sqrt{2}V_{AC\_MAX}\text{-}\Delta V_S}{V_{OUT}+V_{D\_F}} \quad (10)$$

Where $V_{MOS\_(BR)DS}$ is the breakdown voltage of the integrated power MOSFET; V_{D_F} is the forward voltage of secondary power diode; ΔV_S is the overshoot voltage clamped by RCD snubber during OFF time.

In Quasi-Resonant mode, each switching period cycle t_S consists of three parts: current rising time t_1, current falling time t_2 and quasi-resonant time t_3 shown in Fig.8.

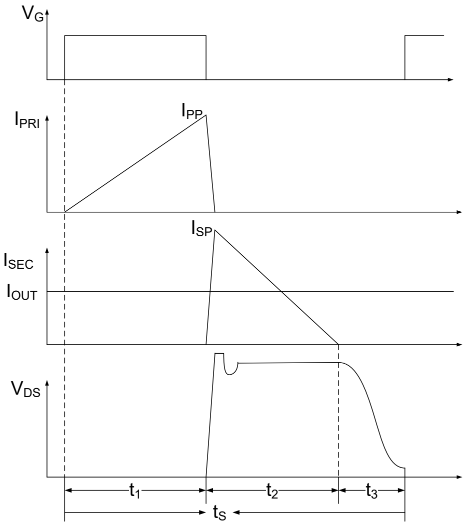

Fig.8 Switching waveforms

When the operation condition is with minimum input AC RMS voltage and full load, the switching frequency is minimum frequency, the maximum peak current through MOSFET and the transformer happens.

Once the minimum frequency f_{S_MIN} is set, the inductance of the transformer could be induced. The design flow is shown as below:

(a) Select N_{PS};

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 80\%\text{-}\sqrt{2}V_{AC\_MAX}\text{-}\Delta V_S}{V_{OUT}+V_{D\_F}} \quad (11)$$

(b) Preset minimum frequency f_{S_MIN};

(c) Compute inductor L_M and maximum primary peak current $I_{P\_PK\_MAX}$;

$$I_{P\_PK\_MAX}=\frac{2P_{OUT}}{\eta\times V_{DC\_MIN}}+\frac{2P_{OUT}}{\eta\times N_{PS}\times(V_{OUT}+V_{D\_F})} +\pi\sqrt{\frac{2P_{OUT}}{\eta}\times C_{Drain}\times f_{S\_MIN}} \quad (12)$$

$$L_M=\frac{2P_{OUT}}{\eta\times I_{P\_PK\_MAX}^2\times f_{S\_MIN}} \quad (13)$$

Where, C_{Drain} is the parasitic capacitance at drain of integrated MOSFET; η is the efficiency; P_{OUT} is rated full load power; V_{DC_MIN} is minimum input DC RMS voltage.

(d) Compute current rising time t_1 and current falling time t_2;

$$t_1=\frac{L_M\times I_{P\_PK\_MAX}}{V_{DC\_MIN}} \quad (14)$$

$$t_2=\frac{L_M\times I_{P\_PK\_MAX}}{N_{PS}\times(V_{OUT}+V_{D\_F})} \quad (15)$$

$$t_S=\frac{1}{f_{S\_MIN}} \quad (16)$$

(e) Compute primary maximum RMS current $I_{P\_RMS\_MAX}$ for the transformer fabrication;

$$I_{P\_RMS\_MAX}=\frac{\sqrt{3}}{3}I_{P\_PK\_MAX}\times\sqrt{\frac{t_1}{t_S}} \quad (17)$$

(f) Compute secondary maximum peak current $I_{S\_PK\_MAX}$ and RMS current $I_{S\_RMS\_MAX}$ for the transformer fabrication.

$$I_{S\_PK\_MAX}=N_{PS}\times I_{P\_PK\_MAX} \quad (18)$$

$$I_{S\_RMS\_MAX}=\frac{\sqrt{3}}{3}N_{PS}\times I_{P\_PK\_MAX}\times\sqrt{\frac{t_2}{t_S}} \quad (19)$$

Transformer design (N_P, N_S, N_{AUX})

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The design of the transformer is similar with ordinary Flyback transformer. The parameters below are necessary:

Necessary parameters	
Turns ratio	N_{PS}
Inductance	L_M
Primary maximum current	$I_{P\_PK\_MAX}$
Primary maximum RMS current	$I_{P\_RMS\_MAX}$
Secondary maximum RMS current	$I_{S\_RMS\_MAX}$

The design rules are as followed:

(a) Select the magnetic core style, identify the effective area A_e;

(b) Preset the maximum magnetic flux ΔB;

$$\Delta B = 0.22\sim0.26\mathrm{T}$$

(c) Compute primary turn N_P;

$$N_P = \frac{L_M \times I_{P\_PK\_MAX}}{\Delta B \times A_e} \quad (20)$$

(d) Compute secondary turn N_S;

$$N_S = \frac{N_P}{N_{PS}} \quad (21)$$

(e) Compute auxiliary turn N_{AUX};

$$N_{AUX} = N_S \times \frac{V_{VIN}}{V_{OUT}} \quad (22)$$

Where V_{VIN} is the working voltage of VIN pin (11V~15V is recommended);

(f) Select an appropriate wire diameter;

With $I_{P\_RMS\_MAX}$ and $I_{S\_RMS\_MAX}$, select appropriate wire to make sure the current density ranges from 4A/mm^2 to 10A/mm^2.

(g) If the winding area of the core and bobbin is not enough, reselect the core style, go to **(a)** and redesign the transformer until the ideal transformer is achieved.

Input capacitor C_{BUS}

Generally, the input capacitor C_{BUS} is selected by

$$C_{BUS} = 2\sim3\mu\mathrm{F/W}$$

Or more accurately by

$$C_{BUS} = \frac{\arcsin\left(1-\frac{V_{DC\_MIN}}{\sqrt{2}V_{AC\_MIN}}\right)+\frac{\pi}{2}}{\pi} \cdot \frac{P_{OUT}}{\eta} \cdot \frac{1}{2f_{IN}V_{AC\_MIN}^2\left(1-\left(\frac{V_{DC\_MIN}}{\sqrt{2}V_{AC\_MIN}}\right)^2\right)} \quad (23)$$

Where V_{DC_MIN} is the minimum voltage of BUS line; f_{IN} is AC line frequency;

RCD snubber for MOSFET

The power loss of the snubber P_{RCD} is evaluated first.

$$P_{RCD} = \frac{N_{PS} \times (V_{OUT}+V_{D\_F})+\Delta V_S}{\Delta V_S} \times \frac{L_K}{L_M} \times P_{OUT} \quad (24)$$

Where N_{PS} is the turns ratio of the Flyback transformer; V_{OUT} is the output voltage; V_{D_F} is the forward voltage of the power diode; ΔV_S is the overshoot voltage clamped by RCD snubber; L_K is the leakage inductor; L_M is the inductance of the Flyback transformer; P_{OUT} is the output power.

The R_{RCD} is related with the power loss:

$$R_{RCD} = \frac{\left[N_{PS} \times (V_{OUT}+V_{D\_F})+\Delta V_S\right]^2}{P_{RCD}} \quad (25)$$

The C_{RCD} is related with the voltage ripple of the snubber ΔV_{C_RCD}:

$$C_{RCD} = \frac{N_{PS} \times (V_{OUT}+V_{D\_F})+\Delta V_S}{R_{RCD} \times f_{S\_MIN} \times \Delta V_{C\_RCD}} \quad (26)$$

Layout

(a) To achieve better EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to the BUS line capacitor first, then to the switching circuit;

(b) The ground of the BUS line capacitor, the ground of the current sample resistor and the signal ground of the IC should be connected in a star connection;

(c) The circuit loop of all switching circuit should be kept small: primary power loop, secondary loop and auxiliary power loop.

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Design Notice

1. VIN voltage prefer to larger than 11V for all conditions.
2. Some transformers structure may induce larger spike or larger ring on the current sample resistor at the initial of the primary switch turning on.This spike or ring may cause wrongly detection of the peak current and make the switch turn off earlier, so the accuracy feedback voltage sample cannot be guaranteed. The recommend structures are:0.5Primary.----Shielding----Second.----Auxiliary.----0.5Primary.or Primary.----Shielding----Second.----Auxiliary; Do not use the structure like 0.5Primary.----Auxiliary----Second.----Shielding.----0.5Primary.
3. Because IC built in CC/CV loop , in order to ensure the stability, output capacitor should be in a range, that is Cout*(Vo/Io) should not be far away from 3.7m.For example, 5V2Aoutput case, Cout=3.7/2.5=1480uF, the output capacitor should be in the range of 1270uF to 1680uF. In other hand, switching frequency ripple should also be considerd. If switching frequency ripple is large, increase the capactiance properly or use low ESR capacitor.

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Design Example

A design example of typical application is shown below step by step.

#1. Identify Design Specification

Design Specification			
V_{AC_MIN}	90V	V_{AC_MAX}	264V
V_{OUT}	12V	I_{OUT}	1A
P_{OUT}	12W	η	85%
f_{S_MIN}	55kHz	ΔV_{BUS}	30% V_{BUS_MIN}

#2. Transformer Design （N_{PS} and L_M）

Refer to Power **Device Design**

Conditions			
V_{AC_MIN}	90V	V_{AC_MAX}	264V
P_{OUT}	12W	f_{S_MIN}	55kHz
Parameters designed			
$V_{MOS\_(BR)DS}$	700V	ΔV_S	75V
C_{Drain}	100pF	V_{D_F}	1V

(a) Compute turns ratio N_{PS} first;

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 80\% - \sqrt{2} V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}}$$
$$= \frac{700V \times 0.8 - \sqrt{2} \times 264V - 75V}{12V + 1V}$$
$$= 8.58$$

N_{PS} is set to

$$N_{PS} = 7$$

(b)f_{S_MIN} is preset ;

$$f_{S\_MIN} = 55kHz$$

(c) Compute inductor L_M and maximum primary peak current $I_{P\_PK\_MAX}$;

$$I_{P\_PK\_MAX} = \frac{2P_{OUT}}{\eta \times \left(\sqrt{2} V_{AC\_MIN} - \Delta V_{BUS}\right)} + \frac{2P_{OUT}}{\eta \times N_{PS} \times (V_{OUT} + V_{D\_F})} + \pi \sqrt{\frac{2P_{OUT}}{\eta} \times C_{Drain} \times f_{S\_MIN}}$$
$$= \frac{2 \times 12W}{0.85 \times (\sqrt{2} \times 90V - 0.3 \times \sqrt{2} \times 90V)} + \frac{2 \times 12W}{0.85 \times 7 \times (12V + 1V)} + \pi \times \sqrt{\frac{2 \times 12W}{0.85} \times 100pF \times 55kHz}$$
$$= 0.666A$$

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$$L_M = \frac{2P_{OUT}}{\eta \times I^2_{P\_PK\_MAX} \times f_{S\_MIN}} = \frac{2 \times 12W}{0.85 \times (0.666A)^2 \times 55kHz} = 1.156mH$$

Set

L_M=1.15mH

(d) Compute current rising time t_1 and current falling time t_2;

$$t_1 = \frac{L_M \times I_{P\_PK\_MAX}}{\sqrt{2}V_{AC\_MIN}} = \frac{1.15mH \times 0.666A}{\sqrt{2} \times 90V} = 6.021\mu s$$

$$t_2 = \frac{L_M \times I_{P\_PK\_MAX}}{N_{PS} \times (V_{OUT} + V_{D\_F})} = \frac{1.15mH \times 0.666A}{5 \times (12V + 1V)} = 8.421\mu s$$

$$t_3 = \pi \times \sqrt{L_M \times C_{Drain}} = \pi \times \sqrt{1.15mH \times 100pF} = 1.065\mu s$$

$$t_S = t_1 + t_2 + t_3 = 6.021\mu s + 8.421\mu s + 1.065\mu s = 15.51\mu s$$

(e) Compute primary maximum RMS current $I_{P\_RMS\_MAX}$ for the transformer fabrication;

$$I_{P\_RMS\_MAX} = \frac{\sqrt{3}}{3} I_{P\_PK\_MAX} \times \sqrt{\frac{t_1}{t_S}} = \frac{\sqrt{3}}{3} \times 0.666A \times \sqrt{\frac{6.021\mu s}{15.51\mu s}} = 0.24A$$

(f) Compute secondary maximum peak current $I_{S\_PK\_MAX}$ and RMS current $I_{S\_RMS\_MAX}$ for the transformer fabrication.

$$I_{S\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} = 7 \times 0.666A = 4.662A$$

$$I_{S\_RMS\_MAX} = N_{PS} \times \frac{\sqrt{3}}{3} I_{P\_PK\_MAX} \times \sqrt{\frac{t_2}{t_S}} = 7 \times \frac{\sqrt{3}}{3} \times 0.666A \times \sqrt{\frac{8.421\mu s}{15.51\mu s}} = 1.984A$$

#3. Select secondary power diode

Refer to **Power Device Design**

Compute the voltage and the current stress of secondary power diode

$$V_{D\_R\_MAX} = \frac{\sqrt{2}V_{AC\_MAX}}{N_{PS}} + V_{OUT} = \frac{\sqrt{2} \times 264V}{7} + 12V = 65.3V$$

$$I_{D\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} = 7 \times 0.666A = 4.662A$$

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$I_{D\_AVG}=I_{OUT}=1A$

#4. Start up design

Refer to **Start up**

Conditions			
V_{DC_MIN}	$90V\times1.414$	V_{DC_MAX}	$264V\times1.414$
I_{ST}	1.2μA (typical)	V_{IN_ON}	14.7V (typical)
I_{VIN_OVP}	9mA (typical)	I_{HV_ON}	0.35mA (typical)
I_{HV_OFF}	5μA (typical)		
Designed by user			
t_{ST}	1s		

(a) Design C_{VIN}

$$C_{VIN}=\frac{(I_{HV\_ON}-I_{HV\_OFF}-I_{ST})\times t_{ST}}{V_{VIN\_ON}}$$
$$=\frac{(0.35*10^3-5-1.2)\times1s}{14.7V}$$
$$=23.38\mu F$$

Set

$C_{VIN}=22\mu F$

#5. Output voltage control

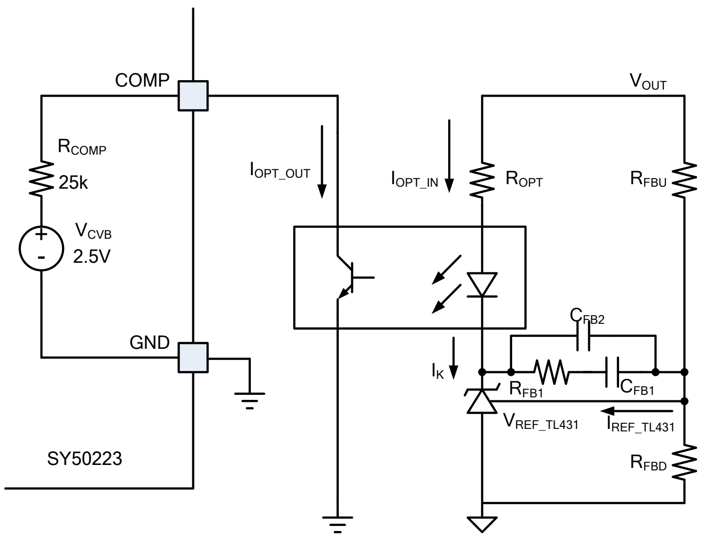

Fig.9 Output voltage feedback circuit

Conditions			
V_{CVB}	2.5V	V_{COMP_ON}	0.4V
R_{COMP}	25kΩ	V_{OPT}	1.2V
β	1	V_{REF_TL431}	2.5V

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I_{K_MIN}	1mA	I_{K_MAX}	100mA
I_{REF_TL431}	2~4μA		

Where V_{OPT} is the input forward voltage of the opto-coupler; I_K is the cathode current of the TL431; I_{REF_TL431} is the reference input current of the TL431.

(a) R_{OPT} Design

The maximum input current of the opto-coupler is limited by

$$I_{OPT\_IN\_MAX} > \frac{V_{CVB}\text{-}V_{COMP\_ON}}{R_{COMP}} \times \frac{1}{\beta} = \frac{2.5V\text{-}0.4V}{25K\Omega} \times 1 = 0.084mA$$

At the same time,

I_{OPT_IN} is limited by the current range of TL431 cathode .

$$I_{K\_MAX} > I_{OPT\_IN} > I_{K\_MIN}$$

And

$$I_{OPT\_IN} = \frac{V_{OUT}\text{-}V_{OPT}\text{-}V_{REF\_TL431}}{R_{OPT}}$$

Hence,

$$R_{OPT} < \frac{V_{OUT}\text{-}V_{OPT}\text{-}V_{REF\_TL431}}{I_{OPT\_IN\_MAX}} = \frac{12V\text{-}1.2V\text{-}2.5V}{0.084mA} = 98.8k\Omega$$

$$R_{OPT} > \frac{V_{OUT}\text{-}V_{OPT}\text{-}V_{REF\_TL431}}{I_{K\_MAX}} = \frac{12V\text{-}1.2V\text{-}2.5V}{100mA} = 83\Omega$$

Set

$$R_{OPT} = 1k\Omega$$

(b) Resistor divider design

To achieve accurate voltage reference, R_{FBD} is limited by

$$R_{FBD} \le \frac{V_{REF\_TL431}}{100 \times I_{REF\_TL431}} = \frac{2.5V}{100 \times 2\mu A} = 12.5K\Omega$$

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Set

R_{FBD}=10kΩ

$$R_{FBU}=\frac{V_{OUT}-V_{REF\_TL431}}{V_{REF\_TL431}}\times R_{FBD}=\frac{12V-2.5V}{2.5V}\times 10k\Omega=38k\Omega$$

Set

R_{FBD}=39kΩ

(c) Feedback Loop Design

Recommended parameters			
C_{FB1}	100nF	C_{FB2}	0pF
R_{FB1}	100kΩ		

#6. Output Current Protection Design

Conditions			
k_1	0.5	K_2	1
V_{REF}	0.42V	N_{PS}	7
Parameters designed			
I_{OUT_LIM}	1.15A		

I_{OUT_LIM} is the maximum output current .

The current sense resistor is

$$R_S=\frac{k_1\times V_{REF}\times N_{PS}}{I_{OUT\_LIM}}$$
$$=\frac{0.5\times 0.42V\times 7}{1.15A}$$
$$=1.278\Omega$$

Set R_S=1.3 Ω

#7. Input Capacitor C_{BUS} Design

Conditions			
V_{AC_MIN}	90V	ΔV_{BUS}	30% V_{BUS_MIN}

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$$C_{BUS}=\frac{\arcsin(1-\frac{\Delta V_{BUS}}{\sqrt{2}V_{AC\_MIN}})+\frac{\pi}{2}}{\pi}\times\frac{P_{OUT}}{\eta}\times\frac{1}{2f_{IN}V_{AC\_MIN}^{2}[1-(1-\frac{\Delta V_{BUS}}{\sqrt{2}V_{AC\_MIN}})^{2}]}$$

$$=\frac{\arcsin(1-\frac{0.3\times\sqrt{2}\times 90V}{\sqrt{2}\times 90V})+\frac{\pi}{2}}{\pi}\times\frac{12W}{0.85}\times\frac{1}{2\times 50Hz\times 90V^{2}\times[1-(1-\frac{0.3\times\sqrt{2}\times 90V}{\sqrt{2}\times 90V})^{2}]}$$

$$=25.52\mu F$$

Set
C_{BUS} =25 μF

#8. Set VSEN pin

First identify R_{VSENU} need for line regulation.

Conditions			
k_3	68		
Parameters Designed			
R_{VSENU}	91kΩ		

Then compute R_{VSEND}

Conditions			
V_{VSEN_OVP}	1.45V		
V_{OUT}	12V		
Parameters designed			
V_{OVP}	14V	R_{VSENU}	91kΩ
N_S/N_{AUX}	15/16		

$$R_{VSEND}=\frac{\frac{V_{VSEN\_OVP}}{V_{OVP}}\times\frac{N_S}{N_{AUX}}}{1-\frac{V_{VSEN\_OVP}}{V_{OVP}}\times\frac{N_S}{N_{AUX}}}\times R_{ZCSU}$$

$$=\frac{\frac{1.45V}{14V}\times\frac{15}{16}}{1-\frac{1.45V}{14V}\times\frac{15}{16}}\times 91k\Omega$$

$$=9.78k\Omega$$

Set R_{VSEND} =9.1k

#9. Design RCD snubber

Refer to **Power Device Design**

Conditions			
V_{OUT}	12V	ΔV_S	75V
N_{PS}	7	L_K/L_M	1%
P_{OUT}	12W		

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The power loss of the snubber is

$$P_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{\Delta V_S} \times \frac{L_K}{L_M} \times P_{OUT}$$
$$= \frac{7 \times (12V+1V)+75V}{75V} \times 0.01 \times 12W$$
$$=0.266W$$

The resistor of the snubber is

$$R_{RCD} = \frac{\left[N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S\right]^2}{P_{RCD}}$$
$$= \frac{[7 \times (12V+1V)+75V]^2}{0.266W}$$
$$=103.6k\Omega$$

Set R_{RCD} =200K

The capacitor of the snubber is

$$C_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{R_{RCD} f_{S\_MIN} \Delta V_{C\_RCD}}$$
$$= \frac{7 \times (12V+1V)+75V}{200k\Omega \times 55kHz \times 25V}$$
$$=604pF$$

Set C_{RCD} =680pF

#10. Final Result

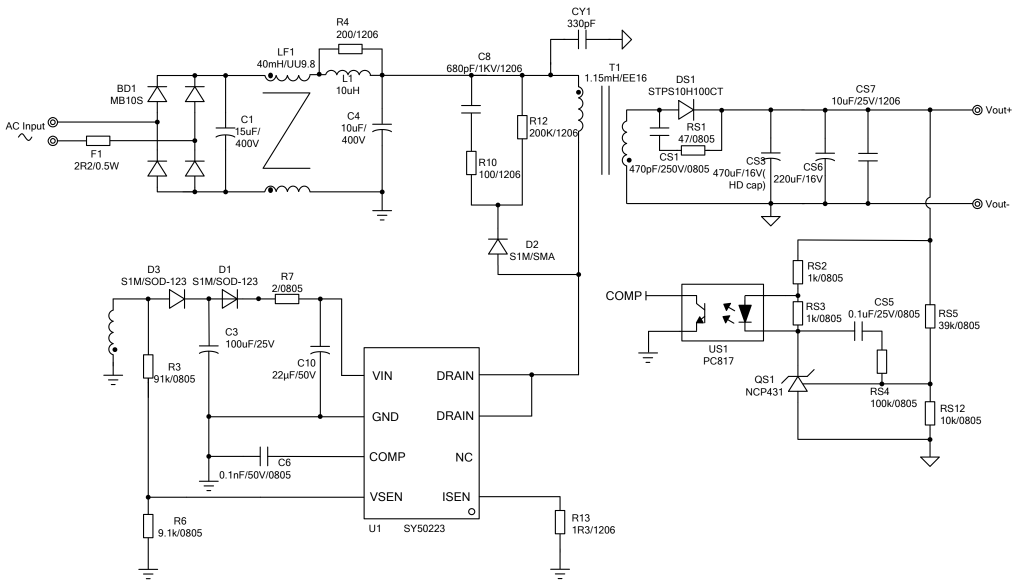

Fig.10 Final Result

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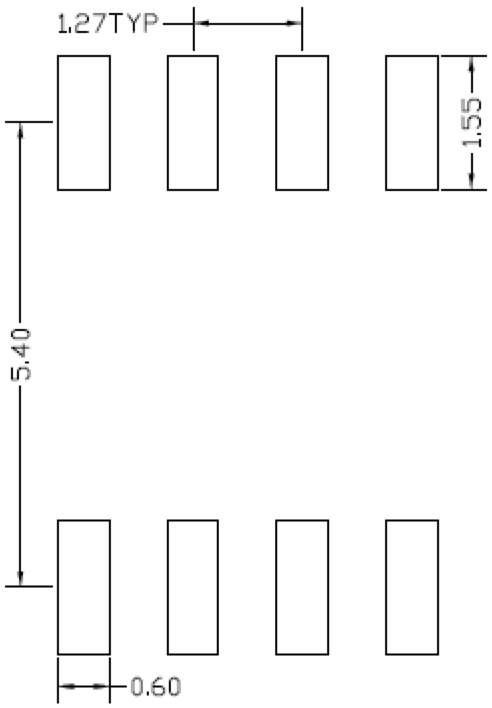
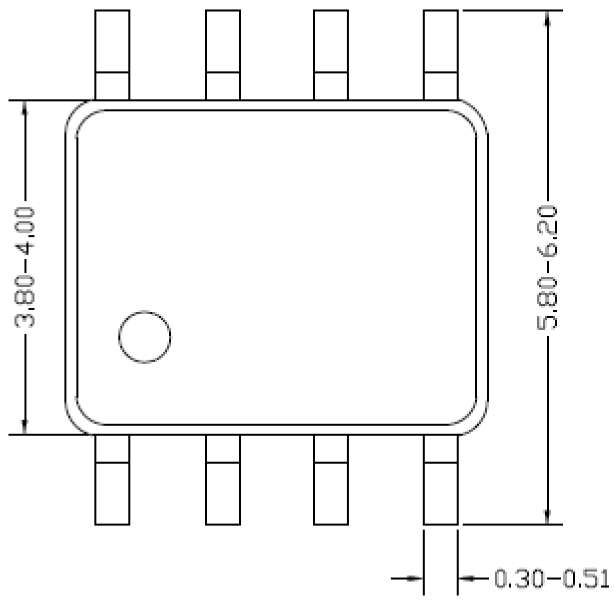
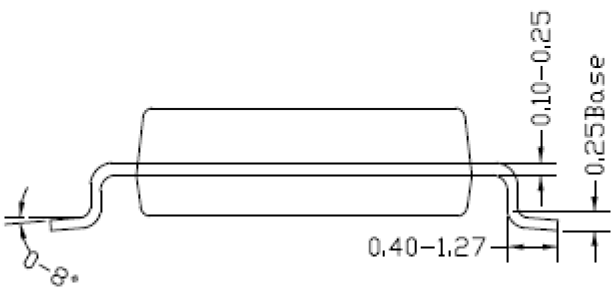
SO8 Package Outline & PCB Layout Design



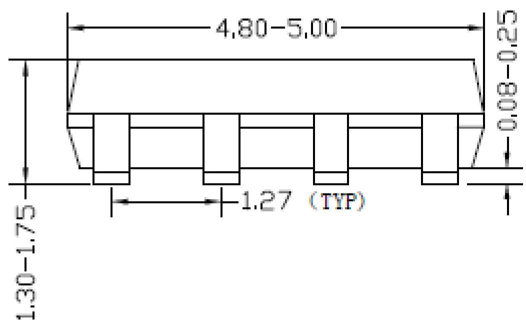
Recommended Pad Layout
(Reference only)



Top view



Side view



Front view

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

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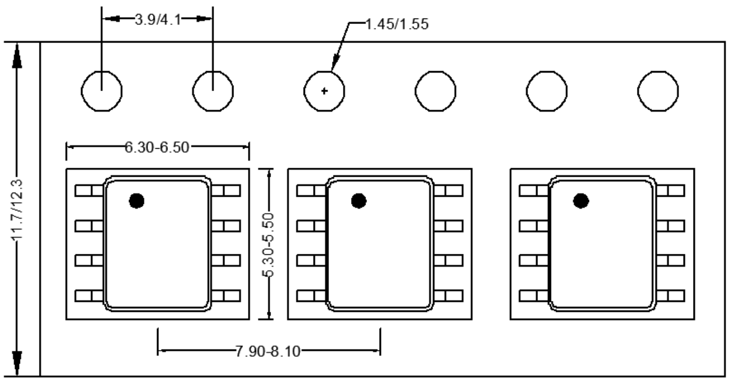
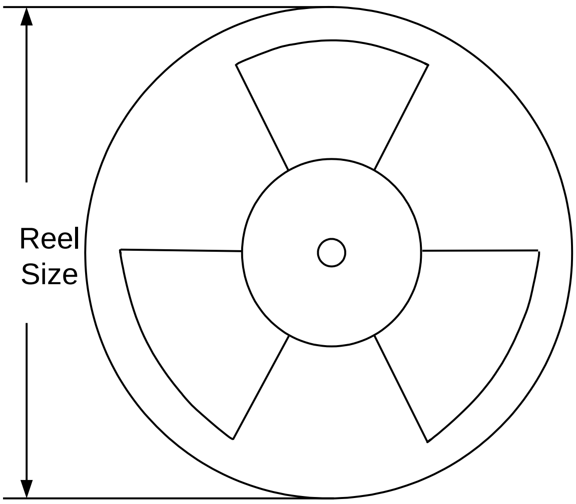
Taping & Reel Specification

1. Taping orientation for packages（SO8）



Feeding direction

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SO8	12	8	13"	400	400	2500

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