Applications Note:AN_SY8031L/SY8031

High Efficiency 2.25MHz, 0.6A/1.2A Synchronous Step Down Regulator

Preliminary Specification

General Description

The SY8031L and SY8031 are high-efficiency 2.25MHz synchronous step-down DC-DC converters capable of delivering 0.6A/1.2A output current. SY8031 operates over a wide input voltage range from 2.5V to 5.5V and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

Ordering Information

SY8031□(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Temperature Range: -40°C to 85°C

Ordering Number	Package type	Note
SY8031AAC	SOT23-5	1.2A
SY8031LAAC	SOT23-5	0.6A

Features

- Low $R_{DS(ON)}$ for internal switches (top/bottom):
  - SY8031L: 300mΩ/200 mΩ, 0.6A
  - SY8031: 200mΩ/150 mΩ, 1.2A continuous,2A peak
- 2.5-5.5V input voltage range
- 2.25MHz switching frequency
- 50uA quiescent current
- Internal softstart limits the inrush current
- 1.5% 0.6V reference
- 100% dropout operation
- RoHS Compliant and Halogen Free
- Compact package: SOT23-5

Applications

- WiFi Card
- Set Top Box
- GPS
- Toy

Typical Applications

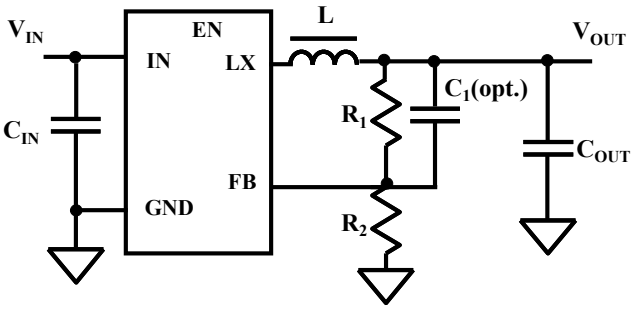


Figure 1. Schematic Diagram

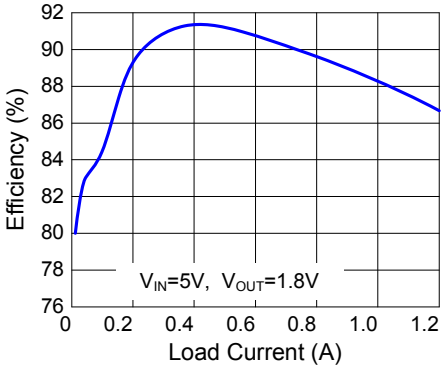
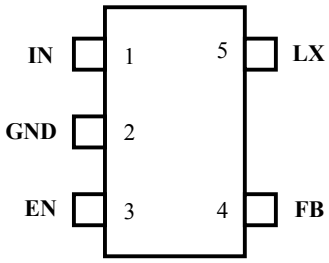


Figure 2. Efficiency vs Load Current

Pinout (top view)



(SOT23-5)

Top Mark: AG*xyz* for SY8031 BY*xyz* for SY8031L
(Device code: AG for SY8031 and BY for SY8031L, *x=year code, y=week code, z= lot number code*)

Pin Name	Pin Number	Pin Description
EN	3	Enable control. Pull high to turn on. Do not float.
GND	2	Ground pin.
LX	5	Inductor pin. Connect this pin to the switching node of inductor.
IN	1	Input pin. Decouple this pin to GND pin with at least 1uF ceramic capacitor.
FB	4	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=V_{REF}*(1+R_1/R_2)$. Add optional C_1(10pF ~ 47pF) to speed up transient response.

Absolute Maximum Ratings (Note 1)

Supply Input Voltage ---------- 6V
EN, FB Voltage---------- VIN + 0.6V
Power Dissipation, PD @ TA = 25°C SOT23-5 ---------- 0.4W
Package Thermal Resistance (Note 2)
θJA ---------- 250°C/W
θJC ---------- 130°C/W
Junction Temperature Range ---------- 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
ESD Susceptibility (Note 2)
HBM (Human Body Mode) ---------- 2kV
MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 3)

EN, IN pins ---------- 2.5V to 5.5V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} = 3.6V, V_{OUT} = 2.5V, L = 2.2uH, C_{OUT} = 10uF, T_A = 25°C, I_{MAX} = 1A unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.5		5.5	V
Quiescent Current	I_Q	I_{OUT}=0, V_{FB}= V_{REF} · 105%		50	90	μA
Shutdown Current	I_{SHDN}	EN=0		0.1	1	μA
Feedback Reference Voltage	V_{REF}		0.591	0.6	0.609	V
FB Input Current	I_{FB}	V_{FB}=V_{IN}	-50		50	nA
PFET RON	$R_{DS(ON),P}$	SY8031L		0.3		Ω
		SY8031		0.2		Ω
NFET RON	$R_{DS(ON),N}$	SY8031L		0.2		Ω
		SY8031		0.15		Ω
PFET Current Limit	I_{LIM}	SY8031L, I_{OUT}=0.6A_{MAX}	0.84			A
		SY8031, I_{OUT}=1.2A_{MAX}	1.68			A
EN Rising Threshold	V_{ENH}		1.26			V
EN Falling Threshold	V_{ENL}				0.4	V
Input UVLO Threshold	V_{UVLO}				2.4	V
UVLO Hysteresis	V_{HYS}			0.2		V
Oscillator Frequency	F_{OSC}	I_{OUT}=100mA	2	2.25	2.5	MHz
Min ON Time				50		ns
Max Duty Cycle			100			%
Thermal Shutdown Temperature	T_{SD}			150		°C

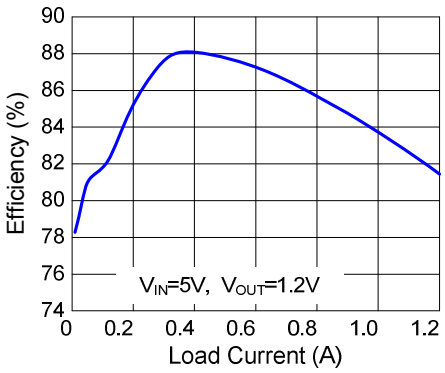
Note 1: Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2: θ JA is measured in the natural convection at TA = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Pin 2 of SOT23-5 package is the case position for θ JC measurement.

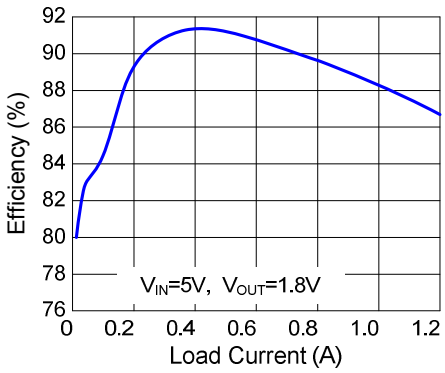
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

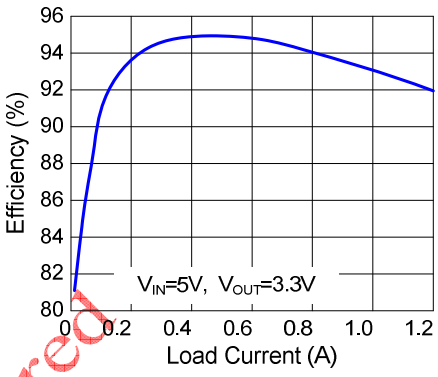
Efficiency vs. Load Current



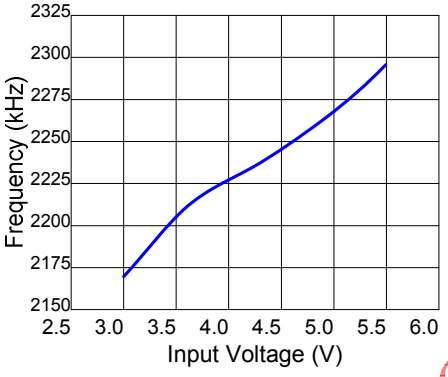
Efficiency vs. Load Current



Efficiency vs Load Current

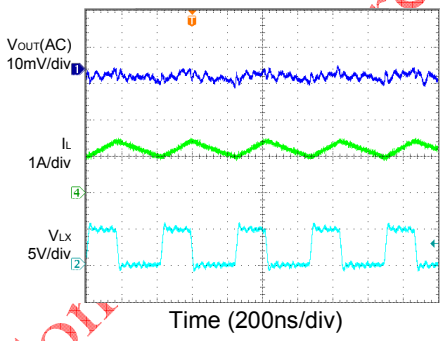


Oscillator Frequency vs Vin



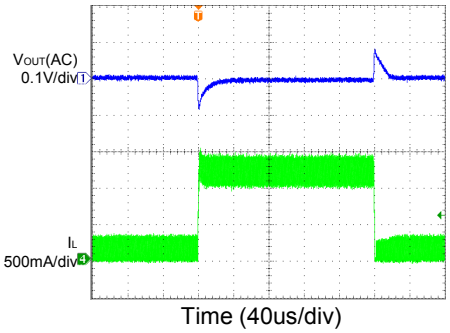
Output Ripple

(VIN=5V, VOUT=1.8V, Iload=1.2A)



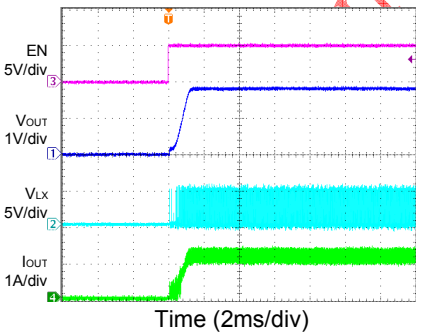
Load Transient

(VIN=5V, VOUT=1.8V, Iload=0.12-1.2A)



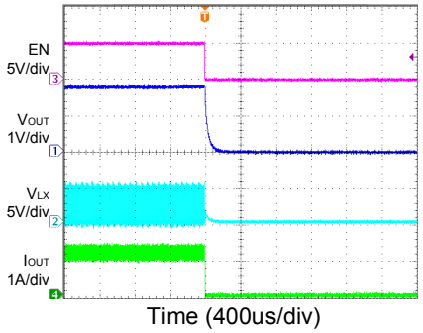
Startup

(VIN=5V, VOUT=1.8V, Iload=1.2A)

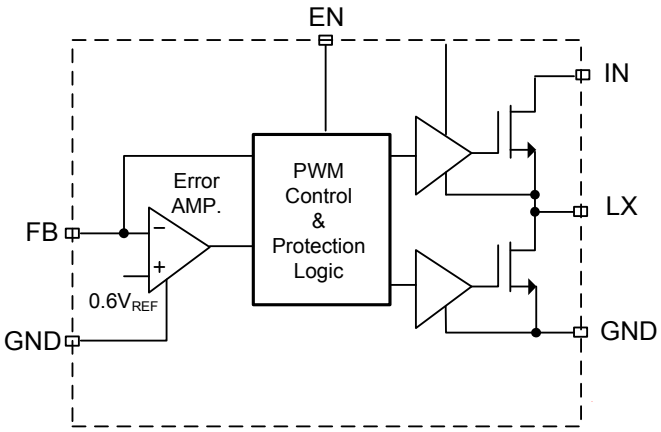


Shutdown

(VIN=5V, VOUT=1.8V, Iload=1.2A)



Block Diagram



Operation

SY8031/SY8031L is a synchronous buck regulator IC that integrates the PWM control, top and bottom switches on the same die to minimize the switching loss and conduction loss. With ultra low $R_{DS(ON)}$ power switches and proprietary PWM control, this regulator IC can achieve the highest efficiency and the highest switching frequency simultaneously to minimize the external inductor and capacitor size, and thus achieving the minimum solution footprint. The internal softstart time is about 1ms.

Applications Information

Because of the high integration in the SY8031/SY8031L IC, the application circuit based on this regulator IC is simple. Only input capacitor C_{IN}, output capacitor C_{OUT}, output inductor L and feedback resistors (R_1 and R_2) need to be selected for the targeted applications specifications.

Feedback resistor dividers R1 and R2:

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2. A value of between 10k and 1M is recommended for both resistors. If R_2=120kΩ is chosen, then R_1 can be calculated to be:

$$R_1 = \frac{(V_{OUT} - 0.6V) \times R_2}{0.6V}$$

Input capacitor CIN:

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \cdot \sqrt{D(1-D)}$$

A typical X7R or better grade ceramic capacitor with above 6V rating and suitable capacitance should be choosen to handle this ripple current well. To minimize the potential noise problem, place this ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and IN/GND pins.

Output capacitor COUT:

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X7R or better grade ceramic capacitor greater than 4.7uF capacitance.

Output inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

where Fsw is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.
The SY8031/SY8031L regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,\,MIN} > I_{OUT,\,MAX} + \frac{V_{OUT}(1-V_{OUT}/V_{IN,MAX})}{2 \cdot F_{SW} \cdot L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<50mΩ to achieve a good overall efficiency.

Layout Design:

The layout design of SY8031/SY8031L regulator is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: C_{IN}, L, R_1 and R_2.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allows, a ground plane is highly desirable.

2) C_{IN} must be close to Pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.

3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

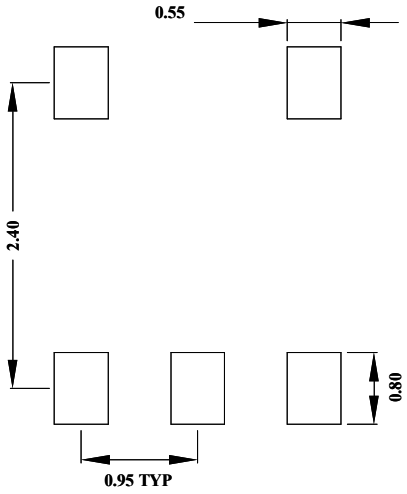
4) The components R_1 and R_2, and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.

5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1Mohm resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

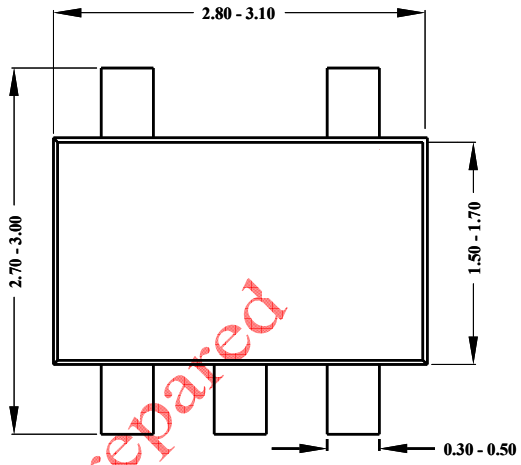
Load Transient Considerations:

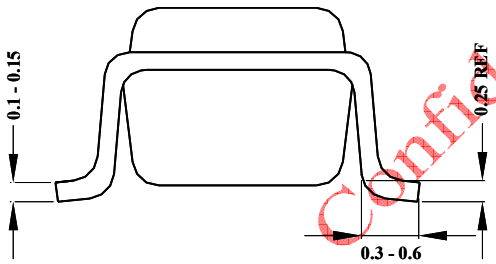
The SY8031/SY8031L regulator IC integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a 22pF~100pF ceramic capacitor in parallel with R_1 may further speed up the load transient responses and is thus recommended for applications with large load transient step requirements.

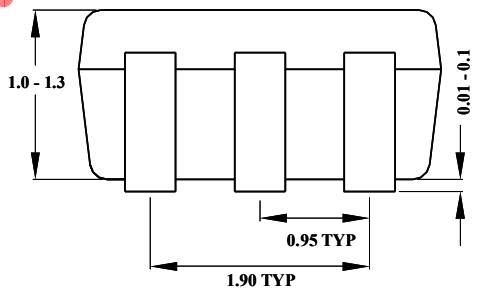
SOT23-5 Package outline & PCB layout design



Recommended Pad Layout







Notes: **All dimensions are in millimeters.**
All dimensions don't include mold flash & metal burr.