General Description

The SY81003 develops high efficiency 500kHz synchronous step-down DC/DC converter capable of delivering 3A current. The device operates over a wide input voltage range from 4.2V to 18V and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

The SY81003 adopts the instant PWM architecture to achieve fast transient responses for high step down applications and high efficiency at light loads. In addition, it operates at pseudo-constant frequency of 500kHz to minimize the size of the inductor and the capacitor.

Ordering Information

SY81003 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY81003ADC	TSOT23-6	--

Features

- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom): 80mΩ/40mΩ
- 4.2-18V Input Voltage Range
- 3A Output Current Capability
- 500kHz Switching Frequency Minimize the External Components
- Stable with 10μF C_{OUT} and 2.2μH Inductor
- Instant PWM Architecture to Achieve Fast Transient Responses
- Internal Soft-start Limits the Inrush Current
- Startup from Pre-biased Output
- Cycle-by-cycle Peak/Valley Current Limitation
- Hic-cup Mode Output Short Circuit Protection
- Over Temperature Protection with Auto Recovery
- Output Auto Discharge Function
- ±1.0% Internal Reference Voltage
- RoHS Compliant and Halogen Free
- Compact Package: TSOT23-6

Typical Application

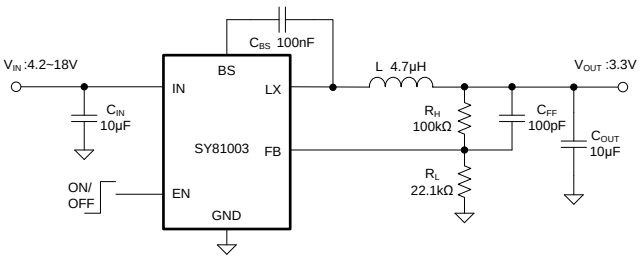

Figure1. Schematic Diagram

Inductor and C_{OUT} Selection Table

V_{OUT} [V]	L [μH]	C_{OUT} [μF] 4.7	10	22
1.2	1.5			√
	2.2			☆
3.3	2.2		√	√
	4.7		☆	√
5	3.3		√	√
	6.8		☆	√

Note: '☆' means recommended for most applications.

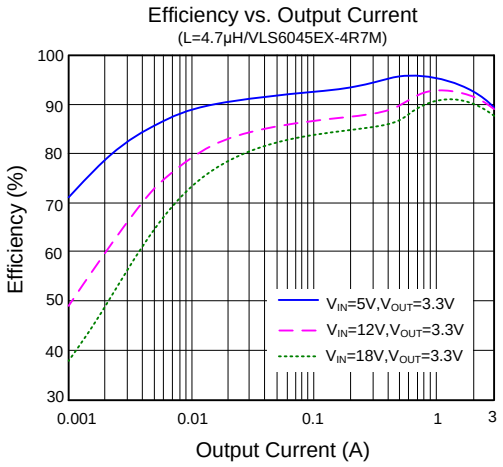

Figure2. Efficiency vs. Output Current

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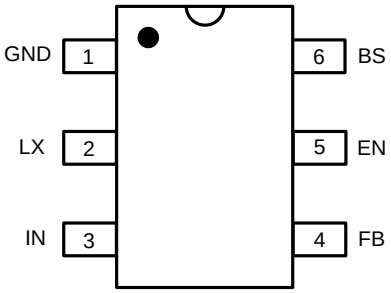
Pin-out (Top View)



(TSOT23-6)

Top Mark: L8*xyz* (device code: L8; ***x=year code, y=week code, z= lot number code*****)**

Pin Name	Pin Number	Pin Description
GND	1	Power ground pin.
LX	2	Inductor pin. Connect this pin to the switching node of the inductor.
IN	3	Input pin. Decouple this pin to the GND pin with at least a 10μF ceramic capacitor.
FB	4	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=0.6\times(1+R_H/R_L)$
EN	5	Enable control. Pull high to turn on. Do not leave this pin floating.
BS	6	Boot-strap pin. Supply high side gate driver. Connect a 0.1μF ceramic capacitor between the BS and the LX pin.

Block Diagram

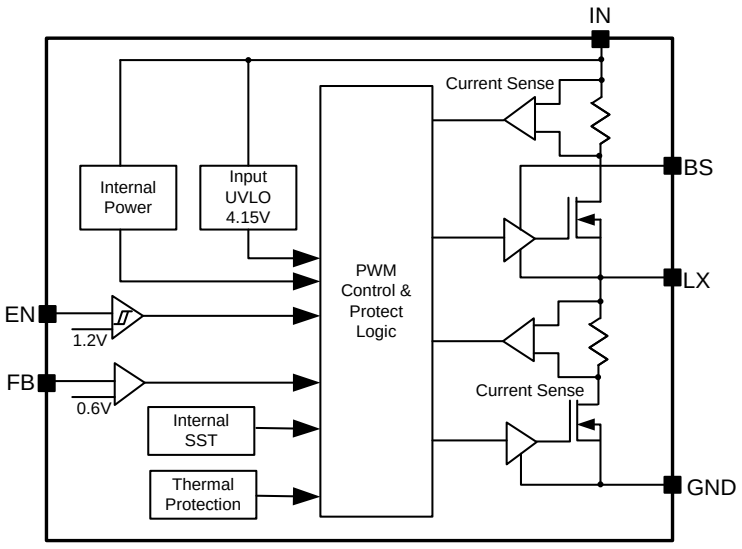


Figure3. Block Diagram

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Absolute Maximum Ratings (Note 1)

Supply Input Voltage ---------- -0.3V to 19V
LX, EN Voltage---------- -0.3V to V_{IN} + 0.3V
FB Voltage---------- -0.3V to 3.3V
BS-LX Voltage---------- -0.3V to 4V
Power Dissipation, P_D @ T_A = 25°C TSOT23-6, ---------- 1.5W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 66°C/W
θ_{JC} ---------- 15°C/W
Junction Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
Dynamic LX Voltage in 10ns Duration (Note3) ---------- IN+3V to GND-5V

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 4.2V to 18V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

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Electrical Characteristics

(V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, C_{OUT} = 10µF, T_A = 25°C, I_{OUT} = 1A unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4.2		18	V
Input UVLO Threshold	V_{UVLO}				4.15	V
UVLO Hysteresis	V_{HYS}			0.6		V
Quiescent Current	I_Q	I_{OUT}=0, V_{FB}=V_{REF}×105%		250		µA
Shutdown Current	I_{SHDN}	EN=0		5	10	µA
Feedback Reference Voltage	V_{REF}	Under CCM condition	594	600	606	mV
FB Input Current	I_{FB}	V_{FB}=3.3V	-50		50	nA
Output Discharge Resistance	R_{DIS}			40		Ω
Top FET RON	$R_{DS(ON)1}$			80		mΩ
Bottom FET RON	$R_{DS(ON)2}$			40		mΩ
EN Rising Threshold	$V_{EN,R}$		1.08	1.2	1.32	V
EN Falling Threshold	$V_{EN,F}$		0.9	1.0	1.1	V
EN Leakage Current	I_{EN}		-1		1	µA
Min ON Time	$t_{ON,MIN}$			50		ns
Min OFF Time	$t_{OFF,MIN}$			200		ns
Turn On Delay	$t_{ON,DLY}$	from EN high to LX start switching		300		µs
Soft-start Time	t_{SS}	V_{OUT} from 0 to 100%		1		ms
Switching Frequency	f_{SW}	V_{OUT}=3.3V, CCM		500		kHz
Top FET Peak Current Limit	$I_{LIM,TOP}$		4.5			A
Bottom FET Valley Current Limit	$I_{LIM,BOT}$		3			A
Output UVP Threshold	V_{UVP}			33		%V_{REF}
Output UVP Delay	$t_{UVP,DLY}$			100		µs
UVP Hiccup On Time	$t_{UVP,ON}$			2		ms
UVP Hiccup Off Time	$t_{UVP,OFF}$			6		ms
Thermal Shutdown Temperature	T_{SD}			150		˚C
Thermal Shutdown Hysteresis	T_{HYS}			15		˚C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a 2-oz two-layer Silergy evaluation board. Paddle of TSOT23-6 package is the case position for SY81003ADC θ_{JC} measurement.

Note 3: The device is not guaranteed to function outside its operating conditions.

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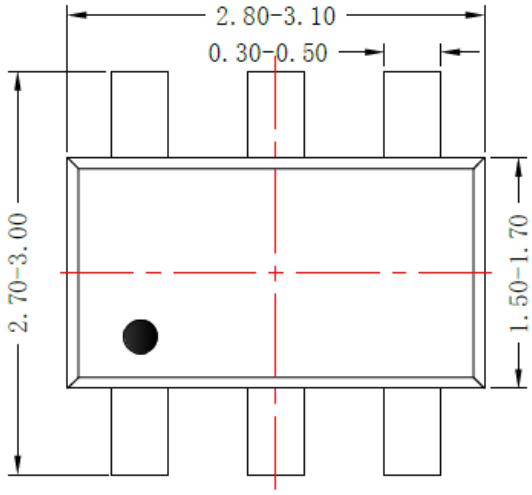
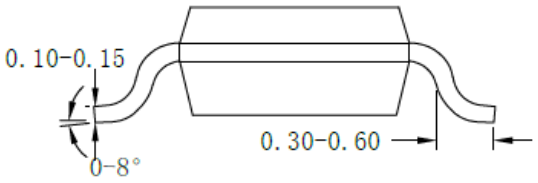
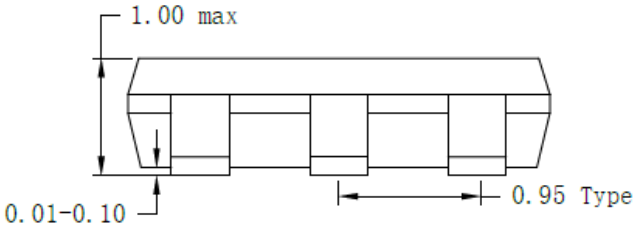
TSOT23-6 Package Outline & PCB Layout



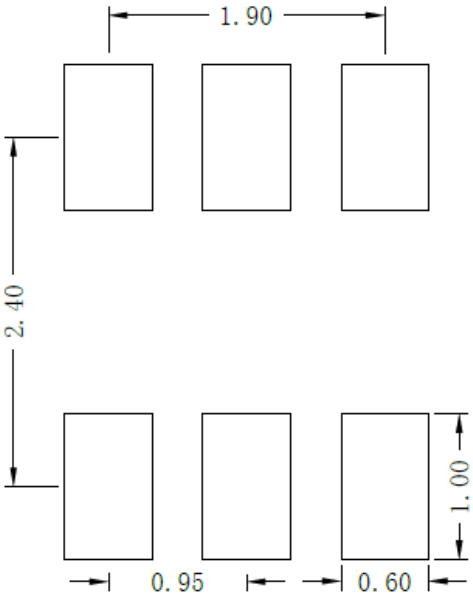
Top view



Side view



Front view



Recommended Pad Layout

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

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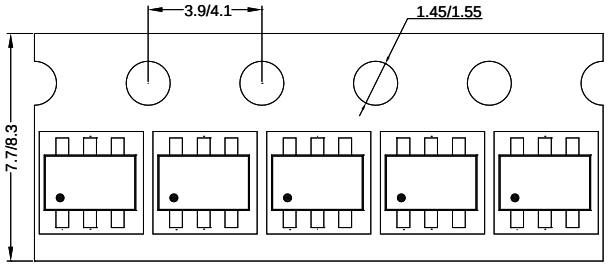
Taping & Reel Specification

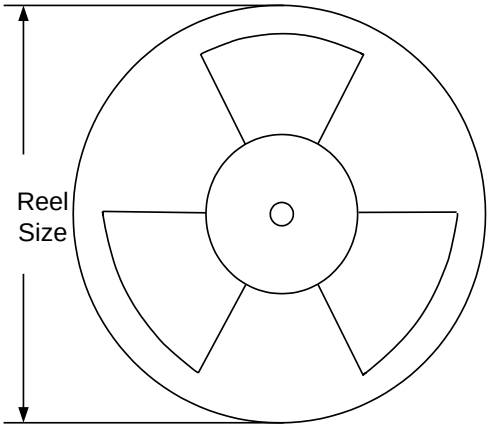
1. Taping orientation

TSOT23-6



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
TSOT23-6	8	4	7"	400	160	3000

3. Others: NA

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